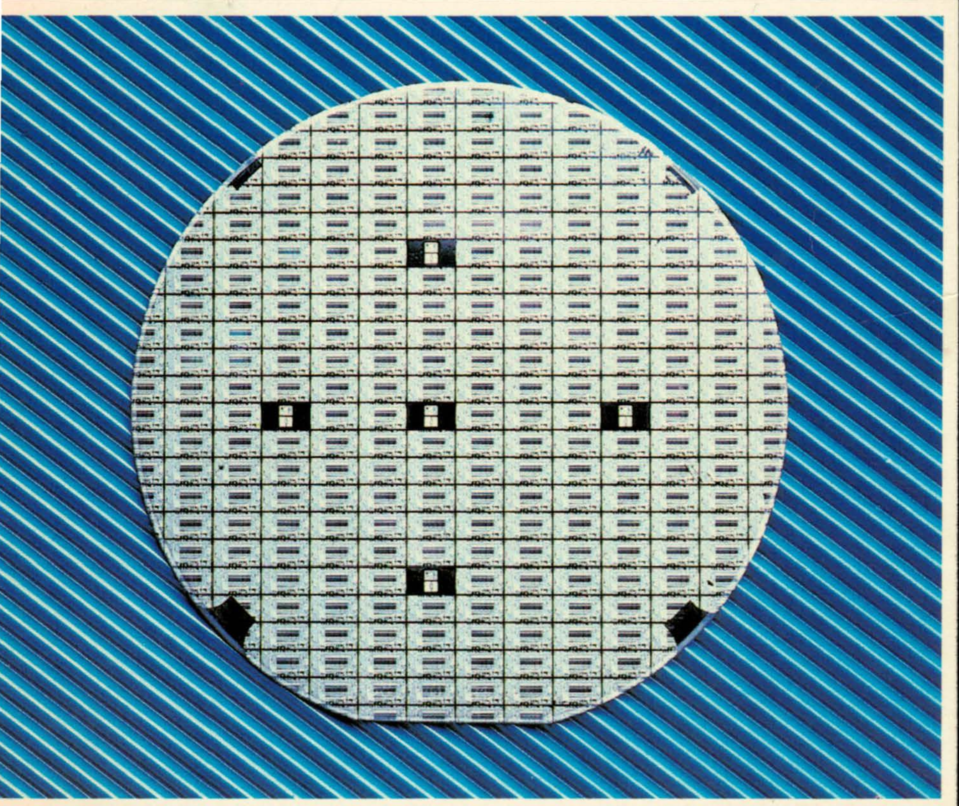
ANALOG

PRODUCT DATA BOOK



HARRIS

Volume 5
$5.00

Harris Semiconductor Sector Capabilities

Harris Semiconductor, one of the top ten U.S. semiconductor merchant suppliers, is a sector of Harris Corporation — a producer of advanced information processing, communication and microelectronic products for the worldwide Information Technology market.

Harris Semiconductor is organized to address the standard products, custom products, and gallium arsenide semiconductor markets.

SEMICONDUCTOR PRODUCTS DIVISION:

Harris Semiconductor offers a wide selection of standard analog and digital circuits through its Semiconductor Products Division:

Analog Products

Harris is a major force in analog integrated circuitry, offering a broad line of products including: analog-to-digital converters, digital-to-analog converters, sample-and-hold circuits, multiplexers, switches, voltage references, operational amplifiers, telecommunications and speech processing products, hybrid subsystems and active filters.

Digital Products

Harris is a pioneer in developing and producing digital CMOS products including: CMOS RAMs, CMOS PROMs, CMOS microprocessors, CMOS peripherals, CMOS data communications products, and a full line of 80C86/88 microprocessors and peripherals. Semicustom circuit design problems are solved by a complete line of SSI, MSI, and LSI standard cells and programmable logic products featuring on-chip testability. The Harris SHIPs™ (Semicustom Highly Integrated Peripherals) service features total in-plant capability, proven LSI cells, and an array of customer design entry levels. (See complete digital product listing, page 13-2)

CUSTOM INTEGRATED CIRCUITS DIVISION (CICD)

Harris designs, develops and manufactures analog, digital bipolar, and CMOS circuits for specialized military and commercial applications. CICD offers a full line of radiation hardened products guaranteed to customer specifications. Strategic, tactical and communications ICs are available as full custom, semicustom and data sheet products. (See complete CICD product listing, page 13-3 & 13-4)

MICROWAVE SEMICONDUCTOR DIVISION

Harris Microwave Semiconductor Division develops and manufactures gallium arsenide field effect transistors (GaAs FETs), digital integrated circuits, monolithic microwave integrated circuits, and GaAs FET microwave amplifiers. (See complete Microwave product listing, page 13-4)

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Harris Linear, Data Acquisition and Telecom Products

Harris Semiconductor's spectrum of analog products meet many specialized requirements ranging from precision to high speed performance. Capitalizing on advanced linear processing technologies developed over the past 19 years, Harris Semiconductor offers analog products of high quality and unmatched performance.

This data book describes Harris Semiconductor's complete line of Linear, Data Acquisition, and Telecommunication products. In addition, it includes a complete set of data sheets for product specifications; a section of application notes with design details for specific applications of Harris products; and a description of Harris' quality and high reliability program.

If you need more information on these and other Harris products, please contact the nearest Harris sales office listed in the back of this data book. Or return the reply card attached inside back cover.

Harris Semiconductor products are sold by description only. All specifications in this data book are applicable only to packaged products; specifications for dice are available upon request. Harris reserves the right to make changes in circuit design, specifications and other information at any time without prior notice. Accordingly, the reader is cautioned to verify that data sheets and other information in this publication are current before placing orders. Information contained in the application notes is intended soley for general guidance; use of the information for user's specific application is at user's risk. Reference to products of other manufacturers are solely for convenience of comparison and do not imply total equivalency of design, performance, or otherwise.

ANALOG

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Ordering Information

Harris products are designated by "Harris Product Code". These products will always begin with the letter'H'and specific device numbers are isolated by hyphens. An example product code is shown below. When ordering, please refer to products by the full code identification.

HARRIS PRODUCT CODE EXAMPLE

H I 1 — 0508A — 5

PREFIX:
H (HARRIS)

FAMILY:
A: Analog
C: Communications
D: Digital
F: Filters
I: Interface
M: Memory
V: Analog, High Voltage
Y: Analog Hybrids

PACKAGE:
1 —: Dual-In-Line, Ceramic
2 —: Metal Can
3 —: Dual-In Line, Plastic
4 —: Ceramic Leadless Chip Carriers (LCC)
4P —: Plastic Leaded Chip Carriers (PLCC)
5 —: LCC Hybrid
7 —: Mini-DIP, Ceramic
0 —: Chip Form

PART NUMBER

TEMPERATURE:
—1: 0°C to +200°C*
—2: -55°C to +125°C
—4: -25°C to +85°C
—5: 0°C to +75°C
—6: 100% +25°C Probe (Dice Only)
—7: Dash-7 High Reliability Commercial Product. 0°C to +75°C
—8: Dash-8 Program, Hi-Rel Processing with Burn-in, -55°C to +125°C
—9: -40°C to +85°C
—9+: -40°C to +85oC with Burn-in
/883: MIL-STD-883 Class B, Full Compliance

* Special high temperature testing available on certain product types. Consult factory for availability.

COMMERCIAL, INDUSTRIAL PRODUCTS

Harris Semiconductor offers a variety of product grades to let you satisfy system requirements. These grades are differentiated in four areas:

1) Operating Temperature Range
2) Electrical Performance
3) Package Type
4) Additional Screening Tests

These parts are marked with appropriate prefix and suffix designations. Product designations for each of the grading parameters are illustrated in the Product Code Example. The information contained in this catalog is intended to describe the expected product performance under the specified operating conditions for each temperature and performance grade.

Device testing sufficient to assure conformance is performed to provide the highest quality in the most cost-effective manner. For those customers who wish to have additional screening (burn-in, etc.), Harris offers DASH 7, DASH 8 and DASH 9+ screening programs (described in section 9 of this catalog).

Military customers are advised that the Harris DASH 8 program is not fully compliant to MIL-STD-883. The Harris DASH 8 program provides products specified over the -55°C to +125°C temperature range with the additional screening indicated in Chapter 9. Please refer to the "Military Products" section for information regarding Harris Semiconductor's MIL-STD-883 compliant program.

SPECIAL ORDERS

For best availability and price, it is urged that standard "Product Code" devices be specified, which are available worldwide from authorized distributors. Where enhanced testing is needed, please refer to the Harris standard DASH 7, DASH 8 or DASH 9+ screening options described in this data book. Harris application engineers may be consulted for information concerning suitability of a product for a given application.

If additional electrical parameter guarantees for reliability screening are absolutely required, a Request For Quotation and Source Control Drawing should be submitted through the local Harris Sales Office or Sales Representative. Harris reserves the right to decline to quote, or to request modification to, special screening requirements.

MILITARY PRODUCTS

Harris offers a full line of products that are processed in full conformance to the provisions of military standards including MIL-STD-883C for

MILITARY PRODUCTS (Continued)

Class B parts. The requirements for these products are controlled in one or two ways:

1. Government standards (such as JAN Slash Sheets or DESC Drawings)
2. Harris Standards

The Harris standard Military Products Program is based on its experience in the JAN program. JAN certifications are maintained on our production and Product Assurance operations and form the basis of our MIL-STD-883 conformance program. These areas are regularly audited by Harris and by the U.S. government to assure compliance.

Selected products have been qualified to the MIL-M-38510 requirements and are listed on the QPL. There are also a number of Harris parts which are specified by DESC Drawings. In addition, Harris offers many products as fully conformant to MIL-STD-883 via an internal standards program. Please contact the factory or your local Harris Sales Office or Representative for the latest status on military standard compliant product offerings.

The information in this catalog is intended to describe the expected part behavior under certain operating conditions. The product descriptions contained in this catalog, particularly in the area of electrical performance, do not precisely reflect those of our JAN qualified, DESC or MIL-STD-883 compliant products and are not necessarily test requirements for Harris military standard compliant products.

The actual product test requirements for JAN and DESC parts are described in the appropriate MIL-M-38510 slash sheet or DESC Drawing, respectively. In addition, Harris will be issuing product data sheets for MIL-STD-883 compliant parts which will describe actual test requirements. These compliant products will be identified by a "/883" suffix on the part number (e.g. HX1-XXXX/883). Please contact the factory or your local Harris Sales Office or Representative for details on MIL-STD-883 compliant product offerings.

IC Handling Procedures

Harris Analog IC processes produce circuits more rugged than similar ones. However, no semiconductor is immune from damage resulting from the sudden application of many thousands of volts of static electricity. While the phenomenon of catastropic failure of devices containing MOS transistors or capacitors is well known, even bipolar circuits can be damaged by static discharge, with altered electrical properties and diminished reliability. None of the common IC internal protection networks operate quickly enough to positively prevent damage.

It is suggested that all semiconductors be handled, tested, and installed using standard "MOS handling techniques" of proper grounding of personnel and equipment. Parts and subassemblies should not be in contact with untreated plastic bags or wrapping material. High impedance IC inputs wired to a P.C. connector should have a path to ground on the card.

HANDLING RULES

Since the introduction of integrated circuits with MOS structures and high quality junctions, a safe and effective means of handling these devices has been of primary importance. One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existance in the industry. In addition most compensation networks in linear circuits are located at high impedance nodes, where protection networks would disturb normal circuit operation. If static discharge occurs at sufficient magnitude (2kV or more), some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10KV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. It is evident, therefore, that proper handling procedures or rules should be adopted.

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Conductive plastic* mats on work benches and floor, connected to ground through a 1MΩ resistor, help eliminate static build-up and discharge, Do not use metallic surfaces.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1MΩ to ground (the 1MΩ resistor will prevent electroshock injury to personnel). Transient product personnel should wear grounding heel straps.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold, or aid, in the generation of a static charge. Where they cannot be eliminated natural materials such as cotton etc., should be used to minimize charge generation capacity. Conductive smocks are also available as an alternative.
- Control relative humidity to as high a level as practical. 50% is generally considered sufficient (operations should cease if R. H. falls below 25%).
- Ionized airblowers reduce charge build-up in areas where grounding is not possible or practical.
- Devices should be in conductive carriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam or foil.
- In automated handlilng equipment, the belts, chutes, or other surfaces should be of conducting non-metal material. If this is not possible, ionized air blowers or ionizing bars may be a good alternative.

*Supplier 3M Company
"Static Control Table Mat 8210/8210R"
"Static Control Floor Mat 8200/8200R"

Harris Analog IC Technologies

JUNCTION ISOLATION (JI)

This is the most common integrated circuit process. Bipolar ICs generally begin with a p-type wafer into which a buried layer pattern, if used, is first diffused. Then the n-type epitaxial layer is grown, and p-type isolation walls are diffused around each area which is to be electrically isolated from the other circuitry. These isolation walls must be diffused deeply into the wafer in order to contact the original p-substrate. In operation, the p-substrate and isolation walls are connected to the most negative circuit potential, so that each active area is surrounded on the sides and bottom by a reverse biased junction through which negligible current flows (Figure 1).

To complete the IC, base and emitter diffusions are performed, the wafer is coated with aluminum and the conductor pattern is etched.

A representative Harris device using this process is the HA-4741.

DIELECTRIC ISOLATION (DI)

A somewhat different process has been proven particularly advantageous for fabricating high performance analog ICs. This is dielectric isolation (DI), where each active area is surrounded on the sides and bottom by an insulating layer of silicon dioxide, and for mechanical strength imbedded in polycrystalline silicon. This process for bipolar ICs begins with a wafer of n-type silicon. The side of the wafer which will eventually be the bottom is deeply etched to form the sidewall pattern, then silicon dioxide and polycrystalline silicon are grown to fill the etched "moats". The opposite side of the wafer is then polished until the insulating sidewalls appear at the wafer surface (Figure 2). Conventional diffusion and metallization processes follow to complete the IC. DI for analog ICs has a number of advantages:

1. Almost all op amp designs require at least one PNP transistor in the signal path. Typical JI op amps must use a lateral PNP which inherently has very low frequency response, limiting typical compensated bandwidth to 1MHz. The DI process makes it practical to build a vertical PNP with much higher bandwidth making possible compensated op amp bandwidths of 12MHz or higher (Figure 3). Also, transistor collector to substrate capacitance is 2/3 less using DI, further enhancing high frequency performance.

2. Other devices such as optimally specified MOS or JFET transistors may be fabricated on the same chip. Isolated diffused and thin film resistors are also practical.

3. The isolation removes the possibility of parasitic SCRs which might create latchup under certain sequences of power and signal application.

4. Leakage currents to the substrate under high temperature conditions are greatly reduced. While the circuits in this data book were not specifically designed for operating temperatures greater than +125°C, many have shown superior performance. For ICs requiring the ultimate in radiation resistance, Harris Semiconductor Custom Integrated Circuits Division should be consulted.

DIELECTRIC ISOLATED CMOS

JI processed CMOS analog ICs, which are generally used in conjunction with several power supplies, are particularly prone to parasitic SCR latchup failures and failures due to input voltage spikes. The DI CMOS process, which is compared in detail in Harris Application Note 521, has proved to be the best solution.

Since analog multiplexers are often used at the input of a data acquisition system, particular attention must be paid to the possibility of damaging input overvoltage conditions. Harris has provided an effective answer in the HI-506A through HI-509A and HI-506LA through HI-509LA multiplexers with built-in overvoltage protection.

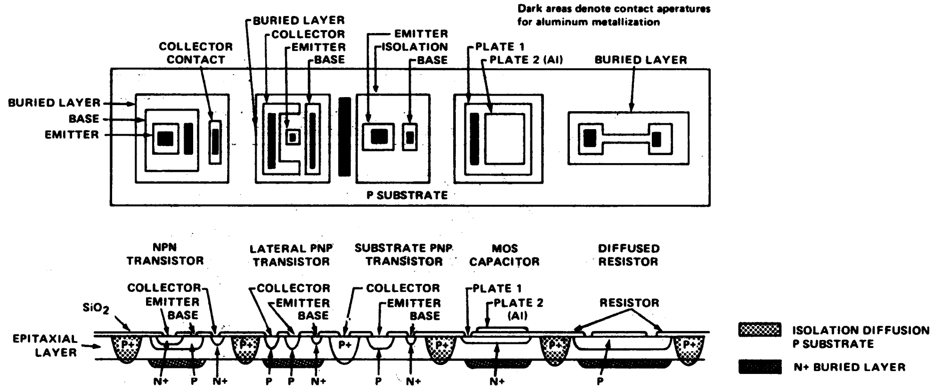

(a)
Dark areas denote contact aperatures for aluminum metallization
COLLECTOR CONTACT
BURIED LAYER
COLLECTOR
EMITTER
BASE
EMITTER
ISOLATION
BASE
PLATE 1
PLATE 2 (Al)
BURIED LAYER
BURIED LAYER
BASE
EMITTER
P SUBSTRATE
(b)
NPN TRANSISTOR
LATERAL PNP TRANSISTOR
SUBSTRATE PNP TRANSISTOR
MOS CAPACITOR
DIFFUSED RESISTOR
SiO2
COLLECTOR
EMITTER
BASE
COLLECTOR
EMITTER
BASE
COLLECTOR
EMITTER
BASE
PLATE 1
PLATE 2 (Al)
RESISTOR
EPITAXIAL LAYER
P+
N+
P
N+
P
P
N+
P
N+
N+
P
ISOLATION DIFFUSION P SUBSTRATE
N+ BURIED LAYER

Figure 1 — Structures of various components formed in the junction-isolation process. (a) Topological view. (b) Cross-sectional view.

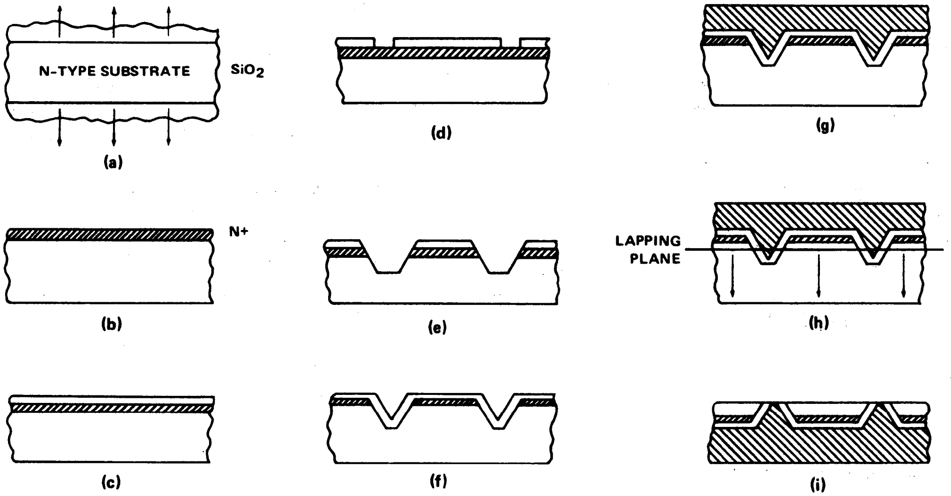

N-TYPE SUBSTRATE
SiO2
(a)
N+
(b)
(c)
(d)
(e)
(f)
(g)
LAPPING
PLANE
(h)
(i)

Figure 2 — Process steps for dielectric isolation. (a) Surface preparation, (b) N- buried layer diffusion, (c) masking oxide, (d) isolation pattern, (e) silicon etch, (f) dielectric oxide, (g) polycrystalline deposition, (h) backlap and polish, (i) finished slice.

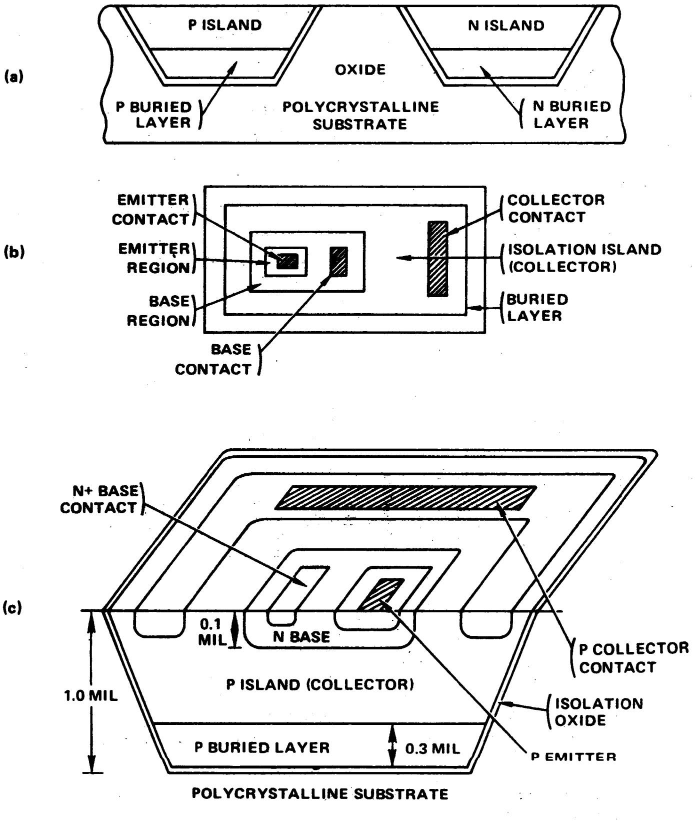

(a)
P ISLAND
N ISLAND
OXIDE
P BURIED LAYER
POLYCRYSTALLINE SUBSTRATE
N BURIED LAYER
(b)
EMITTER CONTACT
EMITTER REGION
BASE REGION
BASE CONTACT
COLLECTOR CONTACT
ISOLATION ISLAND (COLLECTOR)
BURIED LAYER
(c)
N+ BASE CONTACT
0.1 MIL
N BASE
1.0 MIL
P ISLAND (COLLECTOR)
P BURIED LAYER
0.3 MIL
POLYCRYSTALLINE SUBSTRATE
P COLLECTOR CONTACT
ISOLATION OXIDE
P EMITTER

Figure 3 — The high-frequency process. (a) Cross-sectional view of P and N islands for PNP and NPN transistors. (b) Topological view showing relative placement of transistor regions. (c) Cross-sectional view of high-frequency PNP device formation in the D.I. process.

Competitive Cross Reference Chart

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
ADVANCED MICRO DEVICES (AMD)			
AM118		HA-2510	
AM1408		HI-5618-5	Faster, Application Resistors
AM1508		HI-5618-2	Faster, Application Resistors
AM318		HA-2515	
AM6012		HI-562A	Faster, Application Resistors Initial Linearity
		HI-5660	Initial Linearity, Application Resistors
AM6112		HI-774A	
AM6420		HA-5320 HA-5330	
AM7950		HC-5502A HC-5504	Better Noise, Better Longitudinal Balance, Lower Power
LF198		HA-2420	Improved Performance
LF398		HA-2425	Improved Performance
SSS1408		HI-5618-5	Faster, Application Resistors
SSS1508		HI-5618-2	Faster, Application Resistors
ANALOG DEVICES (ADI)			
52		HA-5180	Monolithic
AD1408		HI-5618-5	Faster, Application Resistors
AD1508		HI-5618-2	Faster, Application Resistors
AD380		HA-2541	Monolithic
AD381		HA-2541	Monolithic
AD389		HA-5320	Faster, Monolithic
AD507	HA-2620		Identical
AD509	HA-2520		Identical
AD515		HA-5180	Monolithic
AD518		HA-2515	
AD542L		HA-5170	Better AC
AD545	HA-5180		Monolithic
AD547J	HA-5170		Better AC
AD562		HI-562A	Faster
		HI-5660	Faster
AD563		HI-565A	Faster
AD565	HI-565A		Faster
AD565A	HI-565A		
AD566		HI-5660 HI-562	
AD566A		HI-5660 HI-562A	
AD574A	HI-574A		Digital Timing, Faster
AD575		HI-574A	Faster, 12 Bit Accuracy
AD582		HA-2425	Acquisition Time
AD583K	HA-2425-5		Identical
AD583K	HA-2425-5		Identical
		HA-5320	Faster, Better Accuracy
AD585		HI-5320/5330	Faster, More Accurate
AD7502		HI-1828A	Maximum Power Supply Voltage
AD7503/01		HI-1818A	On Resistance
AD7506	HI-506		Maximum Power Supply Voltage
AD7507	HI-507		Maximum Power Supply Voltage

Competitive Cross Reference Chart (Continued)

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
ANALOG DEVICES (ADI) (Continued)			
AD7511		HI-201	
AD7512		HI-5043	
AD7521/31	HI-7541		Improved Linearity
AD7541/41A	HI-7541		Lower Output Capacitance
ADADC80		HI-574A	Power, Smaller Package
		HI-674A	Faster, Power, Smaller Package
ADADC84/85		HI-674A	Power, Smaller Package
		HI-774A	Faster, Power, Small Package
ADDAC08		HI-5618	Faster, Application Resistors
ADDAC80		HI-5680	Faster
	HI-5690V		Much Faster
ADDAC85		HI-HI-5685	Faster
	HI-5695V		Much Faster
ADDAC87		HI-5687	Faster
	HI-5697V		Much Faster
ADG200		HI-200	
ADLH0032		HA-5190/2542	Monolithic
H0S050		HA-2542	Monolithic
H0S100	HA-5033		Monolithic
ANALOGIC			
MN4708		HI-508	
		HI-1818A	
MP1812A		HI-5680V	Faster, Monolithic, Power Smaller Package
MP250M		HA-2420/25	Faster, Monolithic, Smaller Package
MP260		HA-2420/25	Monolithic, Smaller Package
MP261		HA-2420	Monolithic, Smaller Package
MP270/271		HA-5320	Monolithic, Smaller Package
BECKMAN			
7541	HI-7541		Faster, Monolithic
7556		HI-574A	Faster, Smaller Package
7580		HI-5680	Faster, Monolithic
BURR-BROWN			
3500		HA-2600	Better AC
3503		HA-2505	Identical
3506	HA-2605		Identical
3507	HA-2525		Identical
3508	HA-2625		Identical
3521		HA-5170	Better AC
3522	HA-5180		Better AC and DC
3523		HA-5180	Better AC
3527	HA-5180		Better AC and DC
3528		HA-5180	Better AC
3550		HA-2541	Monolithic
3553		HA-5033	Monolithic
3554		HA-2542	Monolithic

Competitive Cross Reference Chart (Continued)

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
BURR-BROWN (Continued)			
ADC80		HI-574A	Smaller Package, Power
		HI-674A	Faster, Smaller Package, Power
ADC84/85		HI-674A	Smaller Package, Power
		HI-774A	Faster, Smaller Package, Power
ADC87		HI-774A	Smaller Package, Power
ADC574A	HI-574A		Identical
ADC674A	HI-674A		Identical
DAC70		HI-DAC16	Faster, Monolithic
DAC700/701		HI-DAC16	
DAC702/703		HI-DAC16	
DAC71/72		HI-DAC16	Monolithic, "I" Output
DAC80	HI-5680		Faster, Monolithic, Power
DAC800	HI-5680		Faster, Lower Power
	HI-5690V		Much Faster, Lower Power
DAC85	HI-5685		Faster, Monolithic, Power
DAC850	HI-5685		Faster, Lower Power
	HI-5695V		Much Faster, Lower Power
DAC851	HI-5687		Faster, Lower Power
DAC87	HI-5687		Faster, Monolithic, Power
DAC870	HI-5687		Faster, Monolithic
	HI-5697V		Much Faster, Lower Power
MPC16S	HI-506A-5		Identical
MPC4D	HI-509A-5		Identical
MPC800KG	HI-516-5		Identical
MPC801KG	HI-518-5		Identical
MPC801SG	HI-518-2		Identical
MPC8D	HI-507A-5		Identical
MPC8S	HI-508A-5		Identical
OPA101		HA-5170	
OPA102		HA-5170	
OPA103		HA-5180	Better AC
OPA104		HA-5180	
OPA11	HA-2600		
SCH5320	HA-5320		Identical
SHC298AM		HA-2425	Improved Performance
SHC80/85		HA-2425	Faster, Monolithic, Power
SHC85ET		HA-2420	Faster, Monolithic, Power
SHM60		HA-5320	Monolithic, Smaller Package
DATA DEVICE CORPORATION (DDC)			
ADH051		HA-5330	Monolithic, Smaller Package Power
ADH8585		HI-674A	Smaller Package, Power
		HI-774A	Faster, Smaller Package
ADH8586		HI-774A	Smaller Package, Power
DDC5200		HI-574A	Faster
DDC5210/11		HI-674A	
DDC5212/16		HI-674A	
DDC5240		HI-774A	Smaller Package, Power
DDCADC85		HI-674A	Smaller Package, Power
		HI-774A	Faster, Smaller Package, Power

Competitive Cross Reference Chart (Continued)

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
DATA DEVICE CORPORATION (DDC)			
DDCADC87		HI-674A	Smaller Package, Power
		HI-774A	Faster, Smaller Package, Power
DDCDAC85	HI-5680		Monolithic, Power
DDCDAC85LD	HI-5685		Monolithic, Power
DDCDAC87	HI-5687		Monolithic, Power
DGL13		HA-5320	Monolithic, Smaller Package, Power
THC4460		HA-5320	Monolithic, Smaller Package
DATEL			
ADC52XX		HI-674A	Lower Power
		HI-774A	Faster, Lower Power
ADC574A	HI-574A		Identical
ADC8412		HI-674A	Smaller Package, Power
		HI-774A	Faster, Smaller Package, Power
ADC85C12		HI-674A	Smaller Package, Power
		HI-774A	Faster, Smaller Package, Power
ADC8712		HI-674A	Smaller Package, Power
		HI-774A	Faster, Smaller Package, Power
ADCEH12B1		HI-774A	Faster, Smaller Package, Power
ADCHX12B		HI-574A	Smaller Package, Power
		HI-674A	Faster, Smaller Package, Power
ADCL12B2		HI-574A	Smaller Package
		HI-674A	Faster, Smaller Package
ADCM12B2		HI-674A	Smaller Package
		HI-774A	Faster, Smaller Package
ADCMA12B2A		HI-574A	Faster, Smaller Package
ADCMA12B2B		HI-574A	Smaller Package
		HI-674A	Faster, Smaller Package
AM450	HA-2505		
AM452	HA-2525		
AM460	HA-2605		
AM462	HA-2625		
AM464	HA-2645		
DAC08B		HI-5618	Faster, Application Resistors
DAC562	HI-562A		Identical
DAC71/72		HI-DAC16	Monolithic
DAC7541	HI-7541		Equivalent
DAC85	HI-5685		Faster, Monolithic, Power
	HI-5695V		Much Faster, Monolithic
DAC85C	HI-5680		Faster, Monolithic, Power
	HI-5690V		Much Faster, Monolithic
DAC87	HI-5687		Faster, Monolithic, Power
	HI-5697V		Much Faster, Monolithic
DACHA12B	HI-7541		Faster, Monolithic
DACHP16B		HI-DAC16	Monolithic
DACHR16B		HI-DAC16	Monolithic, Smaller Package
DACHZ12B	HI-5680/85/87		Faster, Monolithic
	HI-5690/5/7V		Much Faster, Monolithic
DACIC10B		HI-5610	Faster, Application Resistors

Competitive Cross Reference Chart (Continued)

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
DATEL (Continued)			
DACIC8B		HI-5618	Faster, Application Resistors
MV1606	HI-506		Identical
MV808	HI-1818A		Identical
MVD409	HI-1828A		Identical
MVD807	HI-507		Identical
MX1606	HI-506A		Identical
MX1616	HI-516		Identical
MX808	HI-508A		Identical
MX818	HI-518		Identical
MXD409	HI-509A		Identical
MXD807	HI-507A		Identical
SHM1C-1	HA-2425		Identical
SHM1C-1M	HA-2420		Identical
SHM20	HA-5320		Identical
SHM6M		HA-5320	Monolithic, Smaller Package
		HA-5330	Faster, Monolithic, Smaller Package
SHM9M		HA-2420	Faster, Monolithic, Smaller Package
SHMLM-2		HA-2420	Faster
EXAR			
XR3417		HC55564	
XR4212		HA-4741	
XRT-5670		HC-5560	More Codes
FAIRCHILD			
μA0801/02		HI-5618	Faster, Application Resistors
μA198		HA-2420	Improved Performance
μA398		HA-2425	Improved Performance
μA565	HI-565A		
HITACHI			
HA-17408		HI-5618	Faster, Application Resistors

Competitive Cross Reference Chart (Continued)

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
HYBRID SYSTEM			
ADC550		HI-574A	Faster, Smaller Package, Power
ADC581		HI-574A	
		HI-674A	Faster
DAC328I-16		HI-DAC16	Monolithic, Smaller Package
DAC331-12	HI-7541		Faster
DAC335-12		HI-5687V	Faster, Monolithic
		HI-5697V	Faster, Monolithic
DAC346C-12		HI-5680V	Faster, Monolithic
		HI-5690V	Faster, Monolithic
DAC347LP-12		HI-5687V	Faster, Monolithic
		HI-5697V	Faster, Monolithic
DAC372		HI-5680	Monolithic
DAC3721-10		HI-5610	Faster, Monolithic, Smaller Package
DAC3721-8		HI-5618	Faster, Monolithic
DAC395-8		HI-5618	Monolithic, Smaller Package
HS346		HA-5320	Faster, Monolithic
HS5200		HI-674A	
		HI-774A	Faster
HS574	HI-574A		Digital Timing, Faster
HS730		HA-5320	Monolithic, Smaller Package
		HA-5330	Faster, Monolithic, Smaller Package
HS7541	HI-7541		Lower Output Capacitance
HSDAC80		HI-5680	Faster, Monolithic, Power
HSDAC87	HI-5687		Faster, Monolithic, Power
MUX201	HI-1818A		Lower Power, Smaller Package
SH725		HA-2420	Faster, Monolithic, Smaller Package
INTECH			
104BIN-P		HI-574A	Smaller Package, Power
		HI-674A	Faster, Smaller Package, Power
411-10BIN		HI-5610	Faster, Smaller Package
416BIN		HI-DAC16	Smaller Package
A3101		HI-674A	Smaller Package, Power
		HI-774A	Faster, Smaller Package, Power
A3155		HI-574A	Smaller Package, Power
		HI-674A	Faster, Smaller Package, Power
AA880/880-2		HA-5320	Faster, Monolithic, Power
A881		HA-5320	Monolithic, Smaller Package, Power
A882/884		HA-2420/25	Faster, Monolithic, Power
ADC111		HI-574A	Smaller Package, Power
		HI-674A	Faster, Smaller Package, Power
ADC2812		HI-574A	Smaller Package, Power
		HI-674A	Faster, Smaller Package, Power
ASH240/250		HA-2420/25	Monolithic, Smaller Package, Power
ASH271		HA-5320	Monolithic, Smaller Package, Power
CY2219		HI-7541	Faster, Smaller Package, Power
CYAAD12QM		HI-574A	Smaller Package, Power
		HI-674A	Faster, Smaller Package, Power

Competitive Cross Reference Chart (Continued)

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
INTEL			
D2912	HC-5512		Lower Power, Lower Noise
D2912A	HC-5512		Lower Power, Lower Noise
	HC-5512A		Lower Power, Lower Noise
D2910	HC-5510		Lower Power, Two Supplies
D2910A	HC-5510		Lower Power, Two Supplies
D2911	HC-5511		Lower Power, Two Supplies
D2911A	HC-5511		Lower Power, Two Supplies
INTERSIL			
AD7521/31	HI-7541		Improved Linearity
AD7541	HI-7541		Lower Output Capacitance
DG200	HI-200		Dielectric Isolation
DG201	HI-201		Dielectric Isolation
HA-2500	HA-2500		Identical
HA-2510	HA-2510		Identical
HA-2520	HA-2520		Identical
HA-2600	HA-2600		Identical
HA-2620	HA-2620		Identical
ICL7611	HA-2720		Better Noise
ICL7615	HA-5141		Better AC and Noise
ICL7621	HA-5142		Better AC and Noise
ICL7642	HA-5144		Better AC and Noise
ICL8017		HA-2520	
ICL8021	HA-2720		Better AC
IH201	HI-201		Dielectric Isolation
IH5040	HI-5040		Dielectric Isolation
IH5041	HI-5041		Dielectric Isolation
IH5042	HI-5042		Dielectric Isolation
IH5043	HI-5043		Dielectric Isolation
IH5044	HI-5044		Dielectric Isolation
IH5045	HI-5045		Dielectric Isolation
IH5046	HI-5046		Dielectric Isolation
IH5047	HI-5047		Dielectric Isolation
IH5048	HI-5048		Dielectric Isolation
IH5049	HI-5049		Dielectric Isolation
IH5050	HI-5050		Dielectric Isolation
IH5051	HI-5051		Dielectric Isolation
IH5108		HI-508A	Signal Range, Same Pinout
IH5110/11		HA-2420/25	Monolithic
IH5112/13		HA-2420/25	Monolithic
IH5114/15		HA-2420/25	Monolithic
IH5200	HI-200		Dielectric Isolation
IH5201	HI-201		Dielectric Isolation
IH5208		HI-509A	V_{IN} Range, Same Pinout
IH6108		HI-508	R_{ON}, DI, Same Pinout
IH6116		HI-506	R_{ON}, DI, Same Pinout
IH6208		HI-509	R_{ON}, DI, Same Pinout
IH6216		HI-507	R_{ON}, DI, Same Pinout

Competitive Cross Reference Chart (Continued)

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
INTRONICS			
A-560	HA-2525		
A-561	HA-2625		
MICRO NETWORKS (MNI)			
ADC80		HI-574A	Smaller Package, Power
		HI-674A	Faster, Smaller Package, Power
DAC80	HI-5680		Faster, Monolithic, Power
	HI-5690V		Much Faster, Monolithic
DAC85	HI-5685		Faster, Monolithic, Power
	HI-5695V		Much Faster, Monolithic
DAC87	HI-5687		Faster, Monolithic, Power
	HI-5697V		Much Faster, Monolithic
MN-ADC84/85/87		HI-674A	Smaller Package, Power
		HI-774A	Faster, Smaller Package, Power
MN3009		HI-5618	Monolithic
MN3014		HI-5618	Monolithic
MN3348		HI-5680V/87V	Faster, Monolithic, Power
MN3349		HI-5685V/87V	Faster, Monolithic
MN3412		HI-7541	Monolithic
MN343/344		HA-2420	Faster, Monolithic
MN346/347		HA-5320	Faster, Monolithic
MN370/371		HI-5687V	Monolithic
MN373		HA-5320	Faster, Monolithic
MN375		HA-5330	Monolithic, Lower Power
MN5200		HI-574A	Faster
MN5210		HI-674A	Two Chip Design
		HI-774A	Faster, Two Chip Design
MN5240		HI-774A	Smaller Package, Power
MN565A	HI-565A		
MN574A	HI-574A		Faster
MICRO POWER SYSTEMS (MPS)			
MP200DI	HI-200		
MP201DI	HI-201		
MP5507	HA-OP07		Better AC
MP5527	HA-OP27		
MP5537	HA-OP27		
MP562	HI-562A		Faster
MP574	HI-574A		Digital Timing, Faster
MP7501/03		HI-1818A	
MP7502		HI-1828A	
MP7506	HI-506		DI Processing
MP7507	HI-507		DI Processing
MP7508DI	HI-508		Input Overvoltage Isolation
MP7509DI	HI-509		Input Overvoltage Isolation
MP7521/31	HI-7541		Improved Performance
MP7541	HI-7541		
MP7621/23	HI-7541		

Competitive Cross Reference Chart (Continued)

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
MITEL			
MT8912	HC-5512		Better Noise, Better Cross Talk
MOSTEK			
MK5912	HC-5512		Better Noise
MOTOROLA			
AD562A		HI-562A	Improved Nonlinearity
MC1408		HI-5618-5	Faster, Application Resistors
MC1430		HA-2600	Better AC
MC1431		HA-2600	Better AC
MC1436		HA-2640	Better AC and DC
MC1508		HI-5618-2	Faster, Application Resistors
MC3403		HA-4741	Better Noise
MC3410		HI-5610-5	Faster, Application Resistors
MC3412	HI-565A		
MC3417		HC-55564	Lower Power, Few External Components
MC3419		HC-5502A	Better Longitudinal Balance, Better Transhybrid Loss, Fewer External Components
		HC-5504	Better Longitudinal Balance, Better Transhybrid Loss, Fewer External Components
MC145439			Chip Reset
MC3510		HI-5610-2	Faster Application Resistors
MC4741	HA-4741		Better AC, Fewer External Components
NATIONAL SEMICONDUCTOR (NSC)			
AD7521/31	HI-7541		Improved Linearity
ADC1080/1280		HI-574A	Smaller Package, Lower Power
		HI-674A	Faster, Smaller Package, Power
ADC1210/11		HI-574A	Faster, Complete A/D
DAC0800/01/02		HI-5618	Faster, Application Resistors
DAC0806/06/08		HI-5618	Faster, Application Resistors
DAC1200/01		HI-5685V/87V	Faster, Lower Power
DAC1218/19	HI-7541		
DAC1220/21/22	HI-7541		
DAC1265	HI-565A		
DAC1266		HI-5660	

Competitive Cross Reference Chart (Continued)

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
NATIONAL SEMICONDUCTOR (NSC) (Continued)			
DAC1280	HI-5690V	HI-5680	Monolithic, Performance
		HI-5690V	Faster, Monolithic
DAC1285		HI-5685/87	Monolithic, Performance
LF0023/43		HA-2420	Monolithic, Performance
LF0053		HA-2420/25	Monolithic
		HA-5320	Faster, Monolithic
LF11201	HI-201		CMOS Dielectric Isolation
LF11508	HI-508-2		Faster, R_{ON}, Power
LF11509	HI-509-2		Faster, R_{ON}, Power
LF13201	HI-201		CMOS Dielectric Isolation
LF13508	HI-508-5		Faster, R_{ON}, Power
LF13509	HI-509-5		Faster, R_{ON}, Power
LF147		HA-5104	
LF198		HA-2420	Improved Performance
LF398		HA-2425	Improved Performance
LH0002	HA-5002		Monolithic, Better AC and DC
LH0003		HA-2520	Monolithic
LH004		HA-2640	Monolithic
LH005		HA-2620	Monolithic
LH0022		HA-5180	Monolithic, Better AC and DC
LH0032	HA-2542		Monolithic
LH0033		HA-5033	Monolithic, Better DC
LH0042		HA-5180	Monolithic, Better AC and DC
LH0062		HA-5160	Monolithic, Better AC
LM108A		HA-5135	Better DC and AC
LM124		HA-4741	Better AC
LM144		HA-2640	
LM208A		HA-5135	Better DC and AC
LM308A		HA-5135	Better DC and AC
LM344		HA-2645	
TP3040	HC-5512		Better Noise
TP3040A	HC-5512A		Better Noise
TP3020	HC-5510		Identical
TP3021	HC-5511		Identical
TP3054	HC-5554		
TP3057	HC-5557		
MF-10	HF-10		Better Noise, Better Crosstalk, Milspec Temperature Range
PRECISION MONOLITHICS, INC. (PMI)			
DAC-08		HI-5618	Faster, Application Resistors
DAC-10		HI-5610	Application Resistors
DAC-100		HI-5610	Faster, Monolithic
DAC-1408		HI-5618-5	Faster, Application Resistors
DAC-1508		HI-5618-2	Faster, Application Resistors
DAC-312		HI-562A	Initial Linearity, Application Resistors
DMX-88	HI-508		V_{IN} Range, Lower Power
GAP01		HA-2400	4 Channels
MUX-08	HI-508		Faster Switching
MUX-16	HI-506		Faster Switching

Competitive Cross Reference Chart (Continued)

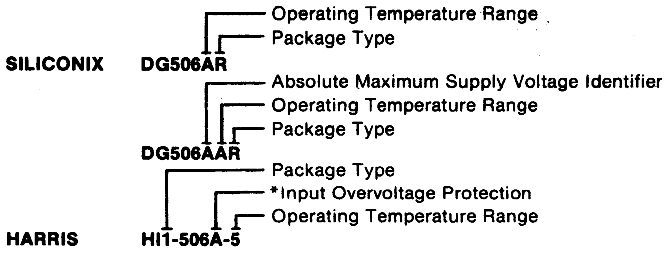
MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
PRECISION MONOLITHICS INC.(PMI) (Continued)			
MUX-24	HI-509		Faster Switching
MUX-28	HI-507		Faster Switching
MUX-88	HI-508		Faster Switching
OP01		HA-2500	Better AC
OP05	HA-5135		Better AC and DC
OP07	HA-OP07		Better AC and DC
OP11		HA-4741	
OP20	HA-5141		Better AC
OP27	HA-OP27		
OP37	HA-OP37		
OP220	HA-5142		Better AC
OP420	HA-5144		Better AC
PM-562		HI-562A	Faster
SMP-10/11		HA-2420/25	Lower Power
		HA-5320	Faster, Improved Accuracy
SMP-81		HA-2420/25	Lower Power
		HA-5320	Faster, Improved Accuracy
RAYTHEON (RAY)			
LM108A		HA-5135	Better AC and DC
LM208A		HA-5135	Better AC and DC
LM308A		HA-5135	Better AC and DC
RC4131	HA-2605		Better AC
RC4136		HA-4741	
		HA-4741	
RC4531	HA-2505		Dielectric Isolation
RC4741	HA-4741		Better AC
RM4131	HA-2600		Better AC
RM4136		HA-4741	
RM4531	HA-2500		Dielectric Isolation
RM4741	HA-4741		Better AC
RCA			
CA3020		HA-2542	
CA3078		HA-5141	
CA31000	HA-2620		
CA6078		HA-2720	
CD4016		HI-201	Better AC and DC
CD22103		HC-5560	More Codes, Asynchronous
SIGNETICS (SIG)			
AM6012		HI-562A	Initial Linearity, Application Resistors
		HI-5660	Initial Linearity, Application Resistors
DAC08		HI-5618	Faster, Application Resistors
LF198		HA-2420	Improved Performance
LF398		HA-2425	Improved Performance
MC1408		HI-5618-5	Faster, Application Resistors
MC1508		HI-5618-2	Faster, Application Resistors
MC3410/10C		HI-5610-5	Faster, Application Resistors

Competitive Cross Reference Chart (Continued)

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
SIGNETICS (SIG) (Continued)			
MC3510		HI-5610-2	Faster, Application Resistors
NE531		HA-2515	
NE5410		HI-5610-5	Faster, Application Resistors
NE5532		HA-5102	Better Noise
NE5533		HA-5112	Better Noise
NE5534		HA-5101/11	
NE5537		HA-2425-5	Lower Power
		HA-5320-5	Faster
NE5539		HA-2539	Better AC
SE531		HA-2510	
SE5410		HI-5610-2	Faster, Application Resistors
SE5532		HA-5102	Better Noise
SE5533		HA-5112	Better Noise
SE5534		HA-5135	
SE5539		HA-2539	Better AC
SILICONIX			
DG181		HI-381	Dielectric Isolation
DG182		HI-381	Dielectric Isolation
DG184		HI-384	Dielectric Isolation
DG185		HI-384	Dielectric Isolation
DG187		HI-387	Dielectric Isolation
DG188		HI-387	Dielectric Isolation
DG190		HI-390	Dielectric Isolation
DG191		HI-390	Dielectric Isolation
DG200A	HI-200		Dielectric Isolation
DG201A	HI-201		Dielectric Isolation
DG211		HI-201	Full Temperature Range Specified
DG300A	HI-300		Dielectric Isolation
DG301A	HI-301		Dielectric Isolation
DG302A	HI-302		Dielectric Isolation
DG303A	HI-303		Dielectric Isolation
DG304A	HI-304		Dielectric Isolation
DG305A	HI-305		Dielectric Isolation
DG306A	HI-306		Dielectric Isolation
DG307A	HI-307		Dielectric Isolation
DG381A	HI-381		Dielectric Isolation
DG384A	HI-384		Dielectric Isolation
DG387A	HI-387		Dielectric Isolation
DG390A	HI-390		Dielectric Isolation
DG5040	HI-5040		Dielectric Isolation
DG5041	HI-5041		Dielectric Isolation
DG5042	HI-5042		Dielectric Isolation

Competitive Cross Reference Chart (Continued)

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
SILICONIX (Continued)			
DG5043	HI-5043		Dielectric Isolation
DG5044	HI-5044		Dielectric Isolation
DG5045	HI-5045		Dielectric Isolation
DG506	HI-506		Lower Power, DI Processing
DG506A	HI-506		Lower Power, DI Processing
DG507	HI-507		Lower Power, DI Processing
DG507A	HI-507		Lower Power, DI Processing
DG508	HI-508		Lower Power, DI Processing
DG508A	HI-508		Lower Power, DI Processing
DG509	HI-509		Lower Power, DI Processing
DG509A	HI-509		Lower Power, DI Processing
DG528		HI-508LA	Overvoltage Protection, DI Processing
DG529		HI-509LA	Overvoltage Protection, DI Processing
SD5200		HI-201HS	Dielectric Isolation
DG271	HI-201HS		Higher Speed
SOLITRON			
CM4016A		HI-201	Better AC and DC
UC4000		HA-2600	
UC4002		HA-2605	
SPRAGUE			
ULN2139		HA-2600	
ULN2151		HA-2600	
ULN2156		HA-2600	
ULN2157		HA-2650	
ULN2158		HA-2650	
ULN2171		HA-2600	
ULN2172		HA-2620	
ULN2173		HA-2600	
ULN2174		HA-2620	
ULN2175		HA-2600	
ULN2176		HA-2600	
TELEDYNE PHILBRICK			
1321	HA-2620		Identical
1322	HA-2520		Identical
1332	HA-2645		Identical
1339		HA-2625	


Operating Temperature Range
Package Type
SILICONIX
DG506AR
Absolute Maximum Supply Voltage Identifier
Operating Temperature Range
Package Type
DG506AAR
Package Type
*Input Overvoltage Protection
Operating Temperature Range
HARRIS
HI1-506A-5

*Note: The Harris HI-50XA family features input overvoltage protection for which there are no Siliconix equivalents.

Competitive Cross Reference Chart (Continued)

MANUFACTURER PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	HARRIS ADVANTAGES
TELEDYNE PHILBRICK (Continued)			
1341	HA-2540		Identical
1342	HA-2539		Identical
1343	HA-5190		Identical
1344	HA-5160		Identical
1345	HA-5162		Identical
1346	HA-5180		Identical
1347	HA-5180A		Identical
1437		HA-2541	Monolithic
1438		HA-2541	Monolithic
1460		HA-2542	Monolithic
1466		HA-2542	Monolithic
4058		HI-5680	Monolithic
4058-83		HI-5687	Monolithic
4068A	HI-562A		Identical
4084	HI-5618		Identical
4088	HI-DAC16		Identical
4189		HI-774A	
4551	HI-507A		Identical
4552	HI-506A		Identical
4553	HI-509A		Identical
4554	HI-508A		Identical
4853		HA-5320	Monolithic, Smaller Package
4854		HA-2420	Faster, Monolithic, Smaller Package
4856	HA-2420/25		Identical
4857		HA-5320	Monolithic, Smaller Package, Power
4866	HA-5320		Identical
7541	HI-7541		Identical
DAC80I/V	HI-5680I/V		Identical
TP5210		HI-674A	
		HI-774A	Faster
TP565A	HI-565A		Identical
TP574A	HI-574A		Identical
TPADC85/87		HI-774A	
TEXAS INSTRUMENTS (TI)			
TCM2201		HC-5560	Lower Power, More Codes
TCM2910A		HC-5510	CMOS
TCM2911A		HC-5511	CMOS
TCM2912C	HC-5512		Better Noise, Better Cross Talk, Lower Power
TCM4110	HC-5510		Lower Power, Two Supplies
TCM4910	HC-5510		Lower Power, Two Supplies
TL022	HA-5142		Better DC
TL044	—	HA-5144	Better DC
TRANSITRON			
TOA7709	HA-2600		
TOA8709	HA-2605		

High Temperature Electronics

To serve the growing need for electronics that will operate in severe high temperature environments, Harris will offer integrated circuits that have been characterized over elevated temperatures and that have electrical characteristics guaranteed at 200°C.

Typical applications include:

- Well Logging
- Industrial Process Control
- Engine Control and Testing
- High Temperature Data Acquisition Systems

It is the intention of Harris Semiconductor to make available in the high temperature series (identified by the -1 suffix following the device part number) all the basic elements required for the designer to build a data acquisition system that will function to specified limits at 200°C.

The devices to be offered:

- Operational Amplifiers
- Analog Switches
- Analog Multiplexers
- 12 Bit Digital to Analog Converter
- Sample & Hold Amplifiers
- A/D Converters

All parts offered in the -1 series have had their electrical performance parameters characterized up to 250°C.

Production flow of -1 parts includes 160 hours burn-in and final electrical test at 200°C.

Devices available Now:

• HA-2420-1	Sample & Hold Amplifier
• HA-2600-1	Operational Amplifier
• HA-2620-1	Operational Amplifier
• HI-200-1	Analog Switch
• HI-201-1	Analog Switch

Consult factory for price and availability information.

Advanced Packaging Techniques

Harris Semiconductor is now offering Leadless Chip Carriers (LCC) as a packaging option on various Analog integrated circuits. An LCC is a square or rectangular package for an Integrated Circuit (IC) that is manufactured in the same manner as a conventional side-braze dual-in-line package (DIP). The LCC is essentially comprised of the cavity and seal ring section of a standard DIP. It offers the user a means of achieving high density system configurations while retaining the reliability benefits of hermetic IC packaging. Figure 1 provides a comparison of the construction of an LCC and a conventional side-braze DIP.

The LCC's two principle advantages over conventional side-braze DIPs are packaging density and electrical performance. Packaging density is the number one advantage to an LCC over a side-braze DIP. The size of a DIP is governed primarily by the number of leads required and not by the size of the IC. As pin count increases, more and more of the DIP package is used only to provide an electrical trace path to the external leads. The size of an LCC is dependent on the size of the die not on the number of leads. As pin count increases, overall size increases but at a much slower rate. Table 1 provides a comparison between the areas of 18, 28 and 48 lead LCCs to 18, 28 and 48 lead side-braze DIPs.

The chart indicates a 270% improvement in packaging area for the 18 lead LCC, and 542% improvement for the 48 lead LCC. Obviously, sizeable savings in circuit board area can be achieved with this packaging option. The second major advantage of the LCC is in electrical performance. The package size and geometry also dictates trace length and uniformity. Figure 2 provides a comparison between the trace lengths for various LCCs and side-braze DIPs. As pin count goes up, trace lengths get longer, adding resistance and capacitance unequally around the package. As ICs get faster and more complex these factors start to become a limiting factor on performance. LCCs minimize this effect by maintaining, as close as possible, uniform trace length so that the package is significantly smaller determinant of system performance.

The LCC also offers environmental advantages over "chip-and-wire" manufacturing techniques used in high density hybrid circuits. An IC can be fully tested, burned-in and processed in an LCC, thereby guaranteeing its performance.

The IC is further protected by a small hermetic package in which internal wafer vapor content can be carefully controlled during production.

Advanced Packaging Techniques (Continued)

In summary, Harris Semiconductor Leadless Chip Carriers use a proven technology to provide a reliable high density, high performance packaging option for today's systems.

A list of products available in LCC form is provided in the Packaging Section on page 13-3. Consult the factory or your Harris sales representative for pricing and availability.

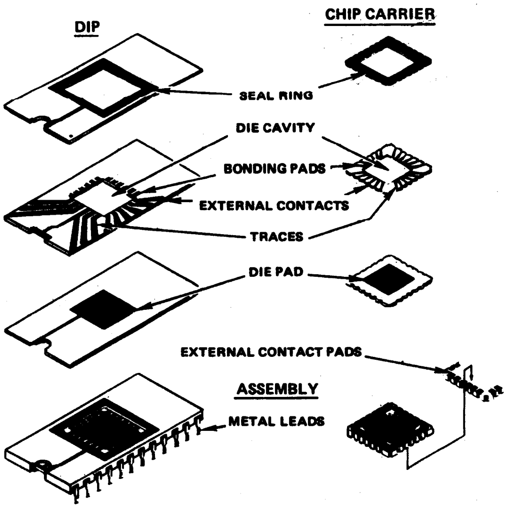
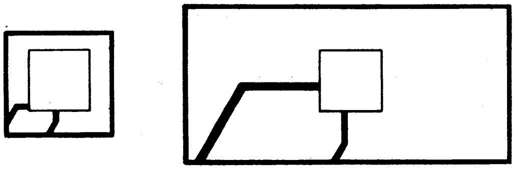

DIP
CHIP CARRIER
SEAL RING
DIE CAVITY
BONDING PADS
EXTERNAL CONTACTS
TRACES
DIE PAD
EXTERNAL CONTACT PADS
ASSEMBLY
METAL LEADS

FIGURE 1. Exploded view of Chip Carrier and DIP.



LEAD COUNT	LONGEST TRACE DIP LONGEST TRACE CC	LONGEST TRACE SHORTEST TRACE	
		CC	DIP
18	2:1	1.5:1	6:1
24	4:1	1.5:1	3:1
40	5:1	1.5:1	6:1
54	6:1	1.5:1	7:1

FIGURE 2. Electrical Performance (Resistance and Speed)

TABLE I

LEAD COUNT	LCC AREA	DIP AREA	DIP AREA VS. LCC AREA
18	0.10	0.22	270%
28	0.20	0.84	420%
48	0.31	1.68	542%

(All units in square inches)

ANALOG

Operational Amplifiers, Comparators & Control Functions

2

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ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

Operational Amplifiers, Comparators and Control Functions

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HA-2650/55	Dual High Performance Operational Amplifiers	2-88
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HA-5033	Wideband, High Slew Rate Buffer Amplifier	2-120
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HA-5102	Dual Low Noise Operational Amplifier	2-129
HA-5104	Quad Low Noise Operational Amplifier	2-129
HA-5112	Dual High Slew Rate, Low Noise Operational Amplifier	2-129
HA-5114	Quad High Slew Rate, Low Noise Operational Amplifier	2-129
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Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H A 7 - 5135 - 5

PREFIX:
H (HARRIS)

FAMILY:
- A — Analog
- C — Communications
- D — Digital
- F — Filters
- I — Interface
- M — Memory
- V — Analog, High Voltage
- Y — Analog Hybrids

PACKAGE:
- 1 — Dual-In-Line, Ceramic
- 2 — Metal Can
- 3 — Dual-In Line, Plastic
- 4 — Leadless Carriers
- 5 — LCC Hybrid
- 7 — Mini-DIP, Ceramic
- 0 — Chip Form

PART NUMBER

TEMPERATURE:
- 1 — 0°C to +200°C ✱
- 2 — -55°C to +125°C
- 4 — -25°C to +85°C
- 5 — 0°C to +75°C
- 6 — 100% +25°C Probe (Dice Only)
- 7 — Dash-7 High Reliability Commercial Product. 0°C to +75°C
- 8 — Dash-8 Program HA2-2520-8 (Example only)
- 9 — -40°C to +85°C

✱ Special high temperature testing available on certain product types. Consult factory for availability.

Standard Products Packaging Availability

PACKAGE	PLASTIC DIP 3-		CERAMIC DIP 1-							CERAMIC MINI DIP 7-				METAL CAN 2-					SURFACE MOUNT LCC 4-	SURFACE MOUNT PLCC 4P-
TEMPERATURE	-5	-7	-1	-2	-4	-5	-7	-8	-9	-2	-4	-5	-8	-1	-2	-4	-5	-8	-8	-5
DEVICE NUMBER																				
HA-OP07	X									X		X	X		X		X	X		
HA-OP27	X										X		X		X	X		X	X	
HA-OP37	X										X		X		X	X		X	X	
HA-2400				X				X											X	
HA-2404					X															
HA-2405						X														
HA-2406	X					X														
HA-2500										X			X		X			X		
HA-2502										X			X		X			X		
HA-2505	X											X					X			
HA-2510										X			X		X			X	X	
HA-2512										X			X		X			X		
HA-2515	X											X					X			
HA-2520										X			X		X			X	X	
HA-2522										X			X		X			X		
HA-2525	X											X					X			
HA-2539	X			X	X	X		X											X	
HA-2540	X			X	X	X		X											X	
HA-2541						X									X		X	X		
HA-2542	X			X		X		X							X		X	X		
HA-2544	X									X		X	X		X		X	X		
HA-2600										X			X	X	X			X		
HA-2602										X			X		X			X		
HA-2605	X											X					X			
HA-2620				X				X		X			X	X	X			X		
HA-2622				X				X							X			X		
HA-2625	X					X						X					X			

Standard Products Packaging Availability (Continued)

PACKAGE	PLASTIC DIP		CERAMIC DIP							CERAMIC MINI DIP				METAL CAN					SURFACE MOUNT LCC	SURFACE MOUNT PLCC
	3-		1-							7-				2-					4-	4P-
TEMPERATURE	-5	-7	-1	-2	-4	-5	-7	-8	-9	-2	-4	-5	-8	-1	-2	-4	-5	-8	-8	-5
DEVICE NUMBER																				
HA-2630															X			X		
HA-2635																	X			
HA-2640										X			X		X			X		
HA-2645												X					X			
HA-2650				X				X		X			X		X			X		
HA-2655						X						X					X			
HA-2720										X			X		X			X		
HA-2725												X					X			
HA-4600				X		X		X												
HA-4602				X				X												
HA-4605						X														
HA-4741	X			X		X	X	X											X	
HA-4900				X				X												
HA-4902				X				X											X	
HA-4905						X														
HA-5002										X		X	X		X		X	X	X	
HA-5033	X														X		X	X		
HA-5101	X									X		X	X		X		X	X		
HA-5102	X									X		X	X		X		X	X	X	
HA-5104	X			X		X		X											X	
HA-5111	X									X		X	X		X		X	X		
HA-5112	X									X		X	X		X		X	X	X	
HA-5114	X			X		X		X											X	
HA-5130	X									X		X	X		X		X	X		
HA-5134				X		X		X												
HA-5135	X									X		X	X		X		X	X	X	
HA-5141	X									X		X	X		X		X	X		
HA-5141A	X									X		X	X		X		X	X		
HA-5142	X									X		X	X		X		X	X	X	
HA-5142A	X									X		X	X		X		X	X		
HA-5144	X			X		X		X											X	
HA-5144A	X			X		X		X											X	
HA-5147	X									X		X	X		X		X	X	X	
HA-5151	X									X		X	X		X		X	X		
HA-5152	X									X		X	X		X		X	X	X	
HA-5154	X			X		X		X											X	
HA-5160															X		X	X		
HA-5162																	X			
HA-5170	X									X	X	X	X		X	X	X	X	X	
HA-5180	X									X	X	X	X		X	X	X	X		
HA-5180A										X	X	X	X		X	X	X	X		
HA-5190				X				X							X			X	X	
HA-5195						X											X			
HV-1000	X	X																		

Selection Guide

OPERATIONAL AMPLIFIERS: HIGH SLEW-RATE

	Part Number	Temp. Range			Slew Rate (V/μs)	Bandwidth Product (MHz)	Full Power Bandwidth (MHz)	Bias Current (nA)	Open Loop Gain (V/mV)	Minimum Gain Stable	Comments	Page
		-55°C to +125°C	0°C to +75°C	-40°C to +85°C								
SINGLES	HA-OP37	X	X		17	63	0.3	8	1500	5	Low Noise	2-25
	HA-5147	X	X		35	100	0.5	8	1800	10	Low Noise	2-148
	HA-2620	X			35	100	0.6	1	150	5		2-76
	HA-2622	X			35	100	0.6	5	150	5		2-76
	HA-2625		X		35	100	0.6	5	150	5		2-76
	HA-2512	X			60	12	1.0	125	15	Unity		2-42
	HA-2515		X		60	12	1.0	125	15	Unity		2-42
	HA-2510	X			65	12	1.0	100	15	Unity		2-42
	HA-5162	X	X		70	100	1.0	0.02	100	10	JFET	2-157
	HA-5160	X	X		120	100	1.9	0.02	150	10	JFET	2-157
	HA-2520	X			120	20	1.9	100	15	3		2-46
	HA-2522	X			120	20	1.9	125	15	3		2-46
	HA-2525		X		120	20	1.9	125	15	3		2-46
	HA-5190	X			200	150	6.5	5000	30	5		2-176
	HA-5195		X		200	150	6.5	5000	30	5		2-176
	HA-2541	X	X		300	40	4.7	6000	10	Unity		2-62
	HA-2542	X	X		350	60	5.5	6000	10	2	Power Output	2-66
	HA-2540	X	X	X	400	400	6.0	5000	15	10		2-56
	HA-2539	X	X	X	600	600	9.5	5000	15	10		2-50
	HA-5111	X	X		20	60	0.3	150	500	10	Low Noise	2-128
DUAL	HA-5112	X	X		20	60	0.3	130	250	10	Low Noise	2-129
QUADS	HA-5114	X	X		20	60	0.3	130	250	10	Low Noise	2-129
	HA-2400	X			30	40	0.5	50	150	10	Addressable	2-30
	HA-2404			X	30	40	0.5	50	150	10	Addressable	2-30
	HA-2405		X		30	40	0.5	50	150	10	Addressable	2-30
	HA-2406		X		30	40	0.5	50	150	10	Addressable	2-34

Selection Guide (Continued)

OPERATIONAL AMPLIFIERS: WIDE BANDWIDTH

	Part Number	Temp. Range			Gain Bandwidth Product (MHz)	Full Power Bandwidth (MHz)	Slew Rate (V/μs)	Bias Current (nA)	Open Loop Gain (V/mV)	Minimum Gain Stable	Comments	Page
		-55°C to +125°C	0°C to +75°C	-40°C to +85°C								
SINGLES	HA-2510	X			12	1.0	65	100	15	Unity		2-42
	HA-2512	X			12	1.0	60	125	15	Unity		2-42
	HA-2515		X		12	1.0	60	125	15	Unity		2-42
	HA-2600	X			12	0.075	7	1	150	Unity		2-72
	HA-2602	X			12	0.075	7	15	150	Unity		2-72
	HA-2605		X		12	0.075	7	5	150	Unity		2-72
	HA-2520	X			20	2.0	120	100	15	3		2-46
	HA-2522	X			20	1.9	120	125	15	3		2-46
	HA-2525		X		20	1.9	120	125	15	3		2-46
	HA-2541	X	X		40	4.7	300	6000	10	Unity		2-62
	HA-2542	X	X		60	5.5	350	6000	10	2	Power Output	2-66
	HA-OP37	X	X		63	0.3	17	8	1800	5	Low Noise	2-25
	HA-5147	X	X		100	0.5	35	8	1800	10	Low Noise	2-148
	HA-2620	X			100	0.6	35	1	150	5		2-76
	HA-2622	X			100	0.6	35	5	150	5		2-76
	HA-2625		X		100	0.6	35	5	150	5		2-76
	HA-5160	X	X		100	1.9	120	0.02	150	10	JFET	2-157
	HA-5162	X	X		100	1.1	70	0.02	100	10	JFET	2-157
	HA-5190	X			150	6.5	200	5000	30	5		2-176
	HA-5195		X		150	6.5	200	5000	30	5		2-176
	HA-2540	X	X	X	400	6.0	400	5000	30	10		2-56
	HA-2539	X	X	X	600	9.5	600	5000	30	10		2-50
DUAL	HA-5112	X	X		60	0.3	20	130	250	10	Low Noise	2-129
QUADS	HA-2400	X			40	0.5	30	50	150	10	Addressable	2-30
	HA-2404			X	40	0.5	30	50	150	10	Addressable	2-30
	HA-2405		X		40	0.5	30	50	150	10	Addressable	2-30
	HA-2406		X		40	0.5	30	50	150	10	Addressable	2-34
	HA-5114	X	X		60	0.3	20	130	250	10	Low Noise	2-129

Selection Guide (Continued)

OPERATIONAL AMPLIFIERS: PRECISION

Part Number	Temperature Range -55°C to +125°C	Temperature Range 0°C to +75°C	Temperature Range -40°C to +85°C	Offset Voltage (μV)	Offset Voltage Drift (μV/°C)	Bias Current (nA)	Open Loop Gain (V/mV)	Noise Current (pA/√Hz)	Noise Voltage (nV/√Hz)	CMRR (dB)	PSRR (dB)	Supply Current (mA)	Comments	Page
HA-5180	X	X	X	100	5	0.00003	1000	0.01	70	110	105	0.8	JFET	2-169
HA-5170	X	X	X	100	2	0.02	600	0.01	10	100	105	1.9	JFET	2-164
HA-5180A	X	X	X	100	5	0.00003	1000	0.01	70	110	105	0.8	JFET	2-169
HA-OP07C		X		60	0.4	1	10000	0.14	9.8	120	130	1		2-12
HA-OP07E		X		10	0.4	1	10000	0.14	9.6	120	130	1		2-12
HA-OP07	X			10	0.4	1	10000	0.14	9.6	120	130	1		2-12
HA-OP07A	X			10	0.4	1	10000	0.14	9.6	120	130	1		2-12
HA-OP27	X	X		10	0.2	10	1500	0.60	3	120	120	3		2-20
HA-OP37	X	X		10	0.2	10	1500	0.60	3	120	120	3	High Speed	2-25
HA-5147	X	X		10	0.2	10	1800	0.60	3	120	120	3	High Speed	2-148
HA-5134	X	X		50	2.5	2.0	1000	0.60	7	120	120	5	Quad	2-141

OPERATIONAL AMPLFIERS: LOW POWER

	Part Number	Temperature Range -55°C to +125°C	Temperature Range 0°C to +75°C	Temperature Range -40°C to +85°C	Supply Current (μA)	Supply Range (V)	Slew Rate (V/μs) at Indicated Supply Current	Gain Bandwidth Product (kHz) at Indicated Supply Current	Output Swing (V) ±15V Power Supplies	Offset Voltage (mV)	Comments	Page
SINGLES	HA-5141	X	X		50	+2/+40	1.0	400	0/+3(+5V_S)	0.7		2-142
	HA-5141A	X	X		45	+2/+40	1.5	400	0/+4(+5V_S)	0.5		2-142
	HA-5151	X	X		200	+2/+40	4	1300	±10	2	Lower Noise	2-153
DUALS	HA-5142	X	X		50	+2/+40	1.0	400	0/+3(+5V_S)	0.7		2-142
	HA-5142A	X	X		45	+2/+40	1.5	400	0/+4(+5V_S)	0.5		2-142
	HA-5152	X	X		200	+2/+40	4	1300	±10	2	Lower Noise	2-153
QUADS	HA-5144	X	X		50	+2/+40	1.0	400	0/+3(+5V_S)	0.7		2-142
	HA-5144A	X	X		45	+2/+40	1.0	400	0/+3(+5V_S)	0.7		2-142
	HA-5154	X	X		200	+2/+40	4	1300	±10	2	Lower Noise	2-153

Selection Guide (Continued)

OPERATIONAL AMPLIFIERS: GENERAL PURPOSE

	Part Number	Temp. Range			Gain Bandwidth Product (MHz)	Slew Rate (V/µs)	Offset Voltage (mV)	Bias Current (nA)	Noise Voltage (nV/√Hz)	Open Loop Gain (V/mV)	Common Mode Range (V) ±15V Power Supplies	Supply Current (mA)	Comments	Page
		-55°C to +125°C	0°C to +75°C	-40°C to +85°C										
SINGLES	HA-2600	X			12	7	0.5	1	16	150	±11	3		2-72
	HA-2602	X			12	7	3	15	16	150	±11	3		2-72
	HA-2605		X		12	7	3	5	16	150	±11	3		2-72
	HA-5101	X	X		8	3	0.5	130	4.3	250	±12	5	Low Noise	2-128
DUALS	HA-5102	X	X		8	3	0.5	130	4.3	250	±12	5	Low Noise	2-129
	HA-5112	X	X		60	20	0.5	130	4.3	250	±12	5	Low Noise	2-129
QUADS	HA-2400	X			40	30	4	50	20	150	±9	4.8	Addressable	2-30
	HA-2404			X	40	30	4	50	20	150	±9	4.8	Addressable	2-30
	HA-2405		X		40	30	4	50	20	150	±9	4.8	Addressable	2-30
	HA-2406		X		40	30	4	50	20	150	±9	4.8	Addressable	2-34
	HA-5104	X	X		8	3	0.5	130	4.3	250	±12	5	Low Noise	2-129
	HA-5114	X	X		60	20	0.5	130	4.3	250	±12	5	Low Noise	2-129

OPERATIONAL AMPLIFIERS: HIGH VOLTAGE

Part Number	Features	Applications	Page
HA-2640	• Slew Rate: 1V/µs	• Industrial Control Systems	2-84
HA-2645	• Bandwidth: 4MHz • Input Offset Voltage: 4mV • Offset Current: 5nA • Output Voltage Swing: ±35V • Input Voltage Range: ±35V • Supply Range: ±10V to ±40V • Output Overload Protection	• Power Supplies • High Voltage Regulators • Resolver Excitation • Signal Conditioning • Signal Conditioning	2-84

Selection Guide (Continued)

OPERATIONAL AMPLIFIERS: ADDRESSABLE

Part Number	Features	Applications	Page
HA-2400 HA-2404 HA-2405	• Four Channels Addressable • High Slew Rate 30V/µs • Wide Gain Bandwidth	• Signal Selection/Multiplexing • Variable gain stages • Oscillators	2-30
HA-2406	• Products: 40MHz • High Gain: 150K • TTL Compatible	• Filters • Comparators • Integrators	2-34

OPERATIONAL AMPLIFIERS: CURRENT BUFFERS

Part Number	Features	Applications	Page
HA-5033	• Differential Phase Error: 0.1° • Differential Gain Error: 0.1% • High Slew Rate: 1300V/µs • Wide Power Bandwidth: 80MHz • Fast Rise Time: 3ns • Wide Power Supply Range: ±5/±16V	• Video Buffers • HF Buffers • Op Amp Isolation Buffers • High Speed Line Drivers • Impedance matching	2-120
HA-5002	• High Slew Rate 1300V/µs • High Output Current 200mA • Low Quiescent Current 9mA		2-116
HA-2630	Also see HA-2542		

COMPARATORS

Part Number	Features	Applications	Page
HA-4900 HA-4902 HA-4905	• Fast Response Time: 130ns • Low Offset Voltage: 2mV • Low Offset Current: 10nA • Single or Dual Supply • Analog and logic supplies separated for easier interface and noise immunity	• Threshold Detectors • Zero Crossing Detectors • Window Detectors • Interface • Oscillators	2-109

CONTROL FUNCTIONS

INDUCTION MOTOR ENERGY SAVER

Part Number	Features	Applications	Page
HV-1000	• HV-1000: Operates directly off 110 VAC line • No Power Supply Required • Provides Power Savings from 10% to 50% for motors with light or variable loads • SCR output triggers Triac directly • Load Anticipator senses shock loads and responds instantly with full power • Withstands line surges up to 3500V • Allows motor to run cooler and quieter • Can be mounted inside motor • Requires only 3 resistors, 3 capacitors and one Triac to assemble complete controller	• Power Tools • Disk Drives • Heat Pumps • Presses • Conveyors • Any application where a single phase motor will occasionally drive at less than its rated load	2-183

Operational Amplifiers Glossary

AVERAGE INPUT OFFSET CURRENT DRIFT ($\Delta IOS/\Delta T$) - The ratio of the change in the offset current to the change in temperature producing it.

AVERAGE OFFSET VOLTAGE DRIFT ($\Delta V_{OS}/\Delta T$) - The ratio of the change in the offset voltage to the change in temperature producing it.

BANDWIDTH (BW) - That frequency at which the gain of the amplifier is 3dB below its low frequency value.

CHANNEL SEPARATION - The ratio of the input of a driven amplifier to the output of an adjacent undriven amplifier.

COMMON MODE INPUT VOLTAGE (V_{IC}) - The average of the two input voltages.

COMMON MODE INPUT VOLTAGE RANGE (V_{ICR}) - The range of voltage that if exceeded at either input terminal will cause the amplifer to cease operating properly.

COMMON MODE REJECTION RATIO (CMRR) - The ratio of the differential voltage gain to the common mode voltage gain.

Note: This is measured by determining the ratio of the change in input common-mode voltage to the resulting change in offset voltage.

COMMON MODE RESISTANCE (r_{ic}) - The value of resistance looking into both inputs tied together.

DIFFERENTIAL INPUT RESISTANCE (r_{id}) - The value of resistance between two ungrounded inputs.

FULL POWER BANDWIDTH (FPBW) - The maximum frequency at which a full size undistorted sine wave can be obtained at the output of the amplifier.

GAIN BANDWIDTH PRODUCT - The product of the gain and bandwidth at some specified frequency.

INPUT BIAS CURRENT (I_{BIAS}) - The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT CAPACITANCE (C_{IN}) - The capacitance of either input with the other grounded.

INPUT NOISE CURRENT (i_n) - The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance.

INPUT OFFSET CURRENT (I_{OS}) - The difference in the currents flowing into the two input terminals when the output is at zero voltage.

INPUT OFFSET VOLTAGE (V_{OS}) - The differential D.C. voltage required to zero the output voltage with no input signal or load. Input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT NOISE VOLTAGE (e_n) - The input noise voltage that would reproduce the noise seen at the output if all the amplifier noise sources and source resistances were set to zero.

INPUT RESISTANCE (R_{IN}) - The ratio of the change in input voltage to the change in input current at either terminal with the other grounded.

LARGE SIGNAL VOLTAGE GAIN (A_v) - The ratio of the peak to peak output voltage swing (over a specified range) to the change in input voltage required to drive the output.

OUTPUT CURRENT (IOUT) - The output current available from the amplifier at some specified output voltage.

OUTPUT RESISTANCE (RO) - The ratio of the change in output voltage to the change in output current.

OUTPUT SHORT CIRCUIT CURRENT (I_{SC}) - The maximum output current available from the amplifier with the output shorted to ground (or other specified potential).

OUTPUT VOLTAGE SWING (VOUT) - The peak to peak output voltage swing, referred to ground, that can be obtained without clipping under specified loading conditions.

OVERSHOOT - Peak excursion above final value of an output step response.

POWER SUPPLY REJECTION RATIO (PSRR) - The ratio of the change in input offset voltage to the change in power supply voltage producing it.

RISE TIME (t_r) - The time required for an output voltage step to change from 10% to 90% of its final value, when the input is subjected to a small voltage pulse.

SETTLING TIME - The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE (SR) - The rate of change of the output under large signal conditions. Slew rate may be specified separately for both positive and negative going changes.

SUPPLY CURRENT (I_S) - The current required from the power supply to operate the amplifier with no load and the output at zero volts.

SUPPLY VOLTAGE RANGE - The range of power supply voltage over which the amplifier may be safely operated.

UNITY GAIN BANDWIDTH - The frequency range from D.C. to that frequency where the amplifiers open loop gain is unity.

HARRIS

HA-OP07

Precision Operational Amplifier

FEATURES

• LOW OFFSET VOLTAGE	10μV
• LOW OFFSET VOLTAGE DRIFT	0.4μV/°C
• LOW NOISE	$9\text{nV}/\sqrt{\text{Hz}}$
• OPEN LOOP GAIN	10^7
• BANDWIDTH (UNITY GAIN)	2.5MHz
• ALL BIPOLAR CONSTRUCTION	
• PIN CONFIGURATION SAME AS OP-07	

APPLICATIONS

- HIGH GAIN INSTRUMENTATION
- PRECISION DATA ACQUISITION
- PRECISION INTEGRATORS
- BIOMEDICAL AMPLIFIERS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

The HA-OP07 is a precision operational amplifier manufactured using a combination of key technological advancements to provide outstanding input characteristics.

A Super Beta input stage is combined with laser trimming, dielectric isolation, and matching techniques to produce 10μV (Max.) input offset voltage and 0.4 μV/°C input offset voltage average drift. Other features enhanced by this process include 9nV (Typ.) Input Noise Voltage, 1nA Input Bias Current, and 140dB Open Loop Gain.

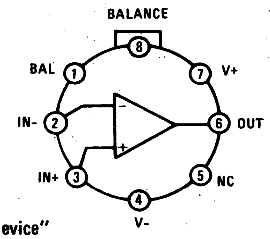
These features coupled with 120dB CMRR and PSRR make the HA-OP07 an ideal device for precision DC instrumentation amplifiers. Excellent input characteristics in conjunction with 2.5MHz bandwidth and 0.8V/μs slew rate, makes this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

The HA-OP07 is packaged in an 8 pin (TO-99) can, an 8 lead Cerdip, an 8 pin epoxy DIP and is compatible with OP-07 configuration.

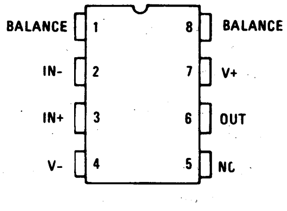
HA-OP07/HA-OP07A are specified for -55°C to +125°C operation while the HA-OP07C/HA-OP07E operate from 0°C to +75°C.

PINOUTS

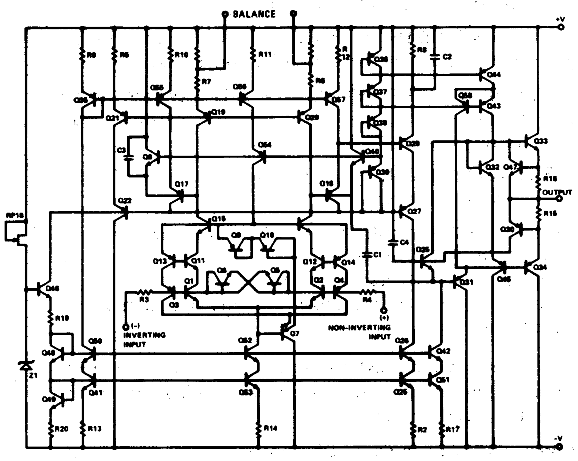
TOP VIEWS



"Caution:
ESD Sensitive Device"



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±22V
Internal Power Dissipation (Note 2)	500mW
Differential Input Voltage	±15V
Input Voltage	±V Supplies
Output Short Circuit Duration	Indefinite

Storage Temperature Range	
J and Z Packages	-65°C to +150°C
Operating Temperature Range	
OP-07A, OP-07	-55°C to +125°C
OP-07E, OP-07C	0°C to +75°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^{\circ}C$, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	HA-OP07A			HA-OP07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		–	10	25	–	10	75	μV
I_{OS}	Input Offset Current				2.0			2.8	nA
I_B	Input Bias Current		–	±1.0	±2.0	–	±1.0	±3.0	nA
e_{np-p}	Input Noise Voltage	0.1Hz to 10Hz	–	–	0.6	–	–	0.6	μV_{p-p}
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 100Hz$ $f_0 = 1000Hz$	– – –	13.0 10.0 9.6	18.0 13.0 11.0	– – –	13.0 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
I_{np-p}	Input Noise Current	0.1Hz to 10Hz	–	15.0	30	–	15.0	30	pA_{p-p}
I_n	Input Noise Current Density	$f_0 = 10Hz$ $f_0 = 100Hz$ $f_0 = 1000Hz$	– – –	0.4 0.17 0.14	0.80 0.23 0.17	– – –	0.4 0.17 0.14	0.80 0.23 0.17	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance - Differential Mode		20	30	–	20	30	–	MΩ
IVR	Input Voltage Range		±12	–	–	±12	–	–	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	110	120	–	110	120	–	dB
PSRR	Power Supply Rejection Ratio	$V_S \pm 3V$ to $\pm 18V$	100	130	–	100	130	–	dB
A_{VO}	Large Signal Voltage Gain	(Note 3)	120	140	–	120	140	–	dB
V_O	Output Voltage Swing	$R_L = 2K\Omega$ $R_L = 600\Omega$	±12 ±10	±12	–	±12 ±10	±12	–	V
SR	Slewing Rate	$R_L \geq 2k\Omega$	0.5	0.8	–	0.5	0.8	–	V/µs
BW	Closed Loop Bandwidth	$A_{VCL} = +1.0$	0.6	2.5	–	0.6	2.5	–	MHz
R_O	Open Loop Output Resistance	f = 100Hz	–	45	–	–	45	–	Ω
I_{CC}	Supply Current	No Load	–	1.0	1.3	–	1.0	1.3	mA
P_D	Power Consumption	$V_{CC} = \pm 15V$ $V_{CC} = \pm 3V$		30 6.0	39 7.8		30 6.0	39 7.8	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	HA-OP07E			HA-OP07C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		–	50	130	–	50	250	μV
TCV_{OS}	Avg. Input Offset Voltage Drift Without External Trim		–	0.4	0.6	–	0.4	1.3	$\mu V/^{\circ}C$
I_{OS}	Input Offset Current		–	–	5.3	–	–	8.0	nA
TCI_{OS}	Avg. Input Offset Current Drift		–	20	40	–	20	50	$pA/^{\circ}C$
I_B	Input Bias Current		–	–	5.5	–	–	9.0	nA
TCI_B	Avg. Input Bias Current Drift		–	20	40	–	20	50	$pA/^{\circ}C$
IVR	Input Voltage Range		±12	–	–	±12	–	–	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	110	120	–	106	120	–	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	100	130	–	94	130	–	dB
A_{VO}	Large Signal Voltage Gain	(Note 3)	120	–	–	100	–	–	dB
V_O	Output Voltage Swing	$R_L = 600\Omega$ $R_L = 2k\Omega$	±10 ±12	–	–	±10 ±11.5	–	–	V

NOTES:
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$; $R_L = 2k\Omega$. Gain dB = $20 \log_{10}$ Average

$$\therefore 120dB = 1000V/mV$$
$$140dB = 10{,}000V/mV$$

SPECIFICATIONS *(Continued)*

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^oC$, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	HA-OP07E MIN	HA-OP07E TYP	HA-OP07E MAX	HA-OP07C MIN	HA-OP07C TYP	HA-OP07C MAX	UNITS
V_{OS}	Input Offset Voltage		–	10	75	–	60	150	μV
I_{OS}	Input Offset Current		–	–	3.8	–	–	6.0	nA
I_B	Input Bias Current		–	±1.0	±4.0	–	±1.0	±7.0	nA
e_{np-p}	Input Noise Voltage	0.1Hz to 10Hz	–	–	0.6	–	–	0.65	μV_{p-p}
e_n	Input Noise Voltage Density	f_o = 10Hz	–	13.0	18.0	–	13.0	20.0	$nV/\sqrt{Hz}$
		f_o = 100Hz	–	10.0	13.0	–	10.2	13.5	
		f_o = 1000Hz	–	9.6	11.0	–	9.8	11.5	
I_{np-p}	Input Noise Current	0.1Hz to 10Hz	–	15.0	30	–	15.0	35	pA_{p-p}
I_n	Input Noise Current Density	f_o = 10Hz	–	0.4	0.80	–	0.4	0.90	$pA/\sqrt{Hz}$
		f_o = 100Hz	–	0.17	0.23	–	0.17	0.27	
		f_o = 1000Hz	–	0.14	0.17	–	0.14	0.18	
R_{IN}	Input Resistance – Differential Mode		20	30	–	20	30	–	MΩ
IVR	Input Voltage Range		±12	–	–	±12	–	–	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	110	120	–	106	120	–	dB
PSRR	Power Supply Rejection Ratio	$V_S \pm 3V$ to $\pm 18V$	100	130	–	94	130	–	dB
A_{VO}	Large Signal Voltage Gain	(Note 3)	120	140	–	100	140	–	dB
V_O	Output Voltage Swing	$R_L = 2K\Omega$	±12			±11.5			V
		$R_L = 600\Omega$	±10	±12	–	±10	±12	–	
SR	Slewing Rate	$R_L \geq 2k\Omega$	0.5	0.8	–	0.5	0.8	–	V/µs
BW	Closed Loop Bandwidth	$A_{VCL} = +1.0$	0.6	2.5	–	0.6	2.5	–	MHz
R_O	Open Loop Output Resistance	f = 100Hz	–	45	–	–	45	–	Ω
I_{CC}	Supply Current	No Load	–	1.0	1.3	–	1.0	1.7	mA
P_D	Power Consumption	$V_{CC} = \pm 15V$			35			50	mW
		$V_{CC} = \pm 3V$			6.0			8	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^oC \leq T_A \leq +70^oC$, unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	HA-OP07E MIN	HA-OP07E TYP	HA-OP07E MAX	HA-OP07C MIN	HA-OP07C TYP	HA-OP07C MAX	UNITS
V_{OS}	Input Offset Voltage		–	50	130	–	50	250	μV
TCV_{OS}	Avg. Input Offset Voltage Drift Without External Trim		–	0.4	0.6	–	0.4	1.3	$\mu V/^oC$
I_{OS}	Input Offset Current		–	–	5.3	–	–	8.0	nA
TCI_{OS}	Avg. Input Offset Current Drift		–	20	40	–	20	50	$pA/^oC$
I_B	Input Bias Current		–	–	5.5	–	–	9.0	nA
TCI_B	Avg. Input Bias Current Drift		–	20	40	–	20	50	$pA/^oC$
IVR	Input Voltage Range		±12	–	–	±12	–	–	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	110	120	–	106	120	–	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	100	130	–	94	130	–	dB
A_{VO}	Large Signal Voltage Gain	(Note 3)	120	–	–	100	–	–	dB
V_O	Output Voltage Swing	$R_L = 600\Omega$	±10	–	–	±10	–	–	V
		$R_L = 2k\Omega$	±12			±11.5			

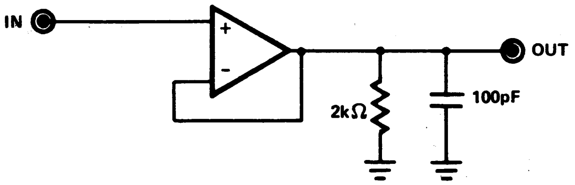
NOTES:
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$; $R_L = 2k\Omega$. Gain dB = 20 $\log_{10}$ Average

   ∴ 120dB = 1000V/mV

   140dB = 10,000V/mV

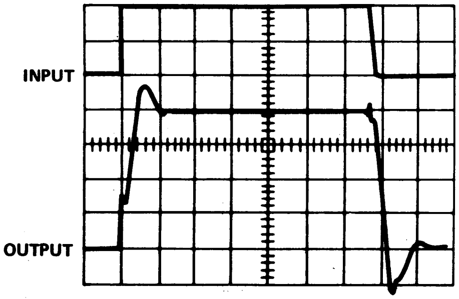
TEST CIRCUITS

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT


IN
+
-
OUT
2kΩ
100pF

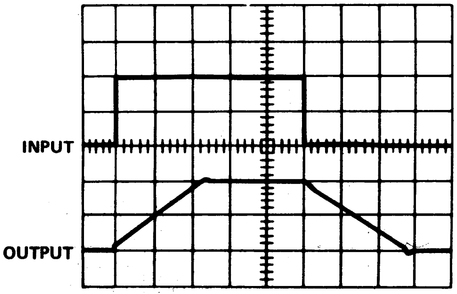
SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: 50mV/Div. Output)
(Volts: 100mV/Div. Input)
Horizontal Scale: (Time: 1μs/Div.)

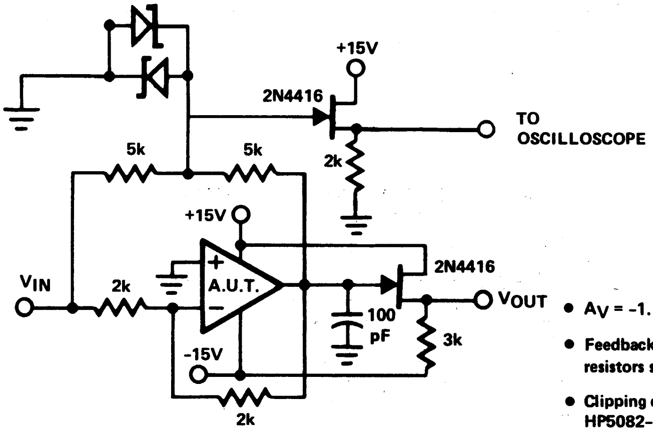


LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: 5V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



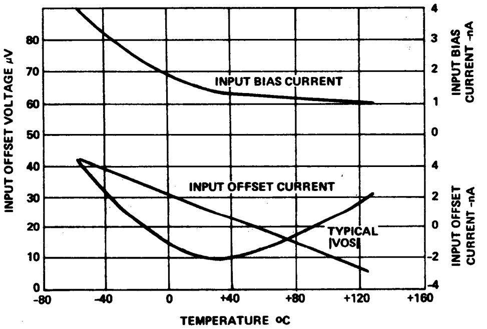
SETTLING TIME CIRCUIT


+15V
2N4416
TO OSCILLOSCOPE
5k
5k
2k
+15V
VIN
2k
+
A.U.T.
−
2N4416
VOUT
100 pF
3k
-15V
2k

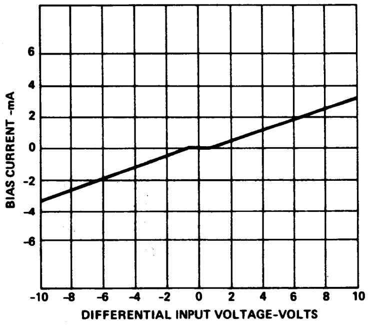
- $A_V = -1$.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

PERFORMANCE CURVES

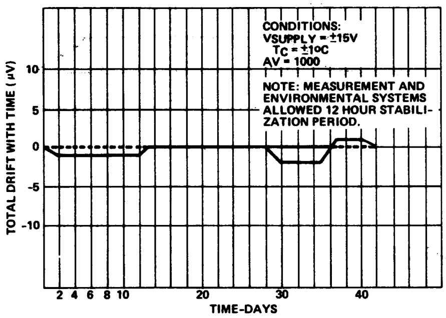
INPUT OFFSET VOLTAGE, INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



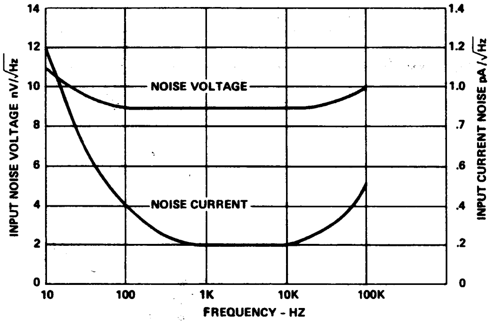
INPUT BIAS CURRENT VS. DIFFERENTIAL INPUT VOLTAGE



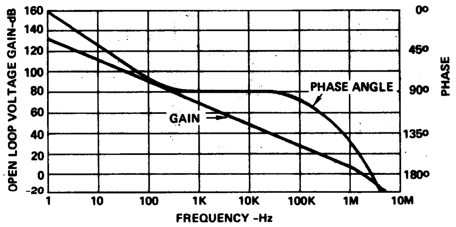
OFFSET VOLTAGE STABILITY VS. TIME



INPUT - NOISE VS. FREQUENCY

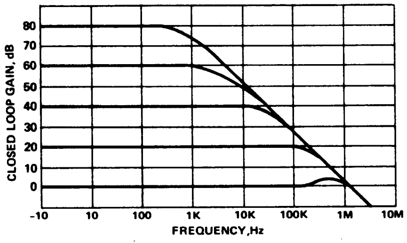


OPEN LOOP FREQUENCY RESPONSE

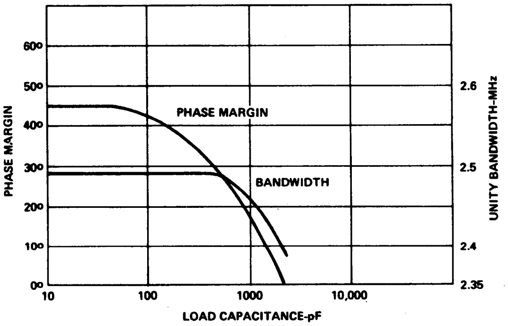


PERFORMANCE CURVES (Continued)

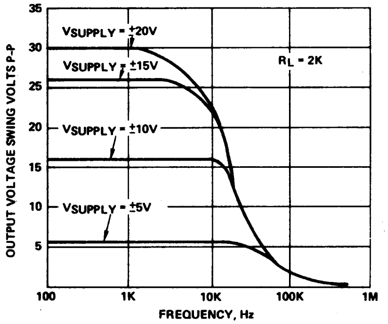
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



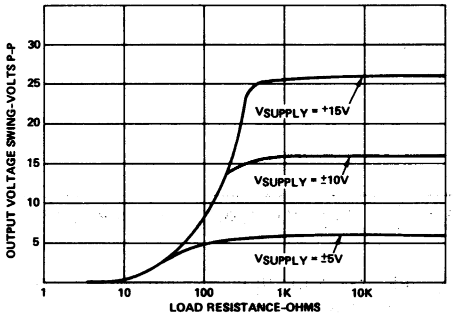
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



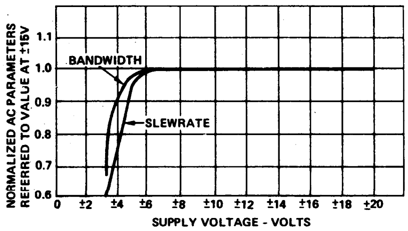
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



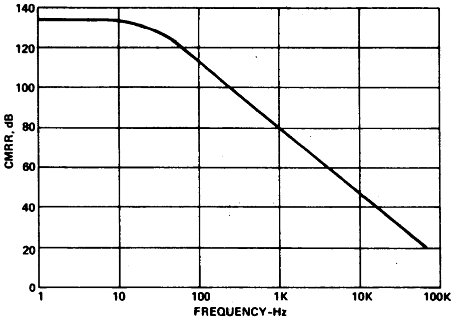
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



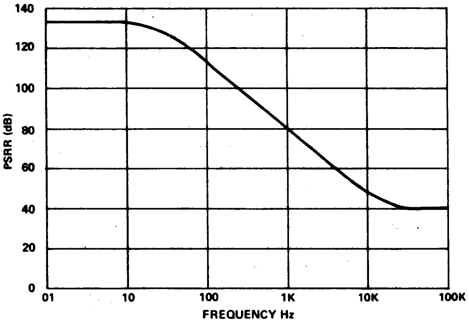
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



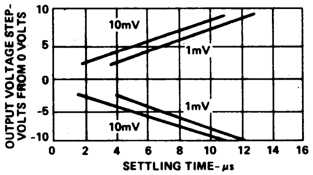
CMRR VS. FREQUENCY



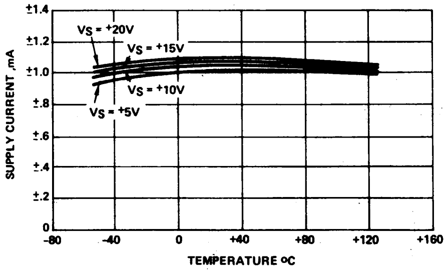
PSRR VS. FREQUENCY



SETTLINGTIME FOR VARIOUS OUTPUT STEP VOLTAGES



POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



APPLYING THE HA-OP07 OPERATIONAL AMPLIFIERS

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. CONSIDERATIONS FOR PROTOTYPING: The following list of recommendations are suggested for prototyping.
   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces, and implementation of moisture barriers when required is suggested.
   - Error voltages generated by theromocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuitry from heat generating components is recommended.
   - Shielded cable input leads, guard rings, and shield drivers are recommended for the most critical applications.

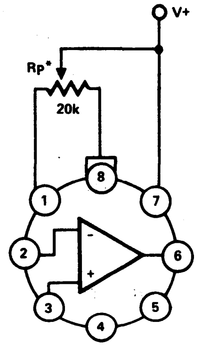
3. When driving large capacitive loads (> 500pF), as small value resistor (≈50 Ω) should be connected in series with the output and inside the feedback loop.

4. OFFSET VOLTAGE ADJUSTMENT: A 20 KΩ balance potentiometer is recommended if offset nulling is required. However, other potentiometer values such as 10KΩ, 50KΩ, and 100KΩ may be used. The minimum adjustment range for given values is ±2mV.

5. SATURATION RECOVERY: Input and output saturation recovery time is negligible in most applications. However, care should be exercised to avoid exceeding the absolute maximum ratings of the device.

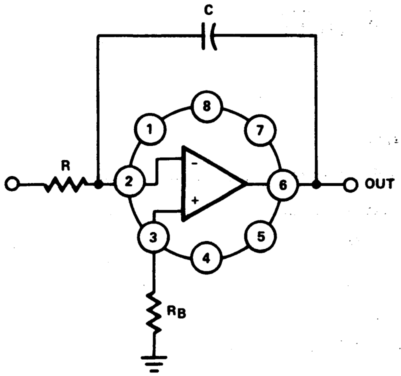
6. DIFFERENTIAL INPUT VOLTAGES: Inputs are shunted with back-to-back diodes for overvoltage protection. In applications where differential input voltages in excess of lV are applied between the inputs, the use of limiting resistors at the inputs is recommended.

OFFSET NULLING CONNECTIONS


V+
Rp*
20k
8
1
7
2
6
3
5
4
-
+

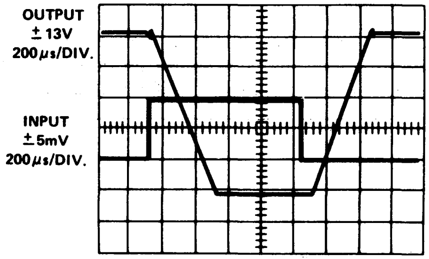
*Although Rp is shown equal to 20k, other values such as 50k, 100k, and 1M may be used. Range of adjustment is approximately ±2.5mV. V_{OS} TC of the amplifier is optimized at minimal V_{OS}.

PRECISION INTEGRATOR

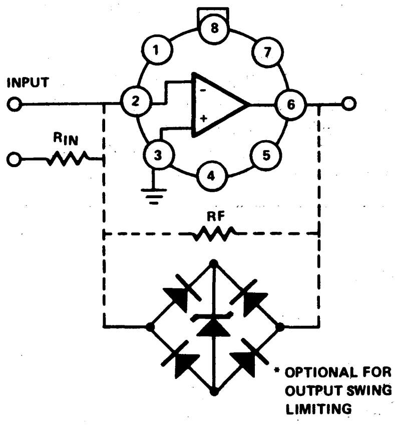

C
R
OUT
8
1
7
2
6
3
5
4
-
+
RB

The excellent input and gain characteristics of HA-OP07 are well suited for precision integrator applications. Accurate integration over seven decades of frequency using HA-OP07, virtually nullifies the need for more expensive chopper-type amplifiers.

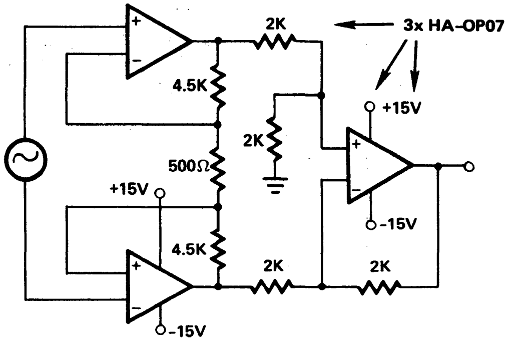
ZERO CROSSING DETECTOR



Low V_{OS} coupled with high open loop Gain, high CMRR, and high PSRR make HA-OP07 ideally suited for precision detector applications.


INPUT
RIN
8
1
7
2
6
3
5
4
-
+
RF
* OPTIONAL FOR OUTPUT SWING LIMITING

PRECISION INSTRUMENTATION AMPLIFIER (A_V = 100)


2K
3x HA-OP07
+15V
4.5K
2K
500Ω
+15V
-15V
4.5K
2K
2K
-15V
+
-

HARRIS

HA-OP27

PRELIMINARY

Ultra-Low Noise, Precision Operational Amplifier

Features

- **High Slew Rate** .... **10 V/μs**
- **Low Noise** .... **$3nV/\sqrt{Hz}$**
- **Low Drift** .... **0.2 μV/°C**
- **Low V_{OS}** .... **10 μV**
- **High Gain** .... **1800 V/mV**
- **High CMRR** .... **126 dB**
- **Wideband** .... **8.5 MHz**

Applications

- **Low Level Transducer Amplifiers**
- **Precision Summing Amplifiers**
- **Audio Preamplifiers**
- **Integrators**
- **Precision Threshold Detectors**

Description

The HA-OP27 is a low noise operational amplifier offering a remarkable blend of AC and DC parameters. Through advanced processing techniques, this design offers $3nV/\sqrt{Hz}$ of noise at 1kHz while combining the characteristics of precision and wideband amplifiers.

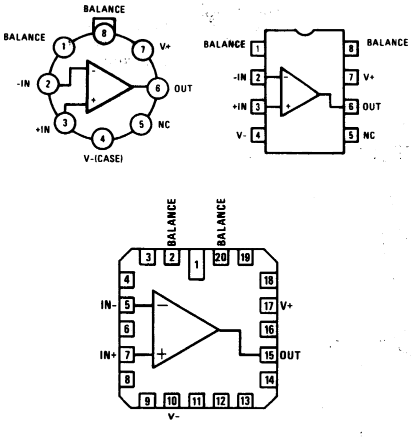
Laser trimming results in a typical input offset voltage of 10μV while stabilizing TCV_{OS} to 0.2μV/°C without affecting the 8.5 MHz bandwidth or the 10V/μs slew rate. Precision performance is further enhanced by A_{VO} of 1800V/mV, PSRR of 1 μV/V, and CMRR exceeding 120 dB. A modest power consumption of 90 mW and on-chip compensation for unity gain stability increase the potential uses of this device.

These features make the HA-OP27 an excellent choice for low level signal transducer applications. Additionally, the HA-OP27 is ideally suited for precision summers, audio preamplifiers, stable integrators, and precision threshold detectors.

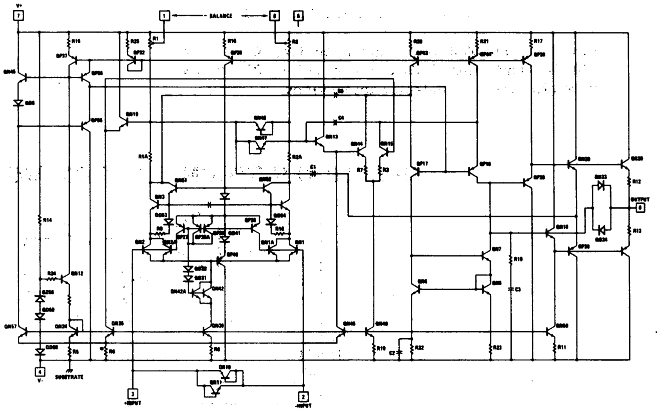
The HA-OP27 can also be used as a design enhancement by directly replacing the 725, OP05, OP06 and OP07. The HA-OP27 is available in TO-99 Metal Can, both Epoxy and Ceramic 8 pin Mini-DIPs, as well as 20 pin LCC packages.

Pinouts

TOP VIEWS


BALANCE
8
BALANCE
1
7
V+
-IN
2
6
OUT
+IN
3
5
NC
4
V-(CASE)
BALANCE 1
-IN 2
+IN 3
V- 4
8 BALANCE
7 V+
6 OUT
5 NC
BALANCE
BALANCE
3
2
1
20
19
4
18
IN- 5
17 V+
6
16
IN+ 7
15 OUT
8
14
9
10
11
12
13
V-

Schematic


V+
BALANCE
OUTPUT
V-
SUBSTRATE
+INPUT
-INPUT

Absolute Maximum Ratings

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 3)	±22V
Output Short Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	±0.7V
Differential Input Current (Note 2)	±25mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
HA-OP27A, OP27B, OP27C (J,Z)	-55°C to +125°C
HA-OP27E, OP27F, OP27G (J,Z)	-25°C to +85°C
HA-OP27E, OP27F, OP27G (P)	0°C to +70°C

NOTES:

1. Maximum Package Power Dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C

2. The OP 27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Electrical Characteristics at V_S = ±15 V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	HA-OP27A/E			HA-OP27B/F			HA-OP27C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	-	10	25	-	20	60	-	30	100	µV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 2)	-	0.2	1.0	-	0.3	1.5	-	0.4	2.0	µV/Mo
Input offset Current	I_{OS}	-	-	7	35	-	9	50	-	12	75	nA
Input Bias Current	I_B	-	-	±10	±40	-	±12	±55	-	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1 Hz to 10 Hz (Note 3, 5)	-	0.08	0.18	-	0.08	0.18	-	0.09	0.25	µVp-p
Input Noise Voltage Density	e_n	f_O = 10 Hz (Note 3)	-	3.5	5.5	-	3.5	5.5	-	3.8	8.0	
		f_O = 30 Hz (Note 3)	-	3.1	4.5	-	3.1	4.5	-	3.3	5.6	nV/√Hz
		f_O = 1000 Hz (Note 3)	-	3.0	3.8	-	3.0	3.8	-	3.2	4.5	
Input Noise Current Density	I_n	f_O = 10 Hz (Note 3)	-	1.7	4.0	-	1.7	4.0	-	1.7	-	
		f_O = 30 Hz (Note 3)	-	1.0	2.3	-	1.0	2.3	-	1.0	-	pA/√Hz
		f_O = 1000 Hz (Note 3)	-	0.4	0.6	-	0.4	0.6	-	0.4	0.6	
Input Resistance—Differential-Mode	R_{IN}	(Note 4)	1.5	6	-	1.2	5	-	0.8	4	-	MΩ
Input Resistance—Common-Mode	R_{INCM}	(Note 4)	-	3	-	-	2.5	-	-	2	-	GΩ
Input Voltage Range	IVR		±11.0	±12.3	-	±11.0	±12.3	-	±11.0	±12.3	-	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11 V	114	126	-	106	123	-	100	120	-	dB
Power Supply Rejection Ratio	PSSR	V_S = ±4 V to ±18 V	-	1	10	-	1	10	-	2	20	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10 V	1000	1800	-	1000	1800	-	700	1500	-	
		R_L ≥ 1kΩ, V_O = ±10 V	800	1500	-	800	1500	-	600	1500	-	V/mV
		R_L = 600Ω, V_O = ±1V, V_S = ±4V, (Note 4)	250	700	-	250	700	-	200	500	-	
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12.0	±13.8	-	±12.0	±13.8	-	±11.5	±13.5	-	
		R_L ≥ 600Ω	±10.0	±11.5	-	±10.0	±11.5	-	±10.0	±11.5	-	V
Slew Rate	SR	R_L ≥ 2kΩ (Note 4)	7.0	10	-	7.0	10	-	7.0	10	-	V/µs
Gain Bandwidth Prod.	GBW	(Note 4)	5.0	8.5	-	5.0	8.5	-	5.0	8.5	-	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0 (Note 4)	-	70	-	-	70	-	-	70	-	Ω
Power Consumption	P_d	V_O = 0	-	90	140	-	90	140	-	100	170	mW
Offset Adjustment Range		R_P = 10 kΩ	-	±4.0	-	-	±4.0	-	-	±4.0	-	mV

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E Grades Guaranteed Fully Warmed up.
2. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5 µV.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and typical 0.1 Hz to 10 Hz noise photograph.

Electrical Characteristics for $V_S = \pm15$ V, $-55^oC \leq T_A \leq +125^oC$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	HA-OP27A			HA-OP27B			HA-OP27C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	-	30	60	-	50	200	-	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	(Note 2)	-	0.2	0.6	-	0.3	1.3	-	0.4	1.8	$\mu V/^oC$
Input Offset Current	I_{OS}		-	15	50	-	22	85	-	30	135	nA
Input Bias Current	I_S		-	±20	±60	-	±28	±95	-	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	-	±10.3	±11.5	-	±10.2	±11.5	-	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm10$ V	108	122	-	100	119	-	94	116	-	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5$ V to ±18 V	-	2	16	-	2	20	-	4	51	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K\Omega$, $V_O = \pm10$ V	600	1200	-	500	1000	-	300	800	-	V/mV
Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±11.5	±13.5	-	±11.0	±13.2	-	±10.5	±13.0	-	V

Electrical Characteristics for $V_S = \pm15$ V, $-25^oC \leq T_A \leq +85^oC$, $0^oC \leq T_A \leq +70^oC$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	HA-OP27E			HA-OP27F			HA-OP27G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		-	20	50	-	40	140	-	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	(Note 2)	-	0.2	0.6	-	0.3	1.3	-	0.4	1.8	$\mu V/^oC$
Input Offset Current	I_{OS}	-	-	10	50	-	14	85	-	20	135	nA
Input Bias Current	I_S	-	-	±14	±60	-	±18	±95	-	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	-	±10.5	±11.8	-	±10.5	±11.8	-	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm10$ V	110	124	-	102	121	-	96	118	-	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5$ V to ±18V	-	2	15	-	2	16	-	2	32	μV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm10$ V	750	1500	-	700	1300	-	450	1000	-	V/mV
Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±11.7	±13.6	-	±11.4	±13.5	-	±11.0	±13.3	-	V

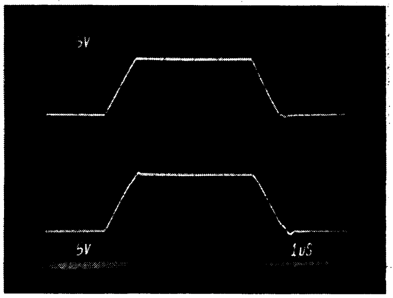
NOTES:

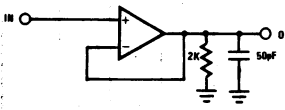
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_p = 8k\Omega$ to $20k\Omega$.

Test Circuits

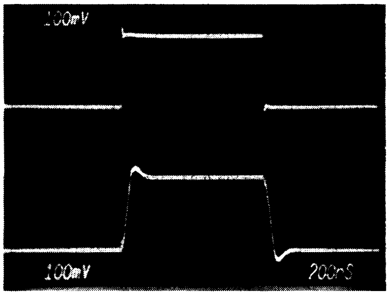
LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

LARGE SIGNAL RESPONSE



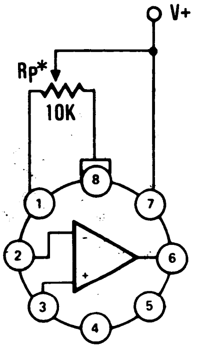


SMALL SIGNAL RESPONSE



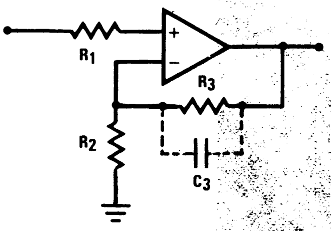
Test Circuits (continued)

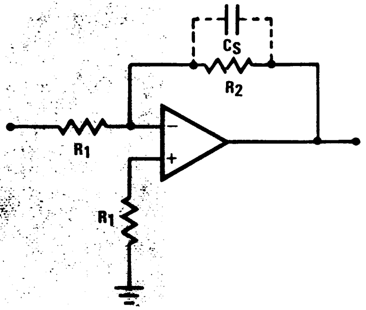
SUGGESTED OFFSET VOLTAGE ADJUSTMENT



* Offset adjustment range is approximately ±4mV

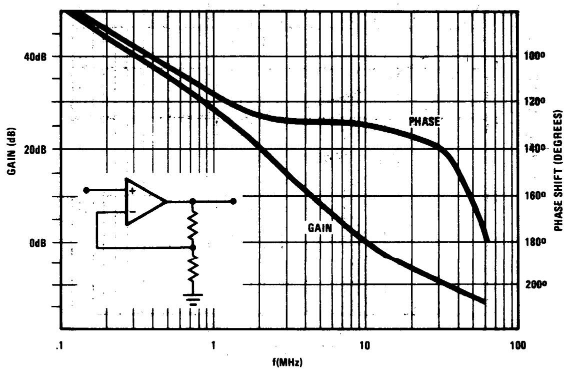
SUGGESTED STABILITY CIRCUITS





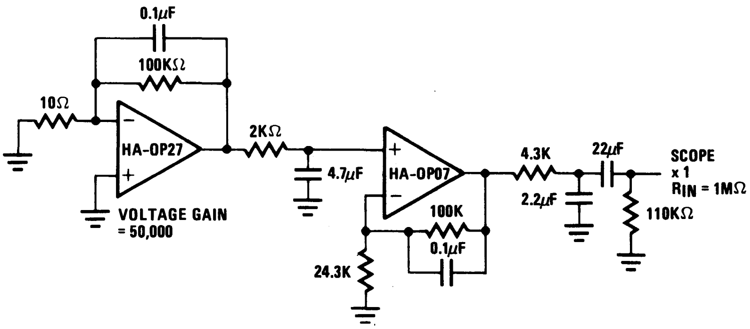
Low resistances are preferred for low noise applications as a 1KΩ resistor has 4nV√Hz of thermal noise. Total resistances of greather than 10KΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

GAIN, PHASE SHIFT FREQUENCY



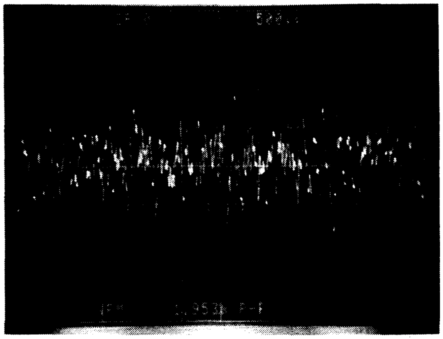
Typical Performance

0.1Hz to 10Hz NOISE TEST CIRCUIT

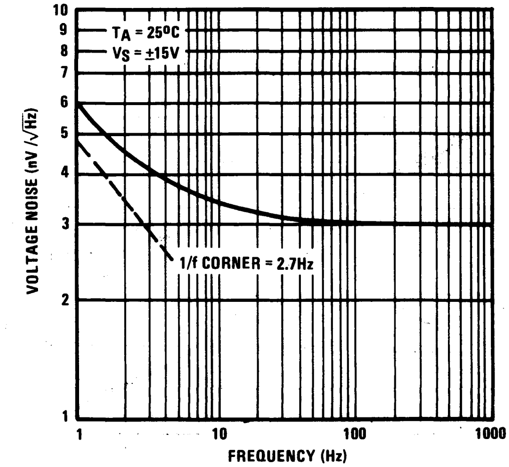

0.1μF
100KΩ
10Ω
HA-OP27
VOLTAGE GAIN = 50,000
2KΩ
4.7μF
HA-OP07
100K
0.1μF
24.3K
4.3K
22μF
2.2μF
SCOPE x 1 R_{IN} = 1MΩ
110KΩ

NOTE: ALL CAPACITOR VALUES ARE FOR NON-POLARIZED CAPACITORS ONLY

LOW FREQUENCY NOISE



VOLTAGE NOISE FREQUENCY



HARRIS

HA-OP37

PRELIMINARY

Ultra-Low Noise, Precision, High-Speed Operational Amplifier

Features

• **Low Noise**	**3nV/√Hz at 1 kHz**
• **Low Drift**	**0.2 μV/°C**
• **Low V_{OS}**	**10 μV**
• **High Gain**	**1800 V/mV**
• **High CMRR**	**126 dB**
• **High Slew Rate**	**20V/μs**

Applications

- **Low Level Transducer Amplifiers**
- **Instrumentation Amplifiers**
- **Audio Preamplifiers**
- **Precision Threshold Detectors**
- **Signal Conditioners**

Description

The HA-OP37 operational amplifier is a connection between precision and high speed performance. The low device noise, 3 nV/√Hz at 1 KHz, allows accurate high speed amplification of extremely low level signals. Precision is attained by a low V_{OS} of typically 10 μV, a high gain of 1800 V/mV, a differential input resistance of 6MΩ and an average input offset drift of just 0.2 μV/°C. High speed is guaranteed by a slew rate of 17V/μs and a gain bandwidth product of 63 MHz. Also the HA-OP37 has a CMRR above 120 dB and a PSRR of typically 1 μV/V.

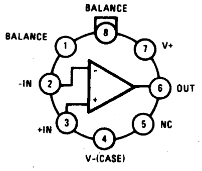
This combination of characteristics makes the HA-OP37 an outstanding choice for all low noise, precision and high speed applications where gains are greater than five. The HA-OP37 can be used for precision threshold detectors, instrumentation amplifiers, many audio circuits such as RIAA phone preamplifiers, and in signal conditioning circuits for data acquisition systems.

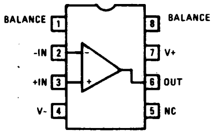
The HA-OP37 can also be used as an enhancement for existing designs by directly replacing the 725, OP05, OP06, OP07 and OP27 where gains are greater than five.

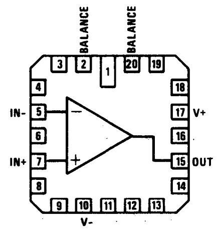
The HA-OP37 is available in TO-99 metal can, both epoxy and ceramic 8 pin mini-DIPs, as well as 20 pin LCC packages.

Pinouts

TOP VIEWS


BALANCE
8
BALANCE
1
7
V+
-IN
2
6
OUT
+IN
3
5
NC
4
V-(CASE)


BALANCE
1
-IN
2
+IN
3
V-
4
8
BALANCE
7
V+
6
OUT
5
NC


BALANCE
BALANCE
3
2
1
20
19
4
18
IN-
5
17
V+
6
16
IN+
7
15
OUT
8
14
9
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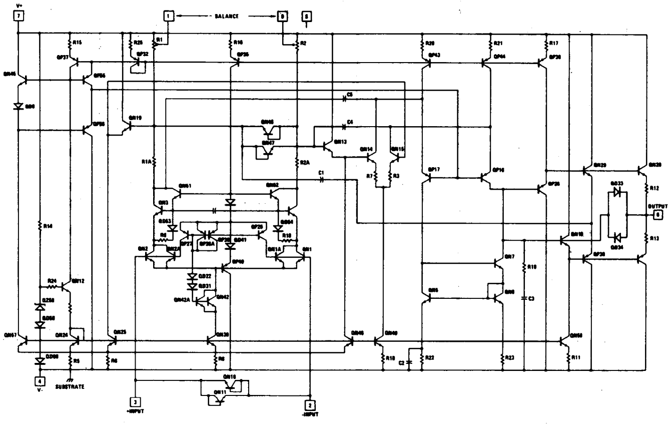
11
12
13
V-

Schematic


V+
7
1
BALANCE
8
OUTPUT
6
4
SUBSTRATE
3
-INPUT
2
+INPUT

Absolute Maximum Ratings

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 3)	±22V
Output Short Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	±0.7V
Differential Input Current (Note 2)	±25mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
HA-OP37A, OP37B, OP37C (J,Z)	-55°C to +125°C
HA-OP37E, OP37F, OP37G (J,Z)	-25°C to +85°C
HA-OP37E, OP37F, OP37G (P)	0°C to +70°C

NOTES:

1. Maximum Package Power Dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C

2. The OP37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Electrical Characteristics at V_S = ±15 V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	HA-OP37A/E			HA-OP37B/F			HA-OP37C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	-	10	25	-	20	60	-	30	100	µV
Long Term V_{OS} Stability	V_{OS}/Time	(Note 2)	-	0.2	1.0	-	0.3	1.5	-	0.4	2.0	µV/Mo
Input Offset Current	I_{OS}		-	7	35	-	9	50	-	12	75	nA
Input Bias Current	I_B		-	±10	±40	-	±12	±55	-	±15	±80	nA
Input Noise Voltage	$e_{np\text{-}p}$	0.1 Hz to 10 Hz (Note 3, 5)	-	0.08	0.18	-	0.08	0.18	-	0.08	0.25	µVp-p
Input Noise Voltage Density	e_n	f_O = 10 Hz (Note 3) f_O = 30 Hz (Note 3) f_O = 1000 Hz (Note 3)	- - -	3.5 3.1 3.0	5.5 4.5 3.8	- - -	3.5 3.1 3.0	5.5 4.5 3.8	- - -	3.8 3.3 3.2	8.0 5.6 4.5	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	f_O = 10 Hz (Note 3) f_O = 30 Hz (Note 3) f_O = 1000 Hz (Note 3)	- - -	1.7 1.0 0.4	4.0 2.3 0.6	- - -	1.7 1.0 0.4	4.0 2.3 0.6	- - -	1.7 1.0 0.4	- - 0.6	$pA/\sqrt{Hz}$
Input Resistance—Differential Mode	R_{IN}	(Note 4)	1.5	6	-	1.2	5	-	0.8	4	-	MΩ
Input Resistance—Common Mode	R_{INCM}	(Note 4)	-	3	-	-	2.5	-	-	2	-	GΩ
Input Voltage Range	IVR		±11.0	±12.3	-	±11.0	±12.3	-	±11.0	±12.3	-	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±11 V	114	126	-	106	123	-	100	120	-	dB
Power Supply Rejection Ratio	PSSR	V_S = ±4 V to ±18 V	-	1	10	-	1	10	-	2	20	µV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥2KΩ, V_O = ±10V R_L ≥1KΩ, V_O = ±10V R_L = 600Ω, V_O = ±1V, V_S = ± 4V, (Note 4)	1000 800 250	1800 1500 700	- - -	1000 800 250	1800 1500 700	- - -	700 400 200	1500 1500 500	- - -	V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ R_L ≥ 600Ω	±12.0 ±10.0	±13.8 ±11.5	- -	±12.0 ±10.0	±13.8 ±11.5	- -	±11.5 ±10.0	±13.5 ±11.5	- -	V
Slew Rate	SR	R_L ≥ 2kΩ (Note 4)	14	20	-	14	20	-	14	20	-	V/µS
Gain Bandwidth Prod	GBW	f_O = 10 kHz (Note 4) f_O = 1 MHz (Note 4)	60 -	80 63	- -	60 -	80 63	- -	60 -	80 63	- -	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0 (Note 4)	-	70	-	-	70	-	-	70	-	Ω
Power Consumption	P_d	V_O = 0	-	90	140	-	90	140	-	100	170	mW
Offset Adjustment Range		R_P = 10 kΩ	-	±4.0	-	-	±4.0	-	-	±4.0	-	mV

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E Grades Guaranteed Fully Warmed up.
2. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5 µV.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and typical 0.1 Hz to 10 Hz noise photograph.

Electrical Characteristics for V_S = ±15 V, -55°C ≤ T_A ≤ 125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	HA-OP37A			HA-OP37B			HA-OP37C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	-	30	60	-	50	200	-	70	300	µV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	(Note 2)	-	0.2	0.6	-	0.3	1.3	-	0.4	1.8	µV/°C
Input Offset Current	I_{OS}		-	15	50	-	22	85	-	30	135	nA
Input Bias Current	I_B		-	±20	±60	-	±28	±95	-	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	-	±10.3	±11.5	-	±10.2	±11.5	-	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±10 V	108	122	-	100	119	-	94	116	-	dB
Power Supply Rejection Ratio	PSSR	V_S = ±4.5 V to ±18 V	-	2	16	-	2	20	-	4	51	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10 V	600	1200	-	500	1000	-	300	800	-	V/mV
Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±11.5	±13.5	-	±11.0	±13.2	-	±10.5	±13.0	-	V

Electrical Characteristics for V_S = ±15 V, -25°C ≤ T_A ≤ 85°C, 0°C ≤ T_A ≤ + 70°C, unless otherwise noted.

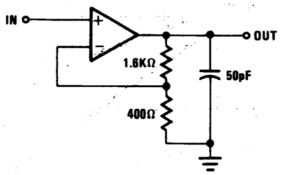
PARAMETER	SYMBOL	CONDITIONS	HA-OP37E			HA-OP37F			HA-OP37G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		-	20	50	-	40	140	-	55	220	µV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	(Note 2)	-	0.2	0.6	-	0.3	1.3	-	0.4	1.8	µV/°C
Input Offset Current	I_{OS}		-	10	50	-	14	85	-	20	135	nA
Input Bias Current	I_B		-	±14	±60	-	±18	±95	-	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	-	±10.5	±11.8	-	±10.5	±11.8	-	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±10 V	110	124	-	102	121	-	96	118	-	dB
Power Supply Rejection Ratio	PSSR	V_S = ±4.5 V to ±18V	-	2	15	-	2	16	-	2	32	µV/V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10 V	750	1500	-	700	1300	-	450	1000	-	V/mV
Output Voltage Swing	V_{OM}	$R_L \geq 2k\Omega$	±11.7	±13.6	-	±11.4	±13.5	-	±11.0	±13.3	-	V

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled R_p = 8kΩ to 20kΩ.

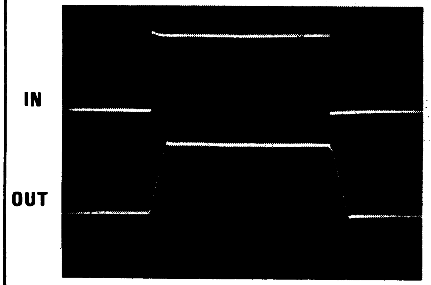
Test Circuits

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



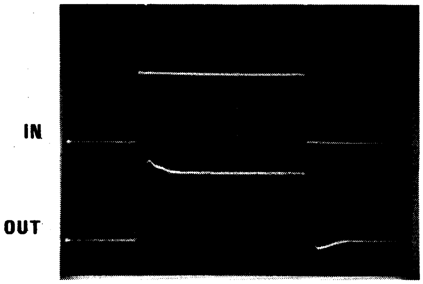
LARGE SIGNAL RESPONSE

(IN = 1V/DIV; OUT = 5V/DIV; TIME = 1ns/DIV)



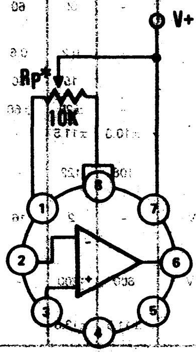
SMALL SIGNAL RESPONSE

(IN = 20mV/DIV; OUT = 100mV/DIV; TIME = 100ns/DIV)



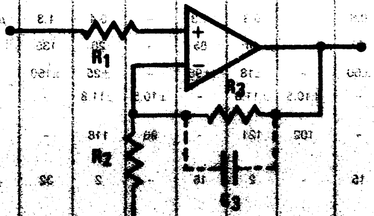
Test Circuits (continued)

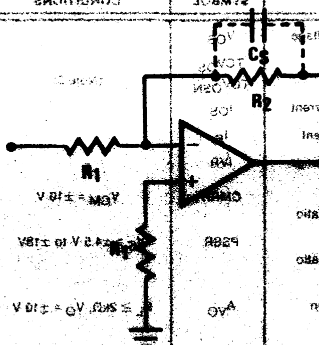
SUGGESTED OFFSET VOLTAGE ADJUSTMENT



* Offset adjustment range is approximately ±4mV

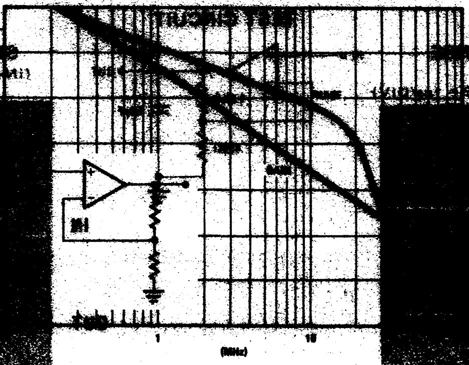
SUGGESTED STABILITY CIRCUITS





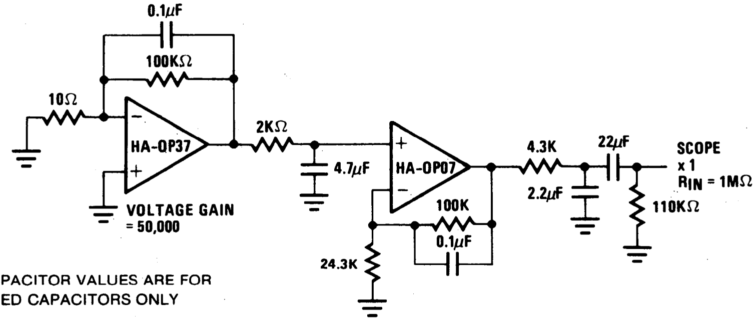
Low resistances are preferred for low noise applications as a 1KΩ resistor has 4nV/√Hz of thermal noise. [illegible] either [illegible] stability. In most [illegible] a few picofarads of capacitance across the feedback resistor will improve stability.

GAIN, PHASE SHIFT VERSUS FREQUENCY



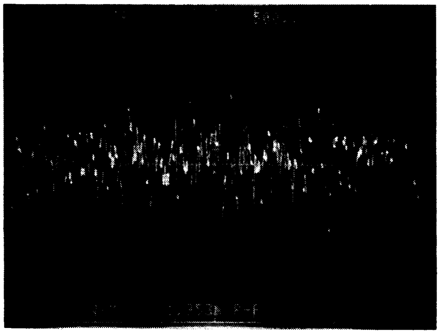
Typical Performance

0.1Hz to 10Hz NOISE TEST CIRCUIT

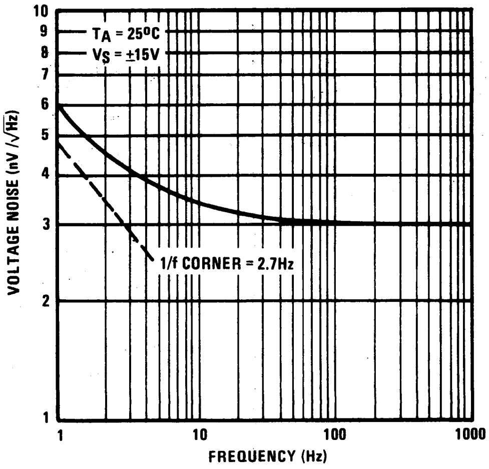

0.1µF
100KΩ
10Ω
HA-OP37
VOLTAGE GAIN = 50,000
2KΩ
4.7µF
HA-OP07
100K
0.1µF
24.3K
4.3K
22µF
2.2µF
110KΩ
SCOPE x 1 R_IN = 1MΩ

NOTE: ALL CAPACITOR VALUES ARE FOR NON-POLARIZED CAPACITORS ONLY

LOW FREQUENCY NOISE



VOLTAGE NOISE VERSUS FREQUENCY



HARRIS

HA-2400/04/05

PRAM Four Channel Programmable Amplifier

FEATURES

• PROGRAMMABILITY	
• HIGH SLEW RATE	30V/μs
• WIDE GAIN BANDWIDTH	40MHz
• HIGH GAIN	150,000
• LOW OFFSET CURRENT	5nA
• HIGH INPUT IMPEDANCE	30MΩ
• SINGLE CAPACITOR COMPENSATION	
• DTL/TTL COMPATIBLE INPUTS	

APPLICATIONS

- THOUSANDS OF NEW APPLICATIONS; PROGRAM
  - SIGNAL SELECTION/MULTIPLEXING
  - OP AMP GAIN
  - OSCILLATOR FREQUENCY
  - FILTER CHARACTERISTICS
  - ADD-SUBTRACT FUNCTIONS
  - INTEGRATOR CHARACTERISTICS
  - COMPARATOR LEVELS

DESCRIPTION

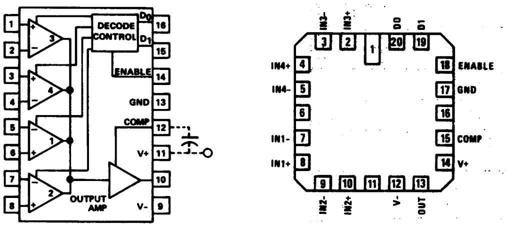
HA-2400/2404/2405 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

Each channel of the HA-2400/2404/2405 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing, signal selection, and mathematical function designs. With 30V/μs slew rate, 40MHz gain bandwidth, and 30M ohms input impedance these devices are ideal building blocks for signal generators, active filters, and data acquisition designs. Programmability coupled with 2mV typical offset voltage and 5nA offset current makes these amplifiers outstanding components for signal conditioning circuits.

HA-2400/2404/2405 are available in a 16 pin dual-in-line package. HA-2400 is specified from -55°C to +125°C. HA-2404 is specified over the -25°C to +85°C range, while HA-2405 operates from 0°C to +75°C.

PINOUT

TOP VIEWS



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	I	H	3
H	H	H	4
X	X	L	NONE

SCHEMATIC

Condensed circuit diagram for a programmable amplifier (PRAM HA-2400)

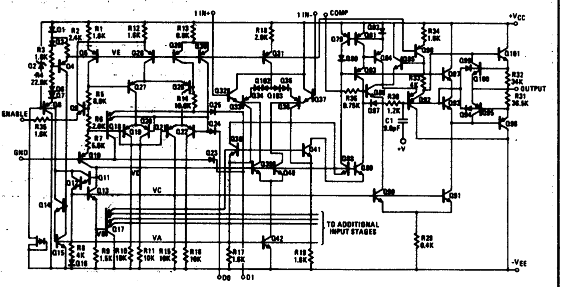


Diagram includes: ONE INPUT STAGE, DECODE CONTROL, BIAS NETWORK AND OUTPUT STAGE

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Internal Power Dissipation (Note 13)	300mW
Differential Input Voltage	$\pm V_{Supply}$	Operating Temperature Range	$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2400)
Digital Input Voltage	-0.76V to +10.0V		$-25^{o}C \leq T_A \leq +85^{o}C$ (HA-2404)
Output Current	Short Circuit Protected		$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2405)
	$(I_{SC} \leq \pm 33mA)$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ Unless Otherwise Specified.
Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$. Limits apply to each of the four channels, when addressed.

PARAMETER	TEMP.	HA-2400/HA-2404 LIMITS MIN.	TYP.	MAX.	HA-2405 LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		4	9		4	9	mV
	Full			11			11	mV
Bias Current (Note 12)	+25°C		50	200		50	250	nA
	Full			400			500	nA
Offset Current (Note 12)	+25°C		5	50		5	50	nA
	Full			100			100	nA
Input Resistance (Note 12)	+25°C		30			30		MΩ
Common Mode Range	Full	±9.0			±9.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 1,5)	+25°C	50K	150K		50K	150K		V/V
	Full	25K			25K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		dB
Gain Bandwidth (Notes 3,14)	+25°C	20	40		20	40		MHz
(Notes 4,14)	+25°C	4	8		4	8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current	+25°C	10	20		10	20		mA
Full Power Bandwidth (Notes 3,5,15)	+25°C	200	500		200	500		kHz
(Notes 4,5,15)	+25°C	100	200		100	200		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C		20	45		20	50	ns
Overshoot (Notes 4,6)	+25°C		25	40		25	40	%
Slew Rate (Notes 3,7)	+25°C	20	30		20	30		V/µs
(Notes 4,7,14)	+25°C	6	8		6	8		V/µs
Settling Time (Notes 4,7,8,14)	+25°C		1.5	2.5		1.5	2.5	µs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full		1	1.5		1	1.5	mA
Digital Input Current (V_{IN} = +5.0V)	Full		5			5		nA
Output Delay (Notes 9,14)	+25°C		100	250		100	250	ns
Crosstalk (Note 10)	+25°C	-80	-110		-74	-110		dB
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.8	6.0		4.8	6.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90		74	90		dB

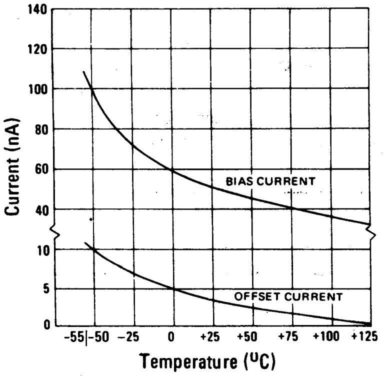
NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 5VDC$
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2k\Omega$, $C_L = 50pF$.
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2k\Omega$, $C_L = 50pF$.
5. V_{OUT} = 20V peak to peak.
6. V_{OUT} = 200mV peak to peak.
7. V_{OUT} = 10.0V peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10VDC$
11. $V_{SUPP} = \pm 10VDC$ to $\pm 20VDC$
12. Unselected channels have approximately the same input parameters.
13. Derate by 4.3mW/°C above 105°C.
14. Guaranteed by design.
15. FullPower Bandwidth based on slew rate measurement using:

$$FPBN = \frac{S.R.}{22\pi V_{peak}}$$

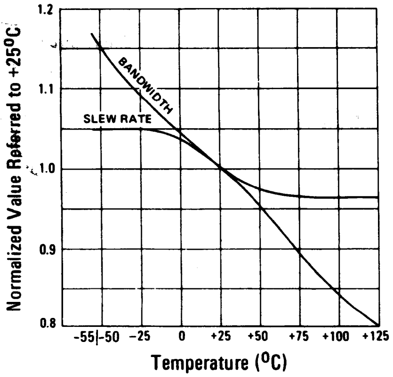
CHARACTERISTIC CURVES

V+ = +15V D. C., V- = -15V D. C., T_A = 25°C unless otherwise stated.

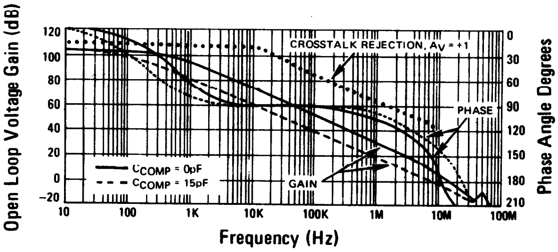
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



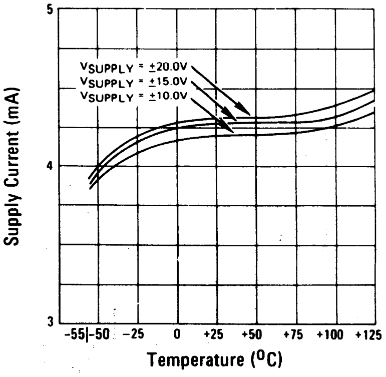
NORMALIZED A.C. PARAMETERS VS. TEMPERATURE



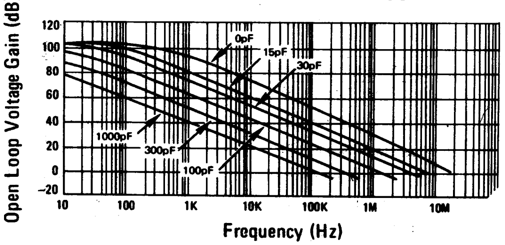
OPEN LOOP FREQUENCY AND PHASE RESPONSE



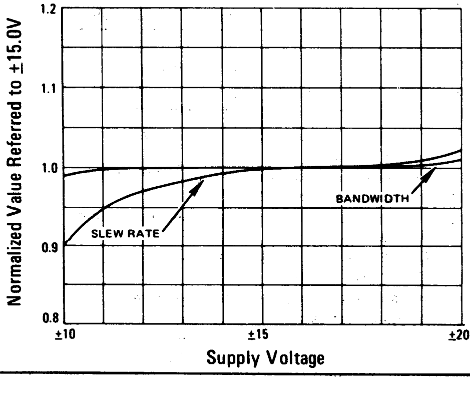
POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



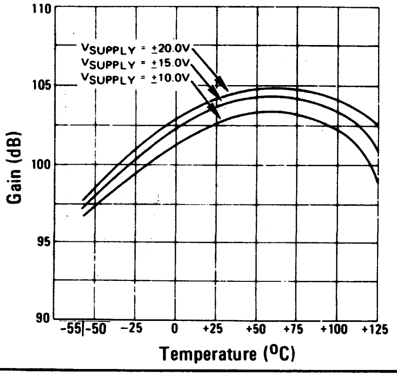
FREQUENCY RESPONSE VS. C_{COMP}



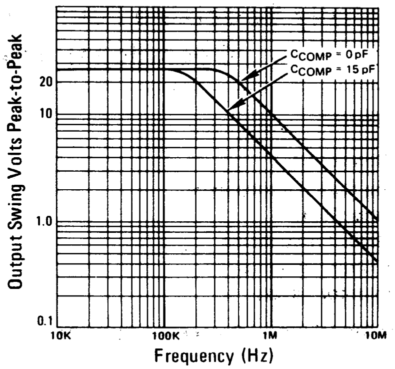
NORMALIZED A.C. PARAMETERS VS. SUPPLY VOLTAGE



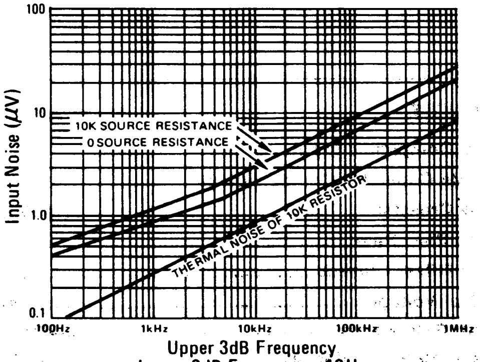
OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE



OUTPUT VOLTAGE SWING VS. FREQUENCY

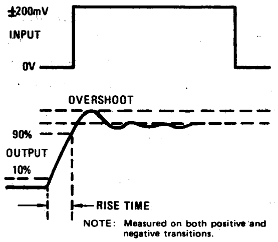


EQUIVALENT INPUT NOISE VS. BANDWIDTH

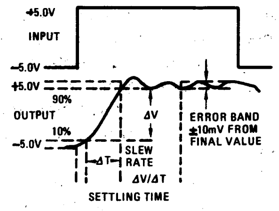


Lower 3dB Frequency - 10Hz
Broadband Noise Characteristics

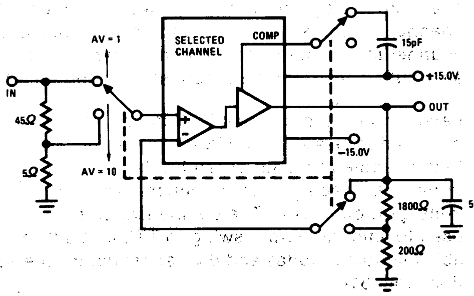
TRANSIENT RESPONSE


±200mV
INPUT
0V
OVERSHOOT
90%
OUTPUT
10%
RISE TIME
NOTE: Measured on both positive and negative transitions.

SLEW RATE AND SETTLING

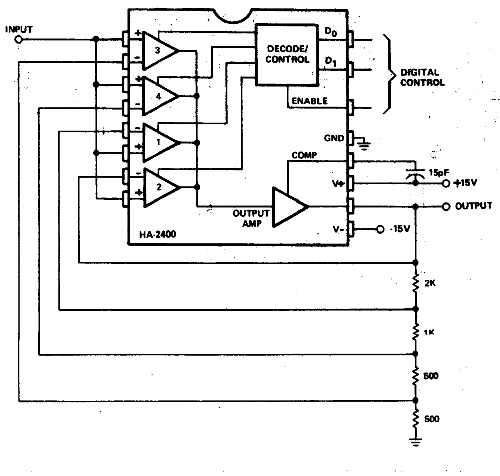

+5.0V
INPUT
-5.0V
+5.0V
OUTPUT
90%
10%
-5.0V
ΔV
ΔT
SLEW RATE
ΔV/ΔT
ERROR BAND
±10mV FROM FINAL VALUE
SETTLING TIME

SLEW RATE AND TRANSIENT RESPONSE

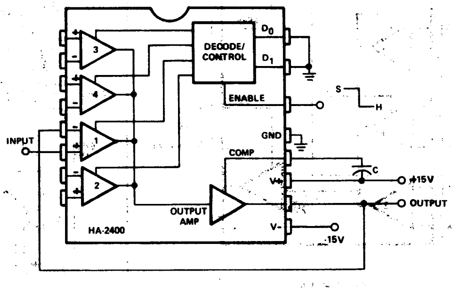

AV = 1
IN
45Ω
5Ω
AV = 10
SELECTED CHANNEL
COMP
15pF
+15.0V
OUT
-15.0V
1800Ω
50pF
200Ω

TYPICAL APPLICATIONS

AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN


INPUT
3
4
1
2
DECODE/ CONTROL
D_0
D_1
DIGITAL CONTROL
ENABLE
GND
COMP
15pF
+15V
V+
OUTPUT
OUTPUT AMP
HA-2400
V-
-15V
2K
1K
500
500

SAMPLE AND HOLD


3
4
1
2
INPUT
DECODE/ CONTROL
D_0
D_1
ENABLE
S
H
GND
COMP
C
+15V
V+
OUTPUT
OUTPUT AMP
HA-2400
V-
-15V

Sample charging rate = $\frac{I_1}{C}$ V/sec.

Hold drift rate = $\frac{I_2}{C}$ V/sec.

Switch pedestal error = $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$ A
$I_2 \approx 200 \times 10^{-9}$ A @ +25°C
$\approx 600 \times 10^{-9}$ A @ -55°C
$\approx 100 \times 10^{-9}$ A @ +125°C
$Q \approx 2 \times 10^{-12}$ Coul.

FOR MORE EXAMPLES, SEE HARRIS APPLICATION NOTE 514

HARRIS

HA-2406

Digitally Selectable Four Channel Operational Amplifier

Features

- TTL Compatible Inputs
- Single Capacitor Compensation
- Low Crosstalk .... -110dB
- High Slew Rate 20V/μs
- Low Offset Current 5nA
- Offset Voltage 7mV
- High Gain-Bandwidth 30MHz
- High Input Impedance 30MΩ

Applications

- Digital Control Of:
  - ▶ Analog Signal Multiplexing
  - ▶ Op Amp Gains
  - ▶ Oscillator Frequencies
  - ▶ Filter Characteristics
  - ▶ Comparator Levels
- Ideal for Digital Signal Processing Systems

Description

The HA-2406 is a monolithic device consisting of four op amp input stages that can be individually connected to one output stage by decoding two TTL lines into four channel select signals. In addition to allowing each channel to be addressed, an enable control disconnects all input stages from the output stage when asserted low.

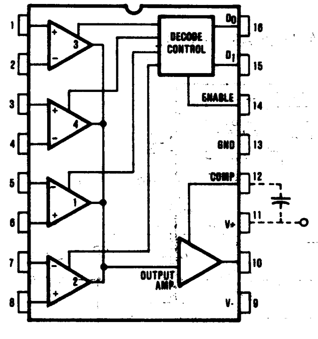
Each input-output combination of the HA-2406 is designed to be a 20V/μs, 30MHz gain-bandwidth amplifier that is stable at a gain of ten but by connecting one external 15pF capacitor all amplifiers are compensated for unity gain operation. The compensation pin may also be used to limit the output swing to TTL levels through suitable clamping diodes and divider networks (see Application Note 514).

Dielectric isolation and short-circuit protected output stages contribute to the quality and durability of the HA-2406 . When used as a simple amplifier, its dynamic performance is very good and when its added versatility is considered, the HA-2406 is unmatched in the analog world. It can replace a number of individual components in analog signal conditioning circuits for digital signal processing systems. Its advantages include saving board space and reducing power supply requirements.

The HA-2406 is available in a 16 pin dual-in-line package and is guaranteed for operation over the full commercial temperature range (0°C to +75°C).

Pinout

TOP VIEW


1
2
3
4
5
6
7
8
+
-
3
4
1
2
DECODE CONTROL
D0
D1
ENABLE
GND
COMP
V+
OUTPUT AMP.
V-
16
15
14
13
12
11
10
9

TRUTH TABLE

D1	D0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

Schematic

HA-2406

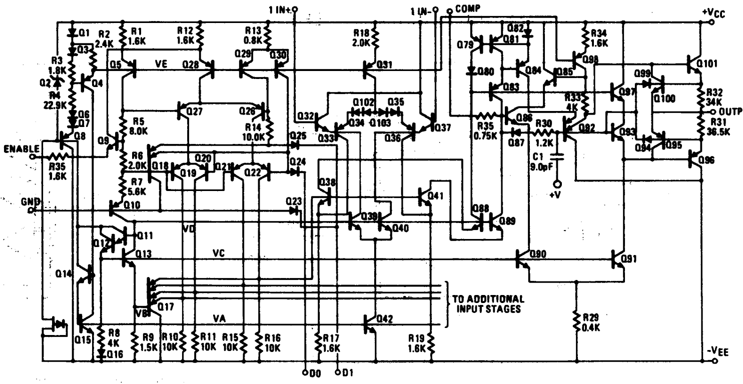

1 IN+
1 IN-
COMP
+VCC
Q1
R2 2.4K
R1 1.6K
R12 1.6K
R13 0.8K
R18 2.0K
Q79
Q82
Q81
R34 1.6K
Q98
Q101
R3 1.8K
Q3
Q5
VE
Q28
Q29
Q30
Q31
Q80
Q84
Q85
Q99
Q100
R32 34K
Q2
Q4
Q83
R4 22.9K
Q6
Q7
Q27
Q26
Q102
Q35
R33 4K
Q97
OUTPUT
R5 8.0K
R14 10.0K
Q32
Q34
Q103
Q37
R35 0.75K
Q86
R30 1.2K
Q92
Q93
R31 36.5K
Q8
Q9
Q25
Q33
Q36
Q87
C1 9.0pF
Q94
Q95
ENABLE
R35 1.6K
R6 2.0K
Q18
Q19
Q20
Q21
Q22
Q24
Q96
R7 5.6K
Q38
Q41
+V
GND
Q10
Q23
Q39
Q40
Q88
Q89
Q11
Q12
VD
Q13
VC
Q90
Q91
Q14
TO ADDITIONAL INPUT STAGES
Q17
VB
VA
Q42
R29 0.4K
Q15
R8 4K
Q16
R9 1.5K
R10 10K
R11 10K
R15 10K
R16 10K
R17 1.6K
R19 1.6K
-VEE
D0
D1

Diagram includes: One Input Stage, Decode Control, Bias Network and Output Stage.

Copyright © Harris Corporation 1985

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 45.0V
Differential Input Voltage .... $\pm V_{Supply}$
Digital Input Voltage .... -0.76V to +10.0V
Output Current .... Short Circuit Protected ($I_{SC} \leq \pm 33mA$)

Internal Power Dissipation 300mW
Operating Temperature Range .... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range .... $-65^oC \leq T_A \leq +150^oC$

Electrical Characteristics

Test Conditions: $V_{Supply} = \pm 15.0V$ Unless Otherwise Specified.
Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$. Limits apply to each of the four channels, when addressed.

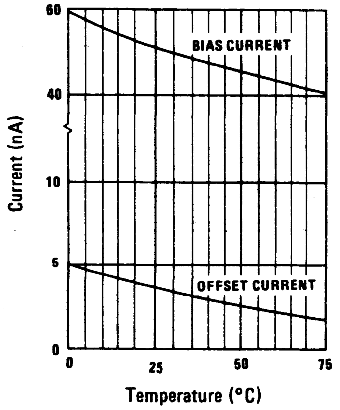
PARAMETER	TEMP	HA-2406 LIMITS MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C		7	10	mV
	Full			12	mV
Bias Current (Note 12)	+25°C		50	250	nA
	Full			500	nA
Offset Current (Note 12)	+25°C		5	50	nA
	Full			100	nA
Input Resistance (Note 12)	+25°C		30		MΩ
Common Mode Range	Full	±9.0			V
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Notes 1, 5)	+25°C	40K	150K		V/V
	Full	20K			V/V
Common Mode Rejection Ratio (Note 2)	Full	74	80		dB
Gain Bandwidth (Note 3, 15)	+25°C	15	30		MHz
Gain Bandwidth (Note 4, 15)	+25°C	3	6		MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		V
Output Current (Note 13)	+25°C	10	15		mA
Full Power Bandwidth (Notes 3, 5, 14, 15)	+25°C	240	320		kHz
Full Power Bandwidth (Notes 4, 5, 14)	+25°C	64	95		kHz
TRANSIENT RESPONSE					
Rise Time (Notes 4, 6)	+25°C		30	100	ns
Overshoot (Notes 4, 6)	+25°C		25	40	%
Slew Rate (Notes 3, 7, 15)	+25°C	15	20		V/μs
Slew Rate (Notes 4, 7)	+25°C	4	6		V/μs
Settling Time (Notes 4, 7, 8, 15)	+25°C		2.0	3.5	μs
CHANNEL SELECT CHARACTERISTICS					
Digital Input Current ($V_{IN} = 0V$)	Full		1	1.5	mA
Digital Input Current ($V_{IN} = +5.0V$)	Full		15		nA
Output Delay (Note 9, 15)	+25°C		150	300	ns
Crosstalk (Note 10)	+25°C	-74	-110		dB
POWER SUPPLY CHARACTERISTICS					
Supply Current	+25°C		4.8	7.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90		dB

Notes:

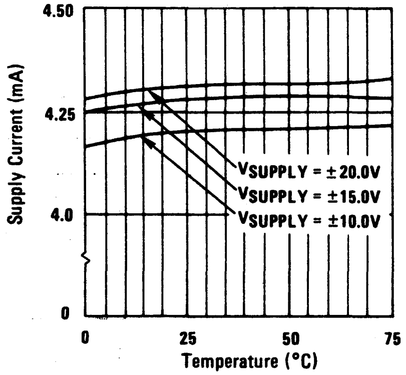
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 5VDC$
3. $A_V = +10$, $C_{COMP} = 0$, $R_L \geq 2k\Omega$, $C_L = 50pF$.
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2k\Omega$, $C_L = 50pF$.
5. $V_{OUT} = 20V$ peak to peak.
6. $V_{OUT} = 200mV$ peak to peak.
7. $V_{OUT} = 10.0V$ peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10VDC$
11. $V_{SUPP} = \pm 10VDC$ to $\pm 20VDC$
12. Unselected channels have approximately the same input parameters.
13. $V_{OUT} = \pm 10V$
14. Full power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{S.R.}{2\pi Vpeak}$
15. Sample tested.

Characteristic Curves V+ = 15VDC, V- = -15VDC, T_A = 25°C unless otherwise stated.

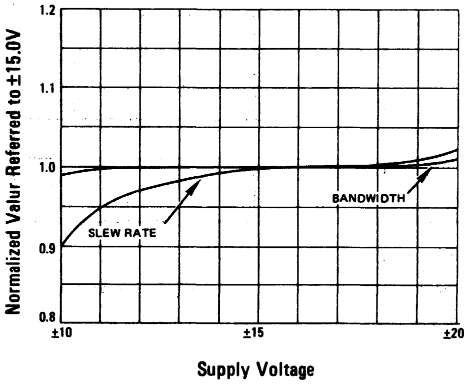
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



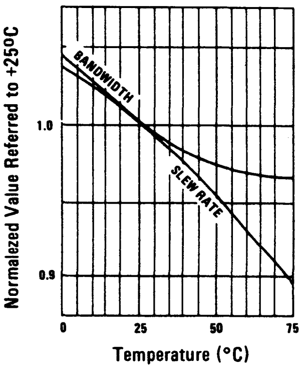
POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



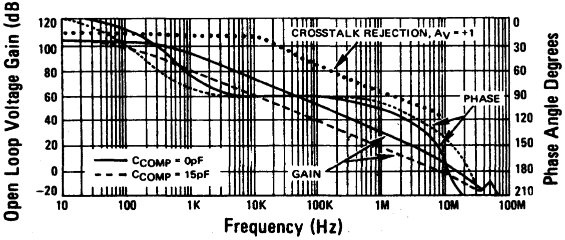
NORMALIZED A. C. PARAMETERS VS. SUPPLY VOLTAGE



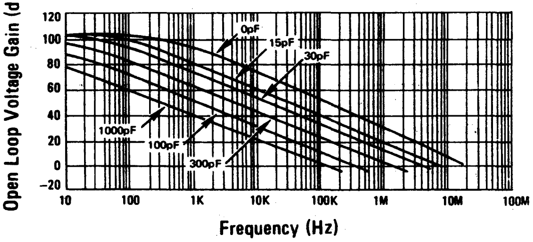
NORMALIZED A. C. PARAMETERS VS. TEMPERATURE



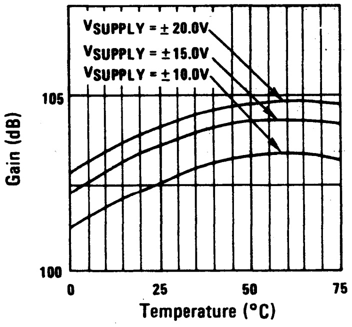
OPEN LOOP FREQUENCY AND PHASE RESPONSE



FREQUENCY RESPONSE VS. C_{COMP}

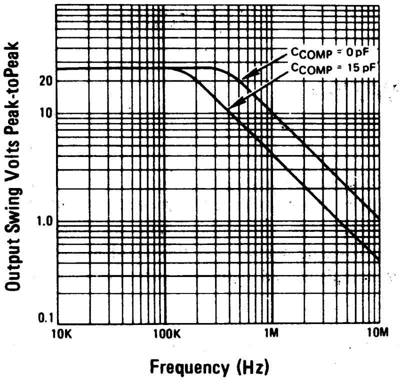


OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

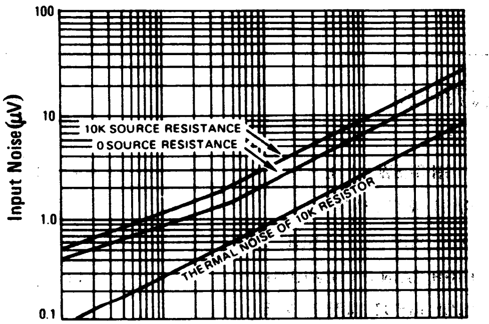


Characteristic Curves (Continued)

OUTPUT VOLTAGE SWING VS. FREQUENCY

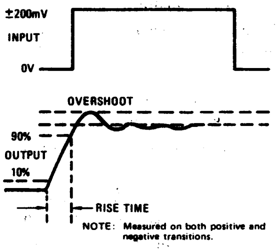


EQUIVALENT INPUT NOISE VS. BANDWIDTH

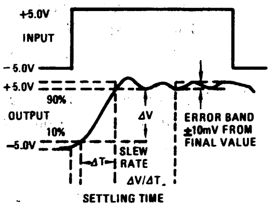


Upper 3dB Frequency
Lower 3dB Frequency - 10Hz
Broadband Noise Characteristics

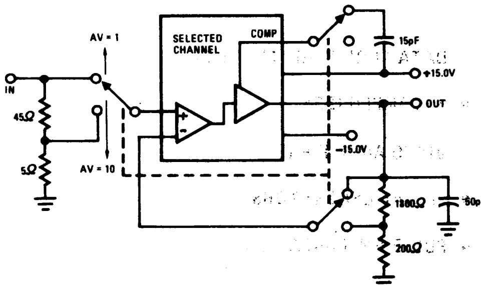
TRANSIENT RESPONSE


±200mV
INPUT
0V
OVERSHOOT
90%
OUTPUT
10%
RISE TIME
NOTE: Measured on both positive and negative transitions.

SLEW RATE AND SETTLING

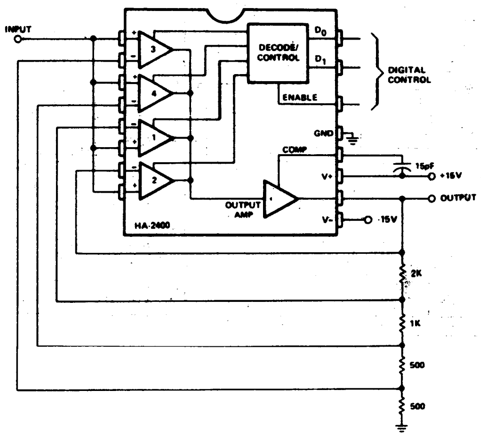

+5.0V
INPUT
-5.0V
+5.0V
90%
OUTPUT
10%
-5.0V
ΔV
ΔT
SLEW RATE
ΔV/ΔT
ERROR BAND ±10mV FROM FINAL VALUE
SETTLING TIME

SLEW RATE AND TRANSIENT RESPONSE

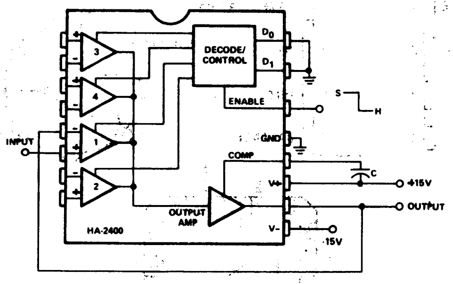

AV = 1
SELECTED CHANNEL
COMP
15pF
+15.0V
OUT
IN
45Ω
5Ω
AV = 10
-15.0V
1800Ω
50pF
200Ω

Typical Applications

AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN


INPUT
DECODE/ CONTROL
D0
D1
ENABLE
DIGITAL CONTROL
3
4
1
2
GND
COMP
15pF
V+
+15V
OUTPUT
OUTPUT AMP
V-
-15V
HA-2400
2K
1K
500
500

SAMPLE AND HOLD


DECODE/ CONTROL
D0
D1
ENABLE
S
H
INPUT
3
4
1
2
GND
COMP
C
V+
+15V
OUTPUT
OUTPUT AMP
V-
-15V
HA-2400

Sample charging rate = $\frac{I_1}{C}$ V/sec.

Hold drift rate = $\frac{I_2}{C}$ V/sec.

Switch pedestal error = $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$ A
$I_2 \approx 200 \times 10^{-9}$ A at +25°C
$\approx 600 \times 10^{-9}$ A at -55°C
$\approx 100 \times 10^{-9}$ A at +125°C
$Q \approx 2 \times 10^{-12}$ Coul.

For more examples, see Harris Application Note 514.

HARRIS

HA-2500/02/05

Precision High Slew Rate Operational Amplifiers

FEATURES

• HIGH SLEW RATE	30V/μS
• FAST SETTLING	330ns
• WIDE POWER BANDWIDTH	500kHz
• HIGH GAIN BANDWIDTH	12MHz
• HIGH INPUT IMPEDANCE	50 MΩ
• LOW OFFSET CURRENT	10nA
• INTERNALLY COMPENSATED	

APPLICATIONS

- DATA ACQUISTION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

HA-2500/2502/2505 comprise a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

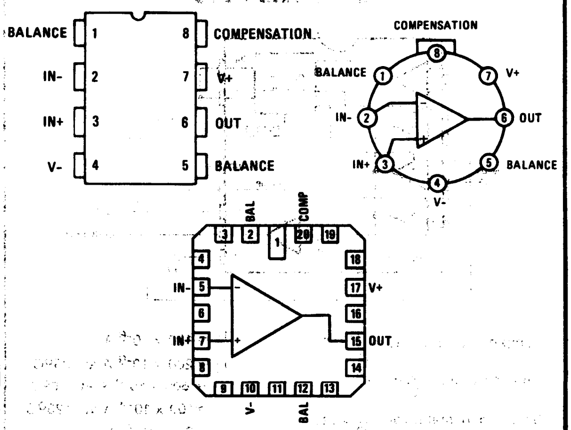
These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rate of ±25V/μs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12 MHz bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500/2502/2505 are particularly useful components in signal conditioning designs.

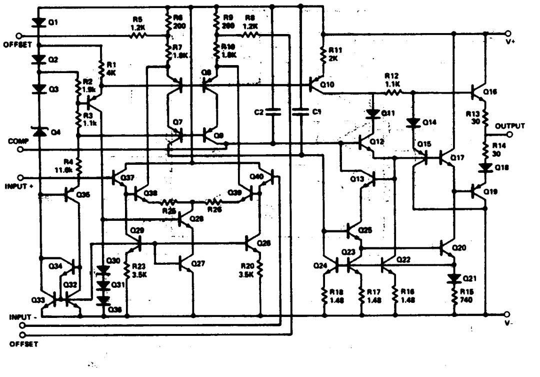
The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

HA-2500/2502/2505 are available in metal can (TO-99) packages. HA-2500 and HA-2502 are specified over the -55°C to +125°C range. HA-2505 is specified from 0°C to +75°C.

PINOUTS

TOP VIEWS


BALANCE 1
IN- 2
IN+ 3
V- 4
8 COMPENSATION
7 V+
6 OUT
5 BALANCE
COMPENSATION
8
BALANCE 1
7 V+
IN- 2
6 OUT
IN+ 3
5 BALANCE
4
V-
BAL
COMP
3 2 1 20 19
4
IN- 5
6
IN+ 7
8
18
17 V+
16
15 OUT
14
9 10 11 12 13
V-
BAL


Q1
OFFSET
Q2
Q3
Q4
COMP
INPUT +
INPUT -
OFFSET
R1 4K
R2 1.9k
R3 1.1k
R4 11.6k
R5 1.2K
R6 200
R7 1.8K
R9 200
R8 1.2K
R10 1.8K
Q6
Q7
Q8
C2
C1
R11 2K
Q10
R12 1.1K
Q11
Q14
Q16
R13 30
OUTPUT
R14 30
Q18
Q12
Q15
Q17
Q19
Q13
Q37
Q38
Q39
Q40
R25
R26
Q28
Q29
Q26
Q27
Q25
Q20
Q23
Q24
Q22
Q21
R23 3.5K
R20 3.5K
R18 1.48
R17 1.48
R16 1.48
R15 740
Q36
Q34
Q32
Q33
Q30
Q31
Q36
V+
V-

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±15.0V	HA-2500/2502	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
Peak Output Current	50mA	HA-2505	$0^{\circ}C \leq T_A \leq +75^{\circ}C$
Internal Power Dissipation	300mW	Storage Temperature Range	$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS V+ = +15V D. C., V- = -15V D. C.

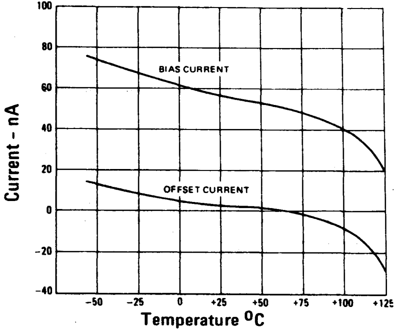
PARAMETER	TEMP.	HA-2500 -55°C to +125°C			HA-2502 -55°C to +125°C			HA-2505 0°C to 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		2	5		4	8		4	8	mV
	Full			8			10			10	mV
Offset Voltage Average Drift	Full		20			20			20		μV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 10)	+25°C	25	50		20	50		20	50		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	20K	30K		15K	25K		15K	25K		V/V
	Full	15K			10K			10K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Notes 4, 11)	+25°C	350	500		300	500		300	500		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±25	±30		±20	±30		±20	±30		V/μs
Settling Time to 0.1% (Notes 1, 5, 8 & 12)	+25°C		0.33			0.33			0.33		μs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $V_O = \pm 200mV$
8. See transient response test circuits and waveforms Page 2-31.
9. $\Delta V = \pm 5.0V$
10. This parameter value is based on design calculations.
11. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = S.R./2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$

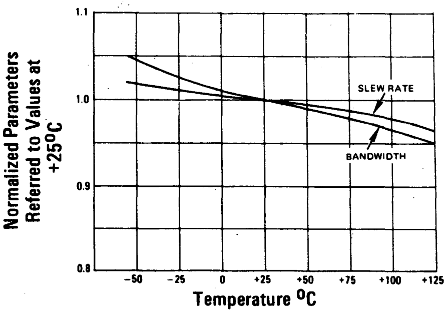
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

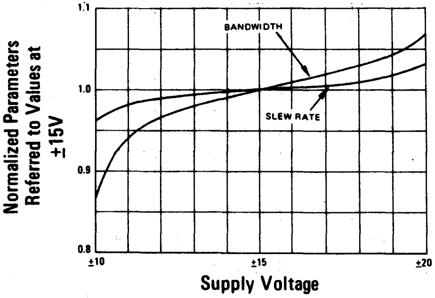
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



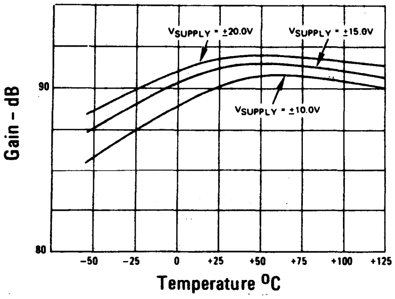
NORMALIZED AC PARAMETERS vs TEMPERATURE



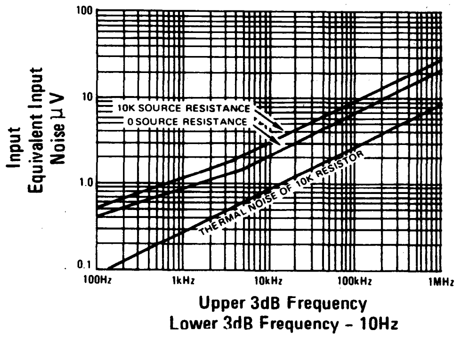
NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



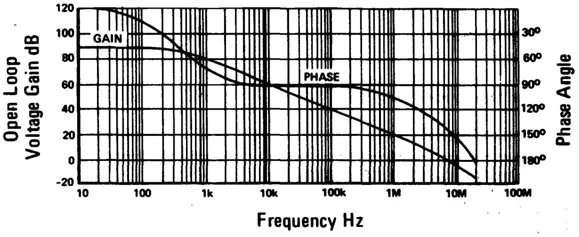
OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



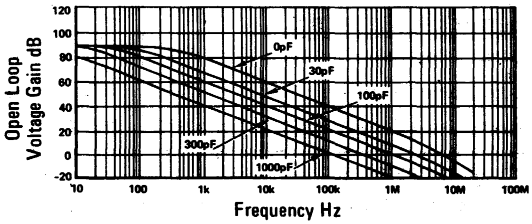
EQUIVALENT INPUT NOISE vs BANDWIDTH



OPEN-LOOP FREQUENCY AND PHASE RESPONSE

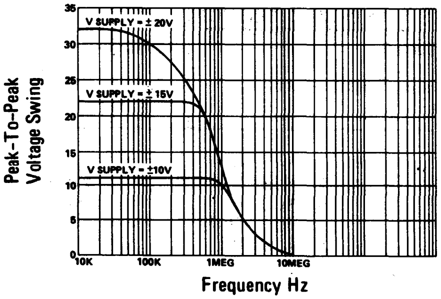


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND



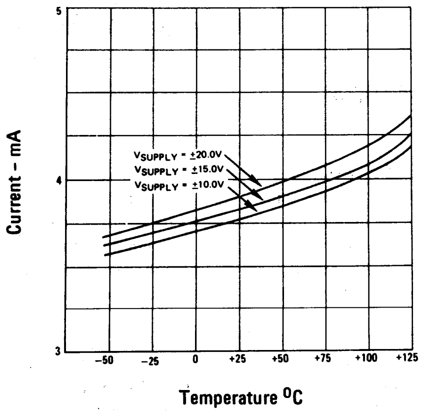
NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

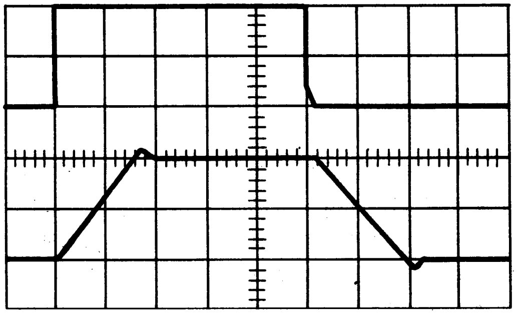


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT vs TEMPERATURE



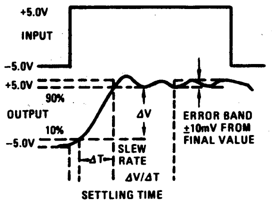
VOLTAGE FOLLOWER PULSE RESPONSE



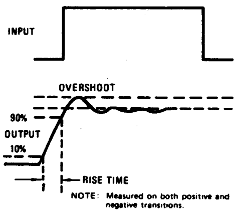
R_L = 2KΩ, C_L = 50pF
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 200ns/Div.
T_A = +25°C, V_S = ±15.0V

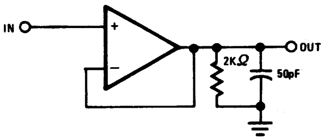
SLEW RATE AND SETTLING TIME


+5.0V
INPUT
-5.0V
+5.0V
90%
OUTPUT
10%
-5.0V
ΔV
ΔT
SLEW RATE
ΔV/ΔT
ERROR BAND ±10mV FROM FINAL VALUE
SETTLING TIME

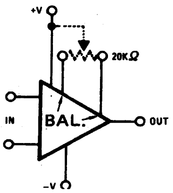
TRANSIENT RESPONSE


INPUT
OVERSHOOT
90%
OUTPUT
10%
RISE TIME
NOTE: Measured on both positive and negative transitions.

SLEW RATE AND TRANSIENT RESPONSE


IN
+
−
2KΩ
50pF
OUT

SUGGESTED VOS ADJUSTMENT


+V
20KΩ
IN
BAL.
OUT
−V

HARRIS

HA-2510/12/15

High Slew Rate Operational Amplifiers

FEATURES

• HIGH SLEW RATE	60V/µs
• FAST SETTLING	250ns
• WIDE POWER BANDWIDTH	1,000kHz
• HIGH GAIN BANDWIDTH	12MHz
• HIGH INPUT IMPEDANCE	100MΩ
• LOW OFFSET CURRENT	10nA
• INTERNALLY COMPENSATED	

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

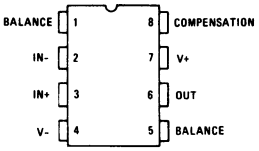
The HA-2510/2512/2515 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidth for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

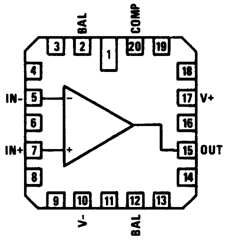
The ±60V/µs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/2512/2515's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in R. F. and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

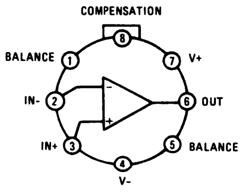
The HA-2510 and HA-2512 have guaranteed operation form -55°C to +125°C and are available in metal can and ceramic mini DIP packages. Both are offered as a military grade part with the HA-2510 also available in LCC package. The HA-2515 has guaranteed operation from 0°C to +75°C and is available in plastic and ceramic mini DIP and metal can packages.

PINOUTS

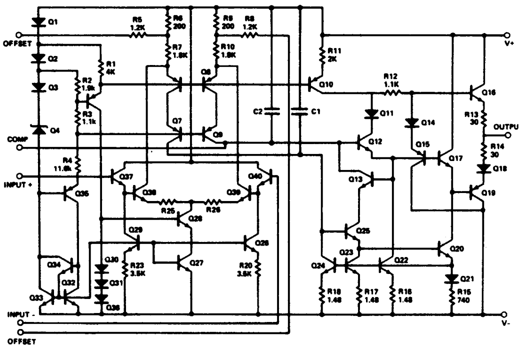
TOP VIEWS


BALANCE 1
IN- 2
IN+ 3
V- 4
8 COMPENSATION
7 V+
6 OUT
5 BALANCE


BAL
COMP
3 2 1 20 19
4
IN- 5
6
IN+ 7
8
18
17 V+
16
15 OUT
14
9 10 11 12 13
V-
BAL


COMPENSATION
8
BALANCE 1
7 V+
IN- 2
6 OUT
IN+ 3
5 BALANCE
4
V-

SCHEMATIC


OFFSET
COMP
INPUT +
INPUT -
OFFSET
V+
OUTPUT
V-
C1
C2

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±15.0V	HA-2510/2512	-55°C $\leq T_A \leq$ +125°C
Peak Output Current	50mA	HA-2515	0°C $\leq T_A \leq$ +75°C
Internal Power Dissipation	300mW	Storage Temperature Range	-65°C $\leq T_A \leq$ +150°C

ELECTRICAL CHARACTERISTICS V+ = +15V D. C., V- = -15V D. C.

PARAMETER	TEMP.	HA-2510 -55°C to +125°C MIN	TYP	MAX	HA-2512 -55°C to +125°C MIN	TYP	MAX	HA-2515 0°C to 75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 10)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4, 11)	+25°C	750	1000		600	1000		600	1000		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±50	±65		±40	±60		±40	±60		V/µs
Settling Time (Notes 1, 5, 8 & 12)	+25°C		0.25			0.25			0.25		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio	Full	80	90		74	90		74	90		dB

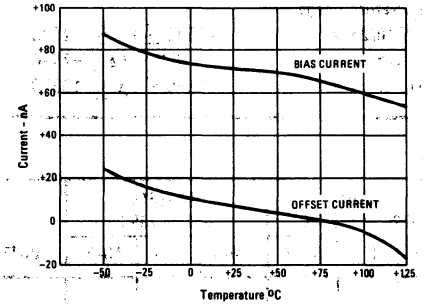
NOTES:

1. R_L = 2kΩ
2. V_{CM} = ±10V
3. A_V > 10
4. V_O = ±10.0V
5. C_L = 50pF
6. V_O = ±200mV
7. V_O = ±200mV
8. See transient response test circuits and waveforms Page 2-35.
9. ΔV = ±5.0V
10. This parameter value is based on design calculations.
11. Full power bandwidth guaranteed based on slew rate measurement using: FPBW = S. R./$2\pi V_{peak}$.
12. V_{OUT} = ±5V

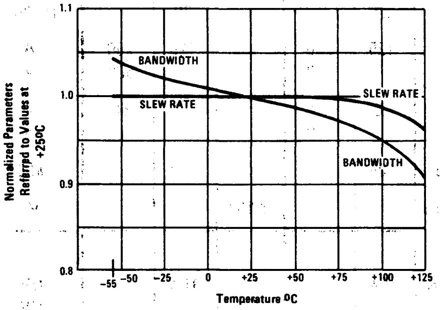
PERFORMANCE CURVES

V+ = 15V D. C., T_A = 25°C unless otherwise stated.

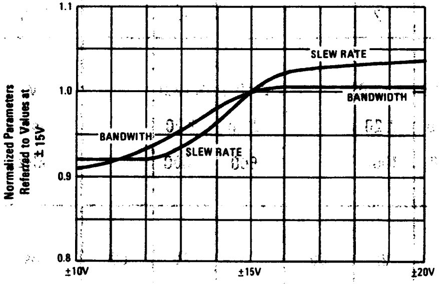
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



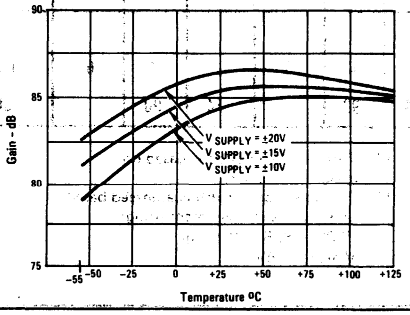
NORMALIZED AC PARAMETERS vs. TEMPERATURE



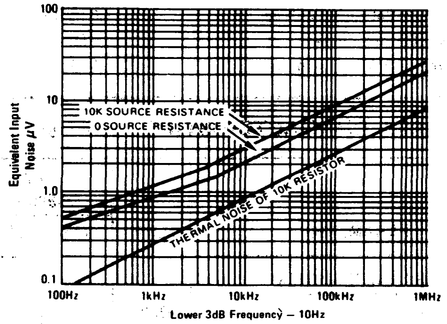
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



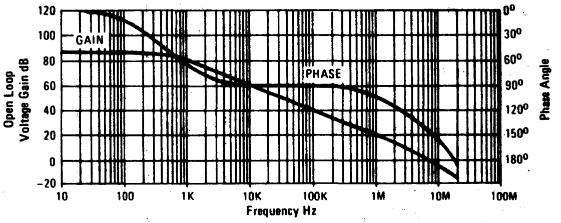
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



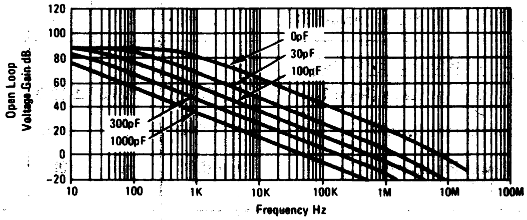
EQUIVALENT INPUT NOISE vs. BANDWIDTH



OPEN LOOP FREQUENCY AND PHASE RESPONSE

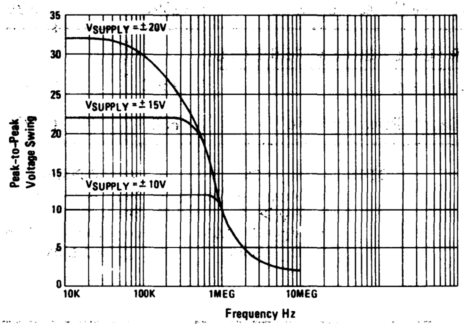


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND



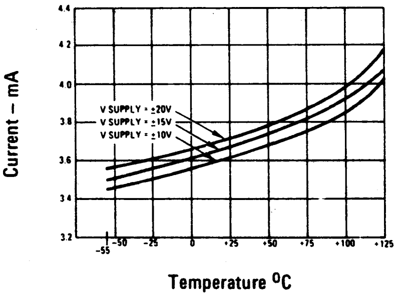
NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C

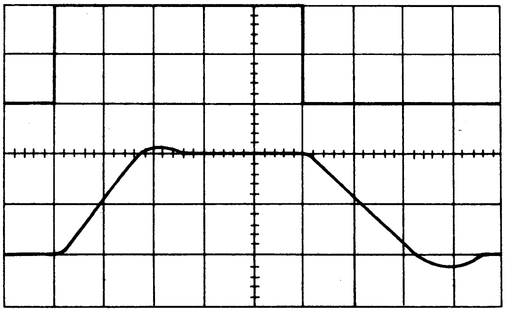


PERFORMANCE CURVES *(continued)*

POWER SUPPLY CURRENT vs TEMPERATURE



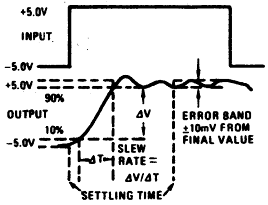
VOLTAGE FOLLOWER PULSE RESPONSE



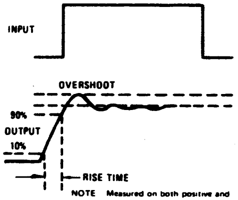
R_L = 2K Ω, C_L = 50pF
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 100n/Div.
T_A = +25°C, V_S = ±15.0V

SLEW RATE AND SETTLING TIME

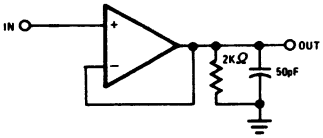

+5.0V
INPUT
-5.0V
+5.0V
90%
OUTPUT
10%
-5.0V
ΔV
ERROR BAND ±10mV FROM FINAL VALUE
ΔT
SLEW RATE = ΔV/ΔT
SETTLING TIME

TRANSIENT RESPONSE

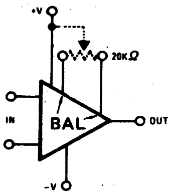

INPUT
OVERSHOOT
90%
OUTPUT
10%
RISE TIME

NOTE Measured on both positive and negative transitions

SLEW RATE AND TRANSIENT RESPONSE


IN
+
-
2KΩ
50pF
OUT

SUGGESTED VOS ADJUSTMENT


+V
20KΩ
IN
BAL
OUT
-V

HARRIS

HA-2520/22/25

Uncompensated High Slew Rate Operational Amplifiers

FEATURES

• HIGH SLEW RATE	120V/μs
• FAST SETTLING	200ns
• WIDE POWER BANDWIDTH	2,000kHz
• HIGH GAIN BANDWIDTH	20MHz
• HIGH INPUT IMPEDANCE	100MΩ
• LOW OFFSET CURRENT	10nA

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

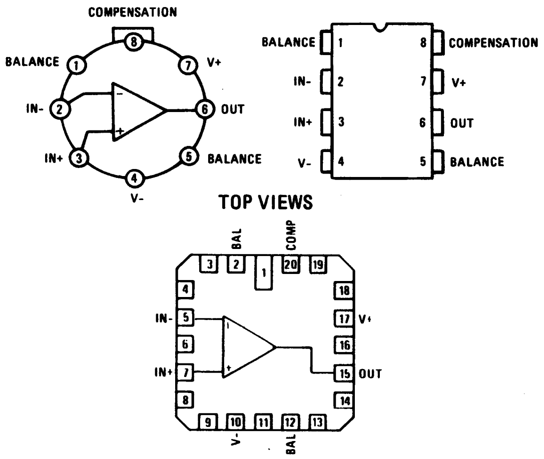
DESCRIPTION

HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at close loop gains greater than 3 without external compensation. In addition, these high performance components also provide low offset current and high input impedance.

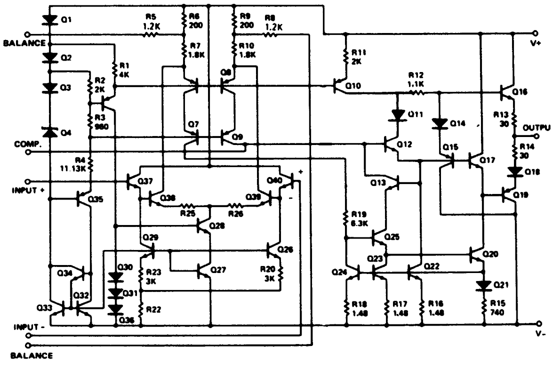
120V/μ s slew rate and 200ns (0.2%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R. F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complimented by 10nA offset current, 200MΩ input impedance and offset trim capability.

The HA-2520 and HA-2522 have guaranteed operation from -55°C to +125°C and are available in metal can and ceramic mini DIP package. Both are offered as a military grade part with the HA-2520 also available in LCC package. The HA-2525 has guaranteed operation from 0°C to +75°C and is available in plastic and ceramic mini DIP and metal can packages.

PINOUTS


COMPENSATION
8
BALANCE
1
7
V+
IN-
2
6
OUT
IN+
3
5
BALANCE
4
V-
BALANCE 1
IN- 2
IN+ 3
V- 4
8 COMPENSATION
7 V+
6 OUT
5 BALANCE
TOP VIEWS
BAL
COMP
3
2
1
20
19
4
18
IN- 5
17 V+
6
16
IN+ 7
15 OUT
8
14
9
10
11
12
13
V-
BAL

SCHEMATIC


Q1
R5 1.2K
R6 200
R9 200
R8 1.2K
BALANCE
V+
R7 1.8K
R10 1.8K
R11 2K
Q2
R1 4K
R2 2K
Q8
Q10
R12 1.1K
Q3
Q16
Q11
Q14
R3 980
R13 30
Q4
Q7
Q9
OUTPUT
COMP.
Q12
Q15
R14 30
Q17
R4 11.13K
Q18
Q37
Q40
+
INPUT +
Q13
Q35
Q38
Q39
-
Q19
R25
R26
R19 6.3K
Q28
Q29
Q25
Q26
Q23
Q20
Q22
Q30
R23 3K
Q27
R20 3K
Q24
Q34
Q21
Q31
Q32
R22
R18 1.48
R17 1.48
R16 1.48
R15 740
Q33
Q36
INPUT -
V-
BALANCE

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V
Differential Input Voltage	± 15.0V
Peak Output Current	50mA
Internal Power Dissipation	300mW

Operating Temperature Ranges:	
HA-2520/HA-2522	$-55^\circ C \leq T_A \leq +125^\circ C$
HA-2525	$0^\circ C \leq T_A \leq +75^\circ C$
Storage Temperature Range:	$-65^\circ C \leq T_A \leq +150^\circ C$

ELECTRICAL CHARACTERISTICS $V+ = +15V$ D. C., $V- = -15V$ D. C.

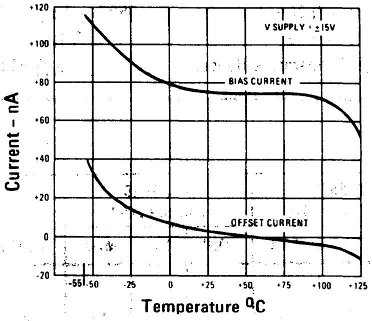
PARAMETER	TEMP	HA-2520 -55°C to +125°C MIN	TYP	MAX	HA-2522 -55°C to +125°C MIN	TYP	MAX	HA-2525 0°C to +75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		μV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 9)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	± 10.0			± 10.0			± 10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Notes 3, 12)	+25°C	10	20		10	20		10	20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	± 10.0	± 12.0		± 10.0	± 12.0		± 10.0	± 12.0		V
Output Current (Note 4)	+25°C	± 10	± 20		± 10	± 20		± 10	± 20		mA
Full Power Bandwidth (Notes 4, 10)	+25°C	1500	2000		1200	1600		1200	1600		kHz
TRANSIENT RESPONSE ($A_V = +3$)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 11)	+25°C	± 100	± 120		± 80	± 120		± 80	± 120		V/μs
Settling Time (Notes 1, 5, 8 & 11)	+25°C		0.20			0.20			0.20		μs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See Transient Response Test Circuits and Waveforms Page 2-39
9. This parameter value is based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement $FPBW = S.R./2\pi V_{peak}$.
11. $V_{OUT} = \pm 5V$
12. Guaranteed by design.

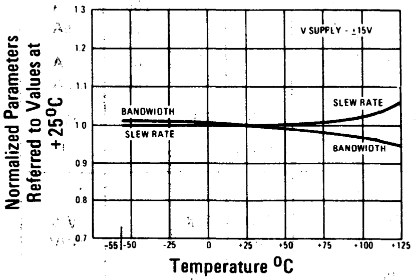
PERFORMANCE CURVES

V+ = 15V D. C., T_A = 25°C unless otherwise stated.

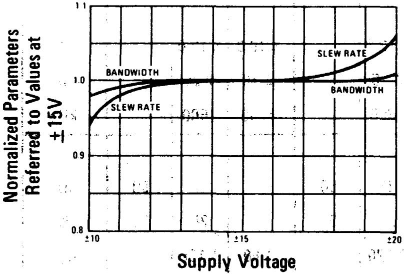
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



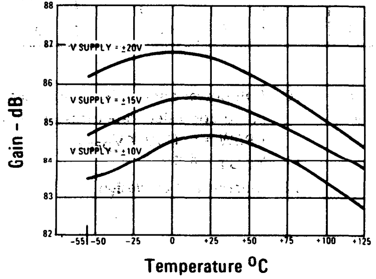
NORMALIZED AC PARAMETERS vs TEMPERATURE



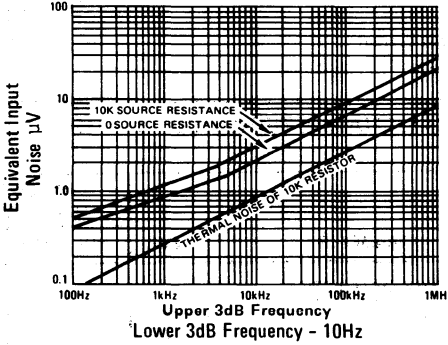
NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



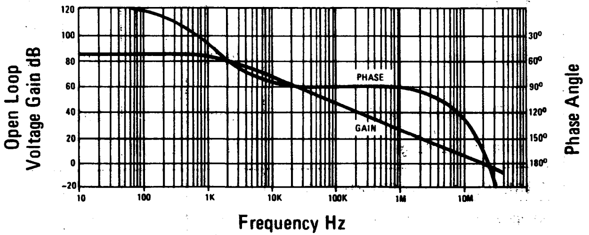
OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



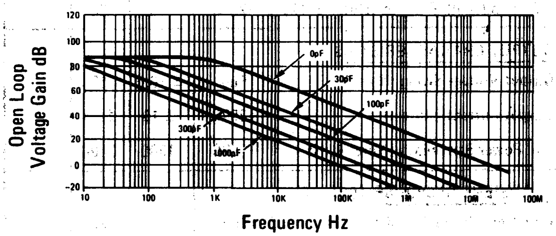
EQUIVALENT INPUT NOISE vs BANDWIDTH



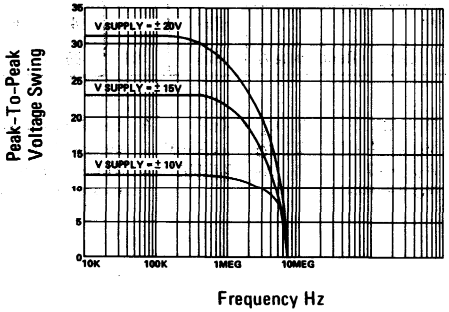
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

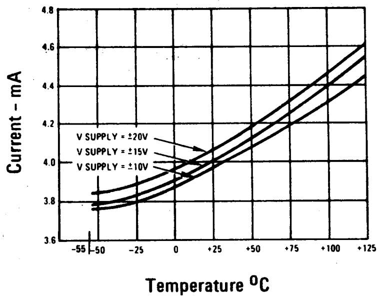


OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C

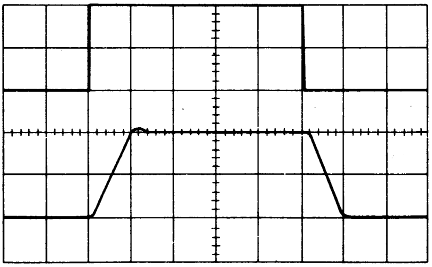


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT vs TEMPERATURE



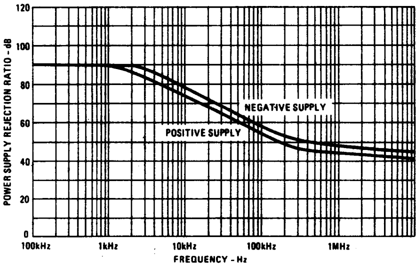
VOLTAGE FOLLOWER PULSE RESPONSE



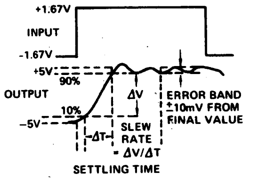
$R_L = 2K\Omega$, $C_L = 50pF$
Upper Trace: Input; 1.67V/Div.
Lower Trace: Output; 5V/Div.

Horizontal = 100ns/Div.
$T_A = +25^oC$, $V_S = \pm15V$

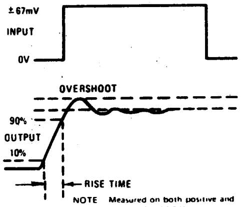
POWER SUPPLY REJECTION RATIO VS. FREQUENCY



SLEW RATE AND SETTLING TIME

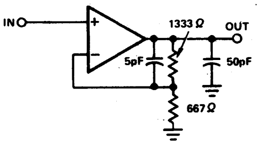

+1.67V
INPUT
-1.67V
+5V
90%
OUTPUT
10%
-5V
ΔV
ΔT
SLEW RATE = ΔV/ΔT
ERROR BAND ±10mV FROM FINAL VALUE
SETTLING TIME

TRANSIENT RESPONSE

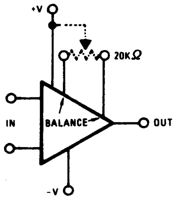

±67mV
INPUT
0V
OVERSHOOT
90%
OUTPUT
10%
RISE TIME

NOTE Measured on both positive and negative transitions

SLEW RATE AND TRANSIENT RESPONSE

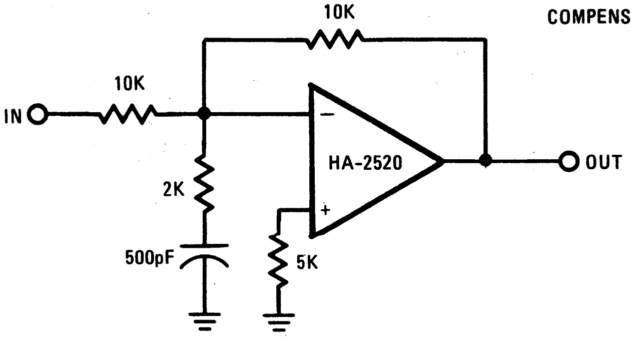

IN
+
-
1333 Ω
OUT
5pF
50pF
667 Ω

SUGGESTED VOS ADJUSTMENT


+V
20K Ω
IN
BALANCE
OUT
-V

TYPICAL APPLICATIONS

COMPENSATION CIRCUIT FOR INVERTING UNITY GAIN


10K
10K
IN
-
+
HA-2520
OUT
2K
500pF
5K

Slew Rate	≈	120V/μs
Bandwidth	≈	10MHz
Settling Time	≈	500ns

HA-2539

Very High Slew Rate Wideband Operational Amplifiers

Features

VERY HIGH SLEW RATE	600V/μs
OPEN LOOP GAIN	15kV/V
WIDE GAIN-BANDWIDTH	600MHz
POWER BANDWIDTH	9.5MHz
LOW OFFSET VOLTAGE	3mV
INPUT VOLTAGE NOISE	$6nV/\sqrt{Hz}$
OUTPUT VOLTAGE SWING	±10V

Applications

- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- RF OSCILLATORS

Description

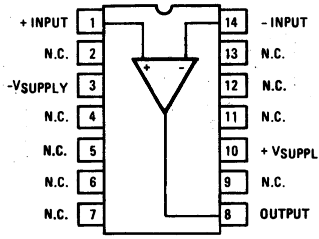
The Harris HA-2539 represents the ultimate in high slew rate wideband, monolithic, operational amplifiers. It has been designed and constructed with the Harris high frequency Bipolar dielectric isolation process and features dynamic parameters never before available from a truly differential device.

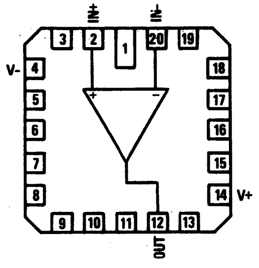
With a 600V/μs slew rate and a 600MHz gain-band-width-product, the HA-2539 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full ±10V swing coupled with outstanding A.C. parameters and complemented by high open loop gain makes the devices useful in high speed data acquisition systems.

The HA-2539 is available in the 14 pin ceramic and epoxy packages, as well as a 20 pin LCC package. The HA-2539-2 denotes -55°C to +125°C operation while the HA-2539-5 operates over the 0°C to +75°C range.

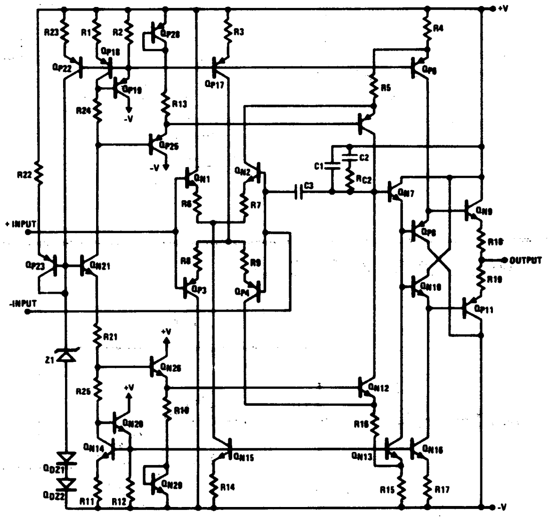
Pinouts

TOP VIEWS


+INPUT
1
N.C.
2
-VSUPPLY
3
N.C.
4
N.C.
5
N.C.
6
N.C.
7
+
-
14
-INPUT
13
N.C.
12
N.C.
11
N.C.
10
+VSUPPLY
9
N.C.
8
OUTPUT


-IN
+IN
3
2
1
20
19
V-
4
5
6
7
8
18
17
16
15
14
V+
9
10
11
12
13
OUT
+
-

Schematic


+V
-V
+INPUT
-INPUT
OUTPUT
R1
R2
R3
R4
R5
R7
R8
R9
R11
R12
R13
R14
R15
R17
R18
R19
R21
R22
R23
R24
R25
RC2
C1
C2
C3
Z1
QDZ1
QDZ2
QP1
QP3
QP4
QP6
QP8
QP11
QP17
QP18
QP19
QP22
QP23
QP25
QP28
QN1
QN2
QN7
QN9
QN10
QN12
QN13
QN14
QN15
QN16
QN21
QN26
QN28
QN29

Specifications

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals		35V
Differential Input Voltage		6V
Output Current		50mA (Peak)
Internal Power Dissipation (Note 2)		870mW (Cerdip)
Operating Temperature Range:	(HA-2539-2)	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
	(HA-2539-5)	$0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range		$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; $R_L =$ 1K ohms, unless otherwise specified.

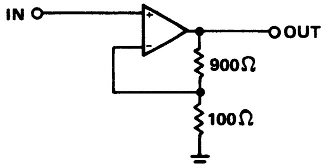
		HA-2539-2 -55°C to +125°C			HA-2539-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		8	10		8	15	mV
	FULL		13	15			20	mV
Average Offset Voltage Drift	FULL		20			20		μV/°C
Bias Current	+25°C		5	20		5	20	μA
	FULL			25			25	μA
Offset Current	+25°C		1	6		1	6	μA
	FULL			8			8	μA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±10			±10			V
Input Voltage Noise (f = 1kHz, $R_g = 0\Omega$)	+25°C		6			6		nV/$\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10K	15K		10K	15K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	60			60			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		600			600		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±10			±10			V
Output Current (Note 3)	+25°C	10			10			mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	8.7	9.5		8.7	9.5		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		7			7		ns
Overshoot	+25°C		15			15		%
Slew Rate	+25°C	550	600		550	600		V/μs
Settling Time: **10V Step to 0.1%**	+25°C		200			200		ns
POWER REQUIREMENTS								
Supply Current	FULL		20	25		20	25	mA
Power Supply Rejection Ratio (Note 9)	FULL	60			60			dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7mW/°C for operation at ambient temperatures above +75°C. Heat sinking required at temperatures above +75°C. T_{JA} = 115°C/W; T_{JC} = 35°C/W. Thermalloy model 6007 heat sink recommended.
3. $R_L = 1K\Omega$, $VO = \pm 10V$
4. $V_{CM} = \pm 10V$
5. $V_O = 90mV$.
6. $A_V = 10$.
7. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.
8. Refer to Test Circuits section of data sheet.
9. $V_{SUPPLY} = \pm 5$ VDC to ± 15 VDC

Test Circuits

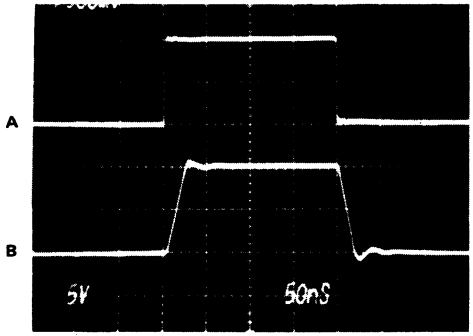
LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT *



$A_V = 10$
$^*C_L \leq 10pF$

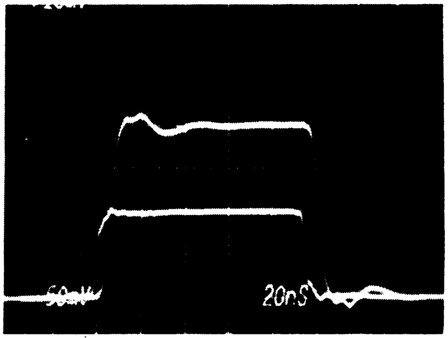
LARGE SIGNAL RESPONSE

Vertical Scale: A=0.5V/Div., B=5.0V/Div.
Horizontal Scale: Time: 50ns/Div.

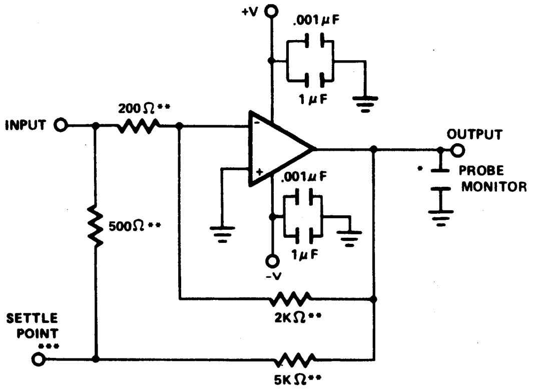


SMALL SIGNAL RESPONSE

Vertical Scale: Input=10mV/Div., Output=50mV/Div.
Horizontal Scale: 20ns/Div.



SETTLING TIME TEST CIRCUIT



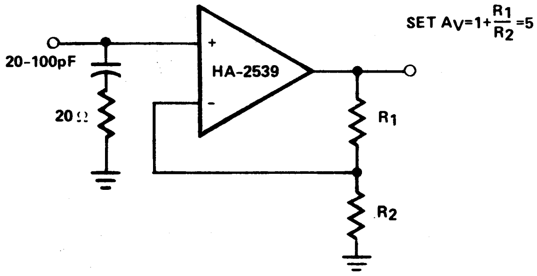
* Load Capacitance should be less than 10pF.

** It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched.

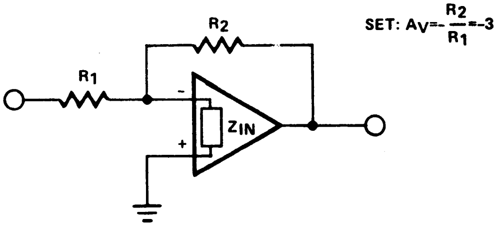
*** SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

Applications

FREQUENCY COMPENSATION
COMPENSATION BY OVERDAMPING

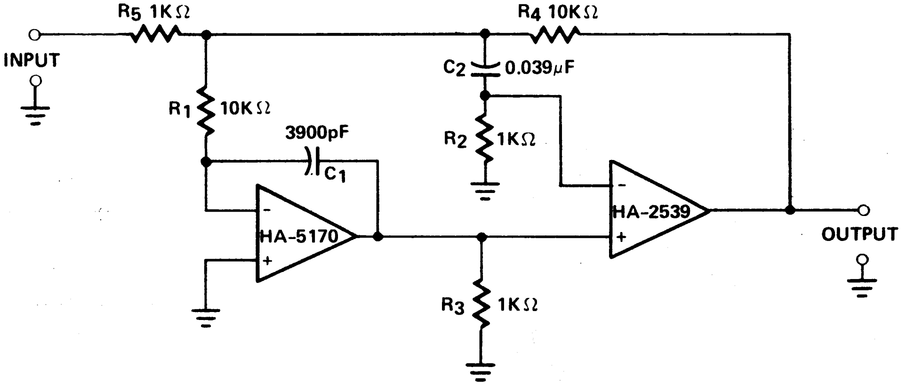

SET $A_V=1+\frac{R_1}{R_2}=5$
20-100pF
20Ω
+
-
HA-2539
R_1
R_2

STABILIZATION USING Z_{IN}

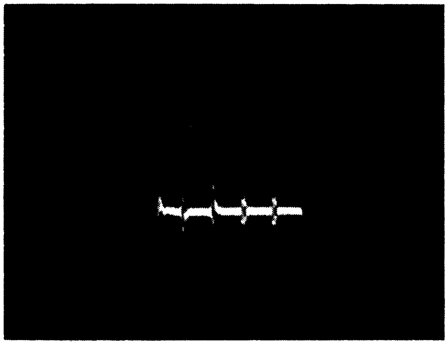

SET: $A_V=-\frac{R_2}{R_1}=-3$
R_2
R_1
-
+
Z_{IN}

REDUCING DC ERRORS

COMPOSITE AMPLIFIER

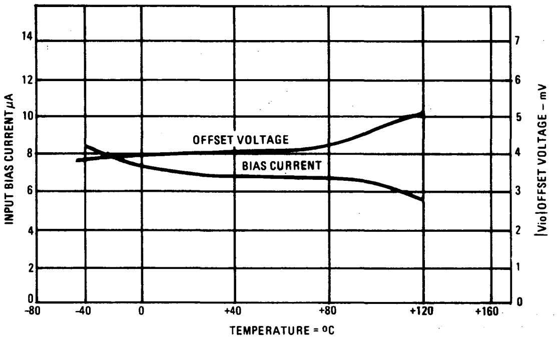

R_5 1KΩ
R_4 10KΩ
INPUT
C_2 0.039μF
R_1 10KΩ
3900pF
C_1
R_2 1KΩ
-
+
HA-5170
HA-2539
OUTPUT
R_3 1KΩ

DIFFERENTIAL GAIN ERROR (3%)
HA-2539 20dB VIDEO GAIN BLOCK

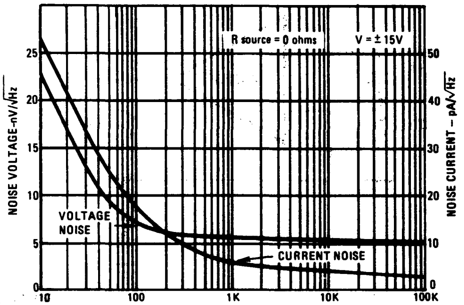


Performance Curves

INPUT OFFSET VOLTAGE AND BIAS CURRENT VS TEMPERATURE



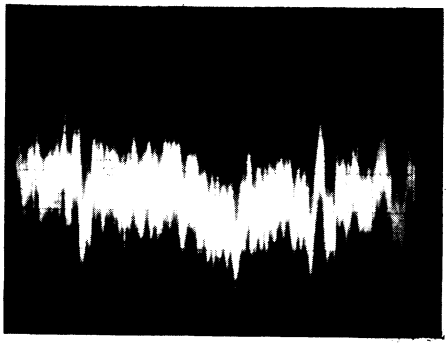
INPUT NOISE VOLTAGE AND NOISE CURRENT VS FREQUENCY



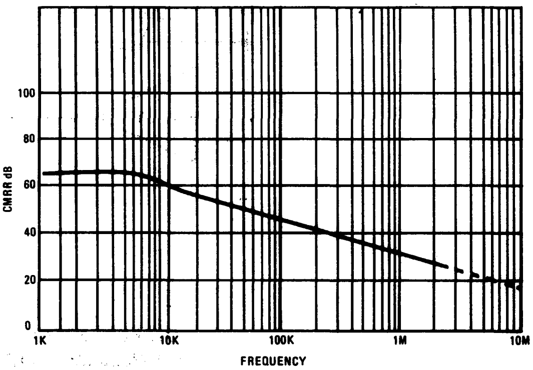
BROADBAND NOISE (0.1Hz to 1mHz)

Vertical Scale: 10 μV/Div.

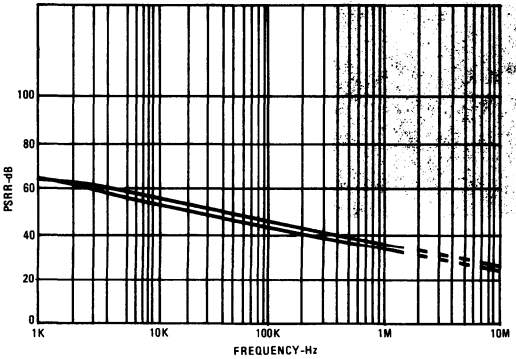
Horizontal Scale: 50ms/Div.



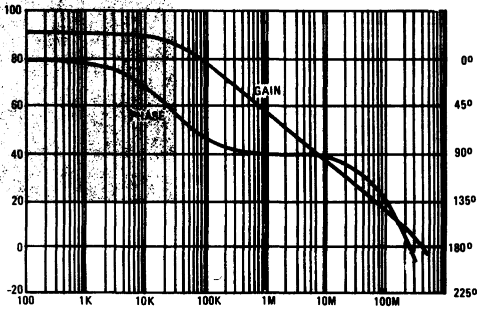
COMMON MODE REJECTION RATIO VS FREQUENCY



POWER SUPPLY REJECTION RATIO VS FREQUENCY

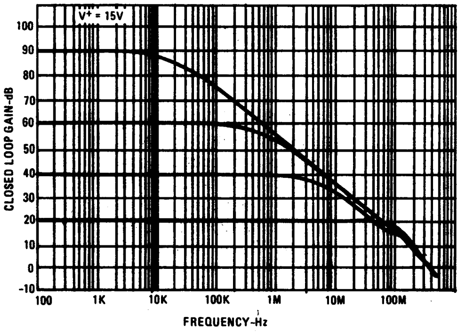


OPEN LOOP GAIN/PHASE VS FREQUENCY HA-2539

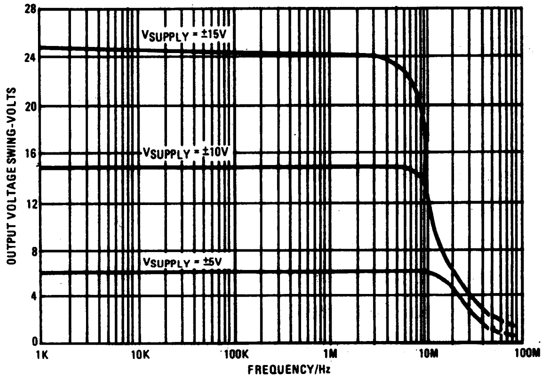


Performance Curves (Continued)

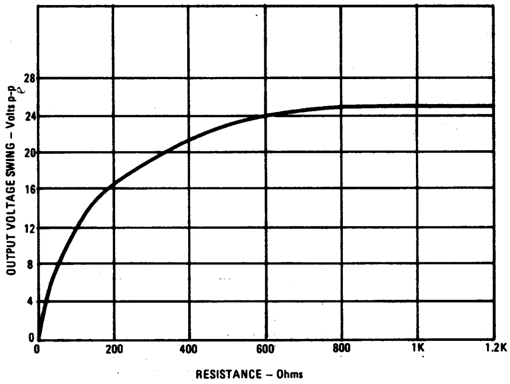
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



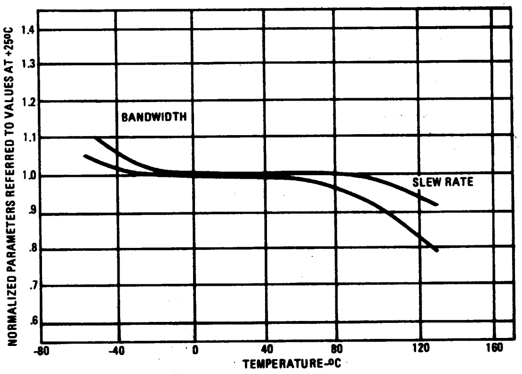
OUTPUT VOLTAGE SWING VS. FREQUENCY



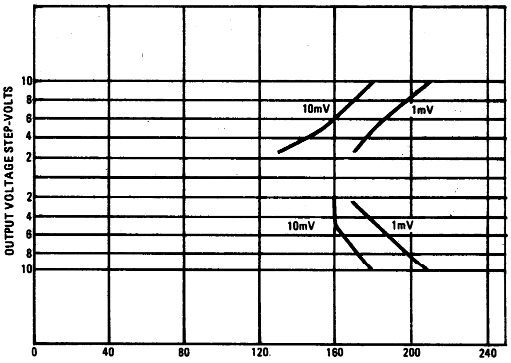
OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



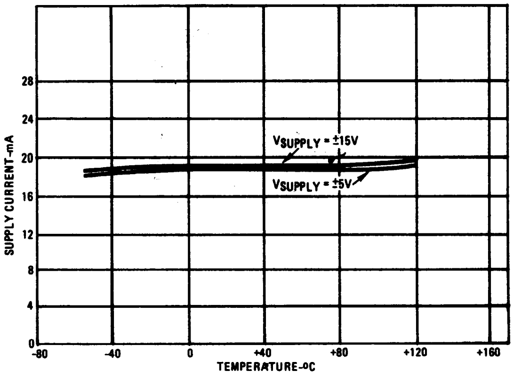
NORMALIZED AC PARAMETERS VS. TEMPERATURE



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



HARRIS

HA-2540

Wideband, Fast Settling Operational Amplifiers

FEATURES

VERY HIGH SLEW RATE	400V/μs
FAST SETTLING TIME	200ns
WIDE GAIN-BANDWIDTH	400MHz
POWER BANDWIDTH	6MHz
LOW OFFSET VOLTAGE	8mV
INPUT VOLTAGE NOISE	6nV/$\sqrt{Hz}$
OUTPUT VOLTAGE SWING	±10V
MONOLITHIC BIPOLAR CONSTRUCTION	

APPLICATIONS

- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- FAST, PRECISE D/A CONVERTERS

GENERAL DESCRIPTION

The Harris HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance in circuits where closed loop gain is 10 or greater. Additionally, the HA-2540 has a drive capability of ±10V into a 1K ohm load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

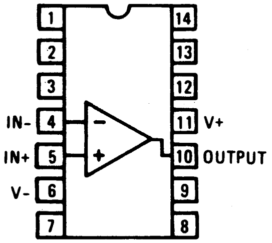
A 400V/ μs slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth-product is ideally suited for wideband signal amplification. A settling time of 200ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

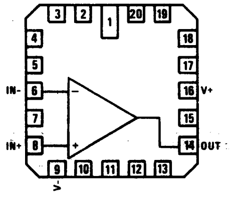
The HA-2540-2 is specified over the -55°C to +125°C range while the HA-2540-5 is specified from 0°C to +75°C.

The HA-2540 is available in the 14 pin ceramic and epoxy packages, as well as a 20 pin LCC package.

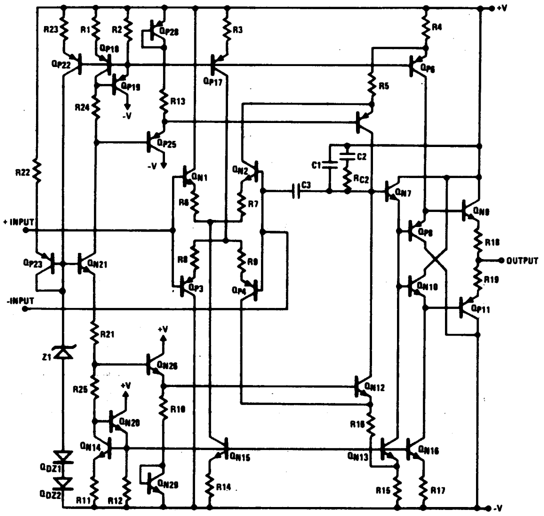
PINOUT

TOP VIEWS


1
2
3
IN- 4
IN+ 5
V- 6
7
14
13
12
11 V+
10 OUTPUT
9
8
-
+


3
2
1
20
19
4
5
IN- 6
7
IN+ 8
18
17
16 V+
15
14 OUT
9
10
11
12
13
V-
-
+

SCHEMATIC


+V
R23
R1
R2
QP28
R3
R4
QP18
QP22
QP19
QP17
QP6
R5
R24
-V
R13
QP25
-V
R22
QN1
QN2
C1
C2
RC2
C3
QN7
R6
R7
QN8
+ INPUT
QP8
R8
R9
R18
QP23
QN21
OUTPUT
QP3
QP4
QN10
R19
-INPUT
QP11
R21
+V
Z1
QN26
QN12
R25
+V
R10
QN20
R16
QN14
QN15
QN13
QN16
QDZ1
QN29
R14
R15
R17
QDZ2
R11
R12
-V

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip)
Operating Temperature Range: (HA-2540-2)	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
(HA-2540-5)	$0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range	$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS

V_{SUPPLY} = ±15 Volts; R_L = 1K ohms, unless otherwise specified.

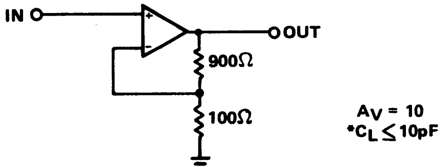
		HA-2540-2 -55°C to +125°C			HA-2540-5 0°C to +75°C			
PARAMETER	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		8	10		8	15	mV
	FULL		13	15			20	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	20		5	20	µA
	FULL			25			25	µA
Offset Current	+25°C		1	6		1	6	µA
	FULL			8			8	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±10			±10			V
Input Noise Voltage (f = 1kHz, R_g = 0Ω)	+25°C		6			6		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10K	15K		10K	15K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	60			60			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		400			400		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±10			±10			V
Output Current (Note 3)	+25°C	10			10			mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	5.5	6		5.5	6		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		14			14		ns
Overshoot	+25°C		5			5		%
Slew Rate	+25°C	350	400		350	400		V/µs
Settling Time: 10V Step to 0.1%	+25°C		200			200		ns
POWER REQUIREMENTS								
Supply Current	FULL		20	25		20	25	mA
Power Supply Rejection Ratio (Note 9)	FULL	60			60			dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7mW/°C for operation at ambient temperatures above +75°c. Heat sinking required at temperatures above +75°c. T_{JA} = 115°C/W; T_{JC} = 35°C/W. Thermalloy model 6007 heat sink recommended.
3. $R_L = 1K\Omega$, $V0 = \pm 10V$
4. $V_{CM} = \pm 10V$
5. $V_0 = 90mV$.
6. $A_V = 10$.
7. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.
8. Refer to Test Circuits section of data sheet.
9. $V_{SUPPLY} = \pm 5$ VDC to ± 15 VDC

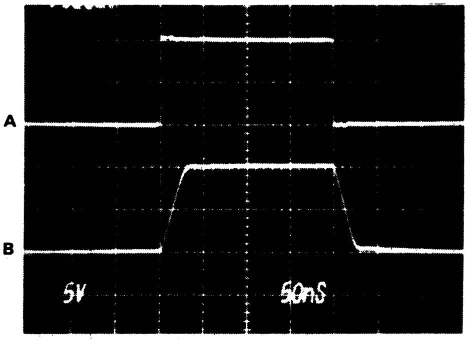
TEST CIRCUITS

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT*



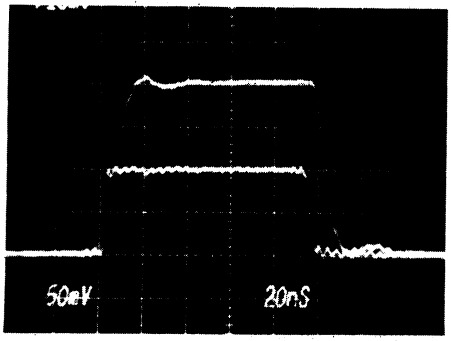
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A=0.5v/Div., B=5.0V/Div.)
Horizontal Scale: (Time: 50ns/Div.)

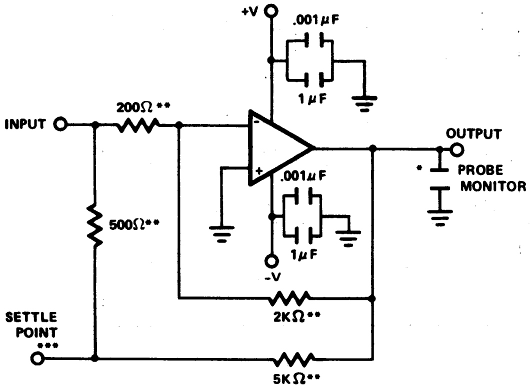


SMALL SIGNAL RESPONSE

Vertical Scale: Input=10mV/Div.; Output=50mV/Div.
Horizontal Scale: 20ns/Div.



SETTLING TIME TEST CIRCUIT



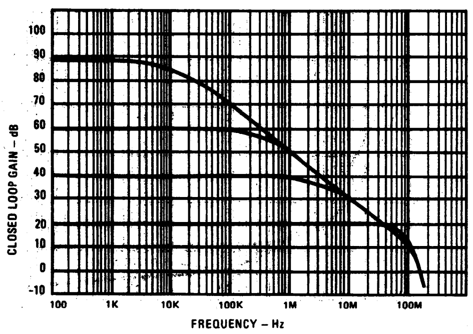
* Load Capacitance should be less than 10pF.

** It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched.

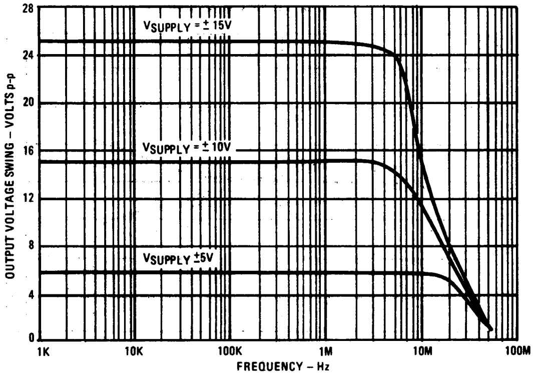
*** SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

PERFORMANCE CURVES (Continued)

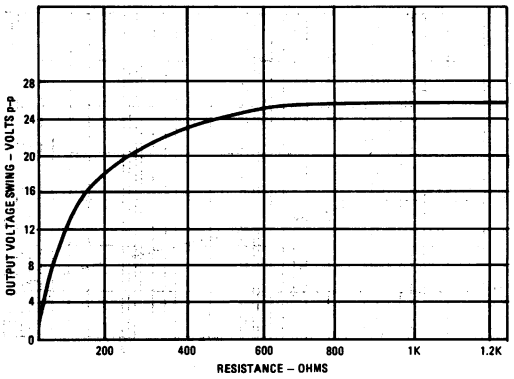
CLOSED LOOP FREQUENCY RESPONSE



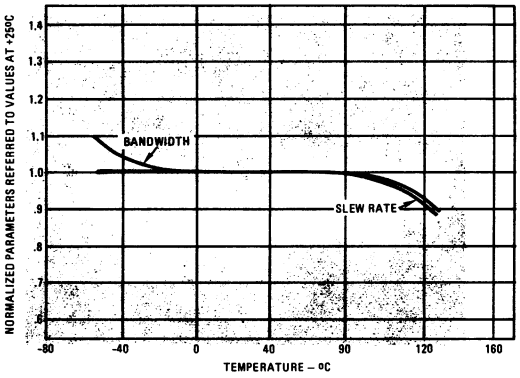
OUTPUT VOLTAGE SWING VS. FREQUENCY



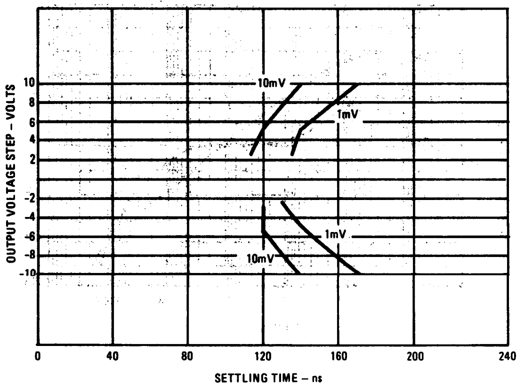
OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



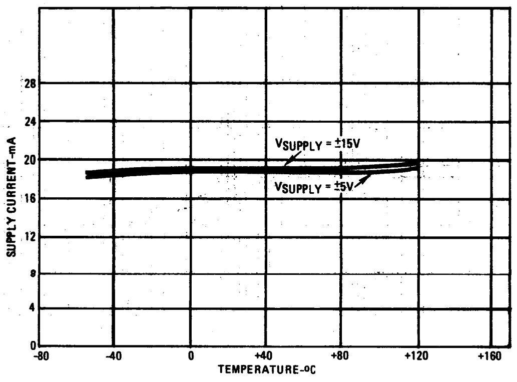
NORMALIZED AC PARAMETERS VS. TEMPERATURE



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

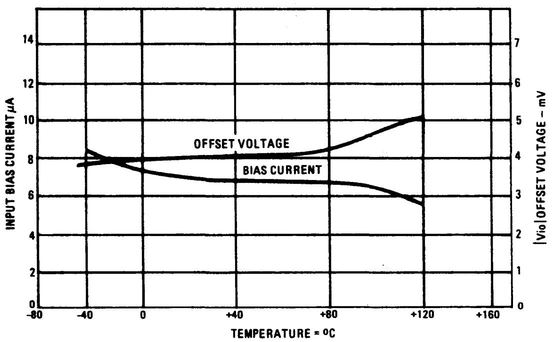


POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE

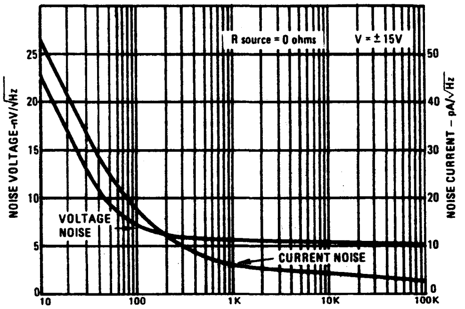


PERFORMANCE CURVES

INPUT OFFSET VOLTAGE AND BIAS CURRENT VS. TEMPERATURE



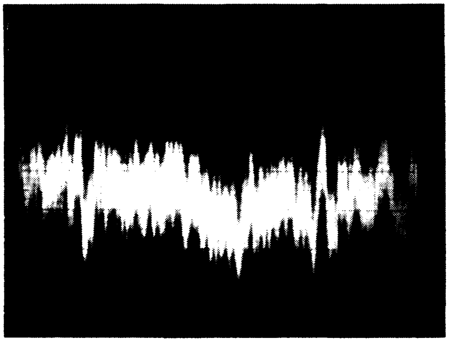
INPUT NOISE VOLTAGE AND NOISE CURRENT VS. FREQUENCY



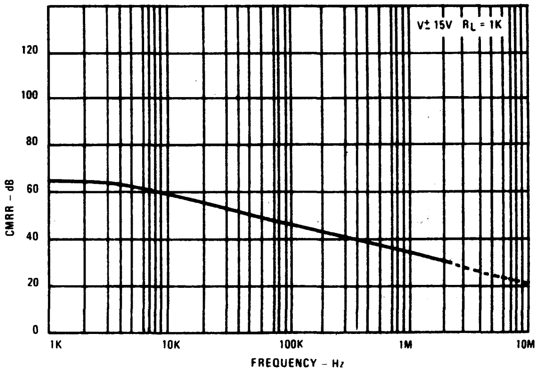
BROADBAND NOISE (0.1Hz TO 1MHz)

Vertical Scale: 10 μV/Div.

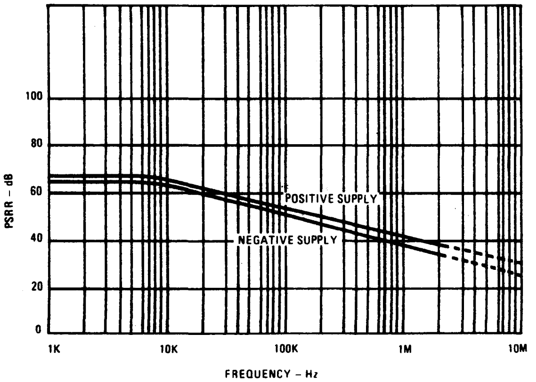
Horizontal Scale: 50ms/Div.



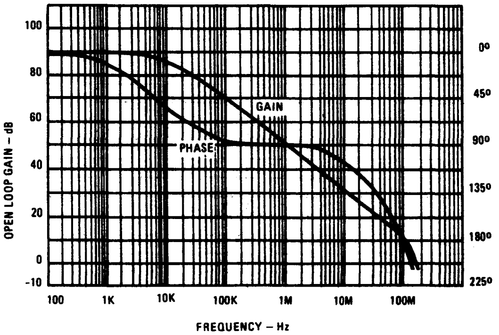
COMMON MODE REJECTION RATIO VS. FREQUENCY



POWER SUPPLY REJECTION RATIO VS. FREQUENCY

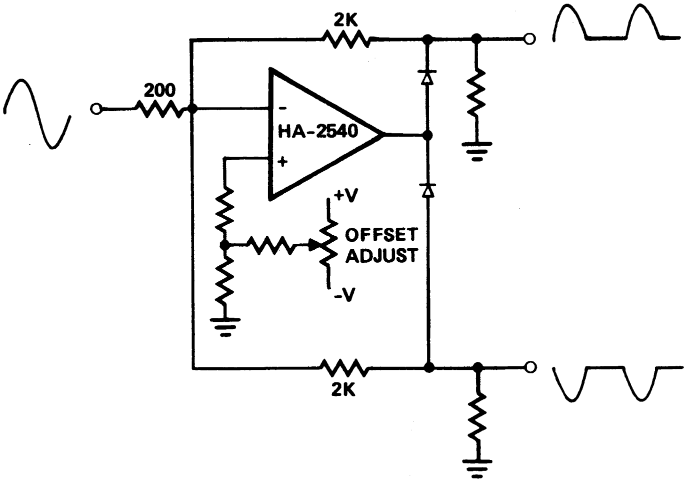


OPEN LOOP GAIN/PHASE VS. FREQUENCY HA-2540

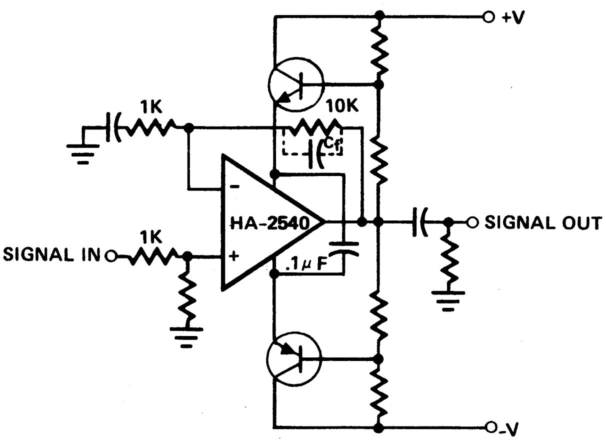


WIDEBAND SIGNAL SPLITTER

With one HA-2540 and two low capacitance switching diodes, signals exceeding 10MHz can be separated. This circuit is most useful for full wave rectification, AM detectors or sync generation.


2K
200
HA-2540
-
+
+V
OFFSET
ADJUST
-V
2K

BOOTSTRAPPING FOR MORE OUTPUT CURRENT AND VOLTAGE SWING


+V
1K
10K
Cf
HA-2540
-
+
SIGNAL IN
1K
.1μF
SIGNAL OUT
-V

HARRIS

HA-2541

PRELIMINARY

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

Features

- **Unity Gain Bandwidth..40MHz**
- **High Slew Rate 280V/μs**
- **Fast Settling Time..90ns**
- **Power Bandwidth..4MHz**
- **Output Voltage Swing.. ±10V**
- **Unity Gain Stability**
- **Monolithic Bipolar Construction**

Applications

- **Pulse and Video Amplifiers**
- **Wideband Amplifiers**
- **High Speed Sample-Hold Circuits**
- **Fast, Precise D/A Converters**
- **High Speed A/D Input Buffer**

Description

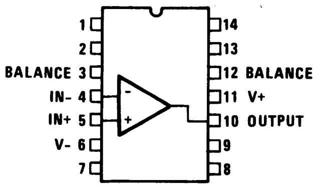
The HA-2541 is the first unity gain stable monolithic operational amplifier to achieve 40MHz unity gain bandwidth. A major addition to the Harris series of high speed, wideband op amps, the HA-2541 is designed for video and pulse applications requiring stable amplifier response at low closed loop gains.

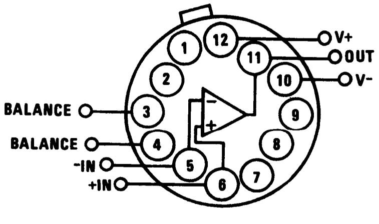
The uniqueness of the HA-2541 is that its slew rate and bandwidth characteristics are specified at unity gain. Historically, high slew rate, wide bandwidth and unity gain stability have been incompatible features for a monolithic operational amplifier. But features such as 280V/μs slew rate and 40MHz unity gain bandwidth clearly show that this is not the case for the HA-2541. These features, along with 90ns settling time, make this product an excellent choice for high speed data acquisition systems.

Packaged in a TO-8 metal can or 14 pin ceramic DIP, the HA-2541 is pin compatible with the HA-2540 and HA-5190 op amps. The HA-2541-2 is specified over the temperature range of -55°C to +125°C.

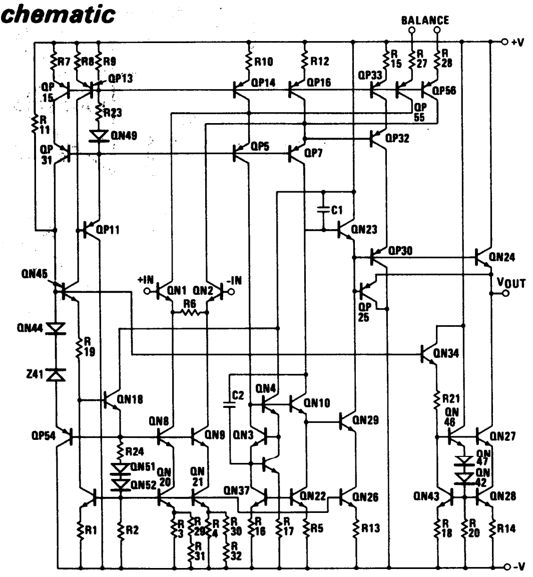
Pinouts

TOP VIEWS


1
2
BALANCE 3
IN- 4
IN+ 5
V- 6
7
14
13
12 BALANCE
11 V+
10 OUTPUT
9
8
-
+


1
2
3
4
5
6
7
8
9
10
11
12
V+
OUT
V-
BALANCE
BALANCE
-IN
+IN
-
+

Schematic


BALANCE
+V
R7
R8
R9
QP13
QP 15
R23
QN49
R 11
QP 31
R10
R12
QP14
QP16
QP33
R 15
R 27
R 28
QP56
QP 55
QP5
QP7
QP32
C1
QP11
QN23
QP30
QN24
QN45
+IN
QN1
QN2
-IN
R6
QP 25
VOUT
QN44
R 19
Z41
QN34
QN18
C2
QN4
QN10
R21
QN 46
QP54
QN8
QN9
QN3
QN29
QN27
R24
QN51
QN52
QN 20
QN 21
QN 47
QN 42
QN37
QN22
QN26
QN43
QN28
R1
R2
R 3
R 29
R 4
R 30
R 16
R 17
R5
R13
R 18
R 20
R14
R 31
R 32
-V

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V-	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2) TO-8	1.5W
Dip	1.6W

Operating Temperature Range:

HA-2541-2	-55°C ≤ T_A ≤ +125°C
HA-2541-5	0°C ≤ T_A ≤ +75°C
Storage Temperature Range	-65°C ≤ T_A ≤ +150°C
Maximum Junction Temperature	+175°C

Electrical Characteristics V_{SUPPLY} = ±15 Volts; R_L = 2K Ohms, Unless Otherwise Specified

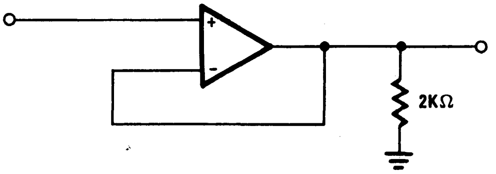
		HA-2541-2 -55°C to +125°C			HA-2541-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage (Note 11)*	+25°C			2			2*	mV
	Full			6			6*	mV
Average Offset Voltage Drift	Full		20			20		μV/°C
Bias Current	+25°C		6	35		6	35	μA
	Full			50			50	μA
Offset Current	+25°C		1	7		1	7	μA
	Full			9			9	μA
Input Resistance	+25°C		100			100		Kohms
Input Capacitance	+25°C		1			1		pF
Common Mode Range	Full	±10			±10			V
Input Noise Voltage (f = 1kHz, R_g = 0Ω)	+25°C		10			10		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10K			10K			V/V
	Full	5K			5K			V/V
Common-Mode Rejection Ratio (Note 5)	Full	70			70			dB
Unity Gain-Bandwidth (Note 6)	+25°C		40			40		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 4)	Full	±10	±11		±10	±11		V
Output Current (Note 4)	+25°C	10			10			mA
Output Resistance	+25°C		2			2		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	3	4		3	4		MHz
Differential Gain	+25°C		0.1			0.1		%
Differential Phase	+25°C		0.2			0.2		Degree
Harmonic Distortion (Note 10)	+25°C		<0.01			<0.01		%
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		4			4		ns
Overshoot	+25°C		40			40		%
Slew Rate	+25°C	200	280		200	280		V/μs
Settling Time:								
10V Step to 0.1%	+25°C		90			90		ns
POWER REQUIREMENTS								
Supply Current	+25°C		33			33		mA
	Full			40			45	mA
Power Supply Rejection Ratio (Note 9)	Full	70			70			dB

Notes:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. T0-8: θ_{jA} = 100°C/W, θ_{jC} = 15°C/W.
   Recommended heat sink: Thermalloy 2240A θ_{SA} = 27°C/W
   Cerdip: θ_{jA} = 91°C/W, θ_{jC} = 35°C/W
   Recommended heat sink: AAVID #5802 θ_{SA} = 15°C/W
3. V0 = ±10V
4. R_L = 1KΩ
5. V_{CM} = ±10V
6. V_0 = 90mV
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of data sheet.
9. V_{SUPPLY} = ±5VDC to ±15VDC
10. V_{IN} = 1VRMS; f = 10KHz; Av = 10
11. Relaxed Offset Voltage "C" version available in 1986.

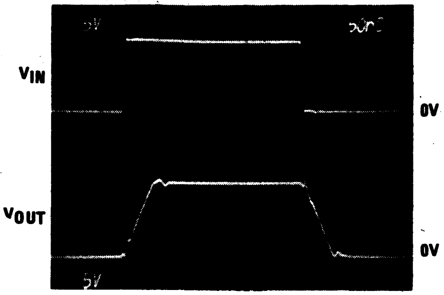
Test Circuits

TEST CIRCUIT *

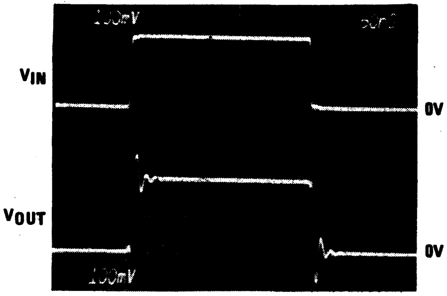


* $C_L \leq 10pF$

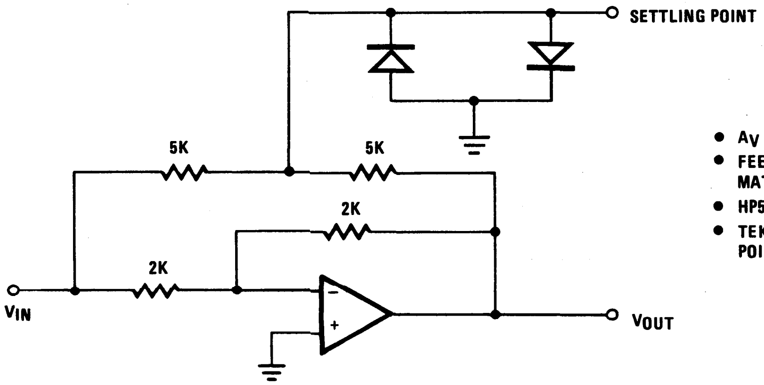
LARGE SIGNAL RESPONSE



SMALL SIGNAL RESPONSE

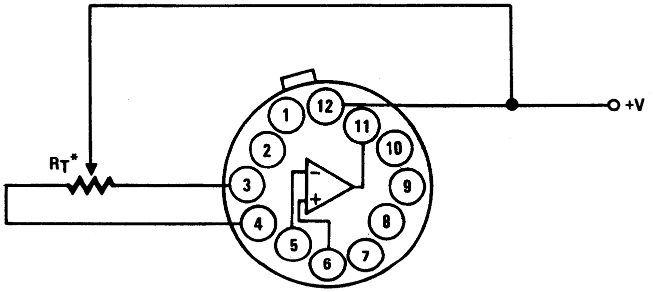


SETTLING TIME TEST CIRCUIT



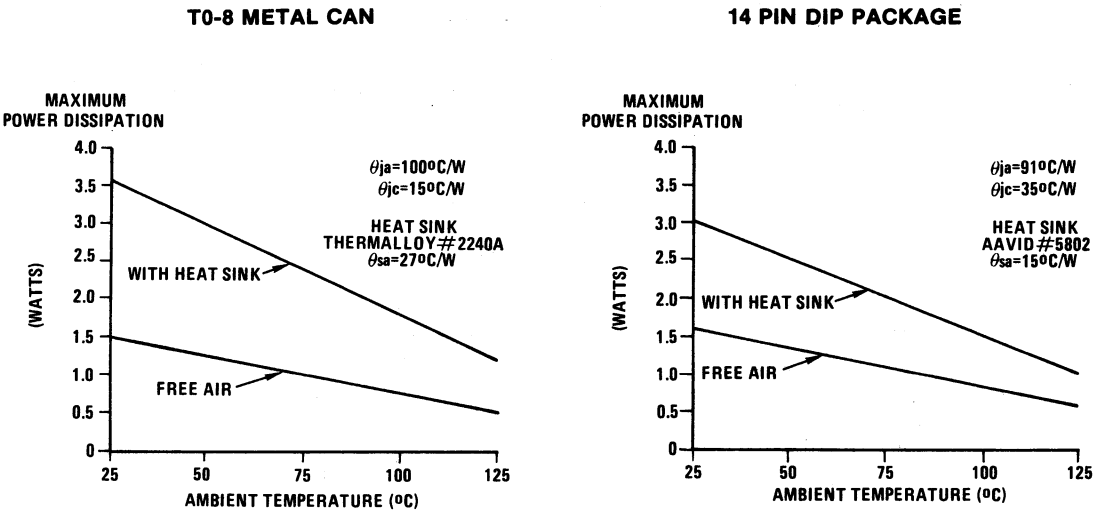
- A_V = -1
- FEEDBACK AND SUMMING RESISTORS MUST BE MATCHED (0.1%)
- HP5082-2810 CLIPPING DIODES RECOMMENDED
- TEKTRONIX P6201 FET PROBE USED AT SETTLING POINT

Suggested Offset Voltage Adjustment



*OFFSET ADJUSTMENT RANGE IS APPROXIMATELY ± 8mV FOR R_T = 5KΩ.

Maximum Power Dissipation Curves



MAXIMUM POWER DISSIPATION vs. TEMPERATURE
($T_j \leq 175°C$)*

*FOR THE GIVEN DIE SIZE AND THERMAL IMPEDANCE DATA, THESE CURVES REPRESENT THE MAXIMUM ALLOWABLE POWER DISSIPATION BEFORE A JUNCTION TEMPERATURE OF 175°C IS EXCEEDED.

HARRIS

PRELIMINARY

HA-2542

Wideband, High Slew Rate, High Output Current Operational Amplifiers

Features

- Stable at Gains of 2 or Greater
- Gain Bandwidth (A_{VCL} = 2) 120MHz
- High Slew Rate 300V/μs
- High Output Current 100mA
- Power Bandwidth 5.5MHz
- Output Voltage Swing .... ±10V
- Monolithic Bipolar Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

Description

The HA-2542 is a wideband, high slew rate, monolithic operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability.

Utilizing the advantages of the Harris D. I. technology this amplifier offers 350V/μs slew rate, 120MHz gain bandwidth, and ±100mA output current. Application of this device is further enhanced through stable operation down to closed loop gains of 2.

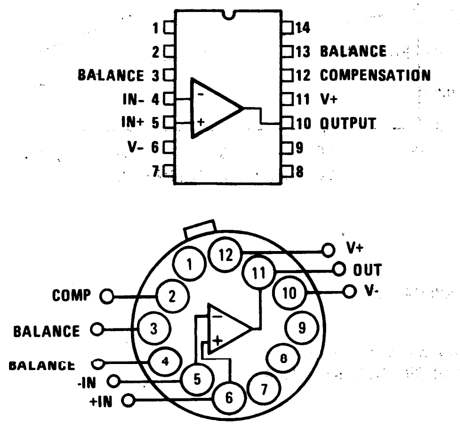
For additional flexibility, offset null and frequency compensation controls are included in the HA-2542 pinout.

The capabilities of the HA-2542 are ideally suited for high speed coaxial cable driver circuits with gain. With 5.5MHz full power bandwidth, this amplifier is most suitable for high frequency signal conditioning circuits and pulse/video amplifiers. Other applications utilizing the HA-2542 advantages include wideband amplifiers and fast sample-hold circuits.

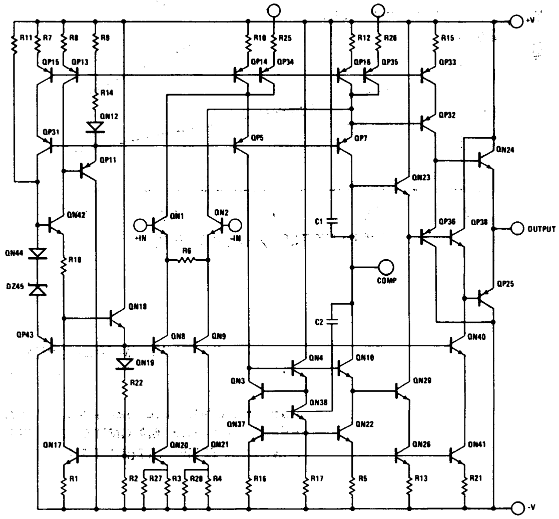
Packaged in a 12 pin (T0-8) can, the HA-2542 is pin compatible with the HA-2540, HA-2541, HA-5190, LH0032, and H0S-050C.

Pinout

TOP VIEWS


1
2
BALANCE 3
IN- 4
IN+ 5
V- 6
7
14
13 BALANCE
12 COMPENSATION
11 V+
10 OUTPUT
9
8
V+
OUT
V-
COMP
BALANCE
BALANCE
-IN
+IN
1
2
3
4
5
6
7
8
9
10
11
12

Schematic


+V
R11
R7
R8
R9
R10
R25
R12
R26
R15
QP15
QP13
QP14
QP34
QP16
QP35
QP33
R14
QN12
QP31
QP5
QP7
QP32
QP11
QN24
QN23
QN42
QN1
QN2
+IN
-IN
C1
QP36
QP38
OUTPUT
QN44
R18
R6
COMP
DZ45
QP25
QN18
C2
QP43
QN8
QN9
QN40
QN19
QN4
QN10
R22
QN3
QN29
QN39
QN37
QN22
QN17
QN20
QN21
QN26
QN41
R1
R2
R27
R3
R28
R4
R16
R17
R5
R13
R21
-V

C

Absolute Maximum Ratings (Note 1)

Voltage between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current .... 125mA (Peak)
$107mA_{RMS}$ (Continuous)
Internal Power Dissipation (Note 2) TO-8 .... 1.5W
Dip 1.6W

Operating Temperature Range:

HA-2542-2 .... $-55^oC \le T_A \le +125^oC$
HA-2542-5 .... $0^oC \le T_A \le +75^oC$
Storage Temperature Range..... $-65^oC \le T_A \le +150^oC$
Maximum Junction Temperature .... $+175^oC$

Electrical Characteristics

$V_{SUPPLY} = \pm15$ Volts; R_L = 1K ohms, unless otherwise specified.

PARAMETER	TEMP	HA-2542-2 -55°C to +125°C MIN	TYP	MAX	HA-2542-5 0°C to +75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C			10			10	mV
	Full			20			20	mV
Average Offset Voltage Drift	Full		20			20		μV/°C
Bias Current	+25°C			35			35	μA
	Full			50			50	μA
Offset Current	+25°C		1	7		1	7	μA
	Full			9			9	μA
Input Resistance	+25°C		100			100		Kohms
Input Capacitance	+25°C		1			1		pF
Common Mode Range	Full	±10			±10			V
Input Noise Voltage (f = 1kHz, $R_g = 0\Omega$)	+25°C		10			10		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10K			10K			V/V
	Full	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	Full	70			70			dB
Gain-Bandwidth-Product (Note 5)	+25°C		120			120		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	Full	±10	±11		±10	±11		V
Output Current (Note 6)	+25°C	100			100			mA
Output Resistance	+25°C		5			5		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	4.7			4.7			MHz
Differential Gain	+25°C		.1			.1		%
Differential Phase	+25°C		.2			.2		degree
Harmonic Distortion (Note 10)	+25°C		<0.04			<0.04		%
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		4			4		ns
Overshoot	+25°C		40			40		%
Slew Rate	+25°C	300	375		300	375		V/μs
Settling Time:								
10V Step to 0.1%	+25°C		100			100		ns
POWER REQUIREMENTS								
Supply Current	+25°C		31			31		mA
	Full			35			40	mA
Power Supply Rejection Ratio (Note 9)	Full	70			70			dB

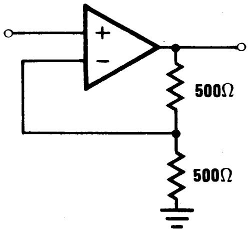
Notes:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. T0-8: θ_{jA} = 100°C/W, θ_{jC} = 15°C/W. Recommended heat sink: Thermalloy 2240A θ_{SA} = 27°C/W Dip: θ_{jA} = 91°C/W, θ_{jC} = 35°C/W. Recommended heat sink: AAVID #5802 θ_{SA} = 15°C/W
3. R_L = 1KΩ, V_0 = ±10V
4. V_{CM} = ±10V
5. A_{VCL} = 2
6. R_L = 50Ω, V_0 = ±5V
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of data sheet.
9. V_{SUPPLY} = ±5VDC to ±15VDC
10. V_{IN} = $1V_{RMS}$; f = 10KHz; A_V = 10

Test Circuits

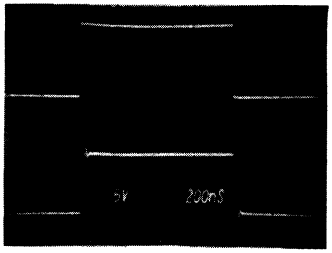
LARGE AND SMALL SIGNAL RESPONSE

TEST CIRCUIT

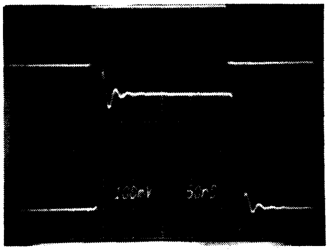


*$C_L \leq$ 10pF

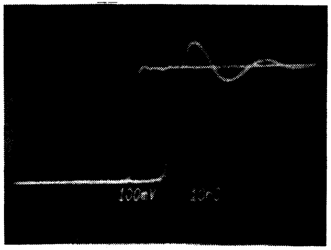
LARGE SIGNAL RESPONSE



SMALL SIGNAL RESPONSE

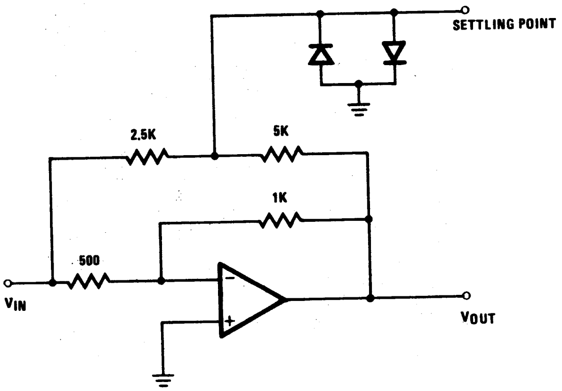


TIME DELAY



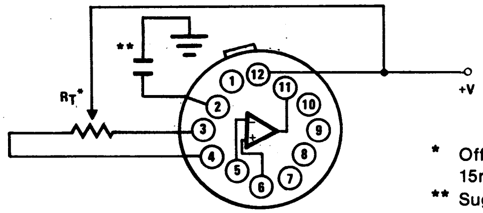
Test Circuits (continued)

SETTLING TIME TEST CIRCUIT


SETTLING POINT
2.5K
5K
1K
500
VIN
VOUT
-
+

- A_V =-2
- Feedback and summing resistors must be matched (.1%)
- HP5082-2810 clipping diodes recommended
- Tektronix P6201 FET probe used at settling point

SUGGESTED OFFSET VOLTAGE ADJUSTMENT

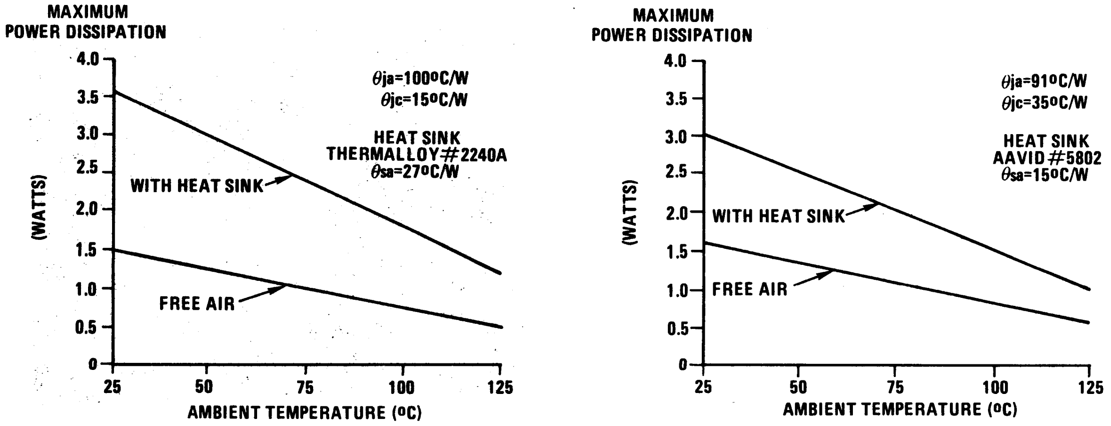

**
R_T*
+V
1
2
3
4
5
6
7
8
9
10
11
12
-
+

* Offset adjustment range is approximately 15mV FOR R_T 5K

** Suggested compensation scheme 10-20pf.

MAXIMUM POWER DISSIPATION CURVES

MAXIMUM POWER DISSIPATION VS. TEMPERATURE

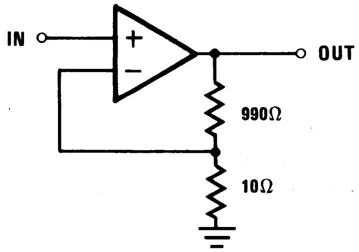


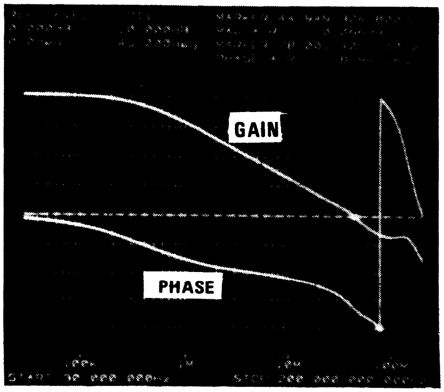
TO-8 METAL CAN

14 PIN DIP PACKAGE

Typical Applications

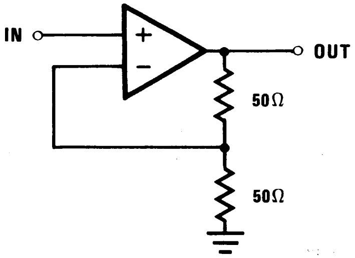
NONINVERTING CIRCUIT (A_{VCL} = 100)

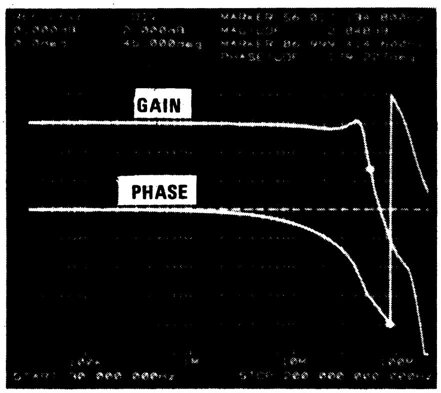

IN
+
−
OUT
990Ω
10Ω



A_{VCL} = 100 - PHASE AND GAIN

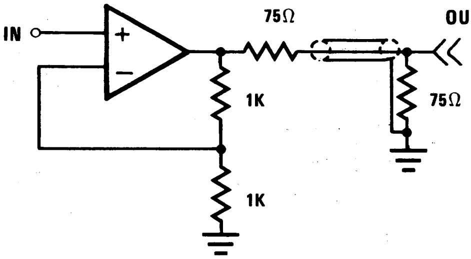
NONINVERTING CIRCUIT (A_{VCL} = 2)

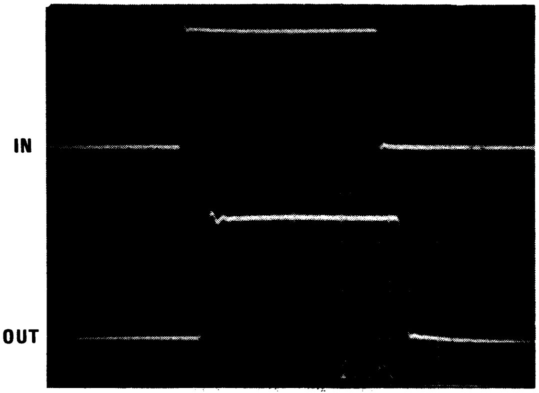

IN
+
−
OUT
50Ω
50Ω



A_{VCL} = 2 - PHASE AND GAIN

VIDEO CABLE DRIVER


IN
+
−
75Ω
OUT
1K
75Ω
1K



VIDEO CABLE DRIVER PULSE RESPONSE
(1V/DIV.; 100ns/DIV.)

HARRIS

ADVANCED

HA-2544

Video Operational Amplifier

Features

- Unity Gain Bandwidth 33MHz
- High Slew Rate 150V/µs
- Low Supply Current 10mA
- Differential Gain Error .... <0.1dB
- Differential Phase Error .... <0.1°
- Gain Tolerance at 5MHz 0.2dB

Applications

- Video Systems
- Video Test Equipment
- Radar Displays
- Imaging Systems
- Pulse Amplifiers
- Signal Conditioning Circuits
- Data Acquisition Systems

Description

The HA-2544 is a dielectrically isolated, monolithic operational amplifier designed and constructed in the Harris High Frequency Process. It is another addition to the Harris series of high speed, wideband op-amps and offers true video performance combined with the versatility of an op-amp.

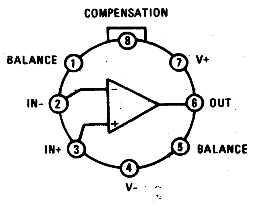
The HA-2544 features 33MHz unity gain bandwidth and 150V/µs slew rate while offering video performance of <0.1dB differential gain error, <0.1° differential phase error, and gain tolerance of just 0.2dB at 5MHz. High performance and low power requirements are met with a supply current of only 10mA.

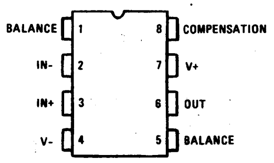
Uses of the HA-2544 range from video and video test equipment to radar displays and other precise imaging systems where stringent gain and phase requirements have previously been met with costly hybrids and discrete circuitry. The HA-2544 can also be used as a standard wideband, high speed, and fast settling op-amp in circuits such as pulse amplifiers and high speed data acquisition systems.

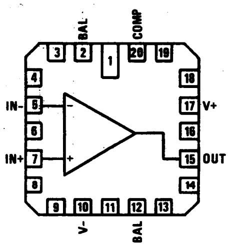
The HA-2544 is guaranteed over the military temperature range (-55°C to +125°C) in either the -2 or -8 versions, and over the commercial temperature range (0°C to +75°C) as a -5 version. The HA-2544 is available in TO-99 metal can, 20 pin LCC, and both epoxy and ceramic Mini-DIP packages.

Pinouts

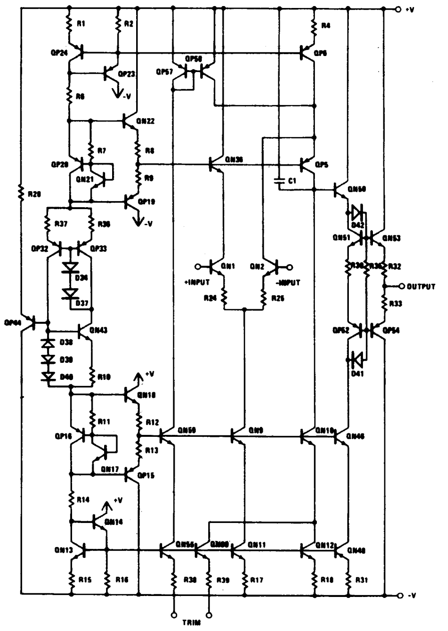
TOP VIEWS


COMPENSATION
BALANCE 1
8
7 V+
IN- 2
6 OUT
IN+ 3
5 BALANCE
4
V-


BALANCE 1
IN- 2
IN+ 3
V- 4
8 COMPENSATION
7 V+
6 OUT
5 BALANCE


BAL
COMP
3 2 1 20 19
4
IN- 5
6
IN+ 7
8
18
17 V+
16
15 OUT
14
9 10 11 12 13
V-
BAL

Schematic


+V
-V
+INPUT
-INPUT
OUTPUT
C1
TRIM

HA-2600/02/05

Wideband, High Impedance Operational Amplifiers

FEATURES

• WIDE BANDWIDTH	12MHz
• HIGH INPUT IMPEDANCE	500MΩ
• LOW INPUT BIAS CURRENT	1nA
• LOW INPUT OFFSET CURRENT	1nA
• LOW INPUT OFFSET VOLTAGE	0.5mV
• HIGH GAIN	150K V/V
• HIGH SLEW RATE	7V/μs
• OUTPUT SHORT CIRCUIT PROTECTION	

APPLICATIONS

- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

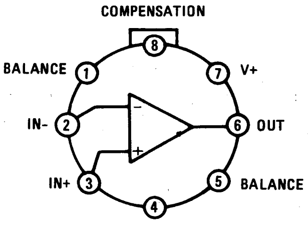
DESCRIPTION

HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500 MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth product, 7V/μs slew rate and 150,000V/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characterisitics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

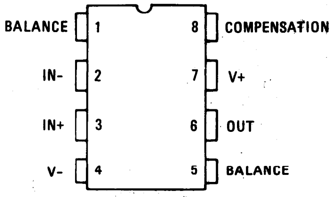
The HA-2600 and HA-2602 have guaranteed operation from -55°C to +125°C and are available in metal can and ceramic mini DIP packages. Both are offered as a military grade part. The HA-2605 has guaranteed operation from 0°C to +75°C and is available in plastic and ceramic mini DIP and metal can packages.

PINOUTS

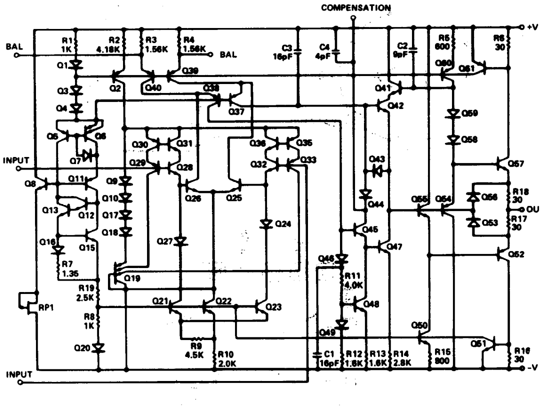

COMPENSATION
8
BALANCE
1
7
V+
IN-
2
6
OUT
IN+
3
5
BALANCE
4
V-

Case Connected to V-

TOP VIEWS


BALANCE
1
8
COMPENSATION
IN-
2
7
V+
IN+
3
6
OUT
V-
4
5
BALANCE

SCHEMATIC


COMPENSATION
+V
BAL
R1 1K
R2 4.18K
R3 1.56K
R4 1.56K
BAL
C3 16pF
C4 4pF
C2 9pF
R5 600
R6 30
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q35
Q36
Q37
Q38
Q39
Q40
Q41
Q42
Q43
Q44
Q45
Q46
Q47
Q48
Q49
Q50
Q51
Q52
Q53
Q54
Q55
Q56
Q57
Q58
Q59
Q60
Q61
INPUT
R7 1.35
R19 2.5K
RP1
R8 1K
R9 4.5K
R10 2.0K
R11 4.0K
C1 16pF
R12 1.6K
R13 1.6K
R14 2.8K
R15 800
R18 30
OUT
R17 30
R16 30
-V
INPUT

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V	Operating Temperature Ranges:	
Differential Input Voltage	± 12.0V	HA-2600/HA-2602	$-55^\circ C \leq T_A \leq +125^\circ C$
Peak Output Current	Full Short Circuit Protection	HA-2605	$0^\circ C \leq T_A \leq +75^\circ C$
Internal Power Dissipation	300mW	Storage Temperature Range:	$-65^\circ C \leq T_A \leq +150^\circ C$

ELECTRICAL CHARACTERISTICS

$V+ = +15V$ D. C., $V- = -15V$ D. C.

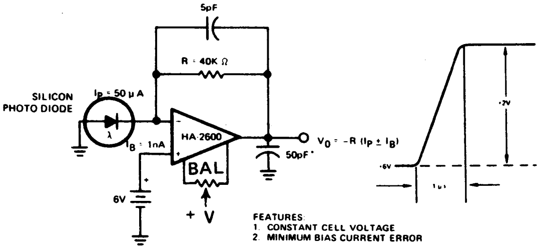
PARAMETER	TEMP	HA-2600 -55°C to +125°C MIN	TYP	MAX	HA-2602 -55°C to +125°C MIN	TYP	MAX	HA-2605 0°C to +75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	4		3	5		3	5	mV
	Full		2	6			7			7	mV
Offset Voltage Average Drift	Full		5								µV/°C
Bias Current	+25°C		1	10		15	25		5	25	nA
	Full		10	30			60			40	nA
Offset Current	+25°C		1	10		5	25		5	25	nA
	Full		5	30			60			40	nA
Input Resistance (Note 10)	+25°C	100	500		40	300		40	300		MΩ
Common Mode Range	Full	± 11.0			± 11.0			± 11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		74	100		dB
Unity Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	± 10.0	± 12.0		± 10.0	± 12.0		± 10.0	± 12.0		V
Output Current (Note 4)	+25°C	± 15	± 22		± 10	± 18		± 10	± 18		mA
Full Power Bandwidth (Notes 4, 11)	+25°C	50	75		50	75		50	75		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 7)	+25°C		30	60		30	60		30	60	ns
Overshoot (Notes 1, 5, 6 & 7)	+25°C		25	40		25	40		25	40	%
Slew Rate (Notes 1, 5, 7 & 12)	+25°C	± 4	± 7		± 4	± 7		± 4	± 7		V/µs
Settling Time (Notes 1, 5, 7 & 12)	+25°C		1.5			1.5			1.5		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:

1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10V$
3. $V_O < 90mV$
4. $V_O = \pm 10V$
5. $C_L = 100pF$
6. $V_O = \pm 200mV$
7. $V_O = \pm 200mV$
8. See Transient Response Test Circuits & Waveforms Page 2-57.
9. $\Delta VS = \pm 5V$
10. This parameter value guaranteed by design calculations.
11. Full power bandwidth guaranteed by slew rate measurement: $FPBW = S.R./2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$

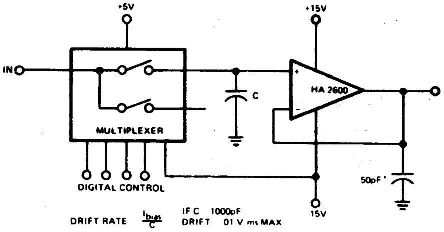
TYPICAL APPLICATIONS

PHOTO-CURRENT TO VOLTAGE CONVERTER


5pF
R = 40K Ω
SILICON PHOTO DIODE
I_P = 50 μA
λ
I_B = 1nA
HA-2600
BAL
6V
+ V
50pF*
$V_0 = -R(I_P \pm I_B)$
+6V
+7V
1 μs

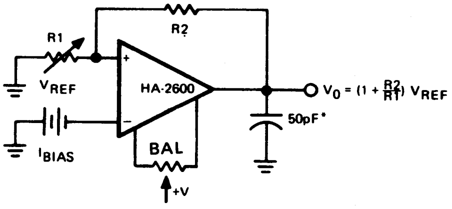
FEATURES:
1. CONSTANT CELL VOLTAGE
2. MINIMUM BIAS CURRENT ERROR

SAMPLE – AND – HOLD


+5V
+15V
IN
C
HA 2600
OUT
MULTIPLEXER
DIGITAL CONTROL
50pF*
15V

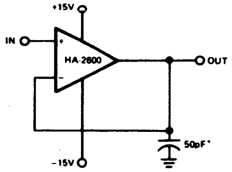
DRIFT RATE $\frac{I_{bias}}{C}$ IF C 1000pF DRIFT 01 V ms MAX

REFERENCE VOLTAGE AMPLIFIER


R1
R2
V_{REF}
I_{BIAS}
HA-2600
BAL
+V
50pF*
$V_0 = (1 + \frac{R2}{R1}) V_{REF}$

FEATURES:
1. MINIMUM BIAS CURRENT IN REFERENCE CELL
2. SHORT CIRCUIT PROTECTION

VOLTAGE FOLLOWER


+15V
IN
HA-2600
OUT
50pF*
−15V

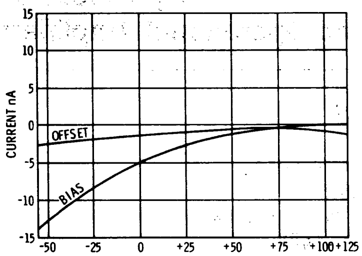
1.000 GAIN 0.9999
$Z_{in} = -10^{12}$ MIN.
$Z_{out} = .01$ MAX.

SLEW RATE = 4V/μs MIN.
B. W. = 12MHz TYP.
OUTPUT SWING = ± 10V MIN. TO 50kHz

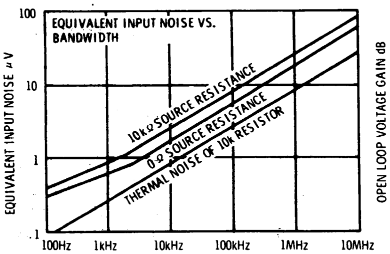
*A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

PERFORMANCE CURVES

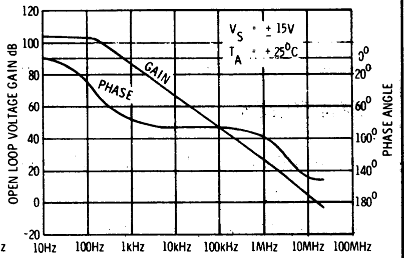
V+ = 15V D. C., T_A = 25°C unless otherwise stated.



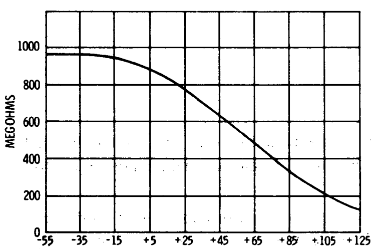
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



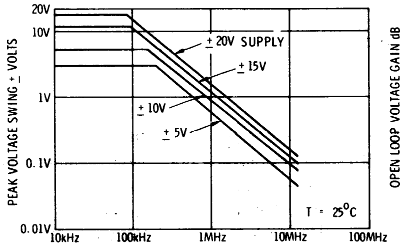
UPPER 3dB FREQUENCY
LOWER 3dB FREQUENCY - 10Hz
BROADBAND NOISE CHARACTERISTICS



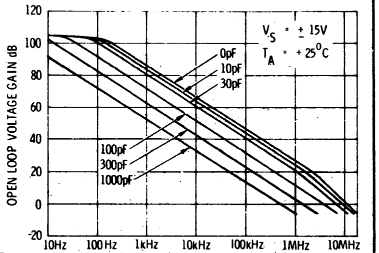
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

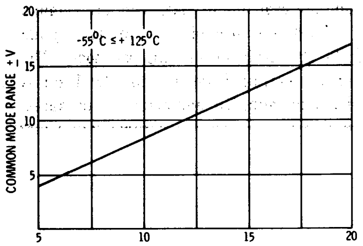


OUTPUT VOLTAGE SWING VS. FREQUENCY

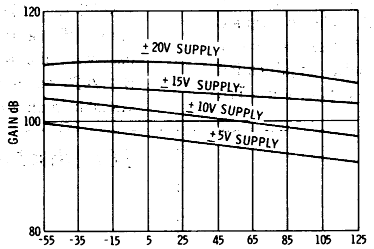


FREQUENCY Hz
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

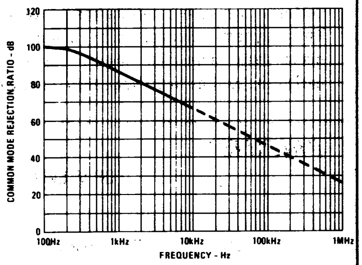
Note: External Compensation Components are not Required for Stability, But May be Added to Reduce Bandwidth if Desired. If External Compensation is Used, Also Connect 100pF Capacitor From Output to Ground.



SUPPLY VOLTAGE - VOLTS
COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

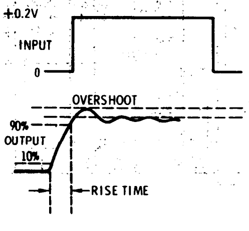


TEMPERATURE °C
OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE



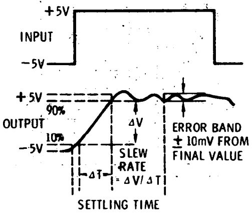
COMMON MODE REJECTION RATIO VS. FREQUENCY

TRANSIENT RESPONSE

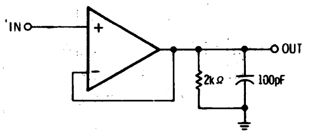

+0.2V
INPUT
0
OVERSHOOT
90%
OUTPUT
10%
RISE TIME

NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

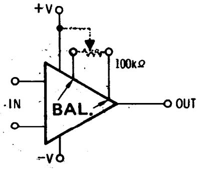
SLEW RATE AND SETTLING TIME


+5V
INPUT
-5V
+5V
90%
OUTPUT
10%
-5V
ΔV
ΔT
SLEW RATE = ΔV/ΔT
ERROR BAND ± 10mV FROM FINAL VALUE
SETTLING TIME

SLEW RATE AND TRANSIENT RESPONSE


IN
+
-
OUT
2kΩ
100pF

SUGGESTED VOS ADJUSTMENT


+V
100kΩ
IN
BAL.
OUT
-V

HARRIS

HA-2620/22/25

Very Wideband, Uncompensated Operational Amplifiers

FEATURES

• GAIN BANDWIDTH PRODUCT($A_V = 5$)	100MHz
• HIGH INPUT IMPEDANCE	500MΩ
• LOW INPUT BIAS CURRENT	1nA
• LOW INPUT OFFSET CURRENT	1nA
• LOW INPUT OFFSET VOLTAGE	0.5mV
• HIGH GAIN	150K V/V
• HIGH SLEW RATE	35V/μs
• OUTPUT SHORT CIRCUIT PROTECTION	

APPLICATIONS

- VIDEO AND R.F. AMPLIFIERS
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

DESCRIPTION

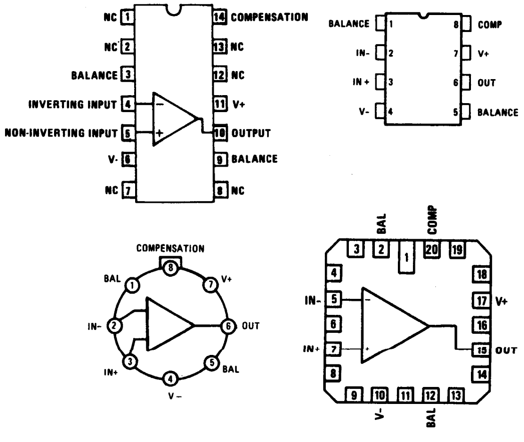
HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 100MHz gain-bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/ μs slew rate and 150,000V/V open-loop gain enables HA-2620/2622/2625 to perform high-gain amplification of very fast, wideband signals. These dynamic characterisitcs, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

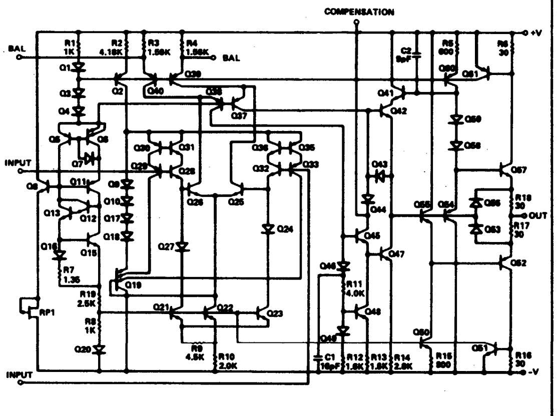
The HA-2620 and HA-2622 have guaranteed operation from - 55°C to + 125°C and are available in metal can and ceramic mini DIP packages. Both are offered as a military grade part with the HA-2620 also available in LCC packages. The HA-2625 has guaranteed operation from 0°C to +75°C and is available in plastic and ceramic mini DIP and metal can packages.

PINOUTS

TOP VIEWS


NC 1
NC 2
BALANCE 3
INVERTING INPUT 4
NON-INVERTING INPUT 5
V- 6
NC 7
14 COMPENSATION
13 NC
12 NC
11 V+
10 OUTPUT
9 BALANCE
8 NC
BALANCE 1
IN- 2
IN+ 3
V- 4
8 COMP
7 V+
6 OUT
5 BALANCE
COMPENSATION
8
BAL 1
V+ 7
IN- 2
6 OUT
IN+ 3
4
V-
5 BAL
BAL
COMP
3 2 1 20 19
4
IN- 5
6
IN+ 7
8
18
17 V+
16
15 OUT
14
9 10 11 12 13
V-
BAL

SCHEMATIC


COMPENSATION
+V
BAL
BAL
INPUT
INPUT
OUT
-V
R1 1K
R2 4.18K
R3 1.56K
R4 1.56K
C2 9pF
R5 600
R6 30
R7 1.35
R19 2.5K
R8 1K
R9 4.5K
R10 2.0K
R11 4.0K
C1 16pF
R12 1.6K
R13 1.6K
R14 2.8K
R15 800
R16 30
R17 30
R18 30
RP1

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

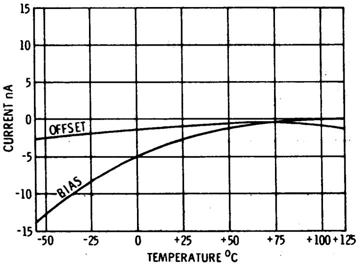
ELECTRICAL CHARACTERISTICS $V^+ = +15$ VDC, $V^- = -15$ VDC

PARAMETER	TEMPERATURE	HA-2620 −55°C to +125°C			HA-2622 −55°C to +125°C			HA-2625 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
Offset Voltage (Note 1)	+25°C		0.5	4		3	5		3	5	mV
	Full			6			7			7	mV
Bias Current	+25°C		1	15		5	25		5	25	nA
	Full		10	35			60			40	nA
Offset Current	+25°C		1	15		5	25		5	25	nA
	Full		5	35			60			40	nA
Input Resistance (Note 11)	+25°C	65	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 2 & 3)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80	100		74	100		74	100		dB
Gain Bandwidth Product (Notes 2, 5, &6)	+25°C		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 3)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Notes 2, 3, 7 &12)	+25°C	400	600		320	600		320	600		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 2, 7 & 8)	+25°C		17	45		17	45		17	45	ns
Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35		± 20	±35		± 20	±35		V/µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

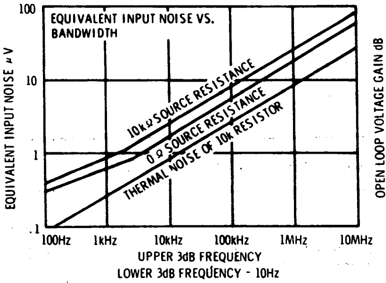
NOTES:
1. Offset may be externally adjusted to zero.
2. $R_L = 2K\Omega$, $C_L = 50pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 10V$
5. $V_O < 90mV$
6. 40dB Gain
7. See transient response test circuits and waveforms
8. $A_V = 5$ (The HA-2620 family is not stable at unity gain without external compensation.)
9. $\Delta V_{Sup} = \pm 5V$
10. $V_{OUT} = \pm 5V$
11. This parameter value based upon design calculations.
12. Full power bandwidth guaranteed based upon slew rate measurement $FPBW = S.R./2\pi V_{peak}$.

TYPICAL PERFORMANCE CURVES

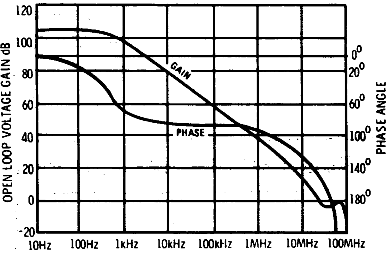
V+ = +15V D. C., V- = -15V D. C., T_A = 25°C unless otherwise stated.



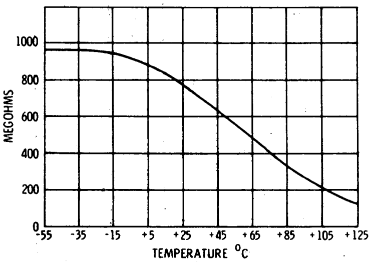
INPUT BIAS CURRENT AND OFFSET CURRENT-
AS A FUNCTION OF TEMPERATURE



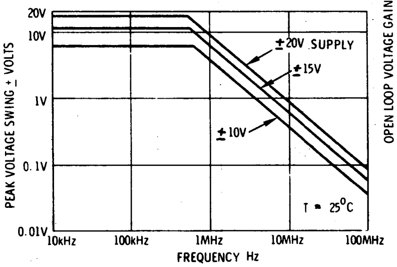
BROADBAND NOISE CHARACTERISTICS



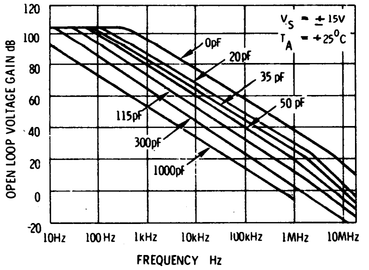
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

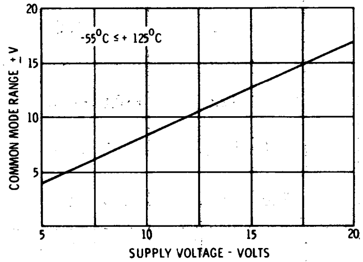


OUTPUT VOLTAGE SWING VS. FREQUENCY

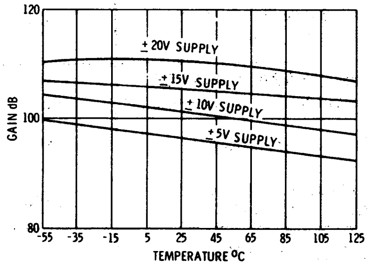


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

Note: External Compensation is Required For Closed Loop Gain < 5. If External Compensation is Used, Also Connect 100 pF Capacitor From Output to Ground.

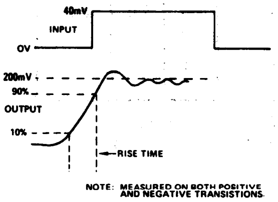


COMMON MODE VOLTAGE RANGE
AS A FUNCTION OF SUPPLY VOLTAGE

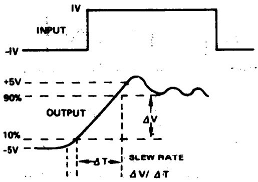


OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE

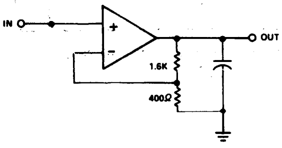
TRANSIENT RESPONSE


40mV
INPUT
0V
200mV
90%
OUTPUT
10%
RISE TIME
NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSISTIONS.

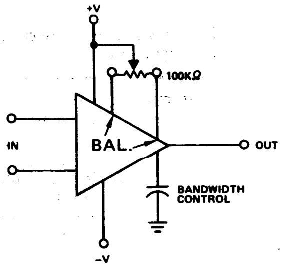
SLEW RATE


1V
INPUT
-1V
+5V
90%
OUTPUT
ΔV
10%
-5V
ΔT
SLEW RATE
ΔV/ΔT

SLEW RATE AND TRANSIENT RESPONSE

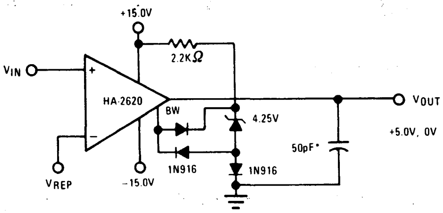

IN
+
-
OUT
1.6K
400Ω

SUGGESTED VOS ADJUSTMENT AND COMPENSATION HOOK-UP

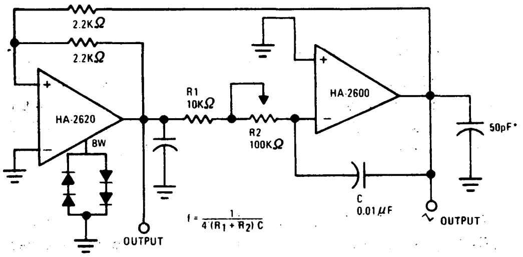

+V
100KΩ
IN
BAL.
OUT
BANDWIDTH CONTROL
-V

TYPICAL APPLICATIONS

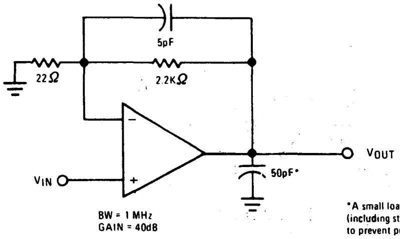
HIGH IMPEDANCE COMPARATOR



FUNCTION GENERATOR



VIDEO AMPLIFIER



*A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

DEFINITIONS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE—The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO—The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING—The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE—The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE—The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN—The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH—The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO—The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE—The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT—The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rate Limiting)—The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing)...restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

HARRIS

HA-2630/35

Not Recommended
For New Designs
See HA-5002

High Performance Current Booster

FEATURES

• OUTPUT CURRENT	±400mA
• SLEW RATE	500V/μs
• BANDWIDTH	8MHz
• FULL POWER BANDWIDTH	8MHz
• INPUT RESISTANCE	2.0 x $10^6 \Omega$
• OUTPUT RESISTANCE	2.0 Ω
• POWER SUPPLY RANGE	±5V to ±20V
• PACKAGE IS ELECTRICALLY ISOLATED	

APPLICATIONS

- COAXIAL CABLE DRIVERS
- AUDIO OUTPUT AMPLIFIERS
- SERVO MOTOR DRIVERS
- POWER SUPPLIES (BIPOLAR)
- PRECISION DATA RECORDING

DESCRIPTION

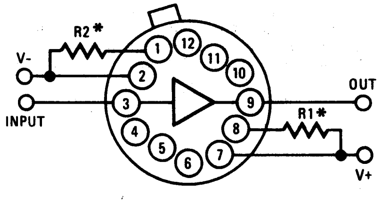
HA-2630 and HA-2635 are monolithic, unity voltage gain current amplifiers delivering extremely high slew rate, wide bandwidth, and full power bandwidth even under heavy output loading conditions. This dielectrically isolated current booster also offers high input impedance and low output resistance. These devices are intended to be used in series with an operational amplifier and inside the feedback loop whenever additional output current is required. Output current levels are programmable by selecting two optional external resistors.

These current amplifiers offer an exceptional 500V/μs slew rate and 8MHz bandwidth which allows them to be used with many high performance op amps in precision data recording and high speed coaxial cable driver designs. 2.0M ohm input resistance and 2 ohm output resistance coupled with ±400mA output current make HA-2630 and HA-2635 ideal components in high fidelity audio output amplifier designs.

HA-2630 and HA-2635 are available in an electrically isolated TO-8 type can for ease of mounting with or without a heat sink. HA-2630 is specified over the -55°C to +125°C range. HA-2635 is specified from 0°C to +75°C.

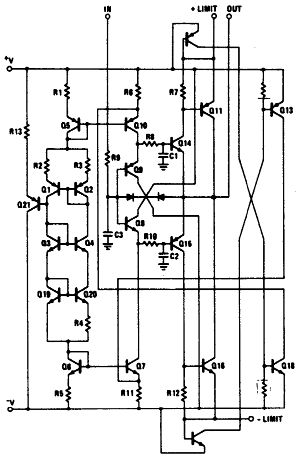
PINOUT

TOP VIEW



* Optional Current Limiting Resistor

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V
Input Voltage Range	± V Supply
Output Current (Note 2)	±700mA
Internal Power Dissipation (Note 6) Free Air:	1W
In Heat Sink:	4W

Operating Temperature Range:
$-55^{\circ}C \leq T_A \leq +125^{\circ}C$ (HA-2630)
$0^{\circ}C \leq T_A \leq +75^{\circ}C$ (HA-2635)
Storage Temperature Range:
$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 15$ Volts $R_L = 50$ Ohms $R_1 = R_2 = 0$ Ohms Unless otherwise specified.

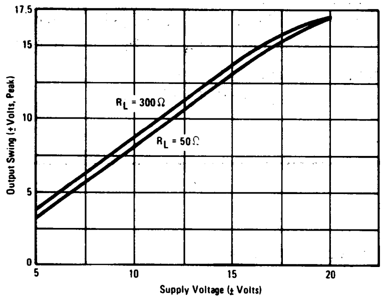
PARAMETER	TEMP.	HA-2630 -55°C to +125°C MIN.	TYP.	MAX.	HA-2635 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Bias Current	+25°C		30	150		30	150	μA
	Full			200			200	μA
Input Resistance	+25°C		2.0			2.0		MΩ
Input Capacitance	+25°C		5.0			5.0		pF
TRANSFER CHARACTERISTICS								
Voltage Gain (Note 1)	Full	.85	.95		.85	.95		V/V
Offset Voltage ($V_{OUT} - V_{IN}$)	+25°C		70	±200		70	±200	mV
	Full			±300			±300	mV
Bandwidth (-3dB)	+25°C		8.0			8.0		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10	±12		±10	±12		V
Output Current (Note 1)	Full	±300	±400		±300	±400		mA
Output Resistance	+25°C		2.0			2.0		Ω
Full Power Bandwidth (Note 1)	+25°C		8.0			8.0		MHz
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C		30			30		ns
Slew Rate (Note 4)	+25°C	200	500		200	500		V/μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		15	20		15	23	mA
Supply Voltage Range	Full	±5		±20	±5		±20	V
Power Supply Rejection Ratio (Note 5)	Full		66			66		dB

NOTES:
1. $V_O = \pm 10V$
2. Heat sink is required for continuous short circuit protection, regardless of current limit setting.
3. $V_O = 0.4V$ p-p.
4. $V_O = 10V$ p-p.
5. $\Delta V_{SUPPLY} = \pm 5V$.
6. Without heat sink, derate by 14mW/°C ambient temperature above 100°C ambient, with heat sink, derate by 67mW/°C case temperature above 115°C case.

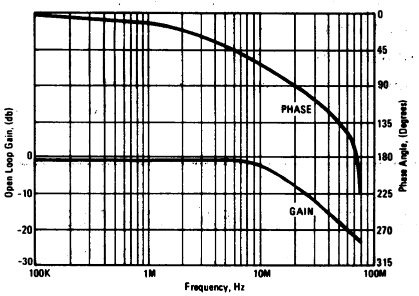
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

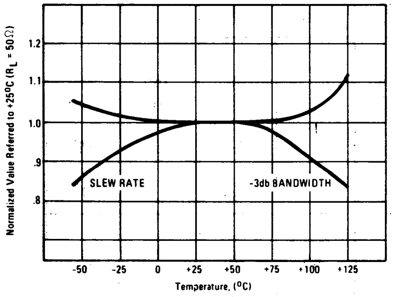
OUTPUT SWING ($R_{LIMIT} = 0\Omega$)



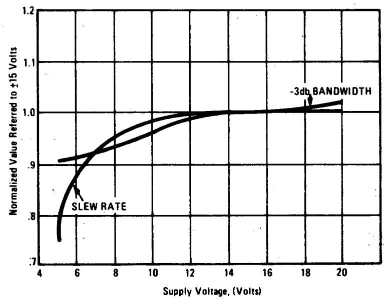
OPEN LOOP FREQUENCY AND PHASE RESPONSE ($R_L = 50\Omega$, $C_L \approx 10pf$)



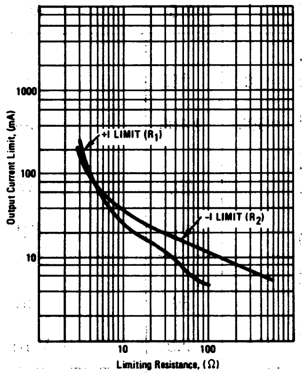
NORMALIZED AC PARAMETERS vs. TEMPERATURE ($R_L = 50\Omega$)



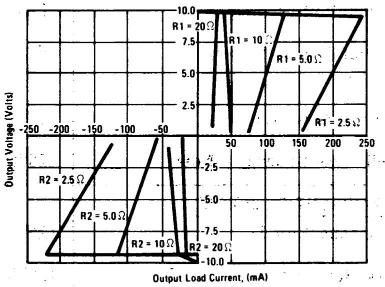
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE ($R_L = 50\Omega$)



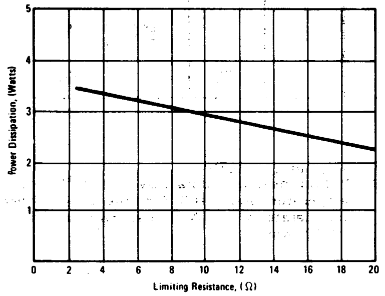
OUTPUT CURRENT LIMITING vs. LIMITING RESISTANCE



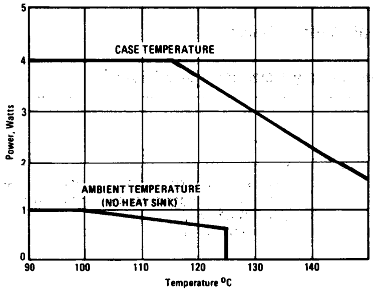
OUTPUT CURRENT CHARACTERISTIC



POWER DISSIPATION vs. LIMITING RESISTANCE WITH OUTPUT SHORTED TO GROUND; V_{IN} = +10V

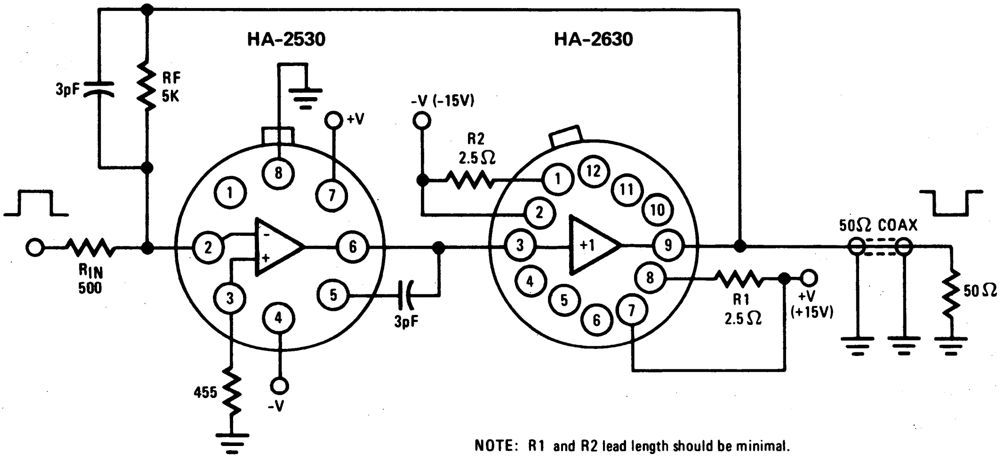


MAXIMUM ALLOWABLE INTERNAL POWER DISSIPATION vs. TEMPERATURE



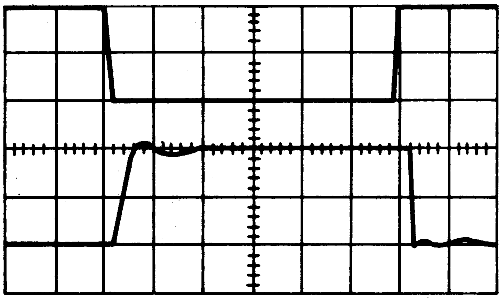
TYPICAL APPLICATION

20dB, 5MHz VIDEO COAXIAL LINE DRIVER


HA-2530
HA-2630
3pF
RF
5K
+V
-V (-15V)
R2
2.5Ω
RIN
500
1
2
3
4
5
6
7
8
9
10
11
12
+1
3pF
455
-V
R1
2.5Ω
+V
(+15V)
50Ω COAX
50Ω

NOTE: R1 and R2 lead length should be minimal.

LINE DRIVER PULSE RESPONSE



Horizontal Scale = 200ns/Div.
Upper Trace: Input, 200mV/Div.
Lower Trace: Output, 2V/Div.

SOME OTHER APPLICATIONS

- BIPOLAR POWER SUPPLY
- FUNCTION GENERATOR OUTPUT
- DEFLECTION COIL DRIVE
- AUDIO OUTPUT AMPLIFIER

HARRIS

HA-2640/45

High Voltage
Operational Amplifier

FEATURES

- OUTPUT VOLTAGE SWING ±35V
- SUPPLY VOLTAGE ±10V TO ±40V
- OFFSET CURRENT 5nA
- BANDWIDTH 4MHz
- SLEW RATE 5V/μs
- COMMON MODE INPUT VOLTAGE SWING ±35V
- OUTPUT OVERLOAD PROTECTION

APPLICATIONS

- INDUSTRIAL CONTROL SYSTEMS
- POWER SUPPLIES
- HIGH VOLTAGE REGULATORS
- RESOLVER EXCITATION
- SIGNAL CONDITIONING

DESCRIPTION

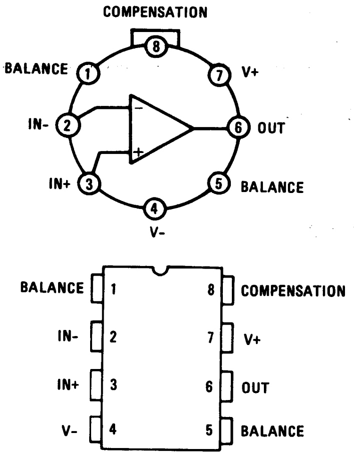
HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

These amplifers deliver ±35V common mode input voltage swing, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/μs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

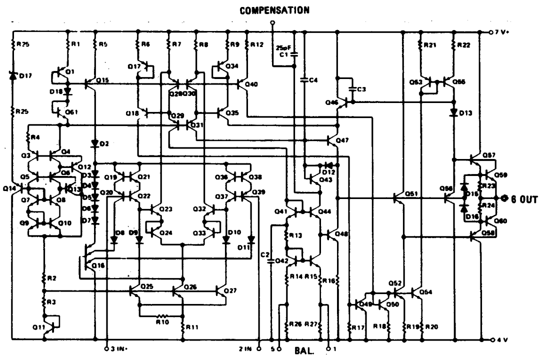
The HA-2640/2645 are available in metal can (TO-99) or ceramic min-dip and can be used as high performance pin-for-pin replacements for many general performance amplifiers. HA-2640 is specified from -55°C to +125°C and HA-2645 is specified over the 0°C to +75°C range.

PINOUTS



TOP VIEWS

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	100V	Operating Temperature Range
Input Voltage Range	±37V	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$ (HA-2640)
Output Current/Full Short Circuit Protection		$0^{\circ}C \leq T_A \leq +75^{\circ}C$ (HA-2645)
Internal Power Dissipation	680mW*	Storage Temperature Range
		$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

*Derate by 4.6mW/°C above +25°C

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 40V$, $R_L = 5K$, Unless Otherwise Specified.

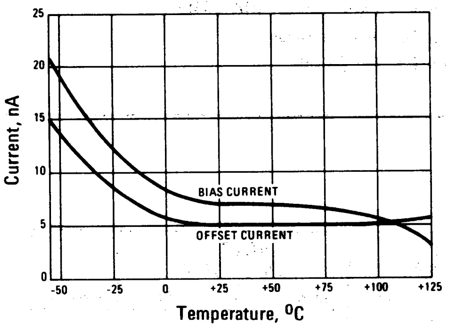
PARAMETER	TEMP.	HA-2640 -55°C to +125°C MIN.	HA-2640 TYP.	HA-2640 MAX.	HA-2645 0°C to +75°C MIN.	HA-2645 TYP.	HA-2645 MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		2	4		2	6	mV
	Full			6			7	mV
Offset Voltage Average Drift	Full		15			15		µV/°C
Bias Current	+25°C		10	25		12	30	nA
	Full			50			50	nA
Offset Current	+25°C		5	12		15	30	nA
	Full			35			50	nA
Input Resistance (Note 10)	+25°C	50	250		40	200		MΩ
Common Mode Range	Full	±35			±35			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 8)	+25°C	100K	200K		100K	200K		V/V
	Full	75K			75K			V/V
Common Mode Rejection Ratio (Note 1)	Full	80	100		74	100		dB
Unity Gain Bandwidth (Note 2)	+25°C		4			4		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±35			±35			V
Output Current (Note 9)	+25°C	±12	±15		±10	±12		mA
Output Resistance	+25°C		500			500		Ω
Full Power Bandwidth (Notes 3 &11)	+25°C		23			23		kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4, 6)	+25°C		60	100		60	100	ns
Overshoot (Notes 4, 6)	+25°C		15	30		15	40	%
Slew Rate (Note 6)	+25°C	±3	±5		±2.5	±5		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.2	3.8		3.2	4.5	mA
Supply Voltage Range	Full	±10		±40	±10		±40	V
Power Supply Rejection Ratio (Note 5)	Full	80	90		74	90		dB

NOTES:
1. $V_{CM} = \pm 20V$
2. $V_O = 90mV$
3. $V_O = \pm 35V$
4. $V_O = \pm 200mV$
5. $V_S = \pm 10V$ to $\pm 40V$
6. $A_V = 1$
7. $C_L = 50pF$, $R_L = 5K$
8. $V_O = \pm 30V$
9. $R_L = 1K$
10. This parameter based upon design calculations.
11. Full power bandwidth guaranteed based upon slew rate measurement. $FPBW = S.R./2\pi V_{peak}$.

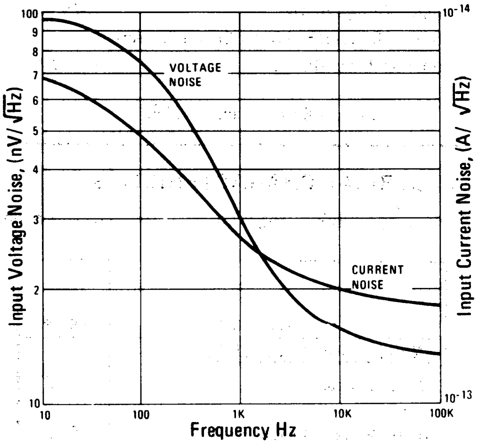
PERFORMANCE CURVES

V+ = V- = 40VDC, T_A = +25°C UNLESS OTHERWISE STATED

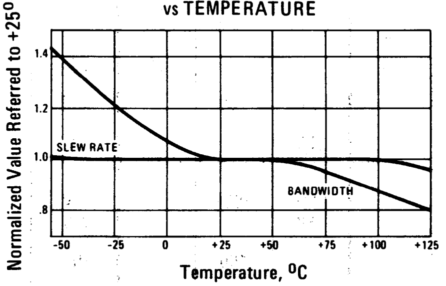
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



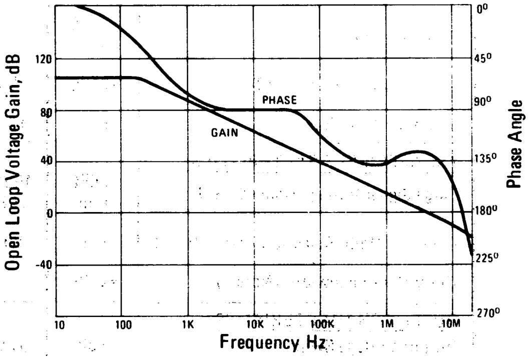
INPUT NOISE CHARACTERISTICS



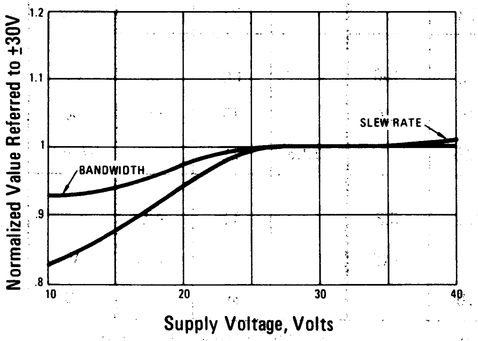
NORMALIZED AC PARAMETERS vs TEMPERATURE



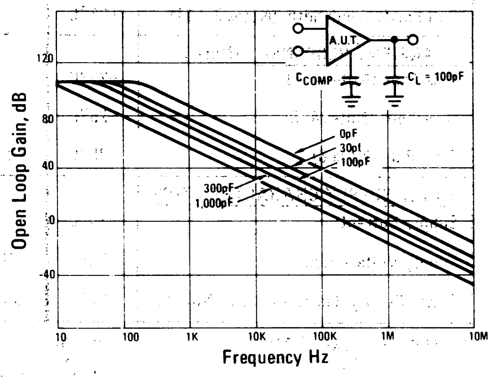
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



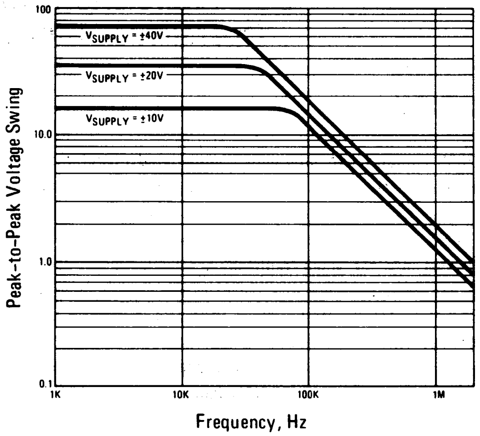
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND



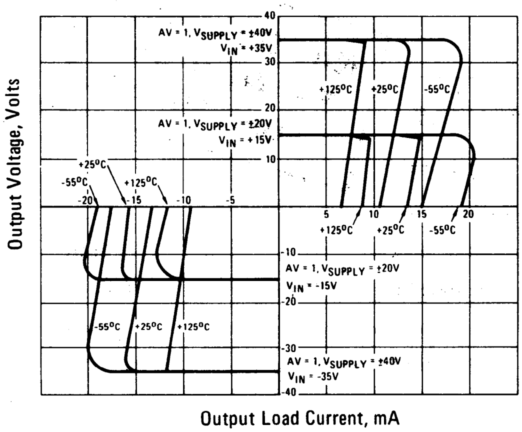
NOTE: External Compensation Components are not Required for Stability. But May be Added to Reduce Bandwidth if Desided. C_L = 100pF is Also Required for Stability Only if External Compensation Capacitor is Used.

PERFORMANCE CURVES (continued)

OUTPUT VOLTAGE SWING
vs FREQUENCY AT +25°C

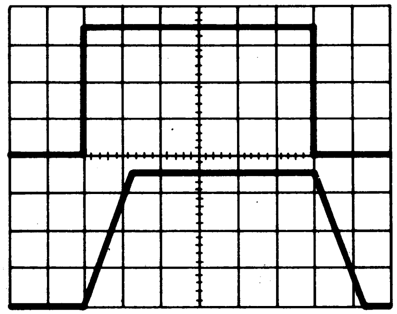


OUTPUT CURRENT CHARACTERISTIC



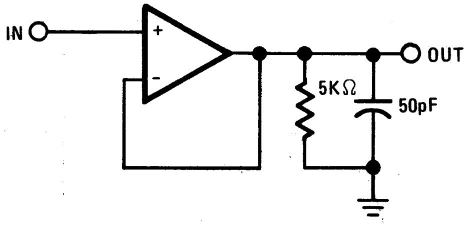
SWITCHING WAVEFORM AND TEST CIRCUIT

VOLTAGE FOLLOWER
PULSE RESPONSE

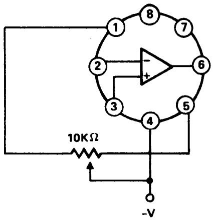


R_L = 5K, C_L = 50pF
Vertical = 10V/Div. T_A = +25°C
Horizontal = 5µs/Div. V_S = ±40V

SLEW RATE AND TRANSIENT
RESPONSE TEST CIRCUIT



SUGGESTED VOS ADJUSTMENT



HARRIS

HA-2650/55

Dual High Performance Operational Amplifier

Not Recommended For New Designs See HA-5102

FEATURES

• SLEW RATE	5V/μs
• BANDWIDTH	8MHz
• BIAS CURRENT	35nA
• AVG. OFFSET VOLTAGE DRIFT	8μV/°C
• POWER CONSUMPTION	75mW
• SUPPLY VOLTAGE RANGE	±2V TO ±20V

APPLICATIONS

- VIDEO AMPLIFIERS
- HIGH IMPEDANCE, WIDEBAND BUFFERS
- INTEGRATORS
- AUDIO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

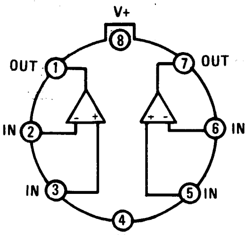
HA-2650/2655 contains two internally compensated operational amplifiers offering high slew rate and high frequency performance combined with exceptional DC characteristics. 5V/μsec slew rate and 8MHz bandwidth make these amplifiers suitable for processing fast, wideband signals extending into the video frequency spectrum. Signal processing accuracy is enhnaced by front-end performance that includes 1.5mV offset voltage, 8μV/°C offset voltage drift and low offset and bias current (1nA and 35nA respectively). Offset voltage can be trimmed to zero on the devices offered in dual-in-line packages. Signal conditioning is further enhanced by 500M input impedance.

Applications for HA-2650/2655 include video circuit designs such as high impedance buffers, integrators, tone generators and filters. These amplifiers are also ideal components for active filtering of audio and voice signals.

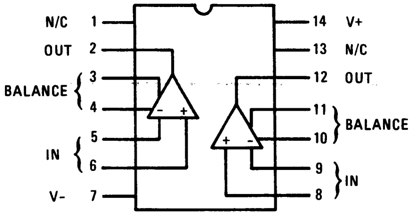
HA-2650/2655 are offered in 14 pin DIP and metal TO-99 packages and are also available in dice form. HA-2650 is specified form -55°C to +125°C. HA-2655 operates from 0°C to +75°C.

PINOUTS

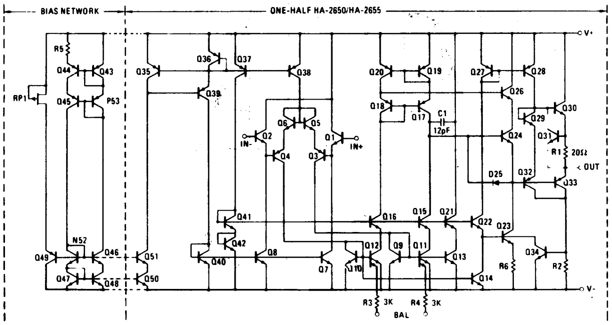
TOP VIEWS


V+
8
OUT 1
7 OUT
IN 2
6 IN
IN 3
5 IN
4
V-

NOTE: Case Connected to V-


N/C 1
OUT 2
BALANCE 3
4
IN 5
6
V- 7
14 V+
13 N/C
12 OUT
11
10 BALANCE
9
8 IN

SCHEMATIC


BIAS NETWORK
ONE-HALF HA-2650/HA-2655
V+
V-
R5
Q44
Q43
RP1
Q45
P53
N52
Q49
Q46
Q47
Q48
Q35
Q36
Q37
Q38
Q39
Q51
Q50
Q41
Q42
Q40
Q8
Q7
Q2
IN-
Q6
Q5
Q1
IN+
Q4
Q3
Q20
Q19
Q18
Q17
C1
12pF
Q27
Q28
Q26
Q30
Q29
Q24
Q31
R1 20Ω
OUT
D25
Q32
Q33
Q16
Q15
Q21
Q22
Q23
Q12
Q9
Q11
Q13
Q10
Q14
Q34
R6
R2
R3 3K
R4 3K
BAL

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

$T_A = +25^oC$ Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration	Indefinite

Power Dissipation (Note 2)	TO-99	300 mW
	TO-116	300 mW
Operating Temperature Range:		
HA-2650		$-55^oC \leq T_A \leq +125^oC$
HA-2655		$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+ = +15V D. C., V- = -15V D. C.

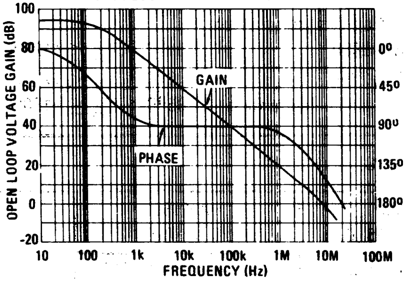
PARAMETER	TEMP.	HA-2650 -55°C to +125°C MIN.	TYP.	MAX.	HA-2655 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		1.5	3		2	5	mV
	Full			5			7	mV
Av. Offset Voltage Drift	Full		8			8		μV/°C
Bias Current	+25°C		35	100		50	200	nA
	Full			200			300	nA
Offset Current	+25°C		1	30		2	60	nA
	Full			60			100	nA
Common Mode Range	Full	±13			±13			V
Differential Input Resistance (Note 9)	+25°C	5	20		5	20		MΩ
Common Mode Input Resistance	+25°C		500			500		MΩ
Input Capacitance	+25°C		5			5		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3ab)	+25°C	20K	40K		15K	40K		V/V
	Full	15K			10K			V/V
Common Mode Rejection Ratio (Note 4)	+25°C	80	100		74	100		dB
	Full	80			74			dB
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 3c)	+25°C	±13	±14		±13	±14		V
	Full	±13			±13			V
Full Power Bandwidth (Notes 5 &10)	+25°C	30	80		30	80		KHz
Output Current (Note 3a)	+25°C		±20			±18		mA
Output Resistance	+25°C		100			100		Ω
TRANSIENT RESPONSE (Note 6)								
Rise Time (Note 7)	+25°C		40	80		40	90	ns
Overshoot (Note 7)	+25°C		15	40		15	40	%
Slew Rate	+25°C	±2	±5		±2	±5		V/μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		2.5	4		3	5	mA
Power Supply Rejection Ratio (Note 8)	+25°C	80	100		74	100		dB
	Full	80			74			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above +110°C.
3. (a) $V_O = \pm 10V$ (b) $R_L = 2K$ (c) $R_L = 10K$
4. $V_{CM} = \pm 5.0V$
5. $A_V = 1, R_L = 2K, V_O = 20V_{pp}$
6. See transient response/slew rate circuit.
7. $V_{in} = 200mV$
8. $\Delta V = \pm 5.0V$
9. This parameter value based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement $FPBW = S.R./2\pi V_{peak}$.

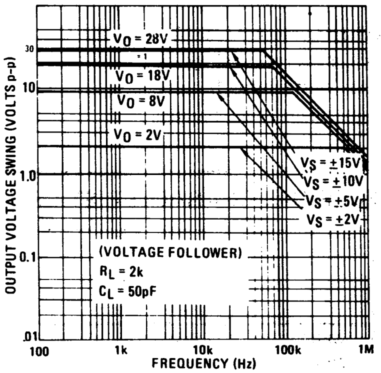
PERFORMANCE CURVES

V+ = +15V, V- = -15V, T_A = +25°C unless otherwise stated.

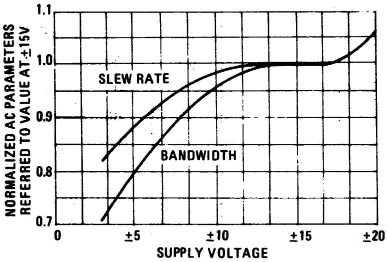
OPEN LOOP FREQUENCY RESPONSE



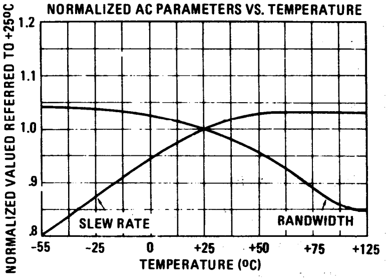
OUTPUT VOLTAGE SWING VS. FREQUENCY



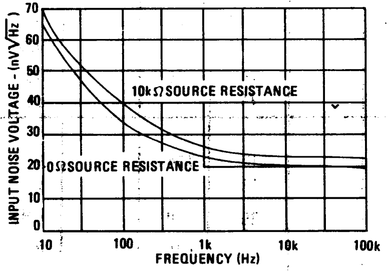
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



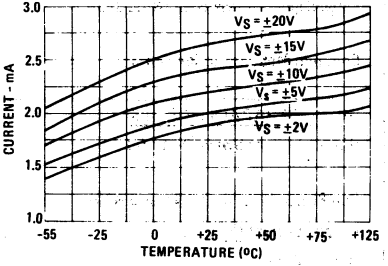
NORMALIZED AC PARAMETERS VS. TEMPERATURE



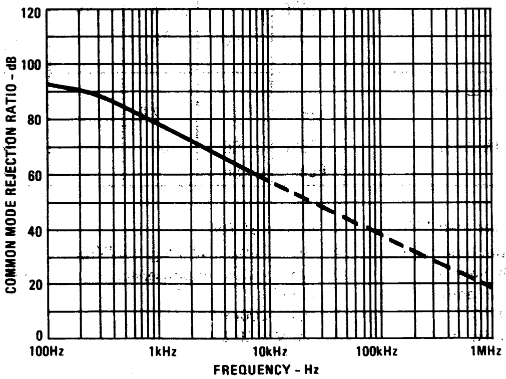
INPUT NOISE VOLTAGE VS. FREQUENCY



POWER SUPPLY CURRENT VS. TEMPERATURE

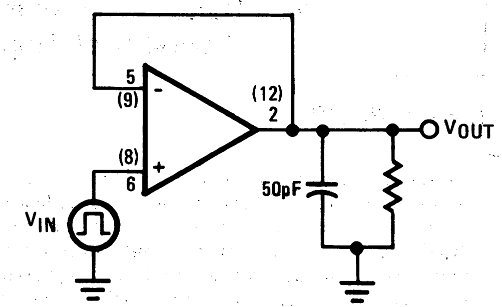


COMMON MODE REJECTION RATIO
VS. FREQUENCY



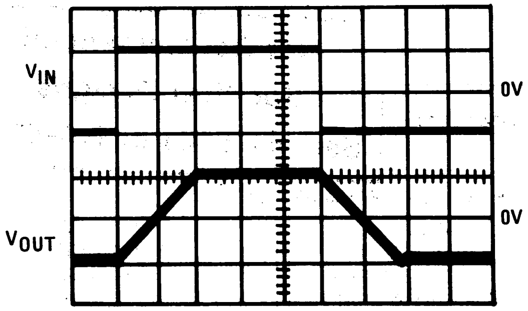
PERFORMANCE CHARACTERISTICS

TRANSIENT RESPONSE/SLEW RATE CIRCUIT


5
(9)
-
(12)
2
VOUT
(8)
+
6
50pF
VIN

Note: Numbers in parentheses refer to the second half of TO-116 package.

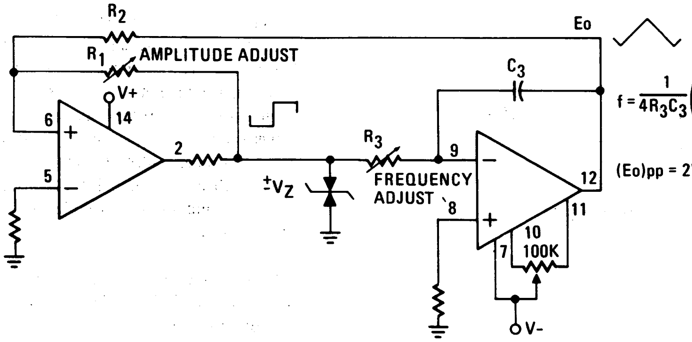
SLEWING WAVEFORM



VERTICAL 5V/DIV. HORIZONTAL 1μs/DIV.

TYPICAL APPLICATIONS

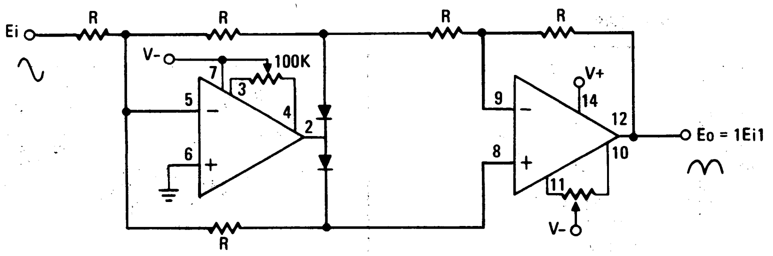
LOW COST HIGH FREQUENCY GENERATOR


R2
Eo
R1
AMPLITUDE ADJUST
C3
V+
14
6
+
2
5
-
R3
±VZ
FREQUENCY ADJUST
9
-
12
8
+
11
10
7
100K
V-

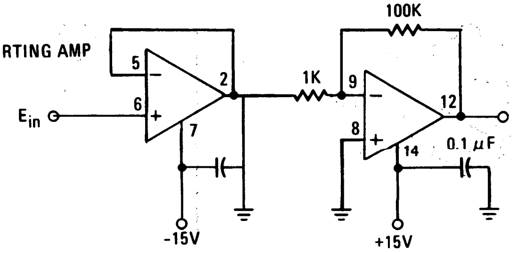
$f = \frac{1}{4R_3C_3}\left(\frac{R_1}{R_2}\right)$

$(E_o)_{pp} = 2V_Z\left(\frac{R_2}{R_1}\right)$

ABSOLUTE-VALUE CIRCUIT


Ei
R
R
R
R
V-
100K
7
3
4
5
-
2
6
+
9
-
V+
14
12
8
+
10
11
V-
R
Eo = 1Ei1

HIGH IMPEDANCE
HIGH GAIN
HIGH FREQUENCY INVERTING AMP


100K
5
-
2
6
+
Ein
7
1K
9
-
12
Eo
8
+
14
0.1 μF
-15V
+15V

BW = 100KHz
$A_V = 100$
$Z_{in} = 2 \times 10^9 \Omega$

HARRIS

HA-2720/25

Wide Range Programmable Operational Amplifier

Not Recommended For New Designs
See HA-5161 or HA-5151

FEATURES

- WIDE PROGRAMMING RANGE

SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

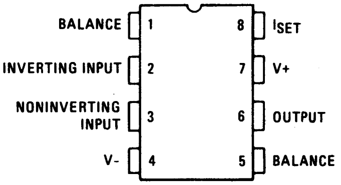
HA-2720/2725 programmable amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables HA-2720/2725 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2720 and HA-2725 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

A major advantage of HA-2720/2725 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipment. A primary application for HA-2720/2725 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2720/2725 can be used for designs such as current controlled oscillators modulators, sample and hold circuits and variable active filters.

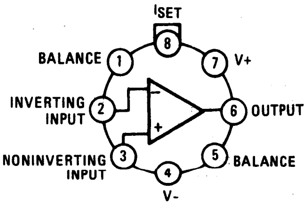
HA-2720 is guaranteed over -55°C to +125°C. HA-2725 is specified from 0°C to +75°C. Both parts are available in TO-99 cans or dice form.

PINOUTS

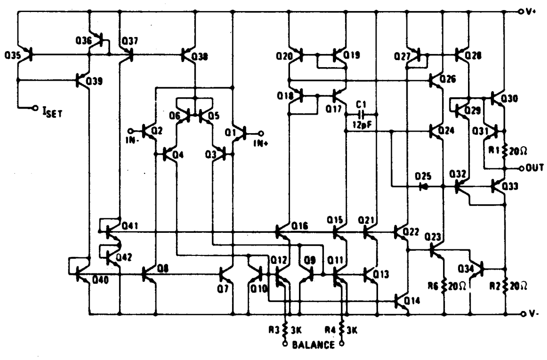
TOP VIEWS


BALANCE
1
8
ISET
INVERTING INPUT
2
7
V+
NONINVERTING INPUT
3
6
OUTPUT
V-
4
5
BALANCE

Note: Case tied to V-


ISET
8
BALANCE
1
7
V+
INVERTING INPUT
2
-
+
6
OUTPUT
NONINVERTING INPUT
3
5
BALANCE
4
V-

SCHEMATIC


V+
Q35
Q36
Q37
Q38
Q39
ISET
Q20
Q19
Q27
Q28
Q26
Q18
Q17
C1
12pF
Q6
Q5
Q2
Q1
IN-
IN+
Q4
Q3
Q30
Q29
Q24
Q31
R1 20Ω
OUT
Q25
Q32
Q33
Q41
Q16
Q15
Q21
Q22
Q23
Q42
Q12
Q9
Q11
Q40
Q8
Q7
Q10
Q13
Q34
R6 20Ω
R2 20Ω
Q14
V-
R3 3K
R4 3K
BALANCE

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
I_{SET} (Current at I_{SET})	500µA
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$
Power Dissipation (Note 2)	300mW
Operating Temperature Range:	
HA-2720	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-2725	$0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range	$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS V+ = +3.0V, V- = -3.0V

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I_{SET} = 1.5µA			I_{SET} = 15µA			I_{SET} = 1.5µA			I_{SET} = 15µA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 9)	25°C	15K	40K		15K	40K		15K	40K		15K	40K		V/V
	Full	10K			10K			10K			10K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±2.0			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		µs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/µs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		15			170			15			170		µA
	Full			25			250			25			250	µA
Power Supply Rejection Ratio (Note 8)	Full	80			80			76			76			dB

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS $V+ = +15.0V$, $V- = -15.0V$

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		$I_{SET} = 1.5\mu A$			$I_{SET} = 15\mu A$			$I_{SET} = 1.5\mu A$			$I_{SET} = 15\mu A$			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	30K	100K		30K	120K		25K	40K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		µs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/µs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		20			210			20			210		µA
	Full			50			450			50			450	µA
Power Supply Rejection Ratio (Note 8)	Full	80			80			76			76			dB

NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

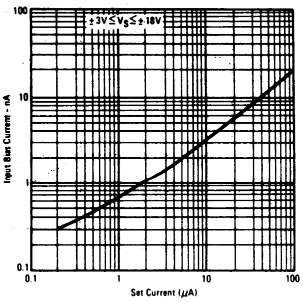
	$V_{SUPPLY} = \pm 3.0V$	$V_{SUPPLY} = \pm 15.0V$	$I_{SET} = 1.5\mu A$	$I_{SET} = 15\mu A$
3.	T = +25°C and Full	T = +25°C	$R_L = 75K\Omega$	$R_L = 5K\Omega$
	—	T = Full	$R_L = 75K\Omega$	$R_L = 75K\Omega$
4.	$V_{CM} = \pm 1.5V$	$V_{CM} = \pm 5.0V$		
5.	$V_O = \pm 2.0V$	$V_O = \pm 10.0V$		
6.	← $A_V = +1$, $V_{IN} = 400mV$, $R_L = 5K$, $C_L = 100pF$ →			
7.	$V_O = \pm 2.0V$	$V_O = \pm 10.0V$	$R_L = 20K$	$R_L = 5K$
8.	$\Delta V = \pm 1.5V$	$\Delta V = \pm 5.0V$		
9.	$V_O = \pm 1.0V$	$V_O = \pm 10.0V$		

10. This parameter based upon design calculations.

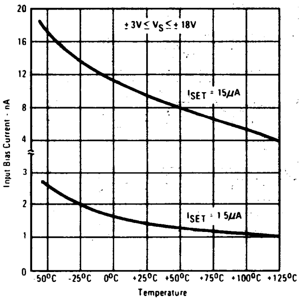
PERFORMANCE CURVES

UNLESS OTHERWISE NOTED: $T_A = +25^{\circ}C$, $V_S = \pm 15VDC$

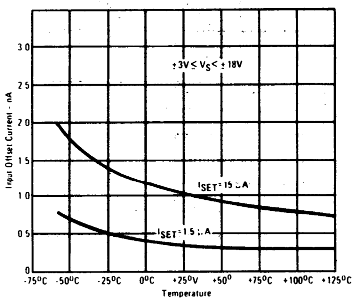
INPUT BIAS CURRENT vs. SET CURRENT



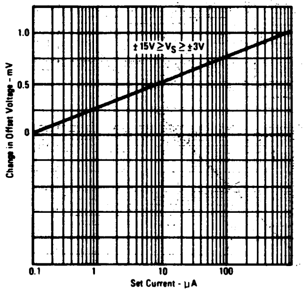
INPUT BIAS CURRENT vs. TEMPERATURE



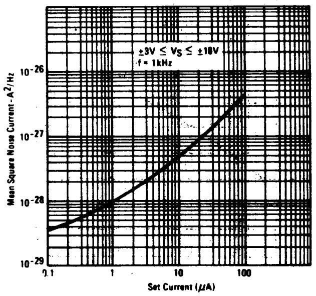
INPUT OFFSET CURRENT vs. TEMPERATURE



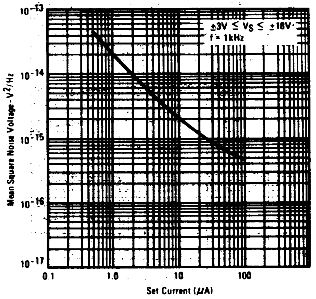
CHANGE IN OFFSET VOLTAGE vs. I_{SET} (UNNULLED)



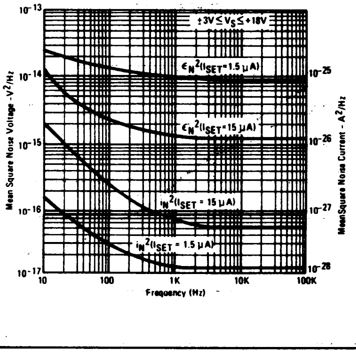
INPUT NOISE CURRENT vs. I_{SET}



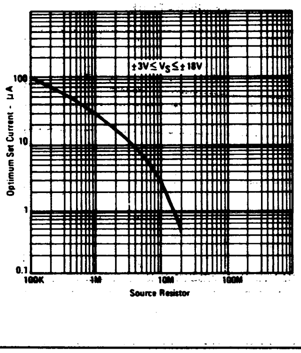
INPUT NOISE VOLTAGE vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT vs. FREQUENCY



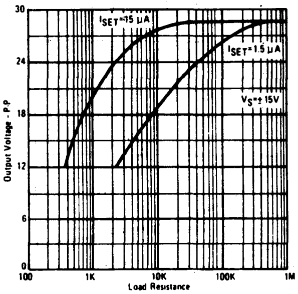
OPTIMUM SET CURRENT FOR MINIMUM NOISE vs. SOURCE RESISTOR



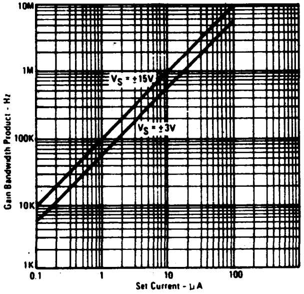
PERFORMANCE CURVES

UNLESS OTHERWISE NOTED: $T_A = +25^\circ C$, $V_S = \pm 15VDC$

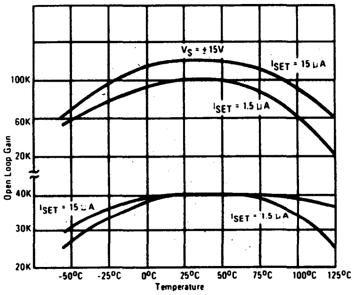
MAXIMUM OUTPUT VOLTAGE SWING
vs. LOAD RESISTANCE



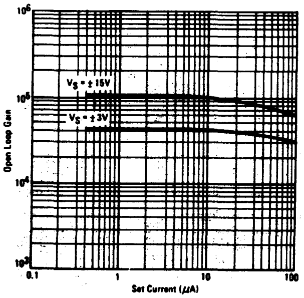
GAIN BANDWIDTH PRODUCT
vs. I_{SET}



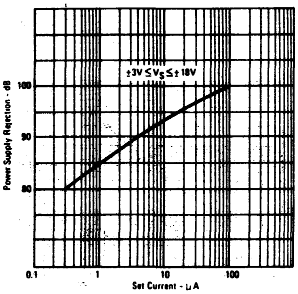
OPEN LOOP VOLTAGE GAIN
vs. TEMPERATURE



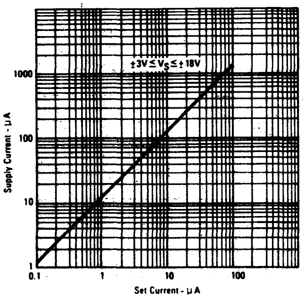
OPEN LOOP VOLTAGE GAIN
vs. I_{SET}



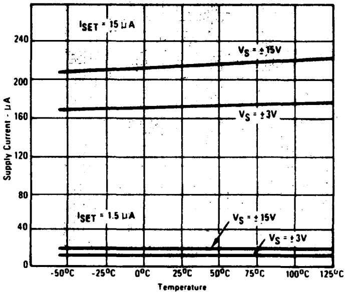
POWER SUPPLY REJECTION
vs. I_{SET}



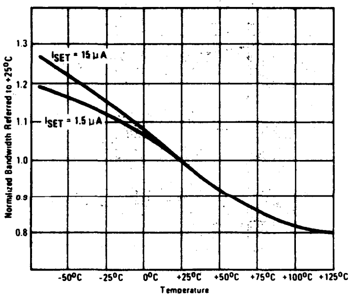
STANDBY SUPPLY CURRENT
vs. I_{SET}



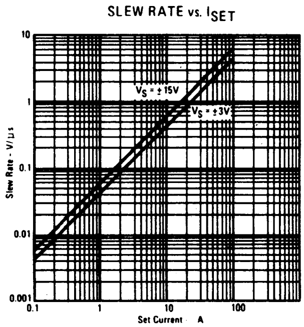
SUPPLY CURRENT vs.
TEMPERATURE

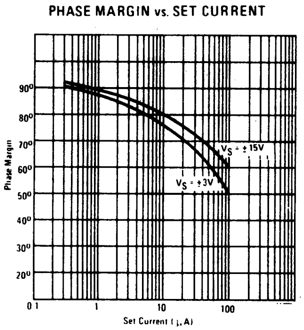


NORMALIZED BANDWIDTH
vs. TEMPERATURE

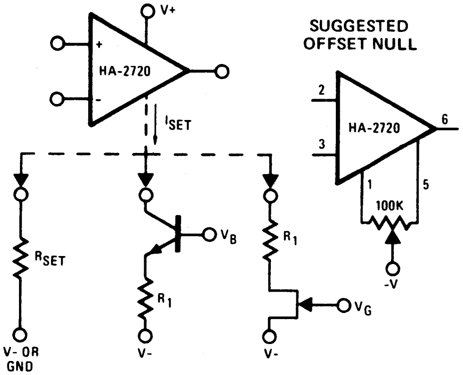


PERFORMANCE CURVES

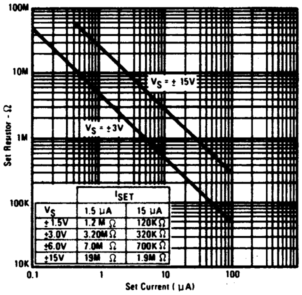

SLEW RATE vs. I_{SET}


PHASE MARGIN vs. SET CURRENT

TYPICAL BIASING CIRCUITS


V+
+
-
HA-2720
I_{SET}
R_{SET}
V- OR GND
V_B
R_1
V-
R_1
V_G
V-
SUGGESTED OFFSET NULL
2
3
HA-2720
6
1
5
100K
-V

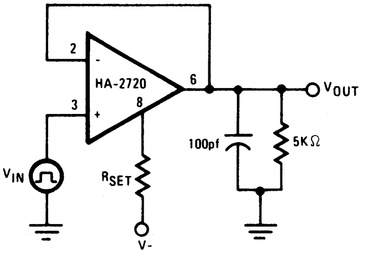
SET CURRENT VS. SET RESISTOR

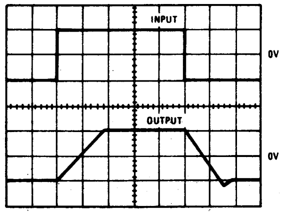


	I_{SET}	
V_S	1.5 µA	15 µA
±1.5V	1.2 M Ω	120K Ω
±3.0V	3.20M Ω	320K Ω
±6.0V	7.0M Ω	700K Ω
±15V	19M Ω	1.9M Ω

TRANSIENT RESPONSE/SLEW RATE CIRCUIT

SLEWING WAVEFORM


2
-
HA-2720
3
+
8
6
V_{OUT}
100pf
5KΩ
V_{IN}
R_{SET}
V-



VERTICAL: 5V/DIV
HORIZONTAL: 1µS/DIV
I_{SET} = 100µA

HARRIS

HA-4600/02/05

High Performance Quad Operational Amplifier

Not Recommended For New Designs See HA-5104

FEATURES

LOW OFFSET VOLTAGE	0.3mV
HIGH SLEW RATE	±4V/μs
WIDE BANDWIDTH	8MHz
LOW DRIFT	2μV/°C
FAST SETTLING (0.01%, 10V STEP)	4.2μs
LOW POWER CONSUMPTION	35mW/AMP
SUPPLY RANGE	±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDE BAND FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- DATA ACQUISITION SYSTEMS
- INTEGRATORS
- ABSOLUTE VALUE CIRCUITS
- TONE DETECTORS

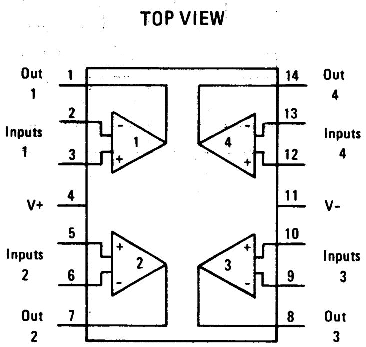
DESCRIPTION

The HA-4600 series are high performance dielectrically isolated monolithic quad operational amplifiers with superior specifications not previously available in a quad amplifier. These amplifiers offer excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

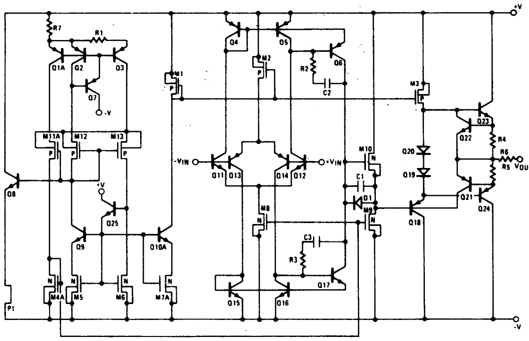
A wide range of applications can be achieved by using the features made available by the HA-4600 series. With wide bandwidth (8MHz), low power (35mW/amp), and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise ($8nV/\sqrt{Hz}$) and excellent full power bandwidth (60kHz). The HA-4602/4605 is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2 μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/ μs) and fast settling time (4.2 μs to 0.01%, 10V step) makes these amplifiers useful components in fast, accurate data acquisition systems.

The HA-4600 series are available in 14 pin CERDIP packages which are interchangeable with most other quad op amps. HA-4600/4602-2 is specified from -55°C to +125°C and HA-4600/4605-5 is specified over 0°C to +75°C range.

PINOUT


TOP VIEW
Out 1
1
2
Inputs 1
3
V+
4
5
Inputs 2
6
Out 2
7
14
Out 4
13
Inputs 4
12
11
V-
10
Inputs 3
9
8
Out 3
1
2
3
4

SCHEMATIC


+V
-V
R7
R1
Q1A
Q2
Q3
Q7
Q4
Q5
M1
M2
R2
Q6
C2
M3
Q23
Q22
R4
R6
R5
VOUT
Q20
Q19
Q21
Q24
Q18
M11A
M12
M13
-VIN
+VIN
Q11
Q13
Q14
Q12
M10
C1
D1
M9
Q8
Q25
Q9
Q10A
M8
C3
R3
Q17
Q15
Q16
M4A
M5
M6
M7A
P1

ONE FOURTH ONLY (HA-4600)

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated	
Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±7V
Input Voltage (Note 2)	±15.0V
Output Short Circuit Duration (Note 3)	Indefinite
Power Dissipation (Note 4)	880mW
Operating Temperature Range	
HA-4600/4602-2	$-55°C \leq T_A \leq +125°C$
HA-4600/4605-5	$0°C \leq T_A \leq +75°C$
Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

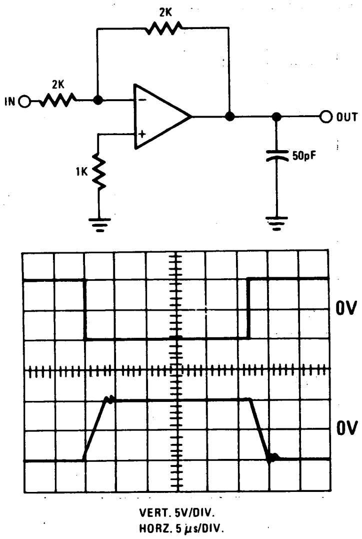
Electrical Characteristics V+ = +15V, V- = -15V

		HA-4600-2 HA-4600-5			HA-4602-2 HA-4605-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.3	2.5		3.0	9	mV
	Full			3.0			10	mV
Av. Offset Voltage Drift	Full		2			5		μV/°C
Bias Current	+25°C		130	200		200	400	nA
	Full			325			500	nA
Offset Current	+25°C		30	75		70	150	nA
	Full			125			175	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance			500			500		kΩ
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
Common Mode Rejection Ratio (Note 9)	Full	86			80			dB
Channel Separation (Note 6)	+25°C		-108			-108		dB
Small Signal Bandwidth	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60			60		kHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		50	150		50	150	ns
Overshoot	+25°C		30	45		30	45	%
Slew Rate	+25°C	±2	±4		±1	±4		V/μs
Settling Time (Note 10)			4.2			4.2		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.6	5.5		5.0	7.5	mA
Power Supply Rejection Ratio (Note 9)	Full	86			74			dB

NOTES:

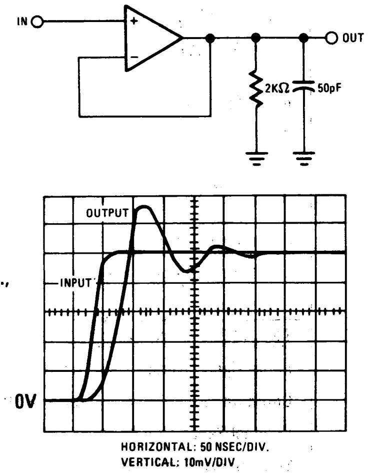
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 2K ohms.
6. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 1K ohms. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
7. Output current is measured with V_{OUT} = ±5 volts.
8. For transient response test circuits and measurement conditions refer to Test Circuits section of the data sheet.
9. ΔV = ±5.0 volts.
10. Settling time is measured to 0.1% of final value for a 10 volt input step, A_V = -1.

TEST CIRCUITS



2K
IN
2K
1K
OUT
50pF
0V
0V
VERT. 5V/DIV.
HORZ. 5 µs/DIV.

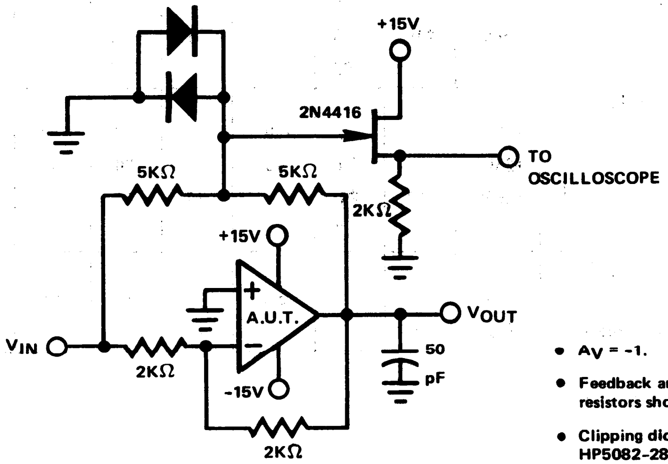
LARGE SIGNAL RESPONSE CIRCUIT
(Volts: 5V/Div., Time: 5µs/Div.)



IN
OUT
2KΩ
50pF
OUTPUT
INPUT
0V
HORIZONTAL: 50 NSEC/DIV.
VERTICAL: 10mV/DIV.

SMALL SIGNAL RESPONSE CIRCUIT
(Volts: 10mV/Div., Time: 50ns/Div.)

SETTLING TIME CIRCUIT



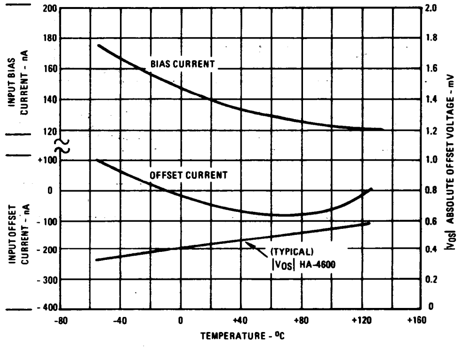
+15V
2N4416
TO OSCILLOSCOPE
5KΩ
5KΩ
2KΩ
+15V
A.U.T.
VOUT
VIN
2KΩ
-15V
50 pF
2KΩ

- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

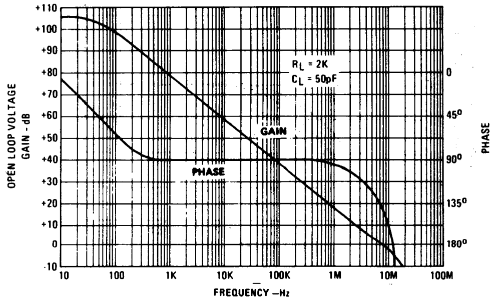
PERFORMANCE CURVES

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

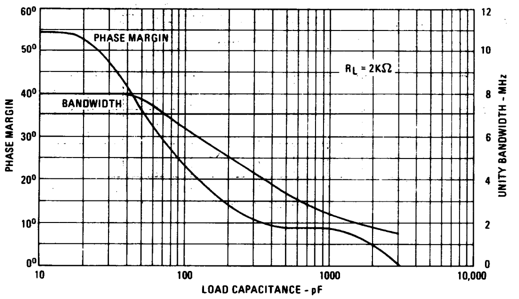
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



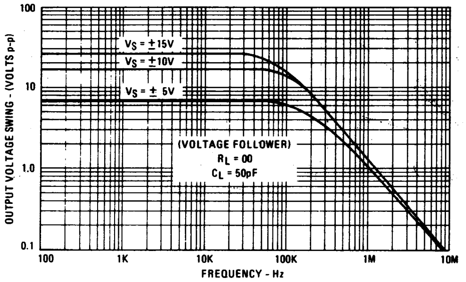
OPEN LOOP FREQUENCY RESPONSE



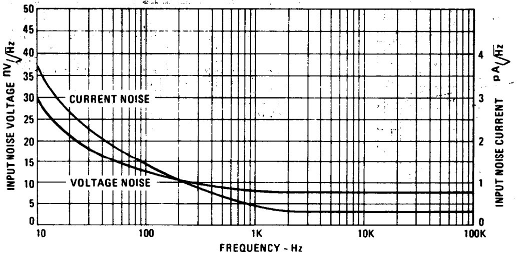
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



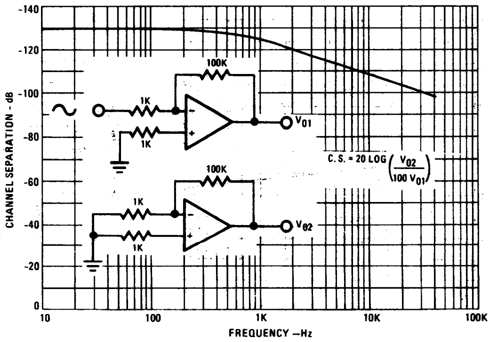
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



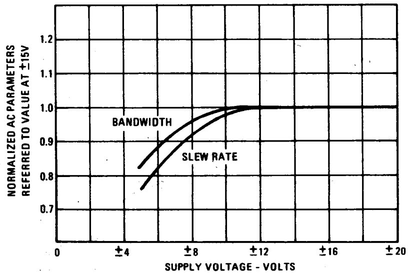
INPUT NOISE VS. FREQUENCY



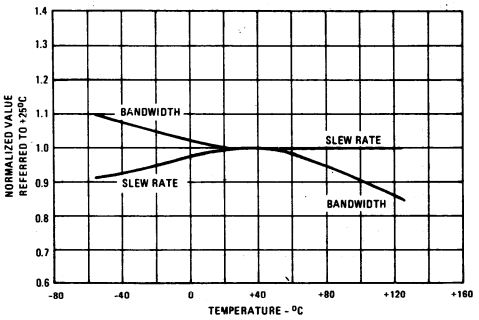
CHANNEL SEPARATION VS. FREQUENCY



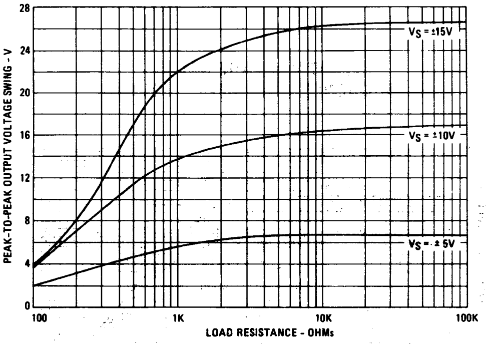
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



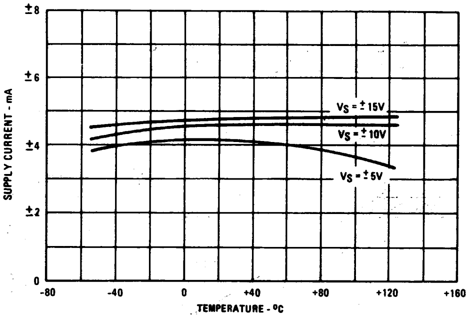
NORMALIZED AC PARAMETERS VS. TEMPERATURE



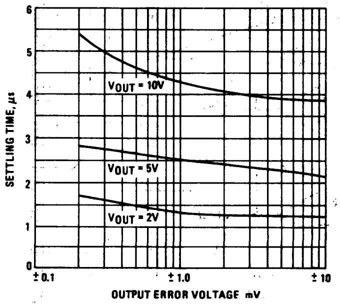
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



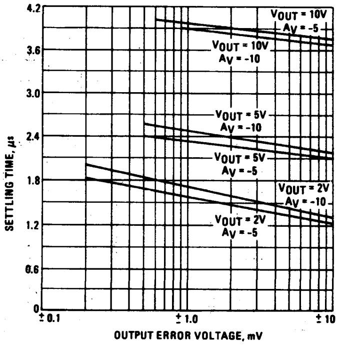
POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



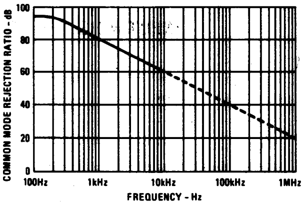
SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -1)



SETTLING TIME VS. OUTPUT AMPLITUDE AND SIGNAL GAIN (A_V = -5 AND A_V = -10)



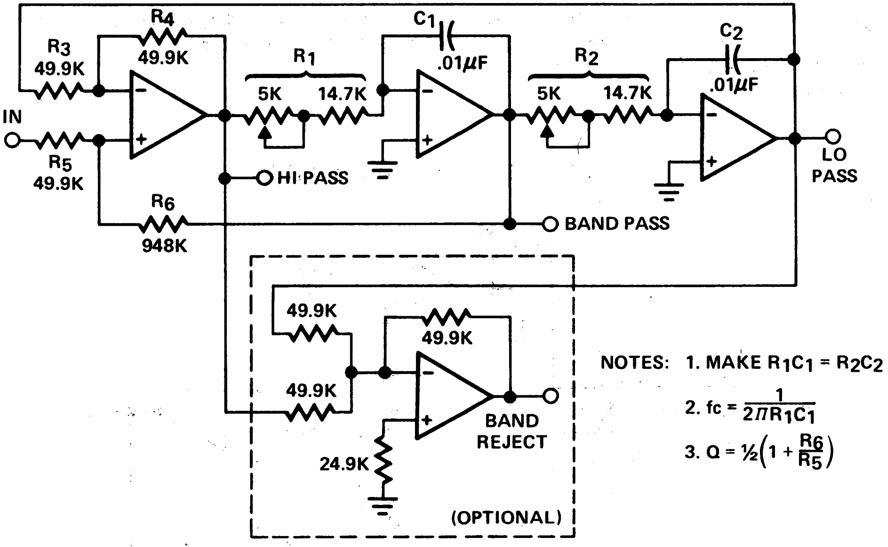
HA-4602 - COMMON MODE REJECTION RATIO VS. FREQUENCY



1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. UNUSED OP AMPS: Unused op amp sections should be connected in a non-inverting follower configuration with the (+) input tied to ground in order to insure optimum performance of devices being used.
3. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

APPLICATIONS

2ND ORDER STATE VARIABLE FILTER (1kHz, Q = 10)



NOTES: 1. MAKE $R_1C_1 = R_2C_2$

2. $f_c = \frac{1}{2\pi R_1C_1}$

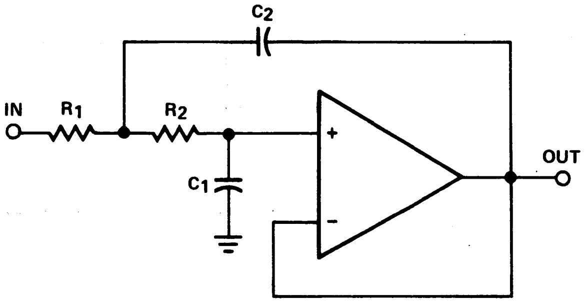
3. $Q = \frac{1}{2}\left(1 + \frac{R_6}{R_5}\right)$

The state variable filter is relatively insensitive to component changes (changes can be adjusted out with potentiometers) and also has low sensitivity to amplifier bandwidths. (Amplifier gain bandwidth product should be $\gg Q \times f_C$). The bandwidth criteria will determine whether a general purpose op amp like Harris HA-4741 or the wide band HA-4602/4605 should be used.

This filter finds wide application because multiple filtering functions are available simultaneously (High pass, Lo pass, Band pass, Band reject). In this circuit the various RC products are matched with pot adjustments allowing for non-interactive adjustment of Q and f_C. This allows capacitors (C_1, C_2) with loose tolerances to be used. To tune for f_C, apply a sine wave at f_C to the input, adjust R_1 for equal amplitudes at the Hi pass and Band pass terminals (they will be phased 90° apart) then adjust R_2 for equal amplitudes at the Band pass and Lo pass terminals.

The state variable filter is often used as building blocks in multiple pole Butterworth of Chebyshev filters. Many references contain normalized tables indicating settings for Q and f_C of each pole-pair section.

SALLEN AND KEY 2ND ORDER LO PASS FILTER



NOTES:

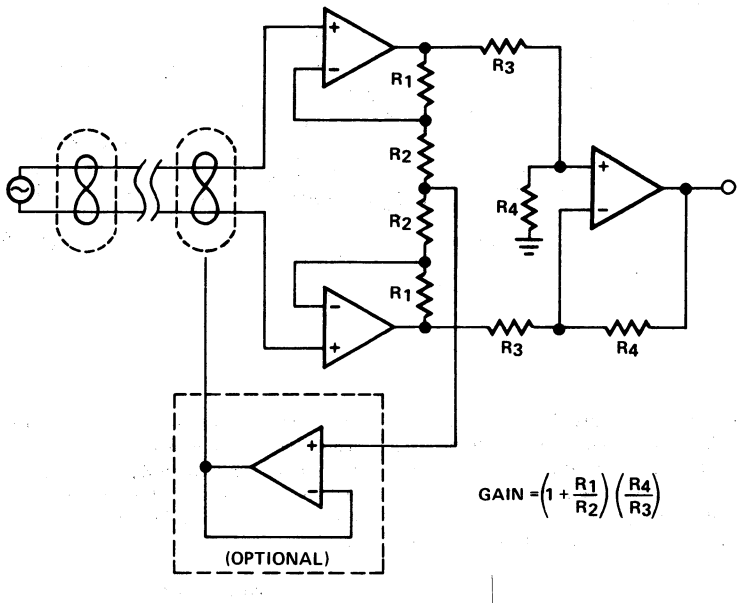
1. Make $R_1 = R_2$
2. $fc = \frac{1}{2\pi R_1\sqrt{C_1C_2}}$
3. $Q = ½ \sqrt{\frac{C_2}{C_1}}$

The advantage of using the Sallen and Key filter is simplicity, but in any application this must be weighed against the state-variable type filter for accuracy, practicality, and cost. Amplifier bandwidth limitations are much more apparent at moderate frequencies and Q values with this filter design. (For accuracy, amplifier gain-bandwidth product should be $\gg f_C \times Q^2$). The wide bandwidth of the HA-4602/4605 is particularly advantageous in this design even at audio frequencies.

In this filter all component values affect both Q and f_C. Precision, temperature stable resistors and capacitors must be used.

For economy, this filter could be used in the low Q stages of multiple-pole filter design, while the state variable type is used in the more critical stages.

INSTRUMENTATION AMPLIFIER



$$GAIN = \left(1 + \frac{R_1}{R_2}\right)\left(\frac{R_4}{R_3}\right)$$

Instrumentation amplifiers (differential amplifiers) are specifically designed to extract and amplify small differential signals from much larger common mode voltages.

To serve as building blocks in instrumentation amplifiers, op amps must have very low offset voltage drift, high gain and wide bandwidth. The HA-4602/4605 is ideally suited for this application, delivering superior input and speed characteristics.

The optional circuitry makes use of the fourth amplifier section as a shield driver which enhances the AC common mode rejection by nullifying the effects of capacitance-to-ground mismatch between input conductors.

HARRIS

HA-4741

Quad Operational Amplifier

FEATURES

• SLEW RATE	1.6V/μs
• BANDWIDTH	3.5MHz
• INPUT VOLTAGE NOISE	9nV√Hz
• INPUT OFFSET VOLTAGE	0.5mV
• INPUT BIAS CURRENT	60nA
• SUPPLY RANGE	±2V TO ±20V
• NO CROSSOVER DISTORTION	
• STANDARD QUAD PIN-OUT	

APPLICATIONS

- UNIVERSAL ACTIVE FILTERS
- D3 COMMUNICATIONS FILTERS
- AUDIO AMPLIFIERS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

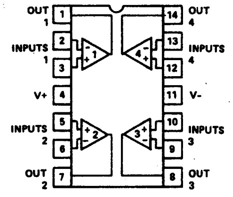
HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/ √Hz at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion. These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (108dB at 1kHz).

A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

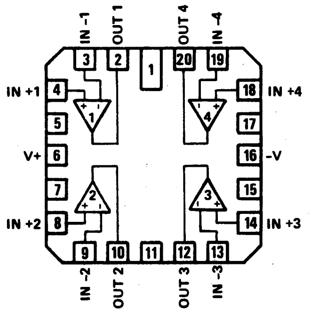
The HA-4741 is available in a 20 pin LCC package as well as both 14 pin ceramic and epoxy mini-dips. The HA-4741-2 operates from -55°C to +125°C and the HA-4741-5 operates over the 0°C to +75°C temperature range.

PINOUT

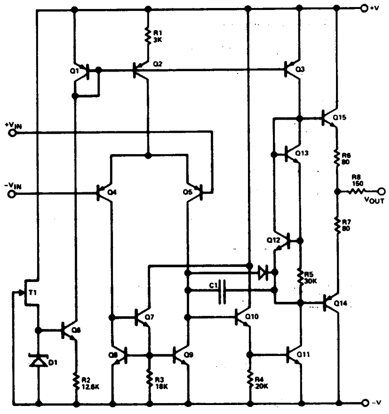
TOP VIEWS


OUT 1
INPUTS 1
V+
INPUTS 2
OUT 2
OUT 4
INPUTS 4
V-
INPUTS 3
OUT 3
1
2
3
4
5
6
7
8
9
10
11
12
13
14

QUAD OP AMP


IN -1
OUT 1
OUT 4
IN -4
IN +1
IN +4
V+
-V
IN +2
IN +3
IN -2
OUT 2
OUT 3
IN -3
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20

SCHEMATIC


+V
-V
+VIN
-VIN
VOUT
R1 3K
R2 12.6K
R3 18K
R4 20K
R5 30K
R6 80
R7 80
R8 150
C1
T1
D1
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15

(¼) HA-4741

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated		Power Dissipation For Epoxy Package. (Note 3)	880mW
Voltage Between V+ and V− Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±30.0V	HA-4741-2	$-55°C \leq T_A \leq +125°C$
Input Voltage (Note 1)	±15.0V	HA-4741-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration (Note 2)	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS V+ = +15V, V− = −15V

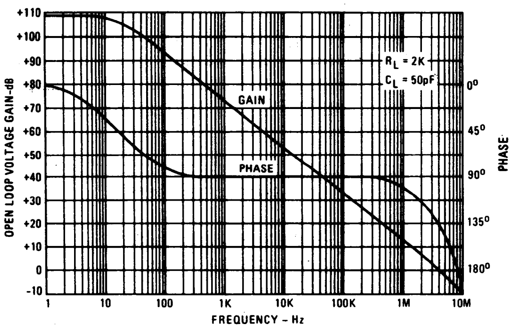
		HA-4741-2 −55°C to +125°C			HA-4741-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.5	3.0		1.0	5.0	mV
	Full		4.0	5.0		4.0	6.5	mV
Av. Offset Voltage Drift	Full		5			5		μV/°C
Bias Current	+25°C		60	200		60	300	nA
	Full			325			400	nA
Offset Current	+25°C		15	30		30	50	nA
	Full			75			100	nA
Common Mode Range	Full	±12			±12			V
Differential Input Resistance	+25°C		5			5		MΩ
Input Voltage Noise (f = 1kHz)	+25°C		9			9		nV/√Hz
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	50K	100K		25K	50K		V/V
	Full	25K			15K			V/V
	+25°C	80			80			dB
Common Mode Rejection Ratio	Full	74			74			dB
Channel Separation (Note 5)	+25°C	90	−108		90	−108		dB
Small Signal Bandwidth	+25°C	2.5	3.5		2.5	3.5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		±10	±12.5		V
Full Power Bandwidth (Notes 4 & 9)	+25°C	14	25		14	25		kHz
Output Current (Note 6)	Full	±5	±15		±5	±15		mA
Output Resistance	+25°C		300			300		Ω
TRANSIENT RESPONSE (Notes 7 & 10)								
Rise Time (Note 11)	+25°C		75	140		75	140	ns
Overshoot (Note 11)	+25°C		25	40		25	40	%
Slew Rate (Note 12)	+25°C		±1.6			±1.6		V/μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C			5.0			7.0	mA
Power Supply Rejection Ratio (Note 8)	Full	80			80			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K.
5. Referred to input; f = 10kHz, R_S = 1K.
6. V_{OUT} = ±10.
7. See Pulse Response Characteristics.
8. ΔV = ±5.0V.
9. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S. R./2 π Vpeak.
10. R_L = 2K, C_L = 50pF.
11. V_{OUT} = ±200mV.
12. V_{OUT} = ±5V.

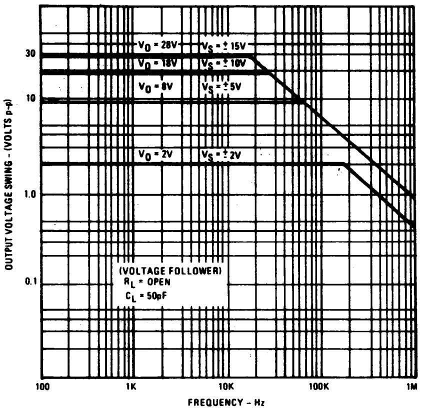
PERFORMANCE CURVES

V+ = +15V, V− = −15V, T_A = +25°C
Unless Otherwise Stated.

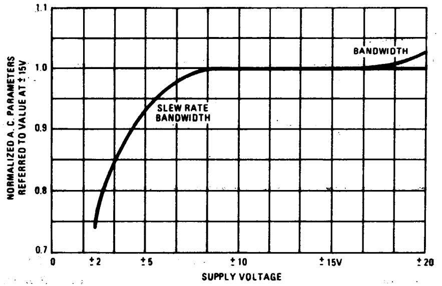
OPEN LOOP FREQUENCY RESPONSE



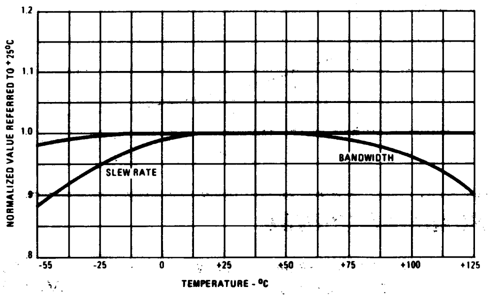
OUTPUT VOLTAGE SWING VS. FREQUENCY



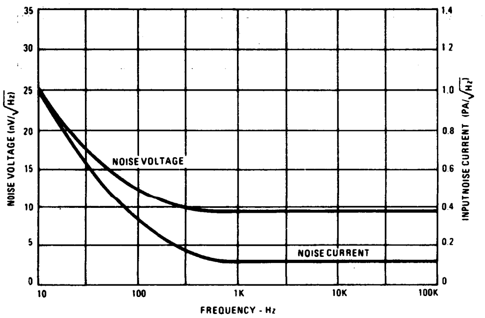
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



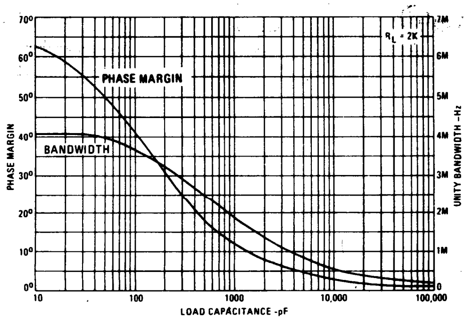
NORMALIZED AC PARAMETERS VS. TEMPERATURE



INPUT NOISE VS. FREQUENCY

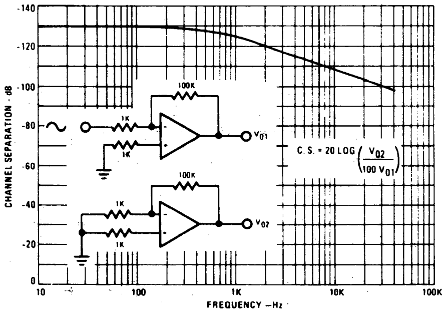


SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE

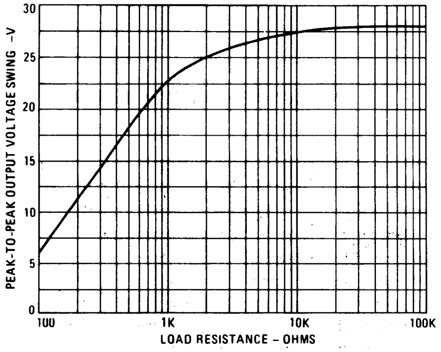


PERFORMANCE CURVES (Continued)

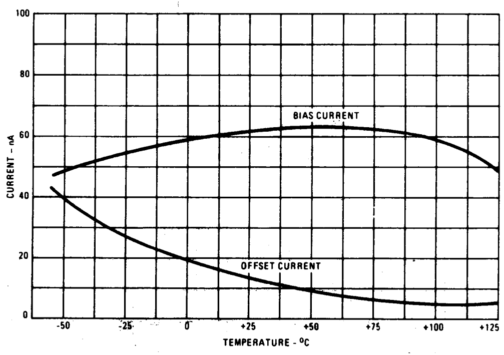
CHANNEL SEPARATION VS. FREQUENCY



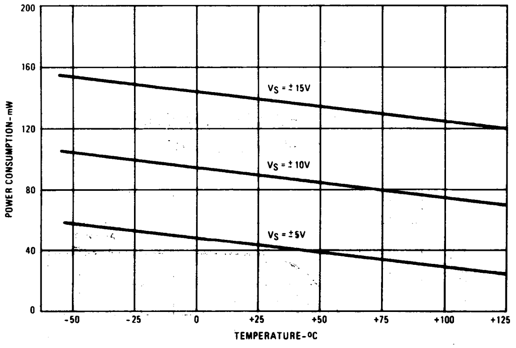
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

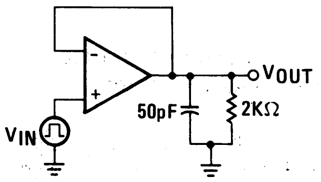


POWER CONSUMPTION VS. TEMPERATURE

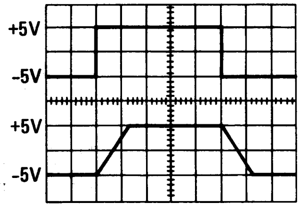


PULSE RESPONSE

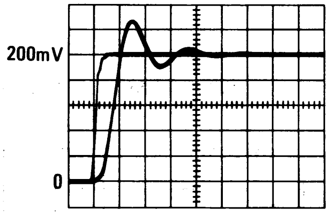
TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEW RESPONSE
(Volts: 5V/Div, Time: 5μs/Div)



TRANSIENT RESPONSE
(Volts: 40mV/Div., Time: 100ns/Div.)



HARRIS

HA-4900/02/05

Precision Quad Comparator

FEATURES

- FAST RESPONSE TIME 130ns
- LOW OFFSET VOLTAGE 2.0mV
- LOW OFFSET CURRENT 10nA
- SINGLE OR DUAL-VOLTAGE SUPPLY OPERATION
- SELECTABLE OUTPUT LOGIC LEVELS
- ACTIVE PULL-UP/PULL-DOWN OUTPUT CIRCUIT - NO EXTERNAL RESISTORS REQUIRED

APPLICATIONS

- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- WINDOW DETECTOR
- ANALOG INTERFACES FOR MICROPROCESSORS
- HIGH STABILITY OSCILLATORS
- LOGIC SYSTEM INTERFACES

DESCRIPTION

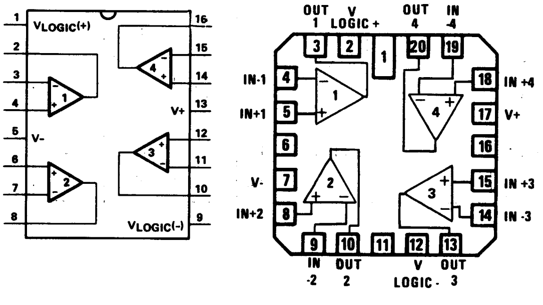
The HA-4900 series are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current, and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5 volt supply (digital systems) or from dual supplies (analog networks) up to ±15 volts. The HA-4900 series contains a unique current driven output stage which can be connected to logic system supplies ($V_{Logic}+$ and $V_{Logic}-$) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900 series input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

These comparators' combination of features makes them ideal components for signal detection and processing in data acquisition systems, test equipment, and microprocessor/analog signal interface networks.

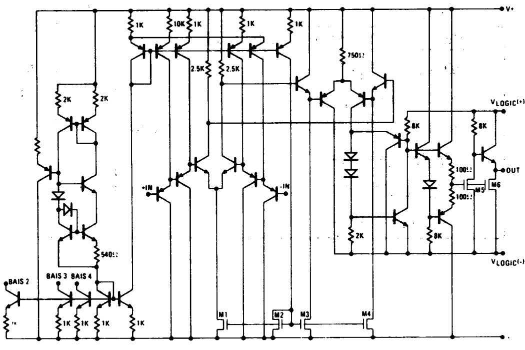
All devices are available in 16 pin dual-in-line ceramic packages. The HA-4900/4902-2 operates from -55°C to +125°C and the HA-4905-5 operates over a 0°C to +75°C temperature range.

PINOUTS

TOP VIEWS


1
VLOGIC(+)
2
3
4
5
V-
6
7
8
16
15
14
13
V+
12
11
10
9
VLOGIC(-)
1
2
3
4
OUT 1
V LOGIC +
OUT 4
IN -4
IN-1
IN+1
V-
IN+2
IN +4
V+
IN +3
IN -3
IN -2
OUT 2
V LOGIC -
OUT 3
3
2
1
20
19
4
5
6
7
8
18
17
16
15
14
9
10
11
12
13

SCHEMATIC


V+
1K
10K
1K
1K
1K
2.5K
2.5K
750Ω
2K
2K
VLOGIC(+)
8K
8K
100Ω
OUT
100Ω
M5
M6
+IN
-IN
2K
8K
540Ω
VLOGIC(-)
BAIS 2
BAIS 3
BAIS 4
1K
1K
1K
1K
M1
M2
M3
M4

ONE FOURTH ONLY (HA-4900 SERIES)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	33V
Voltage Between $V_{Logic}(+)$ and $V_{Logic}(-)$	18V
Differential Input Voltage	±15V
Peak Output Current	±50mA
Internal Power Dissipation (Note 7, 8)	2.0W
Storage Temperature Range	$-65^oC \leq T_A \leq 150^oC$

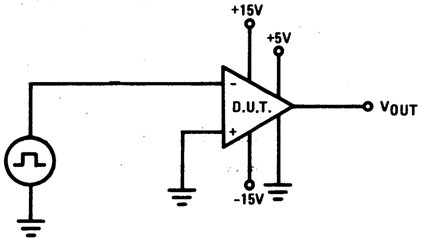
ELECTRICAL CHARACTERISTICS $V+ = +15.0V$, $V- = -15.0V$, $V_{Logic}(+) = 5.0V$, $V_{Logic}(-) = GND$.

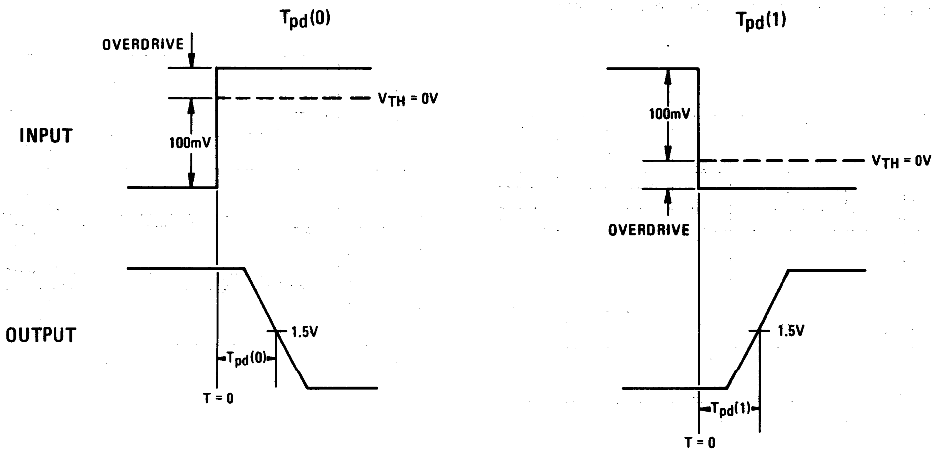
PARAMETER	TEMP	HA-4900-2 -55°C to +125°C			HA-4902-2 55°C to +125°C			HA-4905-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 2)	25°C		2	3		2	5		4	7.5	mV
	Full			4			8			10	mV
Offset Current	25°C		10	25		10	35		25	50	nA
	Full			35			35			70	nA
Bias Current (Note 3)	25°C		50	75		50	150		100	150	nA
	Full			150			200			300	nA
Input Sensitivity (Note 4)	25°C			Vio +.3			Vio +.5			Vio +.5	mV
	Full			Vio +.4			Vio +.6			Vio +.7	mV
Common Mode Range	Full	V-		V+ -2.4	V-		V+-2.6	V-		V+-2.4	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	25°C		400K			400K			400K		V/V
Response Time ($T_{pd}0$) (Note 5)	25°C		130	200		130	200		130	200	ns
Response Time ($T_{pd}1$) (Note 5)	25°C		180	215		180	215		180	215	ns
OUTPUT CHARACTERISITICS											
Output Voltage Level											
Logic "Low State" (V_{OL}) (Note 6)	Full		0.2	0.4		0.2	0.4		0.2	0.4	V
Logic "High State" (V_{OH}) (Note 6)	Full	3.5	4.2		3.5	4.2		3.5	4.2		V
Output Current											
I_{Sink}	Full	3.0			3.0			3.0			mA
I_{Source}	Full	3.0			3.0			3.0			mA
POWER SUPPLY CHARACTERISTICS											
Supply Current, I_{ps} (+)	25°C		6.5	12		6.5	13		7	13	mA
Supply Current, I_{ps} (-)	25°C		4	8		4	8		5	8	mA
Supply Current, I_{ps} (Logic)	25°C		3.5	6		3.5	6		3.5	6	mA
Supply Voltage Range											
V_{Logic} (+) (Note 7)	Full	0		+15.0	0		+15.0	0		+15.0	V
V_{Logic} (-) (Note 7)	Full	-15.0		0	-15.0		0	-15.0		0	V

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Minimum differential input voltage required to ensure a defined output state.
3. Input bias currents are essentially constant with differential input voltages up to ±9 volts. With differential input voltages from ±9 to ±15 volts, bias current on the more negative input can rise to approximately 500 μA.
4. $R_S \leq 200$ ohms; $V_{IN} \leq$ Common Mode Range. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state. This parameter inludes the effects of offset voltage, offset current, common mode rejection, and voltage gain.
5. For $T_{pd}(1)$; 100mV input step, -5mV overdrive. For $T_{pd}(0)$; -100mV input step, 5mV overdrive. Frequency $\approx$ 100Hz; Duty Cycle $\approx$ 50%; Inverting input driven. See Test Circuit below.
6. For V_{OH} and V_{OL}: $I_{Sink} = I_{Source}$ = 3.0mA. For other values of V_{Logic}; V_{OH} (min.) = V_{Logic} + -1.5V.
7. Total Power Dissipation (T. P. D.) is the sum of individual dissipation contributions of V+, V- and V_{Logic} shown in curves of Power Dissipation vs. Supply Voltages (see Performance Curves). The calculated T. P. D. is then located on the graph of Maximum Allowable Package Dissipation vs. Ambient Temperature to determine ambient temperature operating limits imposed by the calculated T. P. D. (See Performance Curves). For instance, the combination of +15V, -15V, +5V, 0V (V+, V-, V_{Logic}+, V_{Logic}-) gives a T.P.D. of 350mW, the combination +15V, -15V, 0V gives a T. P. D. of 450mW.
8. θ_{jA} = 75°C/W
   θ_{jC} = 22°C/W

RESPONSE TIME TEST CIRCUITS



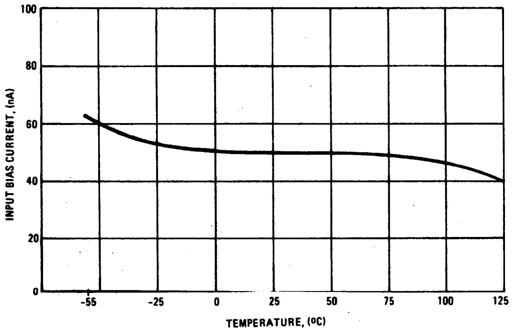


For input and output voltage waveforms for various input overdrives see Performance Curves.

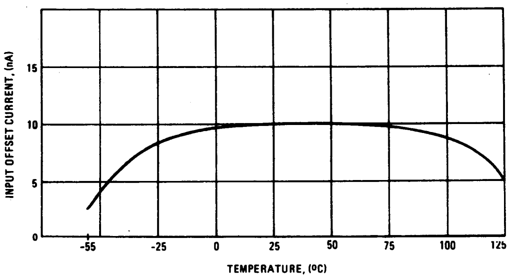
PERFORMANCE CURVES

V+ = 15V, V- = -15V, $V_{Logic}(+)$ = 5.0V, $V_{Logic}(-)$ = 0V, T_A = +25°C, Unless Otherwise Stated.

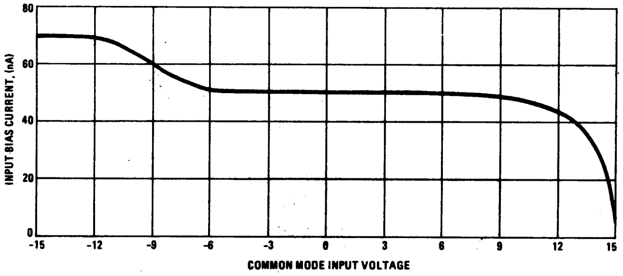
INPUT BIAS CURRENT vs. TEMPERATURE



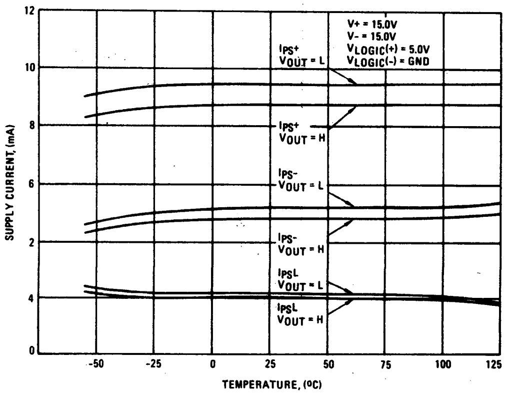
INPUT OFFSET CURRENT vs. TEMPERATURE



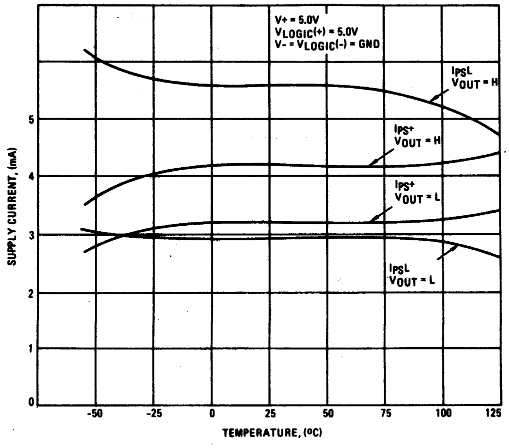
INPUT BIAS CURRENT vs. COMMON MODE INPUT VOLTAGE
($V_{DIFF.}$ = 0V)



SUPPLY CURRENT vs. TEMPERATURE
FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY

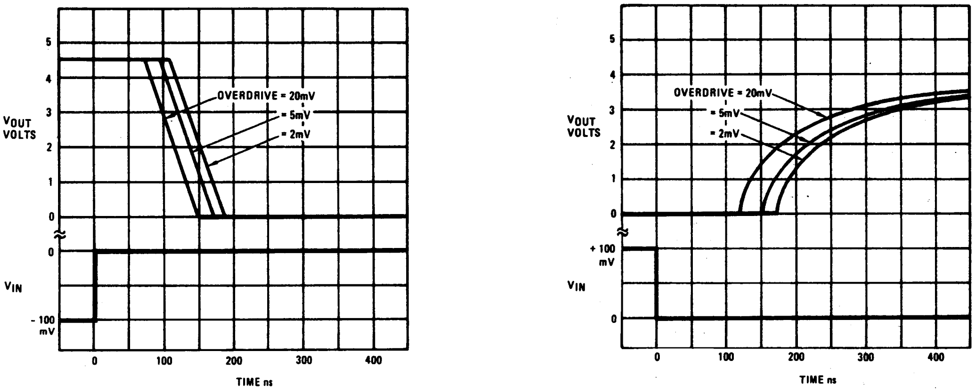


SUPPLY CURRENT vs. TEMPERATURE
FOR SINGLE +5V OPERATION

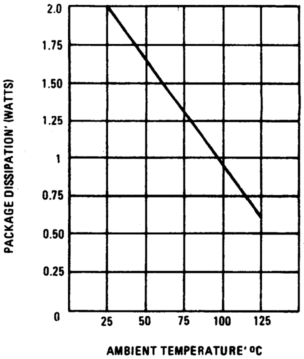


PERFORMANCE CURVES (Continued)

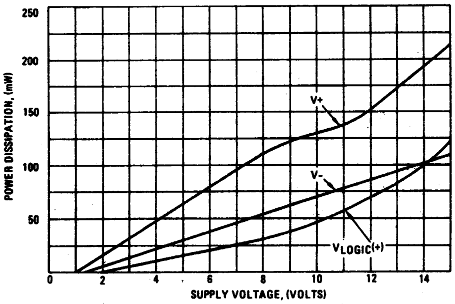
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



MAXIMUM PACKAGE DISSIPATION vs. $T_{AMBIENT}$



MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE (NO LOAD CONDITION)



APPLYING THE HA-4900 SERIES COMPARATORS

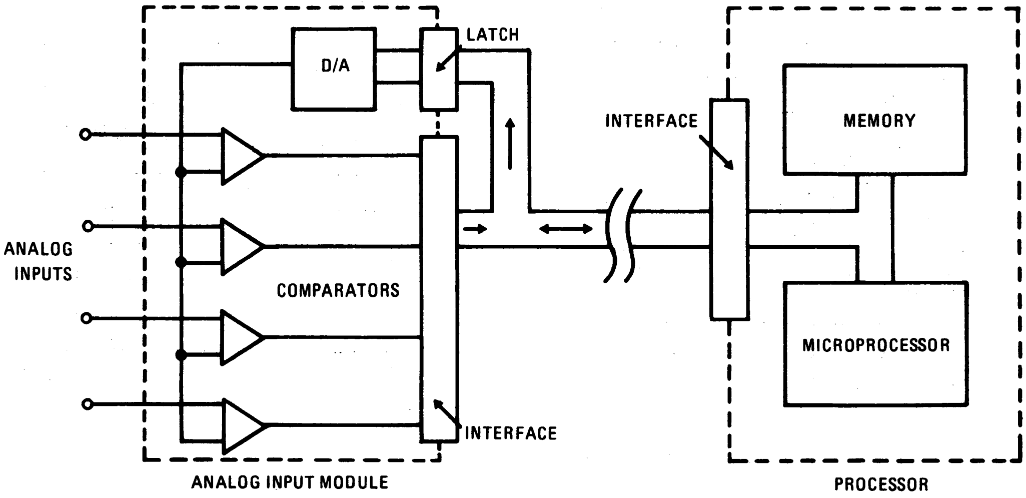
1. SUPPLY CONNECTIONS: This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to $V_{Logic}+$ and $V_{Logic}-$. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_{L-} to a negative supply. Bipolar output swings (15V P-P, max.) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to +15V), V+ and $V_{Logic}+$ may be connected together to the positive supply while V- and $V_{Logic}-$ are grounded. If an input signal could swing negative with respect the V- terminal, a resistor should be connected in series with the input to limit input current to < 5mA since the C-B junction of the input transistor would be forward biased.

2. UNUSED INPUTS: Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter".

3. CROSSTALK: Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

4. POWER SUPPLY DECOUPLING: Decouple all power supply lines with .01 μ F ceramic capacitors to a ground line located near the package to reduce coupling between channnels or from external sources.

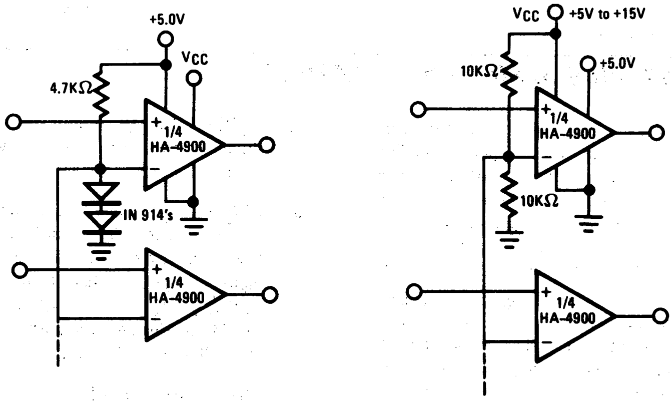
5. RESPONSE TIME: Fast rise time (< 200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.


LATCH
D/A
INTERFACE
MEMORY
ANALOG INPUTS
COMPARATORS
MICROPROCESSOR
INTERFACE
ANALOG INPUT MODULE
PROCESSOR

DATA ACQUISITION SYSTEM

In this circuit the HA-4900 series is used in conjunction with a D to A converter to form a simple, versatile, multi-channel analog input for a data acquisition system. In operation the processor first sends an address to the D to A, then the processor reads the digital word generated by the comparator outputs.

To perform a simple comparison, the processor sets the D to A to a given reference level, then examines one or more comparator outputs to determine if their inputs are above or below the reference. A window comparison consists of two such cycles with 2 reference levels set by the D to A. One way to digitize the inputs would be for the processor to increment the D to A in steps. The D to A address, as each comparator switches, is the digitized level of the input. While stairstepping the D to A is slower than successive approximation, all channels are digitized during one staircase ramp.


+5.0V
VCC
4.7KΩ
+
1/4
HA-4900
−
IN 914's
VCC
+5V to +15V
10KΩ
+5.0V
10KΩ

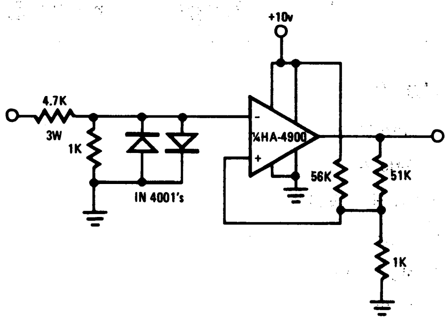
TTL TO CMOS

CMOS TO TTL

LOGIC LEVEL TRANSLATORS

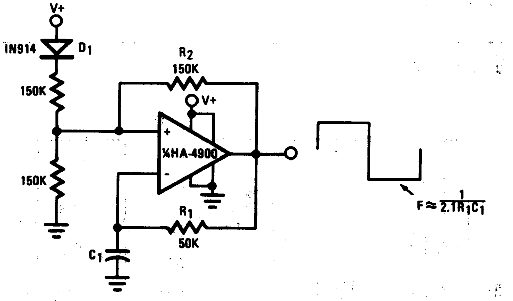
The HA-4900 series comparators can be used as versatile logic interface devices as shown in the circuits above. Negative logic devices may also be interfaced with appropriate supply connections.

If separate supplies are used for V- and V_{Logic-}, these logic level translators will tolerate several volts of ground line differential noise.


+10v
4.7K
3W
1K
IN 4001's
¼HA-4900
56K
51K
1K

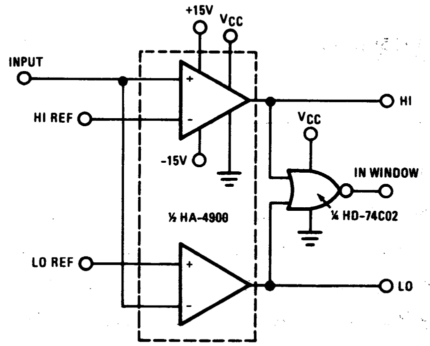
RS-232 TO CMOS LINE RECEIVER

This RS-232 type line receiver to drive CMOS logic uses a Schmitt trigger feedback network to give about 1 volt input hysteresis for added noise immunity. A possible problem in an interface which connects two equipments, each plugged into a different AC receptacle, is that the power line voltage may appear at the receiver input when the interface connection is made or broken. The two diodes and a 3 watt input resistor will protect the inputs under these conditions.


V+
IN914
D1
150K
R2
150K
V+
¼HA-4900
150K
R1
50K
C1
F≈1/(2.1R1C1)

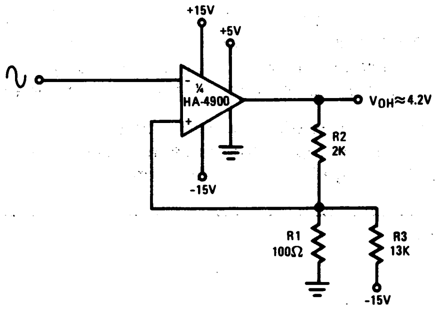
OSCILLATOR/CLOCK GENERATOR

This self-starting fixed frequency oscillator circuit gives excellent frequency stability. R_1 and C_1 comprise the frequency determining network while R_2 provides the regenerative feedback. Diode D_1 enhances the stability by compensating for the difference between V_{OH} and V_{Supply}. In applications where a precision clock generator up to 100kHz is required, such as in automatic test equipment, C_1 may be replaced by a crystal.


+15V
VCC
INPUT
HI REF
-15V
½ HA-4900
LO REF
HI
VCC
IN WINDOW
¼ HD-74C02
LO

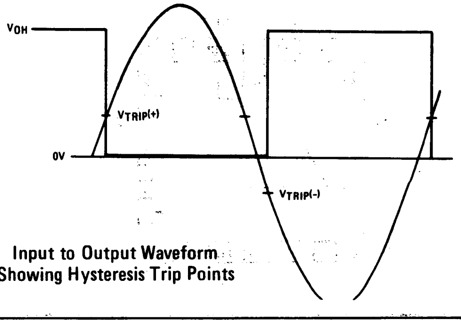
WINDOW DETECTOR

The high switching speed, low offset current and low offset voltage of the HA-4900 series makes this window detector circuit extremely well suited to applications requiring fast, accurate, decision-making. The circuit above is ideal for industrial process system feedback controllers or "out-of-limit" alarm indicators.


+15V
+5V
¼ HA-4900
VOH≈4.2V
R2
2K
-15V
R1
100Ω
R3
13K
-15V

SCHMITT TRIGGER (ZERO CROSSING DETECTOR WITH HYSTERESIS)

This circuit has a 100mV hysteresis which can be used in applications where very fast transition times are required at the output even though the signal input is very slow. The hysteresis loop also reduces false triggering due to noise on the input. The waveforms below show the trip points developed by the hysteresis loop.


VOH
VTRIP(+)
0V
VTRIP(-)

Input to Output Waveform Showing Hysteresis Trip Points

HARRIS

HA-5002

PRELIMINARY

Monolithic, Wideband, High Slew Rate, High Output Current Buffer

Features

- **Voltage Gain 0.995**
- **High Input Impedance .... 3000 KΩ**
- **Low Output Impedance 3Ω**
- **Very High Slew Rate 1300V/μsec**
- **Very Wide Bandwidth 110MHz**
- **High Output Current .... ±200mA**
- **Pulsed Output Current 400mA**
- **Monolithic Construction**

Applications

- **Line Driver**
- **Data Acquisition**
- **110MHz Buffer**
- **High Power Current Booster**
- **High Power Current Source**
- **Sample and Holds**
- **Radar Cable Driver**
- **Video Products**

Description

The HA-5002 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Harris D.I. technologies, the HA-5002 current buffer offers 1300V/μsec slew rate with 110MHz of bandwidth. The ±200mA output current capability is enhanced by a 3 ohm output impedance.

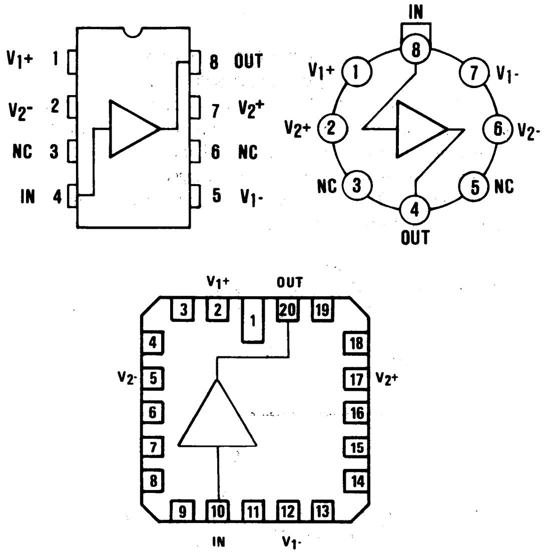
The monolithic HA-5002 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3000K ohm input impedance to the increased output voltage swing. Monolithic design technologies have allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error.

The HA-5002 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

The HA-5002 is available in 8-pin can, 8-pin mini-dip, and 20-pin LCC packages.

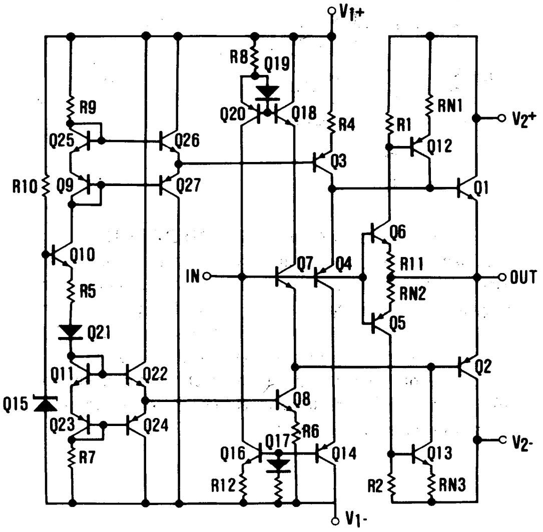
Pinout

TOP VIEWS



V1+ 1
V2- 2
NC 3
IN 4
8 OUT
7 V2+
6 NC
5 V1-
IN 8
V1+ 1
7 V1-
V2+ 2
6 V2-
NC 3
5 NC
4 OUT
V1+ 3 2 1 20 19 OUT
4 18
V2- 5
17 V2+
6 16
7 15
8 14
9 10 11 12 13
IN V1-

Schematic



V1+
R8 Q19
R9
Q20 Q18 R4
Q25 Q26
R1 RN1 Q12 V2+
Q3
R10 Q9 Q27
Q1
Q6
Q10
IN Q7 Q4 R11 OUT
R5 RN2
Q5
Q21
Q11 Q22 Q2
Q15 Q8
Q23 Q24 R6
Q17
R7 Q16 Q14 Q13 V2-
R12 R2 RN3
V1-

Specifications HA-5002

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- pins 44V
Input Voltage .... Equal to Supplies
Output Current .... Continuous ±200mA
Output Current .... (50ms On, 1s Off) ± 400mA
Internal Power Dissipation (Note 2)
TO-99 (+25°C) 1.11W
Mini-DIP (+25°C) 1.87W
LCC (+25°C) 1.51W

Operating Temperature Range

Maximum Junction Temperature .... +175°C
HA-5002-2 .... -55°C ≤ TA ≤ +125°C
HA-5002-5 .... 0°C ≤ TA ≤ +75°C
Storage Temperature Range .... -65°C ≤ TA ≤ +150°C

Electrical Characteristics

V_{SUPPLY} = ± 12V to ± 15V, R_S = 50Ω, R_L = 1KΩ, C_L = 10pF, unless otherwise specified.

PARAMETER	TEMP	−55°C to +125°C			0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		5	20		5	20	mV
	Full		10	30		10	30	mV
Avg. Offset Voltage Drift	Full		10			10		μV/°C
Bias Current	+25°C		2	7		2	7	μA
	Full		3.4	10		2.4	10	μA
Input Resistance	Full	1.5	3		1.5	3		MΩ
Input Noise Voltage (10Hz-1MHz)	+25°C		4			4		μVp-p
TRANSFER CHARACTERISTICS								
Voltage Gain (Note 7)								
R_L = 100Ω	+25°C		0.971			0.971		V/V
R_L = 1KΩ	+25°C		0.995			0.995		V/V
RL = 1KΩ	Full	0.990			0.990			V/V
-3dB Bandwidth (Note 4)	+25°C		110			110		MHz
AC Current Gain	+25°C		40			40		A/mA
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
R_L = 100Ω	+25°C	±10	±10.7		±10	±11.2		V
R_L = 1KΩ (Note 3)	Full	±10	±13.5		±10	±13.9		V
R_L = 1KΩ (Note 5)	Full	±10	±10.5		±10	±10.5		V
Output Resistance	Full		3	10		3	10	Ω
Harmonic Distortion (Note 6)	+25°C		<0.005			<0.005		%
TRANSIENT RESPONSE								
Rise Time	Full			12			12	ns
Rise Time	+25°C		3.6			3.6		ns
Propagation Delay	+25°C		2			2		ns
Overshoot	+25°C		30			30		%
Slew Rate	+25°C	1.0	1.3		1.0	1.3		V/ns
Settling Time to 0.1%	+25°C		50			50		ns
POWER REQUIREMENTS								
Supply Current	+25°C		8.3			8.3		mA
	Full			10			10	mA
Power Supply Rejection Ratio (Note 8)	Full	54			54			dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. HA7- Mini-DIP θ_{JA} = 80°C/W θ_{JC} = 20°C/W
   HA3- Mini-DIP θ_{JA} = 80°C/W θ_{JC} = 20°C/W
   HA2- TO-99 θ_{JA} = 135°C/W θ_{JC} = 41°C/W
   HA4- LCC θ_{JA} = 99°C/W θ_{JC} = 31°C/W
3. V_{SUPPLY} ± 15V
4. V_{IN} 1 V_{RMS}
5. V_{SUPPLY} = ±12V
6. VIN = 1V_{RMS}; f = 10kHz.
7. V_{OUT} = ±10V.
8. ΔV_{SUP} = 10V.

Operating Instructions

Layout Considerations

The wide bandwidth of the HA-5002 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance.

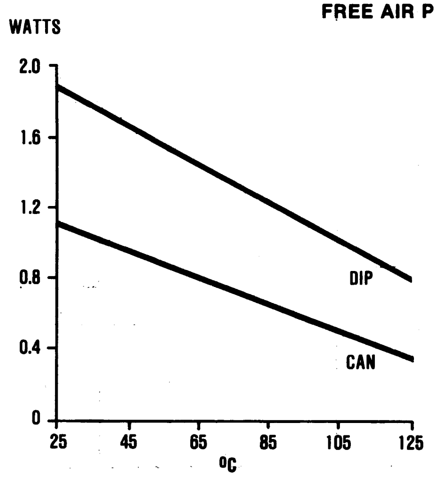
Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimal device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1μF will minimize high frequency variations in supply voltage, while low frequency bypassing requires larger valued capacitors since the impedance of the capacitor is dependent on frequency.

It is also recommended that the bypass capacitors be connected close to the HA-5002 (preferably directly to the supply pins).

**MAXIMUM
FREE AIR POWER DISIPATION**

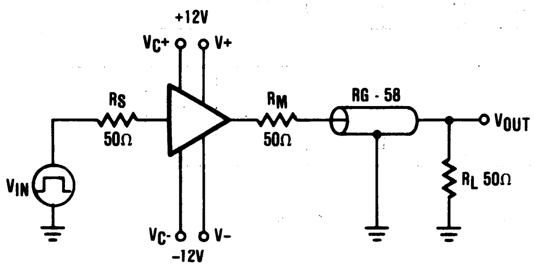


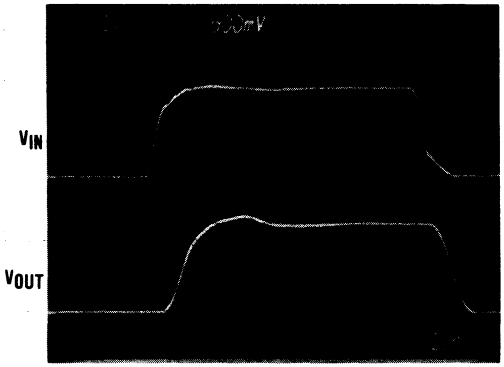
$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j-c} + \theta_{c-s} + \theta_{s-a}}$$

Where: T_{jmax} = Maximum Junction Temperature of the Device
T_A = Ambient
θ_{j-c} = Junction to Case Thermal Resistance
θ_{c-s} = Case to Heat Sink Thermal Resistance
θ_{s-a} = Heat Sink to Ambient Thermal Resistance

Test Circuits

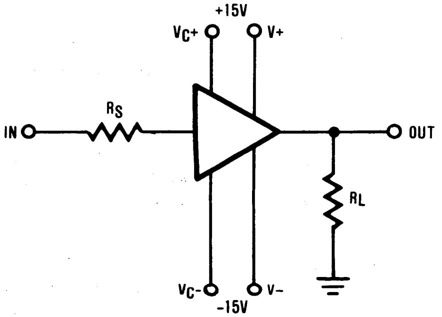
COAXIAL CABLE DRIVER - 50Ω SYSTEM



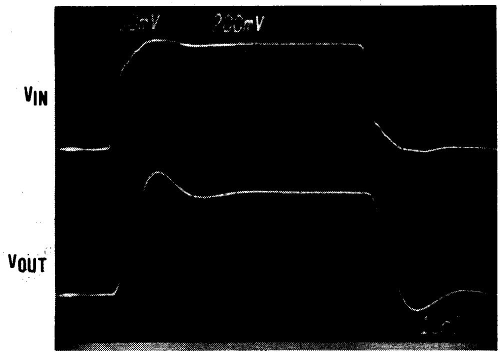


Test Circuits

LARGE AND SMALL SIGNAL RESPONSE

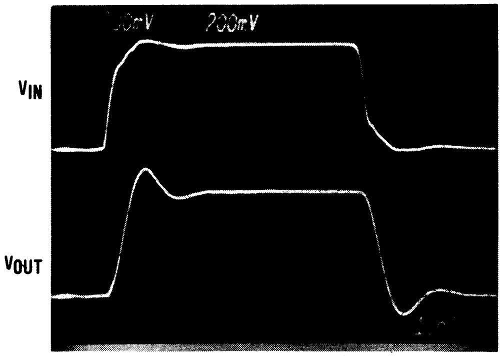


SMALL SIGNAL WAVEFORMS



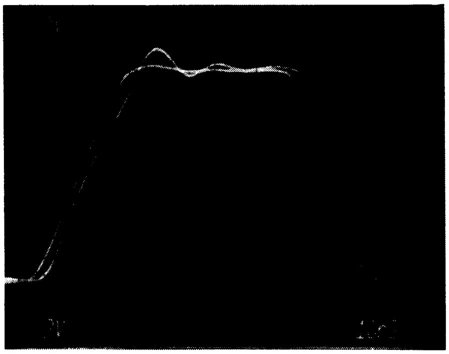
$R_S = 50\Omega$
$R_L = 100\Omega$

SMALL SIGNAL WAVEFORMS



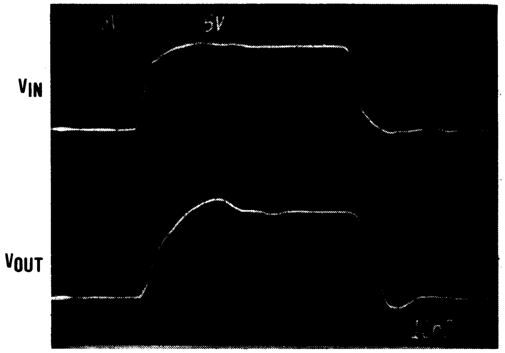
$R_S = 50\Omega$
$R_L = 1K\Omega$

LARGE SIGNAL WAVEFORMS



$R_S = 50\Omega$
$R_L = 1K\Omega$

LARGE SIGNAL WAVEFORMS



$R_S = 50\Omega$
$R_L = 1K\Omega$

HARRIS

HA-5033

Video Buffer

FEATURES

DIFFERENTIAL PHASE ERROR	0.1°
DIFFERENTIAL GAIN ERROR	0.1%
HIGH SLEW RATE (±15V)	1300V/μs
WIDE BANDWIDTH (SMALL SIGNAL)	250MHz
WIDE POWER BANDWIDTH	DC to 65MHz
FAST RISE TIME	3ns
HIGH OUTPUT DRIVE	±10V WITH 100Ω LOAD
WIDE POWER SUPPLY RANGE	±5V TO ±16V
REPLACE COSTLY HYBRIDS	

APPLICATIONS

- VIDEO BUFFER
- HIGH FREQUENCY BUFFER
- ISOLATION BUFFER
- HIGH SPEED LINE DRIVER
- IMPEDANCE MATCHING
- CURRENT BOOSTERS
- HIGH SPEED A/D INPUT BUFFERS

DESCRIPTION

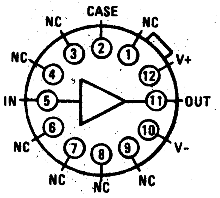
The HA-5033 is a unity gain monolithic I. C. designed for any application requiring a fast, wideband buffer. Featuring a bandwidth of 250MHz and outstanding differential phase/gain characteristics, this high performance voltage follower is an excellent choice for video circuit design. Other features, which include a minimum slew rate of 1000V/μs and high output drive capability, make the HA-5033 applicable for line driver and high speed data conversion circuits.

The high performance of this product is a result of the Harris Dielectric Isolation process. A major feature of this process is that it produces both PNP and NPN high frequency transistors which makes wide bandwidth designs, such as the HA-5033, practical. Alternative process methods typically produce PNP transistors of lower frequency response, which results in a lower AC performance.

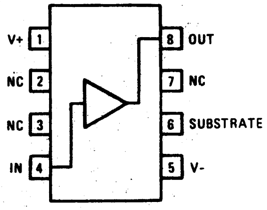
The HA-5033 is available in a 12 pin (TO-8) metal can or an 8 pin epoxy mini-dip. The HA-5033-2 is specified over the military temperature range of -55°C to +125°C. The HA-5033-5 is specified over the commercial temperature range of 0°C to +75°C.

PINOUTS

TOP VIEWS

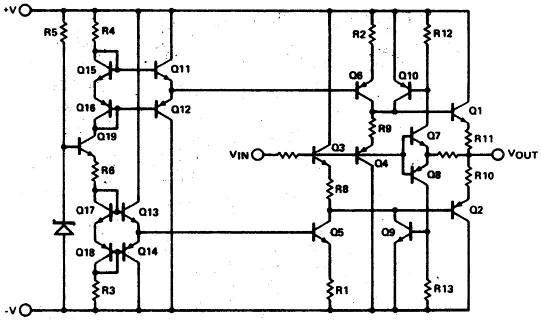

CASE
NC
NC
NC
V+
IN
OUT
NC
V-
NC
NC
NC
1
2
3
4
5
6
7
8
9
10
11
12

METAL CAN PACKAGE


V+ 1
NC 2
NC 3
IN 4
8 OUT
7 NC
6 SUBSTRATE
5 V-

MINI-DIP

SCHEMATIC


+V
-V
R5
R4
R2
R12
Q15
Q11
Q16
Q12
Q19
Q6
Q10
Q1
R9
Q7
R11
VIN
Q3
Q4
Q8
R10
VOUT
R6
R8
Q17
Q13
Q2
Q5
Q9
Q18
Q14
R3
R1
R13

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- pins	40V
Input Voltage	Equal to Supplies
Output Current (Peak)	±200mA
Internal Power Dissipation (Note 2)	
TO-8 (+25°C)	1.75W
Mini-dip (+25°C)	1.95W

Maximum Junction Temperature	200°C
Operating Temperature Range HA-5033-2	-55°C≤T_A≤+125°C
HA-5033-5	0°C≤T_A≤+75°C
Storage Temperature Range	-65°C≤T_A≤+150°C

ELECTRICAL CHARACTERISTICS

V_{SUPPLY} = ±12V, R_S = 50Ω, R_L = 100Ω, C_L = 10pF, unless otherwise specified.

PARAMETER	TEMP	-55°C TO +125°C			0°C TO +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		5	15		5	15	mV
	Full		6	25		6	25	mV
Average Offset Voltage Drift	Full		33			33		µV/°C
Bias Current	+25°C		20	35		20	35	µA
	Full		30	50		30	50	µA
Input Resistance	+25°C		1.5			1.5		MΩ
Input Capacitance	+25°C		1.6			1.6		pF
Input Noise Voltage (Note 3)	+25°C		20			20		µVp-p
TRANSFER CHARACTERISTICS								
Voltage Gain R_L = 100Ω	+25°C	.93			.93			V/V
R_L = 1KΩ	+25°C		.99			.99		V/V
R_L = 100Ω	Full	.92			.92			V/V
-3dB Bandwidth	+25°C		250			250		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
R_L = 100Ω	Full		±10			±10		V
R_L = 1KΩ (Note 4)	Full		±11			±11		V
Output Current	+25°C		±100			±100		mA
Output Resistance	+25°C		5			5		Ω
Full Power Bandwidth (Note 5)	+25°C		65			65		MHz
TRANSIENT RESPONSE								
Rise Time (Note 6)	+25°C		3			3		ns
Propagation Delay	+25°C		1			1		ns
Overshoot	+25°C		10			10		%
Slew Rate (Note 7)	+25°C	1.0	1.3		1.0	1.3		V/ns
Settling Time to .1%	+25°C		50			50		ns
Differential Phase Error } (Note 8)	+25°C		.1			.1		degrees
Differential Gain Error	+25°C		.1			.1		%
POWER REQUIREMENTS								
Supply Current	+25°C		21	25		21	25	mA
	Full		21	30		21	30	mA
Power Supply Rejection Ratio	Full	54			54			dB
Harmonic Distortion (Note 9)	+25°C		<0.1			<0.1		%

NOTES

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. TO-8: θ_{JA} = 99°C/W, θ_{JC} = 31°C/W

   Recommended Heat Sinks for the TO-8:
   Thermalloy 2240A, θ_{SA} = 27°C/W
   IERC Up-T08-48CB, θ_{SA} = 10°C/W

   Mini-dip: θ_{JA} = 90°C/W θ_{JC} = 27°C/W
3. 10Hz to 1MHz
4. $\pm V_{SUPPLY} \pm 15V$.
5. $V_O = 1\ V_{RMS}$, $R_L = 1K\Omega$
6. V_O = 500mV
7. $\pm V_{SUPPLY} = \pm 15V$, $V_O = \pm 10V$, $R_L = 1K\Omega$.
8. Differential gain and phase error are non-linear signal distortions found in video systems and are defined as follows:

   Differential Gain error is defined as the change in amplitude at the color subcarrier frequency as the picture signal is varied from blanking to white level.

   Differential Phase error is defined as the change in the phase of the color subcarrier as the picture signal is varied from blanking to white level.

   Differential gain and phase error were too small to be measured with a Tektronix 520A NTSC Vector Scope.
9. $V_{IN} = 1\ V_{RMS}$

OPERATING INSTRUCTIONS

LAYOUT CONSIDERATIONS

The wide bandwidth of the HA-5033 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance. This ground plane shielding can also incorporate the metal case of the HA-5033 since pin # 2 is internally tied to the package. This feature allows the user to make metal to metal contact between the ground plane and the package, which extends shielding, provides additional heat sinking and eliminates the use of a socket, IC sockets contribute inter-lead capacitance which limits device bandwidth and should be avoided.

For the epoxy mini-dip, pin 6 can be tied to either supply, grounded, or simply not used. But to optimize device performance and improve isolation, it is recommended that this pin be grounded.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

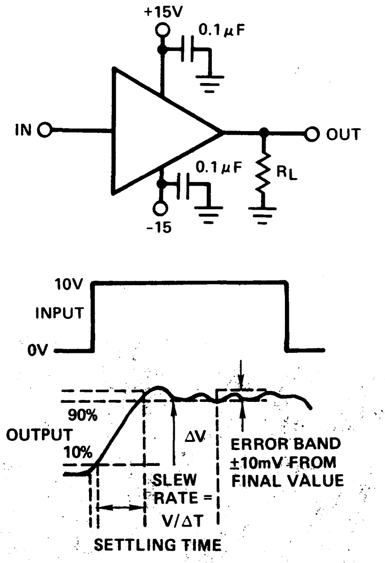
POWER SUPPLY DECOUPLING

For optimum device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from .01 to .1 μF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1μF or larger will optimize low frequency performance.

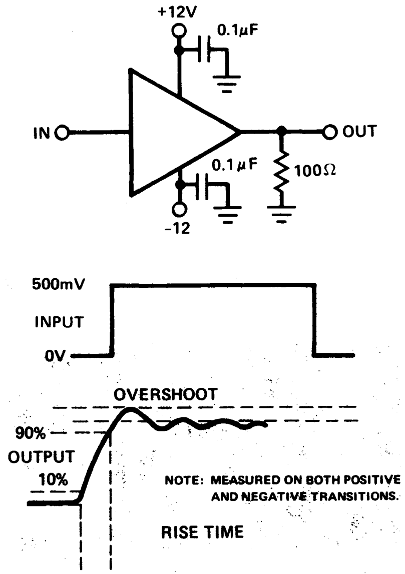
It is also recommended that the bypass capacitors be connected close to the HA-5033 (preferably directly to the supply pins).

TEST CIRCUITS

SLEW RATE AND SETTLING TIME

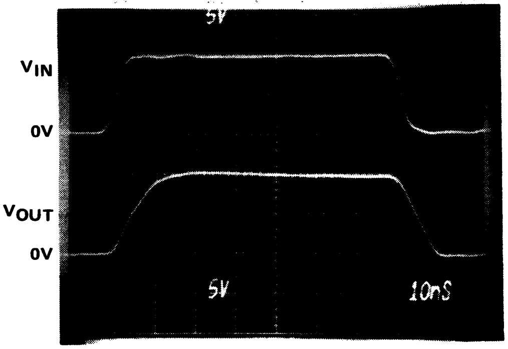

+15V
0.1µF
IN
OUT
0.1µF
R_L
-15
10V
INPUT
0V
90%
OUTPUT
10%
ΔV
ERROR BAND
±10mV FROM
FINAL VALUE
SLEW
RATE =
V/ΔT
SETTLING TIME

TRANSIENT RESPONSE

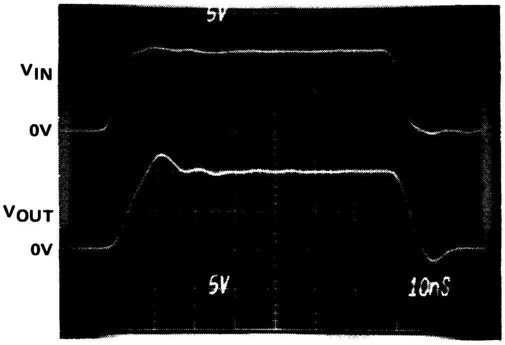

+12V
0.1µF
IN
OUT
0.1µF
100Ω
-12
500mV
INPUT
0V
OVERSHOOT
90%
OUTPUT
10%
RISE TIME

NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

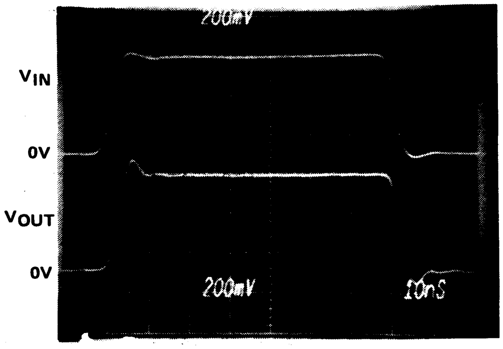
+10V RESPONSE
$T_A = 25^oC$, $R_S = 50\Omega$, $R_L = 100\Omega$

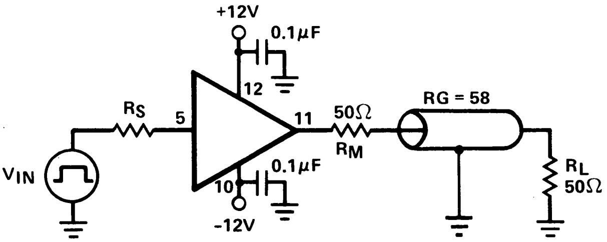


+10V RESPONSE
$T_A = 25^oC$, $R_S = 50\Omega$, $R_L = 1K\Omega$

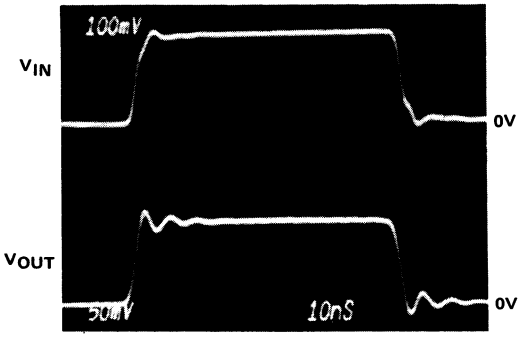


+0.5V PULSE RESPONSE
$T_A = 25^oC$, $R_S = 50\Omega$, $R_L = 100\Omega$



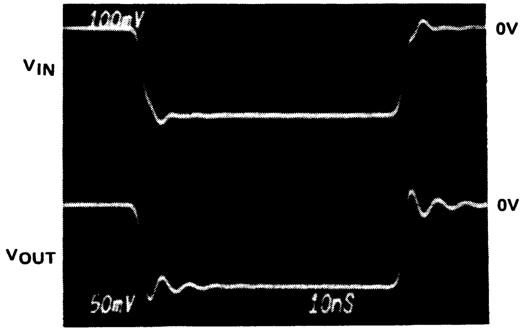

+12V
0.1μF
12
RS
5
11
50Ω
RM
RG = 58
VIN
10
0.1μF
-12V
RL
50Ω

APPLICATION 1. VIDEO COAXIAL LINE DRIVER - 50Ω SYSTEM



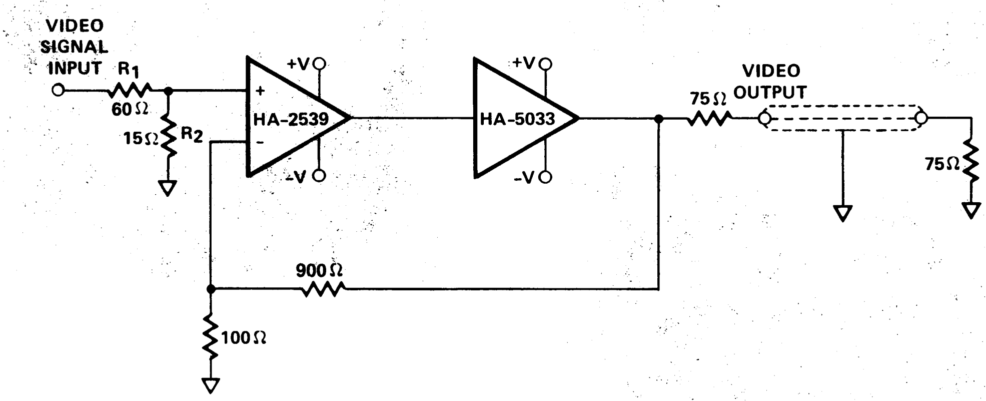
POSITIVE PULSE RESPONSE

$T_A = +25^{o}C$
$R_S = 50\Omega$
$R_M = R_L = 50\Omega$
$$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = 1/2\ V_{IN}$$



NEGATIVE PULSE RESPONSE

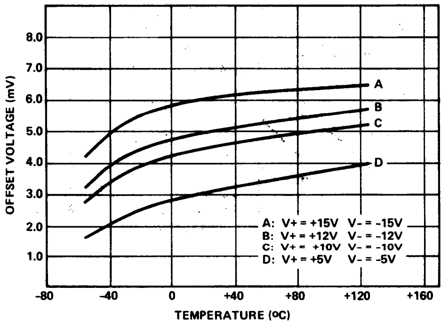
$T_A = +25^{o}C$
$R_S = 50\Omega$
$R_M = R_L = 50\Omega$
$$V_O = -V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = 1/2\ VIN$$


VIDEO
SIGNAL
INPUT
R1
60Ω
15Ω
R2
+
-
HA-2539
+V
-V
HA-5033
+V
-V
75Ω
VIDEO
OUTPUT
75Ω
900Ω
100Ω

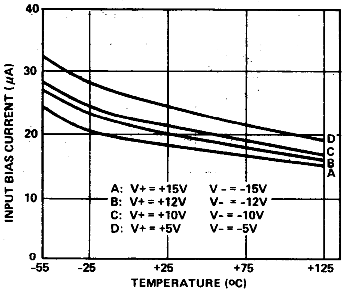
APPLICATION 2. VIDEO GAIN BLOCK

PERFORMANCE CURVES

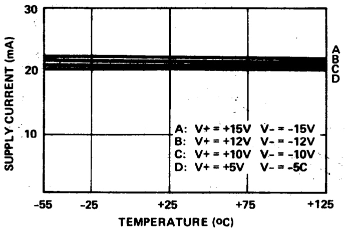
INPUT OFFSET VOLTAGE VS. TEMPERATURE VS. SUPPLY VOLTAGE



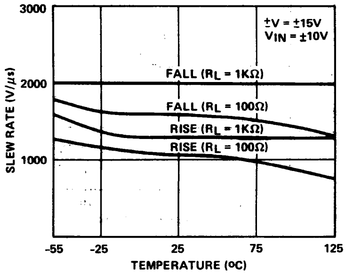
INPUT BIAS CURRENT VS. TEMPERATURE VS. SUPPLY VOLTAGE



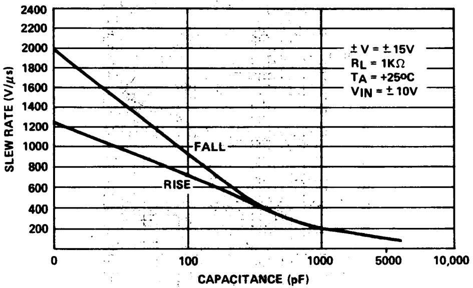
SUPPLY CURRENT VS. TEMPERATURE VS. SUPPLY VOLTAGE



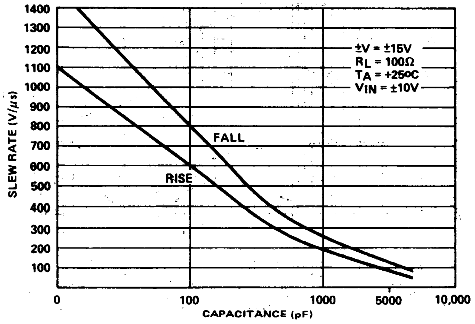
SLEW RATE VS. TEMPERATURE



SLEW RATE VS. LOAD CAPACITANCE ($R_L = 1K\Omega$)

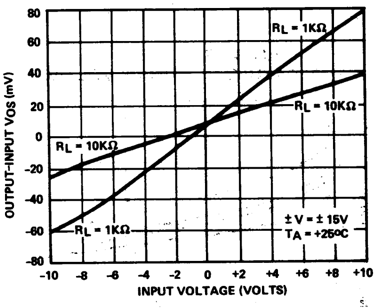


SLEW RATE VS. LOAD CAPACITANCE ($R_L = 100\Omega$)

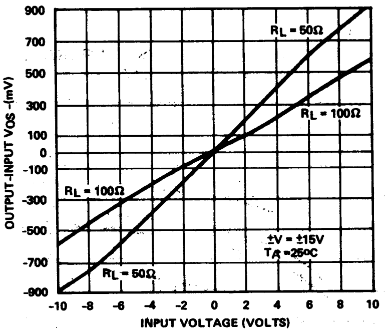


PERFORMANCE CURVES (Continued)

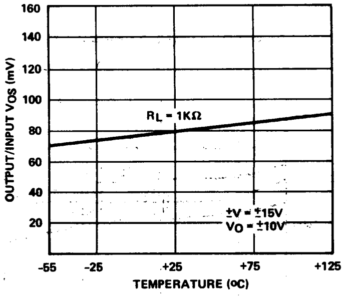
GAIN ERROR VS. INPUT VOLTAGE



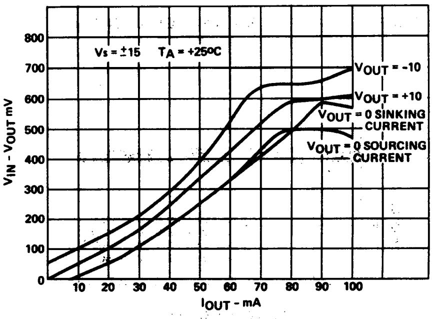
GAIN ERROR VS. INPUT VOLTAGE



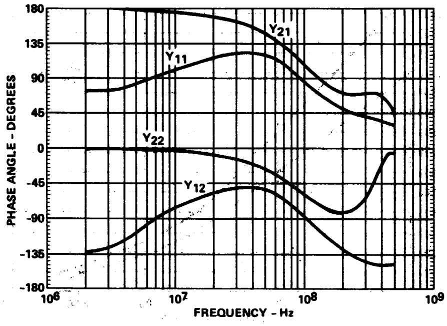
GAIN ERROR VS.TEMPERATURE



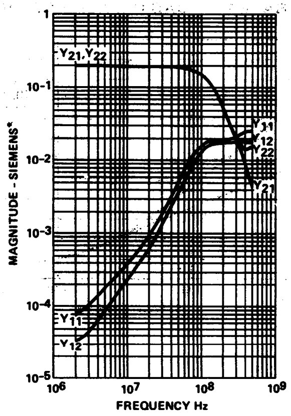
VIN-VOUT VS. IOUT



Y–PARAMETERS PHASE VS. FREQUENCY



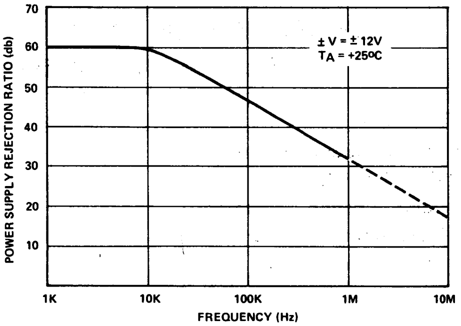
Y–PARAMETER MAGNITUDE VS. FREQUENCY



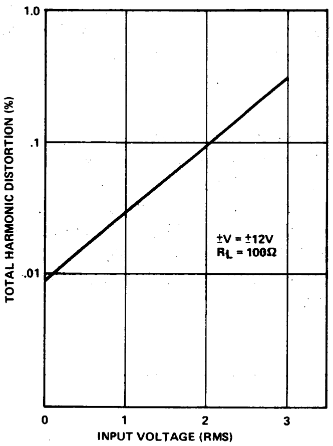
*SIEMENS = Ω^{-1}

PERFORMANCE CURVES (Continued)

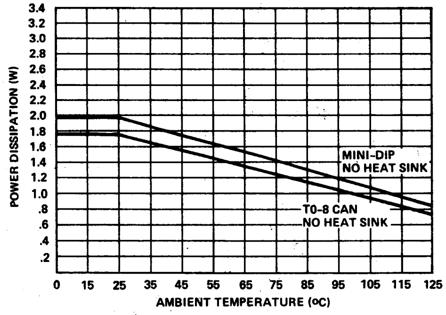
POWER SUPPLY REJECTION RATIO VS. FREQUENCY



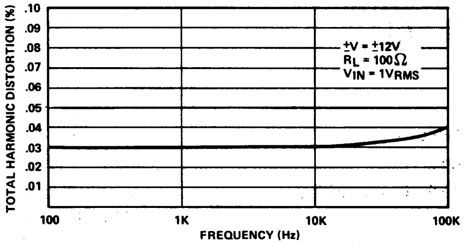
TOTAL HARMONIC DISTORTION VS. RMS INPUT VOLTAGE



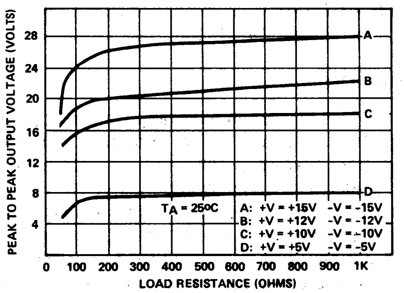
MAXIMUM POWER DISSIPATION VS. AMBIENT TEMPERATURE



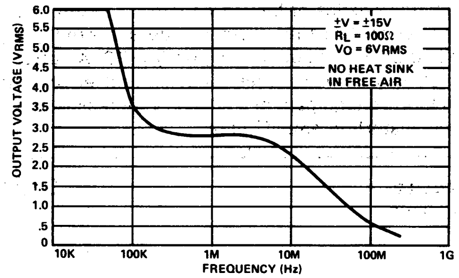
TOTAL HARMONIC DISTORTION VS. FREQUENCY



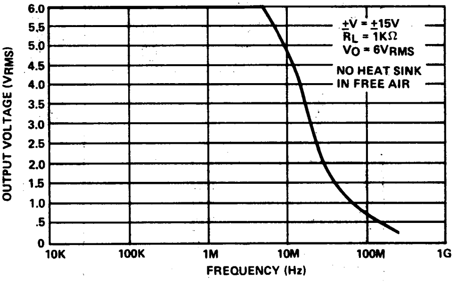
OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE VS. SUPPLY VOLTAGE



OUTPUT SWING VS. FREQUENCY*



OUTPUT SWING VS. FREQUENCY*



*This curve was obtained by noting the output voltage necessary to produce an observable distortion for a given frequency. If higher distortion is acceptable, then a higher output voltage for a given frequency can be obtained.

However, operating the HA-5033 with increased distortion (to the right of curve shown), will also be accompanied by an increase in supply current. The resulting increase in chip temperature must be considered and heat sinking will be necessary to prevent thermal runaway.

This characteristic is the result of the output transistor operation. If the signal amplitude or signal frequency or both are increased beyond the curve shown, the NPN, PNP output transistors will approach a condition of being simultaneously on. Under this condition, thermal runaway can occur.

HARRIS HA-5101/5111

ADVANCE

Low Noise, High Performance Operational Amplifiers

Features

- **Low Noise .... 3.5nV/√Hz at 1KHz**
- **Wide Bandwidth .... 10MHz (Comp.)**
  60MHz (Uncomp.)
- **High Slew Rate .... 10V/μs (Comp.)**
  30V/μs (Uncomp.)
- **Low Offset Voltage Drift .... 3μV/°C**
- **High Gain .... 6 x 10^6V/V**
- **High CMRR/PSRR 100dB**
- **High Output Drive Capability 30mA**

Applications

- **High Quality Audio Preamplifiers**
- **High Q Active Filters**
- **Low Noise Function Generators**
- **Low Distortion Oscillators**
- **Low Noise Comparators**

Description

The HA-5101/5111 are dielectrically isolated operational amplifiers featuring low noise and high performance. Both amplifiers have an excellent noise voltage density of 3.5nV/√Hz at 1KHz. The uncompensated HA-5111 is stable at a minimum gain of ten and has the same DC specifications as the unity gain stable HA-5101. The difference in compensation yields a 60MHz gain-bandwidth product and a 30V/μs slew rate for the HA-5111 versus a 10MHz unity gain bandwidth and a 10V/μs slew rate for the HA-5101.

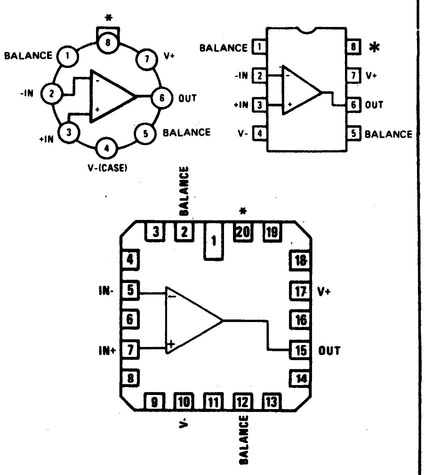
DC characteristics of the HA-5101/5111 assure accurate performance. The 1mV offset voltage is externally adjustable and offset voltage drift is just 3μV/°C. An offset current of only 30nA reduces input current errors and an open loop voltage gain of 6 x 10^6V/V increases loop gain for low distortion amplification.

The HA-5101/5111 are ideal for audio applications, especially low-level signal amplifiers such as microphone, tape head, and phono cartridge preamplifiers. Additionally, it is well suited for low distortion oscillators, low noise function generators, and high Q filters.

The HA-5101/5111-2 has guaranteed operation from -55°C to +125°C and can be ordered as a military grade part (HA-5101/5111-8). The HA-5101/5111-5 has guaranteed operation from 0°C to 75°C. All devices are available in ceramic mini DIP and TO-99 can packages. Additionally, the HA-5101/5111-8 is available in a 20 pin LCC package and the HA-5101/5111-5 is available in a plastic mini DIP package.

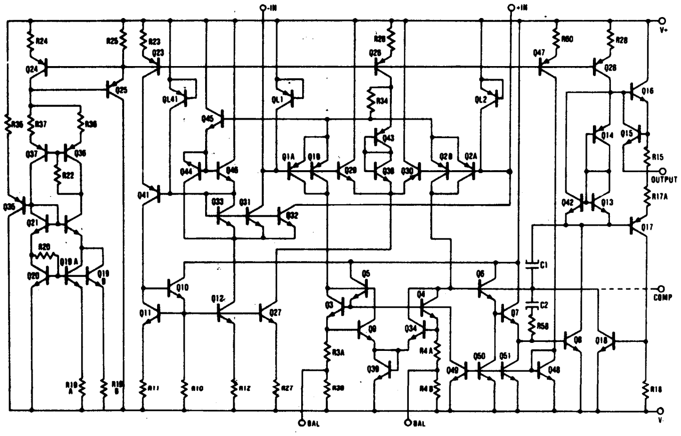
Pinouts

TOP VIEWS


*
BALANCE
1
2
-IN
3
+IN
4
V- (CASE)
5
BALANCE
6
OUT
7
V+
8
BALANCE 1
-IN 2
+IN 3
V- 4
8 *
7 V+
6 OUT
5 BALANCE
BALANCE
*
3
2
1
20
19
4
IN- 5
6
IN+ 7
8
18
17 V+
16
15 OUT
14
9
10
11
12
13
V-
BALANCE

* HA-5101 NC/HA-5111 Compensation

Schematic


-IN
+IN
V+
V-
OUTPUT
COMP
BAL
BAL
C1
C2
R15
R17A
R18
Q16
Q17
Q14
Q15
Q13
Q42
Q28
Q47
R60
R28

HARRIS

PRELIMINARY

HA-5102/04/12/14

Low Noise High Performance Operational Amplifiers

FEATURES

LOW NOISE	4.3 nV/√Hz
WIDE BANDWIDTH	8MHz (COMP.) 60MHz (UNCOMP.)
HIGH SLEW RATE	3V/µs (COMP.) 20V/µs (UNCOMP.)
LOW OFFSET VOLTAGE	0.5mV
SINGLE SUPPLY OPERATION	
AVAILABLE IN DUALS OR QUADS	

APPLICATIONS

- HIGH Q, ACTIVE FILTERS
- AUDIO AMPLIFIERS
- INSTRUMENTATION AMPLIFIERS
- INTEGRATORS
- SIGNAL GENERATORS

DESCRIPTION

Low noise and high performance are key words describing HA-5102/04/12/14. These general purpose amplifiers offer an array of dynamic specifications ranging from 3V/µs slew rate and 8MHz bandwidth (5102/04) to 20V/µs slew rate and 60MHz gain-bandwidth-product (HA-5112/14). Complementing these outstanding parameters is a very low noise specification of 4.3 nV/√Hz at kHz.

Fabricated using the Harris standard high frequency process, these operational amplifiers also offer excellent input specifications such as 0.5mV offset voltage and 30nA offset current. Complementing these specifications are 108dB open loop gain and 108dB channel separation. Consuming a very modest amount of power (90mW/package for duals and 150mW/package for quads), HA-5102/04/12/14 also provide the flexibility of operating from a single +5V supply.

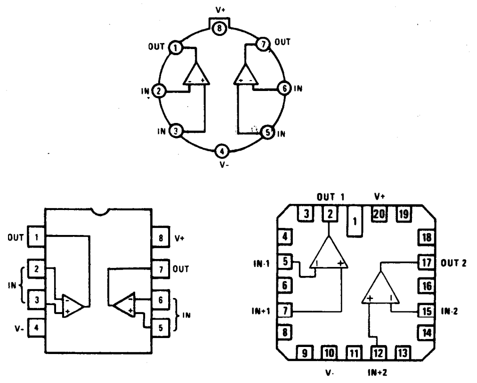
This impressive combination of features make this series of amplifiers ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

These operational amplifiers are available in dual or quad form with industry standard pinouts allowing for immediate interchangeability with most other dual and quad operational amplifiers.

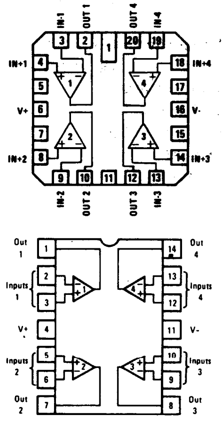
HA-5102	Dual, Compensated
HA-5112	Dual, Uncompensated
HA-5104	Quad, Compensated
HA-5114	Quad, Uncompensated

PINOUTS

TOP VIEWS



HA-5102/12



HA-5104/14

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated		Power Dissipation (Note 4)	880mW
Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±7V	HA-5102/5104/5112/5114-2	$-55°C \leq T_A \leq +125°C$
Input Voltage (Note 2)	±15.0V	HA-5102/5104/5112/5114-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration (Note 3)	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC

		HA-5102-2 HA-5112-2 -55°C to +125°C			HA-5104-2 HA-5114-2 -55°C to +125°C			HA-5102-5 HA-5112-5 0°C to +75°C			HA-5104-5 HA-5114-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	+25°C		0.5	2.0		0.5	2.5		0.5	2.0		0.5	2.5	mV
	Full			2.5			3.0			2.5			3.0	mV
Offset Voltage Average Drift	Full		3			3			3			3		μV/°C
Bias Current	+25°C		130	200		130	200		130	200		130	200	nA
	Full			325			325			325			325	nA
Offset Current	+25°C		30	75		30	75		30	75		30	75	nA
	Full			125			125			125			125	nA
Input Resistance	+25°C		500			500			500			500		kΩ
Common Mode Range	Full	±12			±12			±12			±12			V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 5)	+25°C													
	Full	100K	250K		100K	250K		100K	250K		100K	250K		V/V
Common Mode Rejection Ratio (Note 6)	Full	86			86			86			86			dB
Small Signal Bandwidth	+25°C													
HA-5102/5104			8			8			8			8		MHz
Gain Bandwidth Product	+25°C													
HA-5112/5114 A_V = 10			60			60				60		60		MHz
Channel Separation (Note 7)	+25°C		108			108			108			108		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		±10	±12		±10	±12		V
Output Current (Note 8)	Full	±10	±15		±10	±15		±10	±15		±10	±15		mA
Full Power Bandwidth														
(Note 9) HA-5102/5104	+25°C		50			50			50			50		kHz
HA-5112/5114	+25°C		250			250			250			250		kHz
Output Resistance	+25°C		110			110			110			110		Ω

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC

		HA-5102-2 HA-5112-2 -55°C to +125°C			HA-5104-2 HA-5114-2 -55°C to +125°C			HA-5102-5 HA-5112-5 0°C to +75°C			HA-5104-5 HA-5114-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TRANSIENT RESPONSE (Note 10)														
Rise time														
HA-5102/5104	+25°C		50	100		50	100		50	100		50	100	ns
HA-5112/5114	+25°C		38	60		38	60		38	60		38	60	ns
Overshoot														
HA-5102/5104	+25°C		20	35		20	35		20	35		20	35	%
HA-5112/5114	+25°C		30	40		30	40		30	40		30	40	%
Slew Rate														
HA-5102/5104	+25°C	±1	±3		±1	±3		±1	±3		±1	±3		V/μs
HA-5112/5114	+25°C	±12	±20		±12	±20		±12	±20		±12	±20		V/μs
Settling Time (Note 11)														
HA-5102/5104	+25°C		4.5			4.5			4.5			4.5		μs
HA-5112/5114	+25°C		0.6			0.6			0.6			0.6		μs
NOISE CHARACTERISTICS														
Input Noise Voltage	+25°C													
f = 10Hz			17			17			17			17		nV/√Hz
f = 1KHz			4.3			4.3			4.3			4.3		nV/√Hz
Input Noise Current	+25°C													
f = 10Hz			5.1			5.1			5.1			5.1		pA/√Hz
f = 1KHz			.57			.57			.57			.57		pA/√Hz
Broadband Noise Voltage	+25°C													
f = DC to -30KHz			870			870			870			870		nVrms
POWER SUPPLY CHARACTERISTICS														
Supply Current														
HA-5102/5112	+25°C		3.0	5.0		3.0	5.0		3.0	5.0		3.0	5.0	mA
HA-5104/5114	+25°C		5.0	6.5		5.0	6.5		5.0	6.5		5.0	6.5	mA
Power Supply Rejection Ratio (Note 6)	Full	86			86			86			86			dB

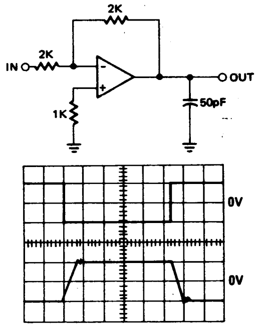
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages < ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V, R_L = 2K .
6. V = ±5.0V.
7. Channel separation value is refferred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak to peak; R_S = 1KΩ. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
8. Output current is measured with V_{OUT} = ±5V.
9. Full power bandwidth is guaranteed by equation:

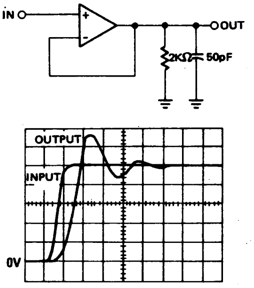
   $$\text{Full power bandwidth} = \frac{\text{Slew Rate}}{2\pi V\ \text{Peak}}$$
10. Refer to Test Circuits section of the data sheet.
11. Setting time is measured to 0.1% of final value for a 1 volt input step, and A_V = -10 for HA-5112/5114 and 0.1% of final value for a 10 volt input step, A_V = -1 for HA-5102/5104.

TEST CIRCUITS

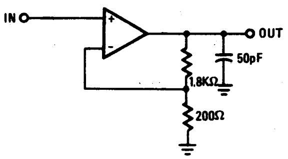
LARGE SIGNAL RESPONSE CIRCUIT
(Volts: 5V/Div., Time: 5µs/Div.)
HA-5102/5104

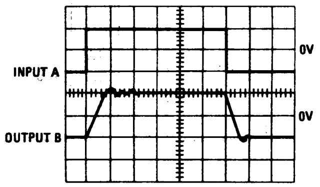


SMALL SIGNAL RESPONSE CIRCUIT
(Volts: 10mV/Div., Time: 50ns/Div.)
HA-5102/5104

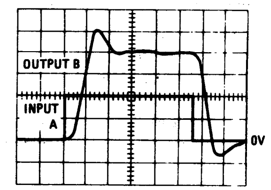


LARGE AND SMALL SIGNAL RESPONSE CIRCUIT
HA-5112/5114



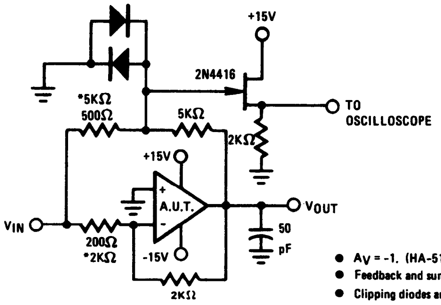


VOLTS: Input A: .5V/Div., Output B: 5V/Div.
TIME: 500ns/Div.



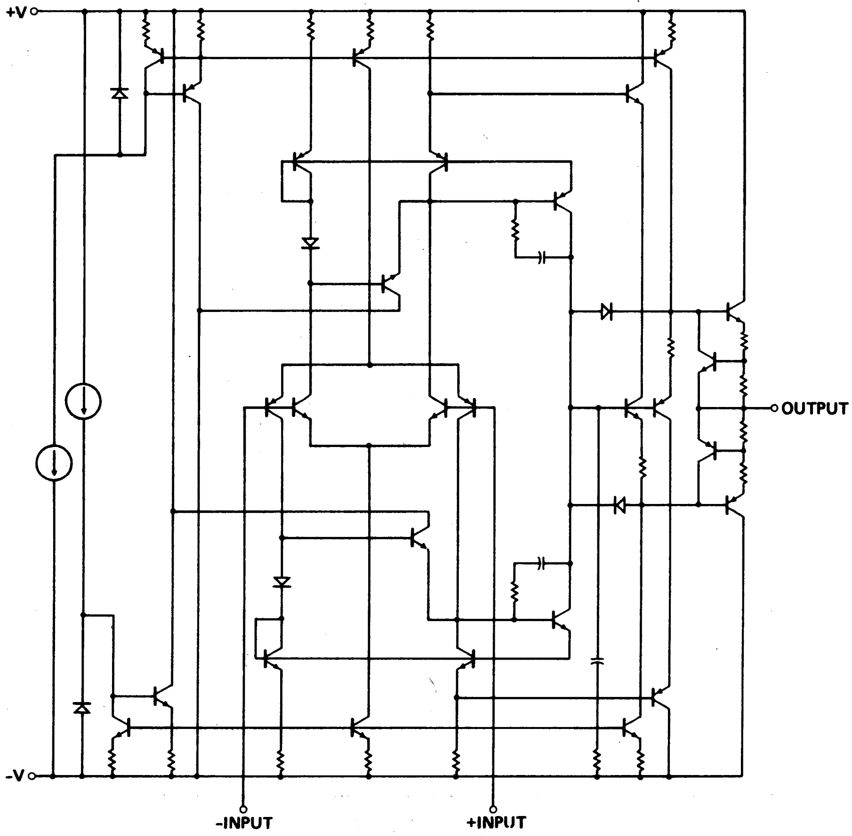
VOLTS: Input A: .01V/Div., Output B: 50mV/Div.
TIME: 50ns/Div.

SETTLING TIME CIRCUIT



- A_V = -1. (HA-5102/5104), $*A_V$ = -10 (HA-5112/5114)
- Feedback and summing resistors should be 0.1%
- Clipping diodes are optional HP5082-2810 recommended.

SCHEMATIC


+V
-V
OUTPUT
-INPUT
+INPUT

HARRIS

HA-5130/35

Precision Operational Amplifier

FEATURES

• LOW OFFSET VOLTAGE	10μV
• LOW OFFSET VOLTAGE DRIFT	0.4μV/°C
• LOW NOISE	9nV/$\sqrt{\text{Hz}}$
• OPEN LOOP GAIN	10^7
• BANDWIDTH (UNITY GAIN)	2.5MHz
• ALL BIPOLAR CONSTRUCTION	

APPLICATIONS

- HIGH GAIN INSTRUMENTATION
- PRECISION DATA ACQUISITION
- PRECISION INTEGRATORS
- BIOMEDICAL AMPLIFIERS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

HA-5130/5135 are precision operational amplifiers manufactured using a combination of key technological advancements to provide outstanding input characteristics.

A Super Beta input stage is combined with laser trimming, dielectric isolation, and matching techniques to produce 25μV (Max.) input offset voltage and 0.4μV/°C input offset voltage average drift. Other features enhanced by this process include 9nV (Typ.) Input Noise Voltage, 1nA Input Bias Current, and 140dB Open Loop Gain.

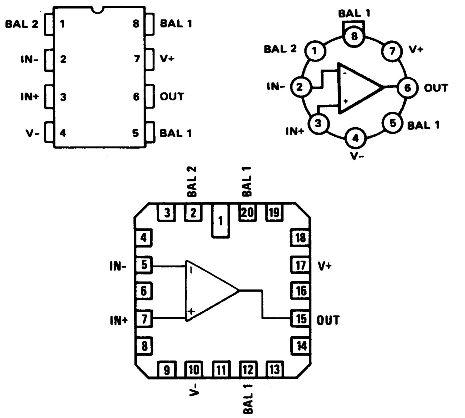
These features coupled with 120dB CMRR and PSRR make HA-5130/5135 an ideal device for precision DC instrumentation amplifiers. Excellent input characteristics in conjunction with 2.5MHz bandwidth and 0.8V/μs slew rate, makes this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

HA-5130/35 is packaged in an 8 pin (TO-99) can and an 8 lead Cerdip and is pin compatible with many existing op amp configurations. The HA-5135 is also available in a 20 pin LCC.

HA-5130/5135-2 is specified for -55°C to +125°C operation while HA-5130/5135-5 operate from 0°C to +75°C.

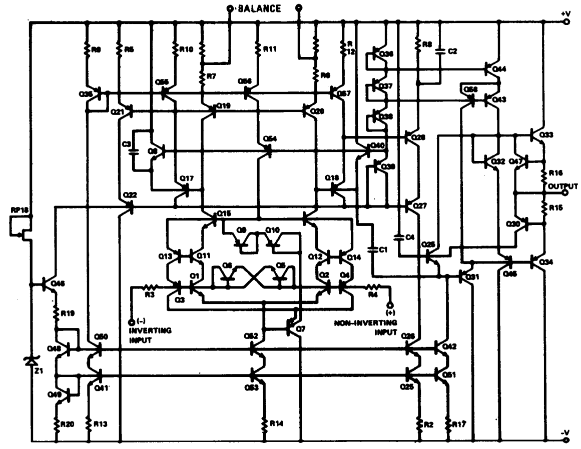
PINOUTS

TOP VIEWS


BAL 2
1
8
BAL 1
IN-
2
7
V+
IN+
3
6
OUT
V-
4
5
BAL 1
BAL 1
8
BAL 2
1
7
V+
IN-
2
6
OUT
IN+
3
5
BAL 1
4
V-
BAL 2
BAL 1
3
2
1
20
19
4
18
IN-
5
17
V+
6
16
IN+
7
15
OUT
8
14
9
10
11
12
13
V-
BAL 1

(BOTH BAL 1 PINS ARE INTERNALLY CONNECTED)

SCHEMATIC


BALANCE
+V
OUTPUT
(-) INVERTING INPUT
(+) NON-INVERTING INPUT
-V

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated		Power Dissipation (Note 2)	300mW
Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	± 15.0V	HA-5130/5135-2	$-55°C \leq T_A \leq +125°C$
		HA-5130/5135-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V

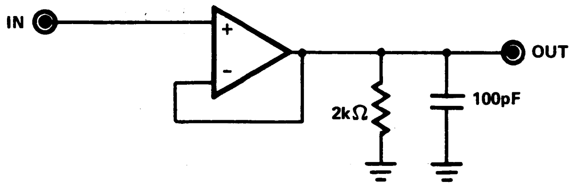
PARAMETER	TEMP.	HA-5130-2/-5 MIN.	HA-5130-2/-5 TYP.	HA-5130-2/-5 MAX.	HA-5135-2/-5 MIN.	HA-5135-2/-5 TYP.	HA-5135-2/-5 MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		10	25		10	75	µV
	Full		50	60		50	130	µV
Average Offset Voltage Drift	Full		0.4	0.6		0.4	1.3	µV/°C
Bias Current	+25°C		± 1	± 2		± 1	± 4	nA
	Full			± 4			± 6	nA
Bias Current Average Drift	Full		0.02	0.04		0.02	0.04	nA/°C
Offset Current	+25°C			2			4	nA
	Full			4			5.5	nA
Offset Current Average Drift	Full		0.02	0.04		0.02	0.04	nA/°C
Common Mode Range	Full	± 12			± 12			V
Differential Input Resistance	+25°C	20	30		20	30		MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 3)	+25°C			0.6			0.6	μV_{p-p}
Input Noise Voltage Density (Note 3)	+25°C							$nV/\sqrt{Hz}$
f_0 = 10Hz			13.0	18.0		13.0	18.0	
f_0 = 100Hz			10.0	13.0		10.0	13.0	
f_0 = 1000Hz			9.0	11.0		9.0	11.0	
Input Noise Current (Note 3) 0.1Hz to 10Hz	+25°C		15	30		15	30	pA_{p-p}
Input Noise Current Density (Note 3)	+25°C							$pA/\sqrt{Hz}$
f_0 = 10Hz			0.4	0.8		0.4	0.8	
f_0 = 100Hz			0.17	0.23		0.17	0.23	
f_0 = 1000Hz			0.14	0.17		0.14	0.17	
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	120	140		120	140		dB
	Full	120			120			dB
Common Mode Rejection Ratio (Note 5)	Full	110	120		106	120		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	0.6	2.5		0.6	2.5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	± 10	± 12		± 10	± 12		V
	Full	± 10			± 10			V
Full Power Bandwidth (Note 7)	+25°C	8	10		8	10		kHz
Output Current (Note 8)	+25°C	±15	±20		±15	±20		mA
Output Resistance (Note 9)	+25°C		45			45		Ω
TRANSIENT RESPONSE (Note 10)								
Rise Time	+25°C		340			340		ns
Slew Rate	+25°C	0.5	0.8		0.5	0.8		V/µs
Settling Time (Note 11)	+25°C		11			11		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		1.0	1.3		1.0	1.7	mA
Power Supply Rejection Ratio (Note 12)	Full	100	130		94	130		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temp.'s above +75°C.
3. Not tested. 90% of units meet or exceed these specifications.
4. $V_{OUT} = \pm 10V$; $R_L = 2k$. Gain dB = 20 $\log_{10}$ Average
   ∴ 120dB = 1000V/mV
   140dB = 10,000V/mV
5. $V_{CM} = \pm 10V$ DC
6. $R_L = 600\Omega$
7. R_L = 2k; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{SLEW RATE}}{2\pi V_{PEAK}}$
8. V_{OUT} = 10V
9. Output resistance measured under open loop conditions (f = 100Hz)
10. Refer to test circuits section of the data sheet.
11. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
12. $V_{SUPP} = \pm 5V$ DC to $\pm 20V$ DC.

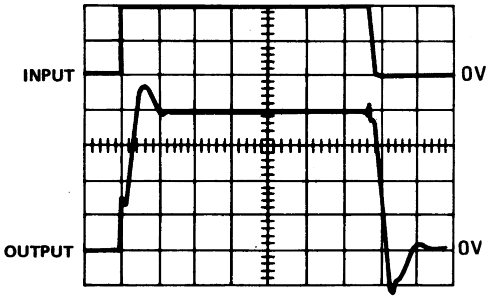
TEST CIRCUITS

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT


IN
+
-
OUT
2kΩ
100pF

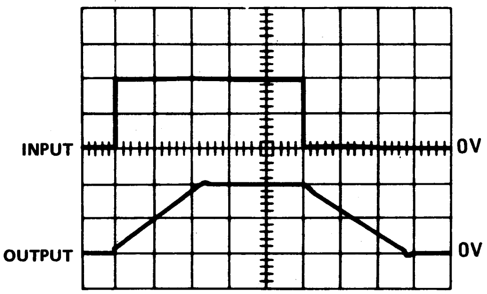
SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: 50mV/Div. Output)
(Volts: 100mV/Div. Input)
Horizontal Scale: (Time: 1μs/Div.)

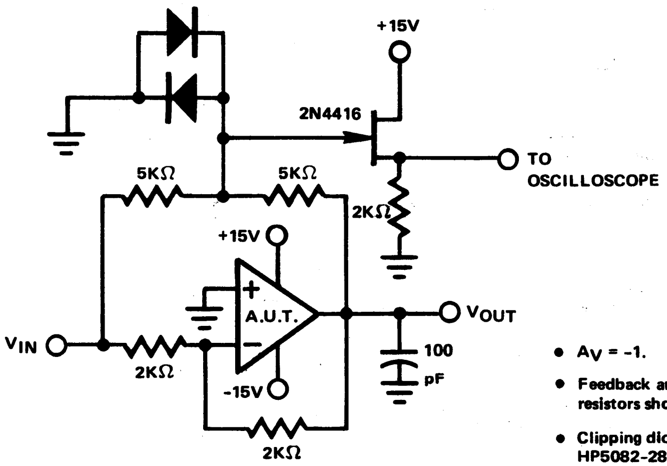


LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: 5V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



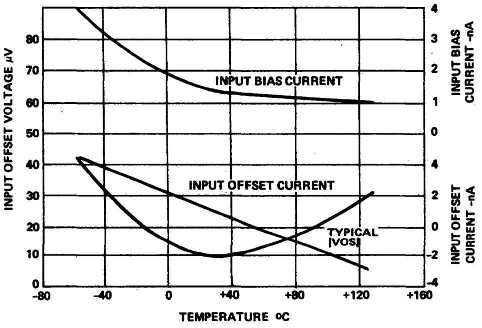
SETTLING TIME CIRCUIT


+15V
2N4416
TO OSCILLOSCOPE
5KΩ
5KΩ
2KΩ
+15V
+
A.U.T.
-
VOUT
VIN
2KΩ
-15V
100 pF
2KΩ

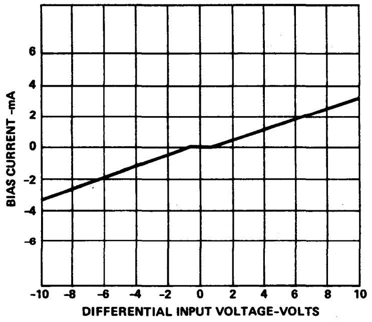
- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

PERFORMANCE CURVES

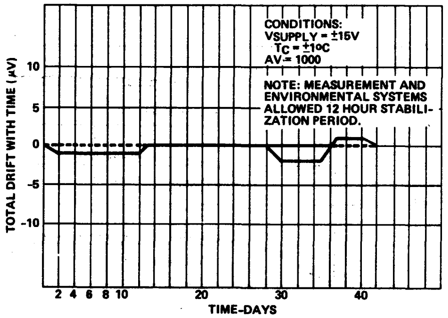
INPUT OFFSET VOLTAGE, INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



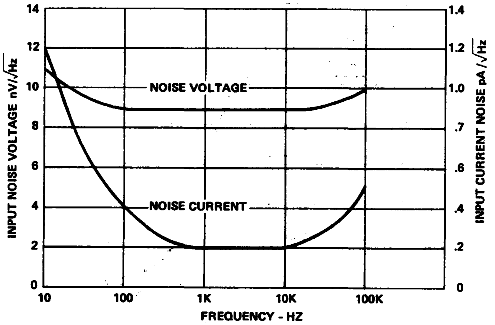
INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



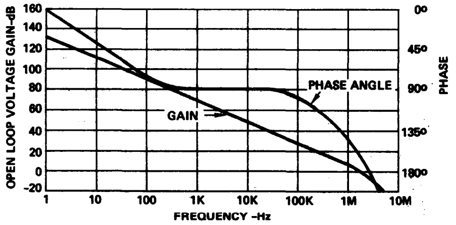
HA-5130 OFFSET VOLTAGE STABILITY vs. TIME



INPUT NOISE vs. FREQUENCY

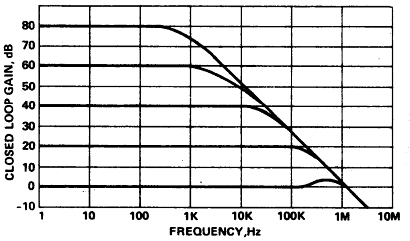


OPEN LOOP FREQUENCY RESPONSE

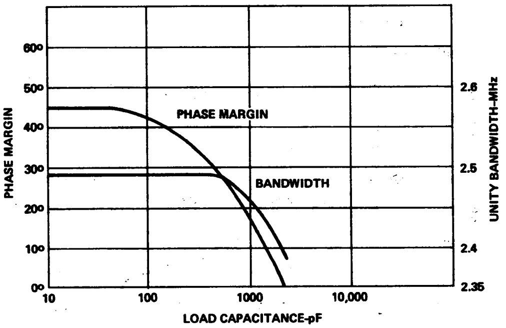


PERFORMANCE CURVES (Continued)

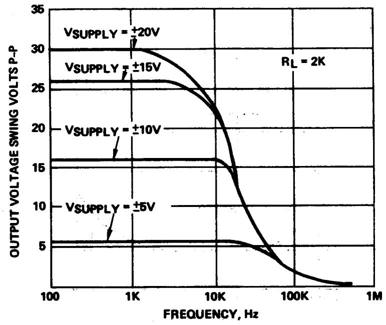
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



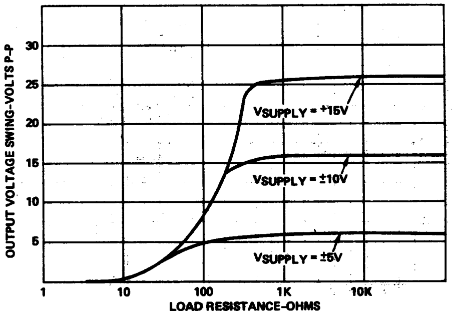
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



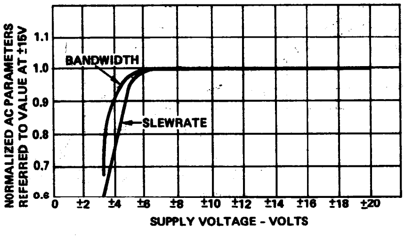
OUTPUT VOLTAGE SWING vs. FREQUENCY AND SUPPLY VOLTAGE



MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE AND SUPPLY VOLTAGE

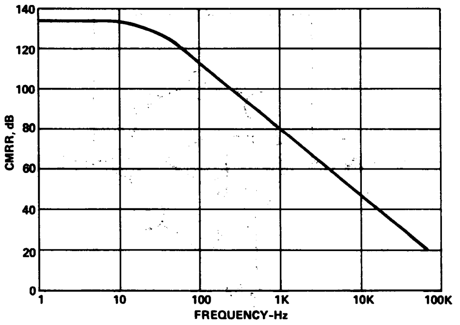


NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE

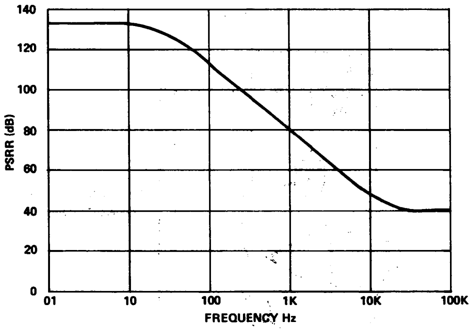


PERFORMANCE CURVES (Continued)

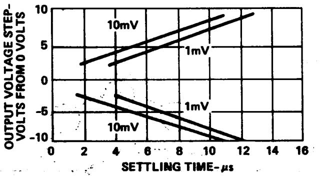
CMRR vs. FREQUENCY



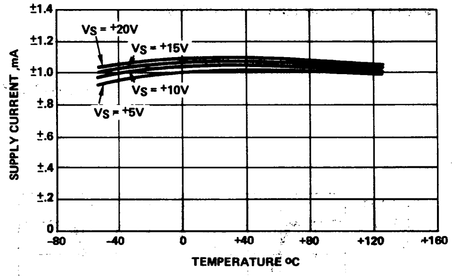
PSRR vs. FREQUENCY



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE



APPLYING THE HA-5130/5135 OPERATIONAL AMPLIFIERS

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. CONSIDERATIONS FOR PROTOTYPING: The following list of recommendations are suggested for prototyping.
   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces, and implementation of moisture barriers when required is suggested.
   - Error voltages generated by theromocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuitry from heat generating components is recommended.
   - Shielded cable input leads, guard rings, and shield drivers are recommended for the most critical applications.

3. When driving large capacitive loads (> 500pF), as small value resistor (≈50 Ω) should be connected in series with the output and inside the feedback loop.

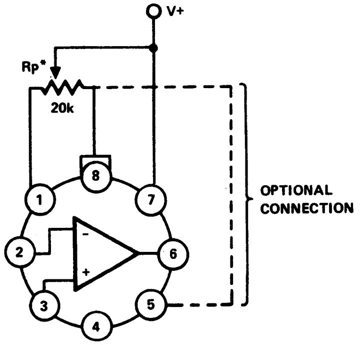
4. OFFSET VOLTAGE ADJUSTMENT: A 20 KΩ balance potentiometer is recommended if offset nulling is required. However, other potentiometer values such as 10KΩ, 50KΩ, and 100KΩ may be used. The minimum adjustment range for given values is ±2mV.

5. SATURATION RECOVERY: Input and output saturation recovery time is negligible in most applications. However, care should be exercised to avoid exceeding the absolute maximum ratings of the device.

6. DIFFERENTIAL INPUT VOLTAGES: Inputs are shunted with back-to-back diodes for overvoltage protection. In applications where differential input voltages in excess of IV are applied between the inputs, the use of limiting resistors at the inputs is recommended.

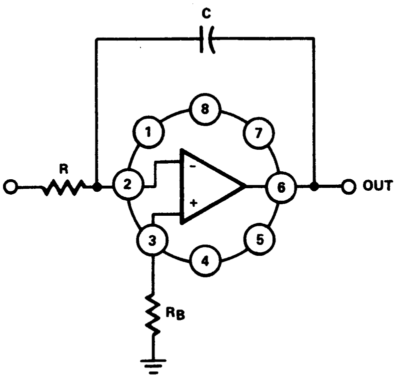
APPLICATIONS

OFFSET NULLING CONNECTIONS


V+
Rp*
20k
OPTIONAL CONNECTION
1
2
3
4
5
6
7
8
-
+

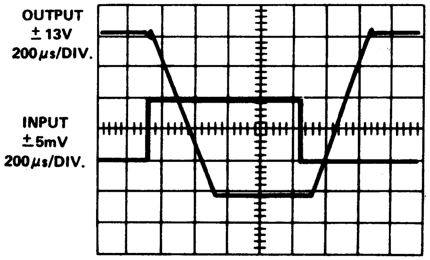
*Although Rp is shown equal to 20k, other values such as 50k, 100k, and 1M may be used. Range of adjustment is approximately ±2.5mV. V_{OS} TC of the amplifier is optimized at minimal V_{OS}.

PRECISION INTEGRATOR

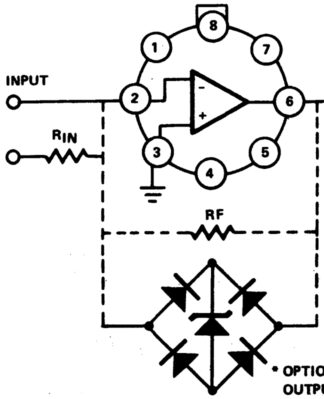

C
R
OUT
R_B
1
2
3
4
5
6
7
8
-
+

The excellent input and gain characteristics of HA-5130 are well suited for precision integrator applications. Accurate integration over seven decades of frequency using HA-5130, virtually nullifies the need for more expensive chopper-type amplifiers.

ZERO CROSSING DETECTOR

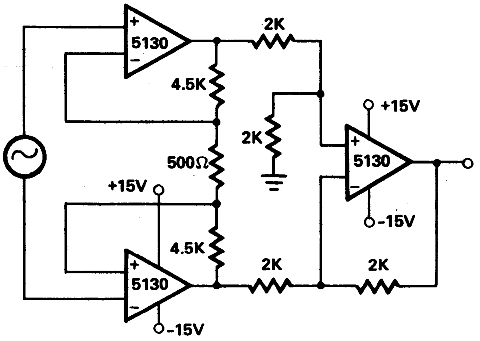


Low V_{OS} coupled with high open loop Gain, high CMRR, and high PSRR make HA-5130 ideally suited for precision detector applications.


INPUT
R_{IN}
RF
1
2
3
4
5
6
7
8
-
+

* OPTIONAL FOR OUTPUT SWING LIMITING

PRECISION INSTRUMENTATION AMPLIFIER (A_V = 100)


5130
5130
5130
+
-
2K
2K
2K
2K
4.5K
4.5K
500Ω
+15V
-15V
+15V
-15V

HARRIS

HA-5134

ADVANCED

Precision Quad Operational Amplifier

Features

- **Low Offset Voltage .... Typ 25μV**
- **Low Offset Voltage Drift .... Max 5μV/$^{\circ}$C**
- **Offset Voltage Match .... Full Temp. Max 250μV**
- **High Channel Separation 120dB**
- **Low Noise .... 7nV/$\sqrt{\text{Hz}}$**
- **Wider Bandwidth 4MHz**
- **High CMRR/PSRR 120dB**
- **Dielectric Isolation**

Applications

- **Instrumentation Amplifiers**
- **State-Variable Filters**
- **Precision Integrators**
- **Threshold Detectors**
- **Precision Data Acquisition Systems**
- **Low-Level Transducer Amplifiers**

Description

The HA-5134 is a precision quad operational amplifier that is pin compatible with the LT1014, OP11, RM4156, and LM148 as well as the HA-4741. Each amplifier features guaranteed maximum values for offset voltage of 250μV, offset voltage drift of 5μV/$^{\circ}$C, and offset current of 25nA over the full military temperature range while CMRR/PSRR is guaranteed greater than 94dB and A_{VOL} is guaranteed above 250K V/V from -55°C to +125°C.

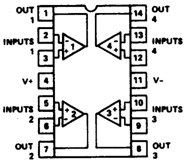
Precision performance of the HA-5134 is enhanced by a noise voltage density of 7nV/$\sqrt{\text{Hz}}$ at 1KHz, noise current density of 2pA/$\sqrt{\text{Hz}}$ at 1KHz and channel separation of 120dB. Each unity-gain stable quad amplifier is fabricated using the dielectric isolation process to assure performance in the most demanding applications.

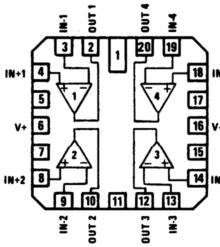
The HA-5134 is ideal for compact circuits such as instrumentation amplifiers, state-variable filters, and low-level transducer amplifiers. Other applications include precision data acquisition, precision integrators, and accurate threshold detectors in designs where board space is a limitation.

The HA-5134-2 has guaranteed operation from -55°C to +125°C and can be ordered as a military grade part (HA-5134-8). The HA-5134-5 is guaranteed from 0°C to +75°C and all devices are available in ceramic dual-in-line packages. The HA-5134-8 is also available in a 20 pin leadless chip carrier (LCC) package.

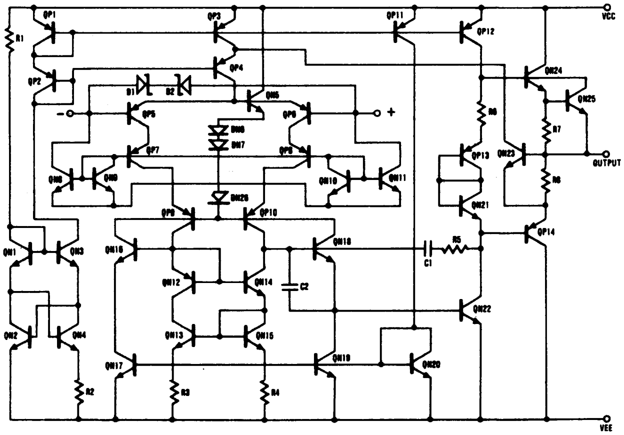
Pinouts

TOP VIEWS


OUT 1
INPUTS 1
V+
INPUTS 2
OUT 2
OUT 4
INPUTS 4
V-
INPUTS 3
OUT 3
1
2
3
4
5
6
7
8
9
10
11
12
13
14


IN-1
OUT 1
OUT 4
IN-4
IN+1
V+
IN+2
IN+4
V-
IN+3
IN-2
OUT 2
OUT 3
IN-3
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20

Schematic


QP1
QP2
R1
QP3
QP4
D1
D2
QN5
QP5
QP6
DN6
DN7
QP7
QP8
QN8
QN9
QN10
QN11
DN26
QP9
QP10
QN1
QN2
QN3
QN4
QN16
QN12
QN13
QN14
QN15
QN17
QN18
QN19
QN20
C1
C2
R2
R3
R4
R5
R6
R7
R8
QP11
QP12
QP13
QP14
QN21
QN22
QN23
QN24
QN25
VCC
OUTPUT
VEE
-
+

HA-5141/42/44

Ultra-Low Power Operational Amplifiers

Features

- Low Supply Current .... $45\mu A$/AMP
- Wide Operating Voltage Range .... 2V to 3V
- Single or Dual Supply Operation
- High Slew Rate .... $1.5V/\mu s$
- High Gain 100kV/V
- Unity Gain Stable
- "A" Suffix Devices Combine the Above Characteristics with Percision Input Specifications
- Available in Singles, Duals and Quads

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Instrumentation

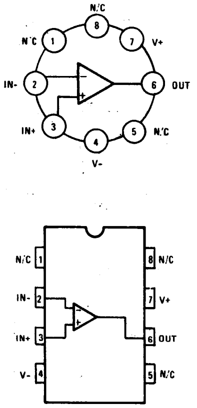
Description

The HA-5141/42/44 ultra-low power operational amplifiers provide AC and DC performance characteristics similar to or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. These amplifiers are well suited to applications which require low power dissipation and good electrical characteristics.

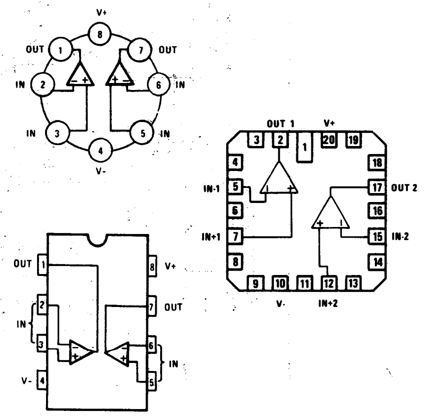
The HA-5141/42/44 provides accurate signal processing by virtue of their low input offset voltage (0.5mV), low input bias current (45nA), high open loop gain (100kV/V) and low noise, for low power operational amplifiers ($20nV/\sqrt{Hz}$). These characteristics coupled with a $1.5/\mu s$ slew rate and a 400kHz bandwidth make the HA-5141/42/44 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (2V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment.

These amplifiers are available in singles (HA-5141, can or Mini-Dip), duals (HA-5142, Can Mini-Dip or 20 pin LCC) or quads (HA-5144, 14 pin Dip or 20 pin LCC) with industry standards pinouts which allow the HA-5141/5142/5144's to be interchangeable with most other operational amplifiers.

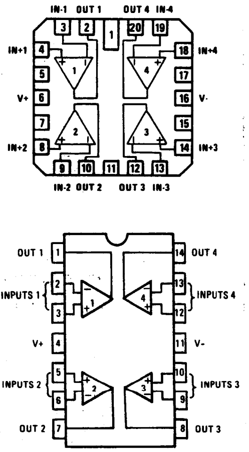
TOP VIEWS


N/C
N/C
V+
IN-
OUT
IN+
N/C
V-
1
2
3
4
5
6
7
8
N/C
IN-
IN+
V-
N/C
V+
OUT
N/C

HA-5141


V+
OUT
OUT
IN
IN
IN
IN
V-
OUT 1
V+
IN-1
IN+1
OUT 2
IN-2
V-
IN+2
OUT
IN
V-
V+
OUT
IN

HA-5142


IN-1
OUT 1
OUT 4
IN-4
IN+1
IN+4
V+
V-
IN+2
IN+3
IN-2
OUT 2
OUT 3
IN-3
OUT 1
OUT 4
INPUTS 1
INPUTS 4
V+
V-
INPUTS 2
INPUTS 3
OUT 2
OUT 3

HA-5144

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	40V	Operating Temperature Range	0°C≤TA≤+75°C
Differential Input Voltage	±7V		-55°C≤TA≤+125°C
Output Current	S/C Protected	Storage Temperature Range	-65°≤TA≤+150°C
Internal Power Dissipation	500mW		

ELECTRICAL CHARACTERISTICS V+ = 5V, V- = 0V

PARAMETER	TEMP	HA-5141/42/44A -2 or -5 MIN	TYP	MAX	HA-5141/42/44 -2 or -5 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage (Note 12)	+25°C Full		0.5	2 5		2	6 8	mV mV
Average Offset Voltage Drift	Full		3			3		µV/°C
Bias Current	+25°C Full		45	75 100		45	100 125	nA nA
Offset Current	+25°C Full		0.3	10 15		[illegible]	10 20	nA nA
Common Mode Range	+25°C [illegible]	0 to 4 0 to 4			0 to 3.5			V
[illegible]	[illegible]	50K 30K						
[illegible]	[illegible]	80						
TRANSIENT RESPONSE								
Rise Time (Notes 2,3)	+25°C		600			600		ns
Slew Rate (Notes 2,3)	+25°C	1	1.5		0.5	1		V/µs
Settling Time (Note 6)	+25°C		10			10		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current per Amplifier	+25°C		45	65		50	80	µA
[illegible]	[illegible]	80						

5. VO = +3.5V (Source), +1.5V (Sink)

6. [illegible]

7. [illegible]

8. [illegible]

9. [illegible]

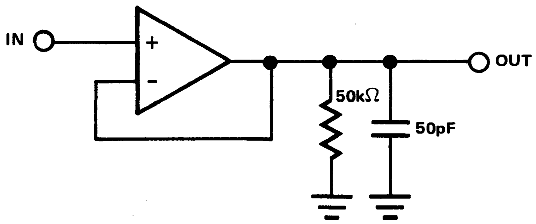
10. [illegible]

11. [illegible]

12. [illegible]

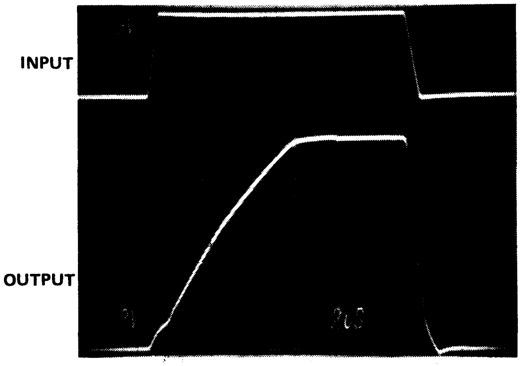
TEST CIRCUITS

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



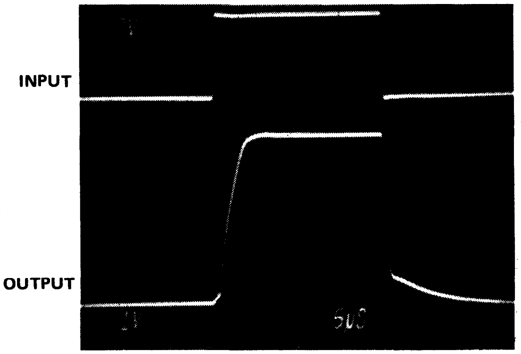
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: Input = 5V/Div.)
(Volts: Output = 2V/Div.)
Horizontal Scale: (Time: 2μs/Div.)



+VSUPPLY = +15V, -VSUPPLY = -15V

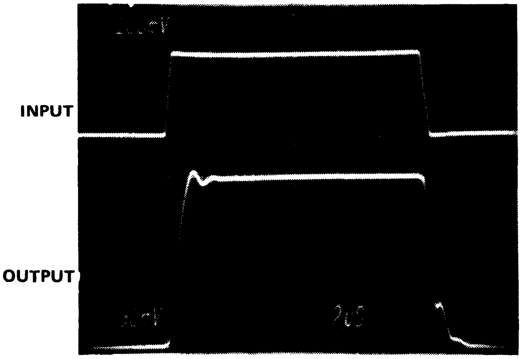
Vertical Scale: (Volts: Input = 2V/Div.)
(Volts: Output = 1V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



+VSUPPLY = +5V, -VSUPPLY = 0V

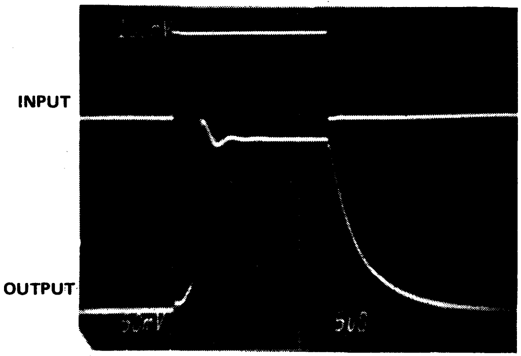
SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: Input = 100mV/Div.)
(Volts: Output = 50mV/Div.)
Horizontal Scale: (Time: 2μs/Div.)



+VSUPPLY = +15V, -VSUPPLY = -15V

Vertical Scale: (Volts: Input = 100mV/Div.)
(Volts: Output = 50mV/Div.)
Horizontal Scale: (Time: 5μs/Div.)

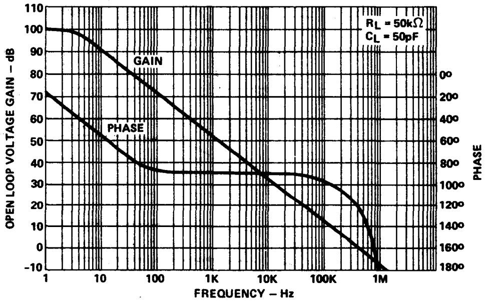


+VSUPPLY = +5V, -VSUPPLY = 0V

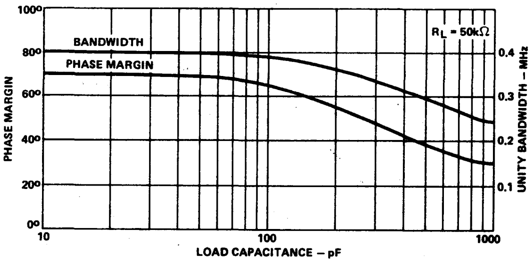
PERFORMANCE CURVES

$V_S = \pm 2.5V$, $T_A = +25^{\circ}C$ Unless Otherwise Stated

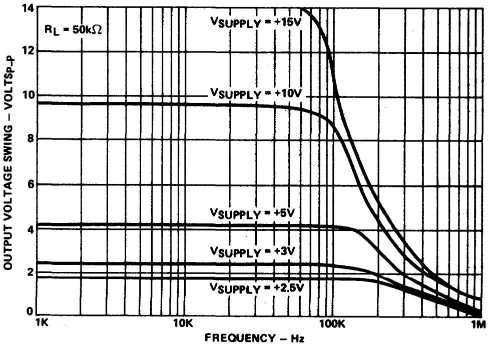
OPEN LOOP FREQUENCY RESPONSE



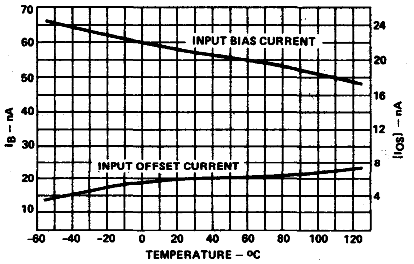
BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



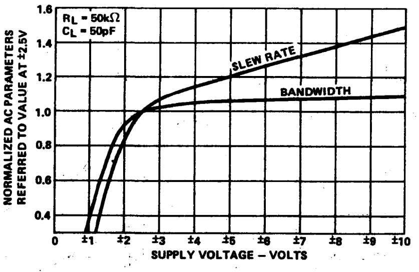
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SINGLE SUPPLY VOLTAGE



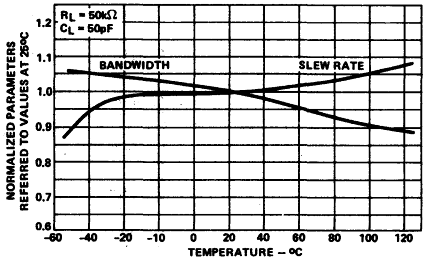
INPUT OFFSET CURRENT AND BIAS CURRENT VS. TEMPERATURE



NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE

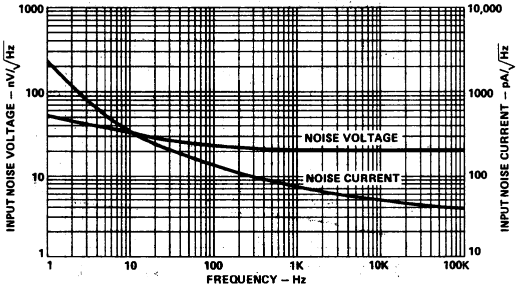


NORMALIZED AC PARAMETERS VS. TEMPERATURE

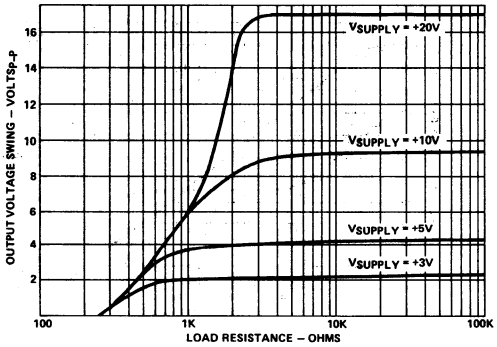


PERFORMANCE CURVES (continued)

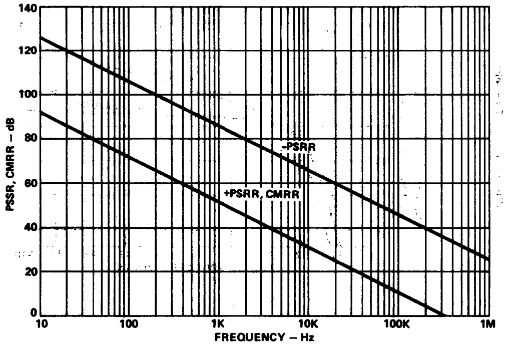
INPUT NOISE VS. FREQUENCY



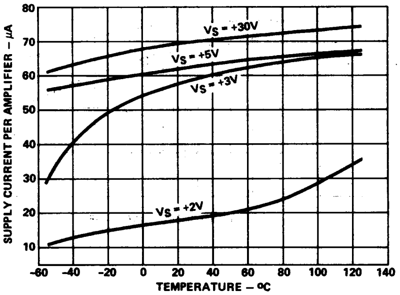
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SINGLE SUPPLY VOLTAGE



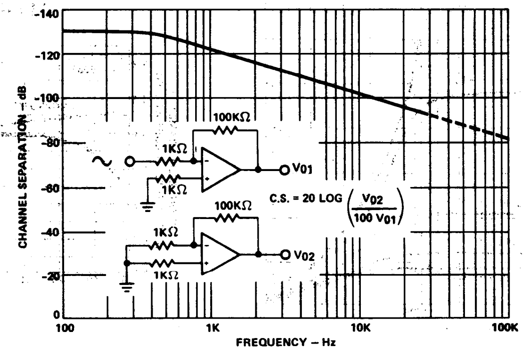
PSRR AND CMRR VS. FREQUENCY



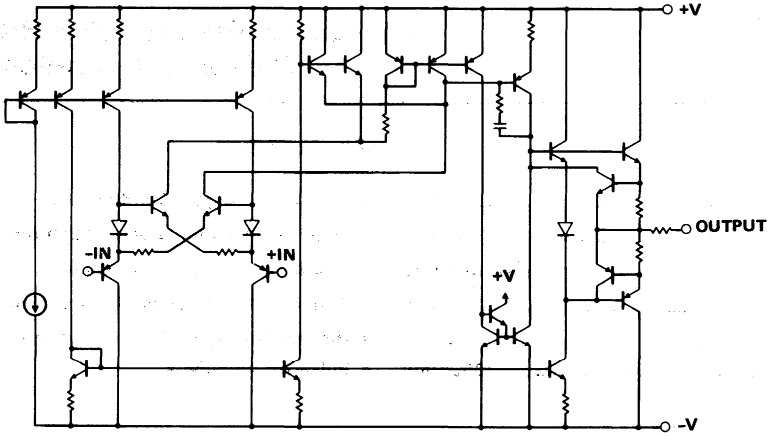
POWER SUPPLY CURRENT VS. TEMPERATURE AND SINGLE SUPPLY VOLTAGE



CHANNEL SEPARATION VS. FREQUENCY



SCHEMATIC


+V
-IN
+IN
+V
OUTPUT
-V

HARRIS

HA-5147

PRELIMINARY

Ultra-Low Noise Precision High Slew Rate Wideband Operational Amplifiers

Features

- **High Speed** **35V/μs**
- **Wide Gain Bandwidth** .... **120 MHz**
- **Low Noise** .... **3 nV/$\sqrt{\text{Hz}}$ at 1 KHz**
- **Low V_{OS}** **10μV**
- **High CMRR** .... **126 dB**
- **High Gain** **1800V/mV**

Applications

- **High Speed Signal Conditioners**
- **Wide Bandwidth Instrumentation Amplifiers**
- **Low Level Transducer Amplifiers**
- **Fast, Low Level Voltage Comparators**
- **Highest Quality Audio Preamplifiers**
- **Pulse/RF Amplifiers**

Description

The HA-5147 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3 nV/$\sqrt{\text{Hz}}$) precision instrumentation performance with high speed (35V/μs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10 μV), wide gain-bandwidth (120 MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140 mW of power.

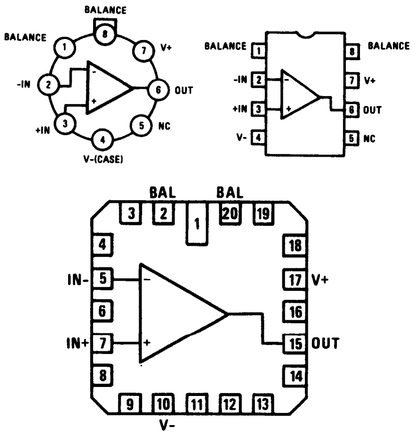
Using the HA-5147 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5147's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

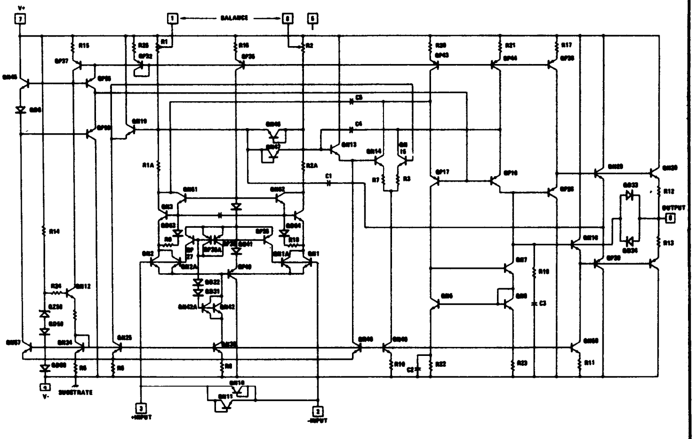
This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than ten. The HA-5147 is available in TO-99 metal can, both epoxy and ceramic 8 pin mini-DIPs, as well as 20 pin LCC packages.

Pinouts

TOP VIEWS



Schematic



Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals .... ±22V

Differential Input Voltage (Note 2) .... ±0.7V

Internal Power Dissipation .... 500 mW

Output Short Circuit Duration .... Indefinite

Operating Temperature Ranges:

HA-5147 -2,8 .... −55°C ≤ TA ≤ +125°C

HA-5147 -5 .... 0°C ≤ TA ≤ +75°C

Storage Temperature Range ..... −65°C ≤ TA ≤ +150°C

Electrical Characteristics V+ = 15V, V− = −15V, C_L ≤ 10pF, Rs = 100Ω

PARAMETER	TEMP	HA-5147A MIN	HA-5147A TYP	HA-5147A MAX	HA-5147 MIN	HA-5147 TYP	HA-5147 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		10	25		30	100	μV
	Full		30	60		70	300	μV
Average Offset Voltage Drift	Full		0.2	0.6		0.4	1.8	μV/°C
Bias Current	+25°C		±10	±40		±15	±80	nA
	Full		±20	±60		±35	±150	nA
Offset Current	+25°C		7	35		12	75	nA
	Full		15	50		30	135	nA
Common Mode Range	Full	10.3	11.5		10.3	11.5		V
Differential Input Resistance (Note 3)	+25°C	1.5	6		0.8	4		MΩ
Input Noise Voltage 0.1 Hz to 10 Hz (Note 4)	+25°C		0.08	.18		0.09	0.25	μVp-p
Input Noise Voltage Density (Note 5)	+25°C							nV/$\sqrt{Hz}$
f_O = 10 Hz			3.5	5.5		3.8	8.0	
f_O = 30 Hz			3.1	4.5		3.3	5.6	
f_O = 1000 Hz			3.0	3.8		3.2	4.5	
Input Noise Current Density (Note 5)	+25°C							pA/$\sqrt{Hz}$
f_O = 10 Hz			1.7	4.0		1.7		
f_O = 30 Hz			1.0	2.3		1.0		
f_O = 1000 Hz			0.4	0.6		0.4	0.6	
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 6)	+25°C	1000	1800		700	1500		V/mV
	Full	600	1200		300	800		V/mV
Common Mode Rejection Ratio (Note 7)	Full	114	126		100	120		dB
Gain Bandwidth Product f_O = 10 kHz	+25°C	120	140		120	140		MHz
(Note 3) f_O = 1 MHz	+25°C		120			120		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing R_L = 600 Ω	+25°C	±10.0	±11.5		±10.0	±11.5		V
R_L = 2K Ω	Full	±11.7	13.8		±11.4	13.5		V
Full Power Bandwidth (Note 8)	+25°C	445	500		445	500		kHz
Output Resistance, Open Loop	+25°C		70			70		Ω
TRANSIENT RESPONSE (Note 9)								
Rise Time	+25°C		22	50		22	50	ns
Slew Rate (Note 11)	+25°C	28	35		28	35		V/μs
Setting Time (Note 10)	+25°C		400			400		ns
Overshoot	+25°C		20	40		20	40	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.5			3.5		mA
	Full			4.0			4.0	mA
Power Supply Rejection Ratio (Note 12)	Full		2	4		16	51	μV/V

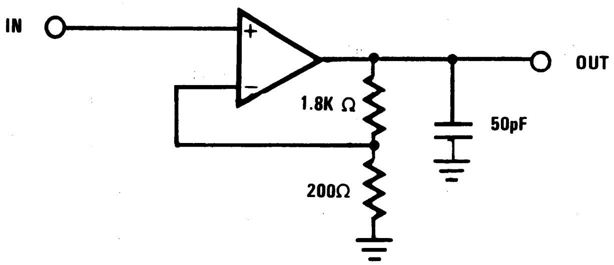
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25 mA to protect the back-to-back input diodes.
3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. Sample tested.
6. $V_{OUT} = \pm 10V$, $R_L = 2K\ \Omega$
7. $V_{CM} = \pm 10V$
8. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
9. Refer to Test Circuits section of the data sheet.
10. Settling time is specified to 0.1% of final value for a 10V output step and $A_V = -10$.
11. V_{OUT} = 10V Step
12. $V_S = \pm 4V$ to $\pm 18V$

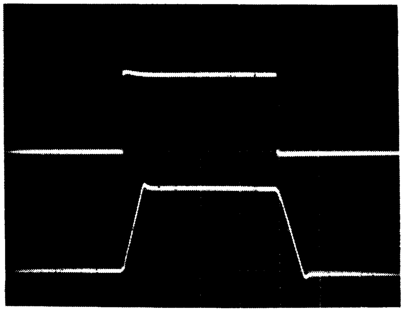
Test Circuits

LARGE AND SMALL SIGNAL RESPONSE

TEST CIRCUIT

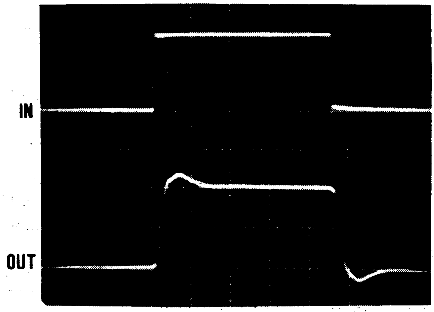


LARGE SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 0.5V/Div.)
(Volts: Output = 5V/Div.)
Horizontal Scale: (Time: 500ns/Div)

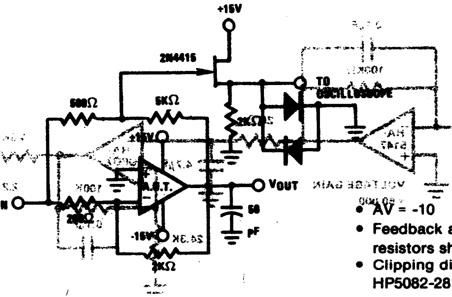
SMALL SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 10mV/Div)
(Volts: Output = 100mV/Div)
Horizontal Scale: (Time: 100ns)

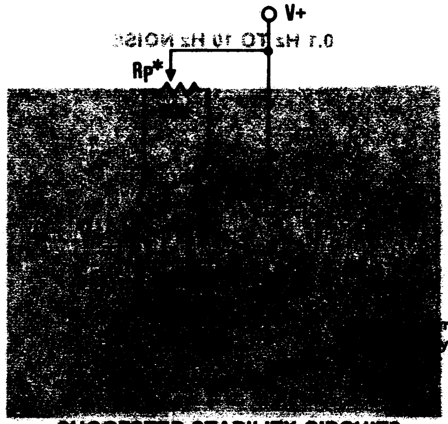
Test Circuits (continued)

SETTLING TIME TEST CIRCUIT


+15V
2N4416
500Ω
5KΩ
2KΩ
TO OSCILLOSCOPE
+15V
100K
VIN
200Ω
A.U.T.
-15V
3KΩ
VOUT
50 pF

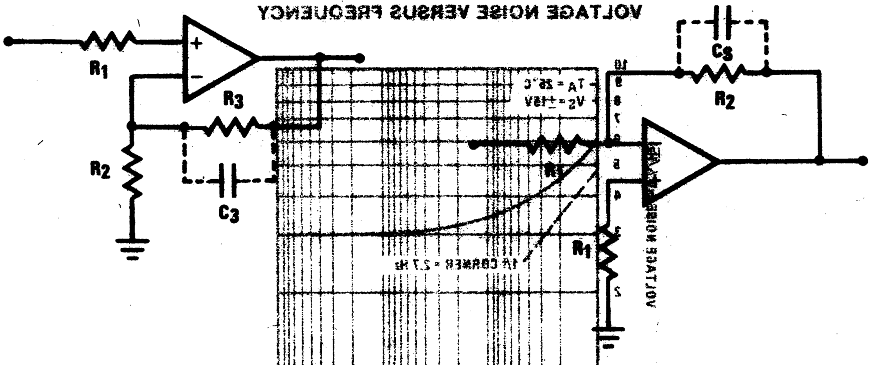
- AV = -10
- Feedback and summing resistors should be 0.1%
- Clipping diodes are optional. HP5082-2810 recommended.

SUGGESTED OFFSET VOLTAGE ADJUSTMENT



ment range is
y ±4mV.

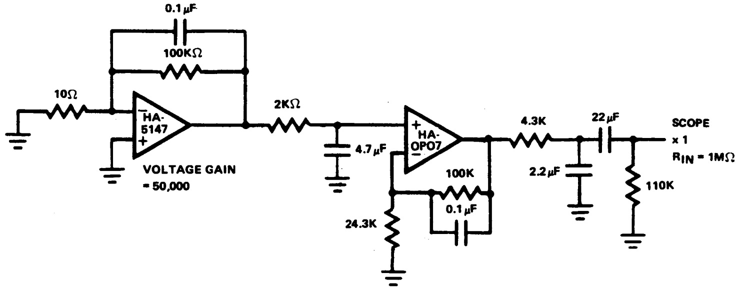
SUGGESTED STABILITY CIRCUITS


R1
R3
R2
C3
Cs
R2
R1
R1

Low resistances are preferred for low noise applications as a 1KΩ resistor has 4 nV/$\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10KΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

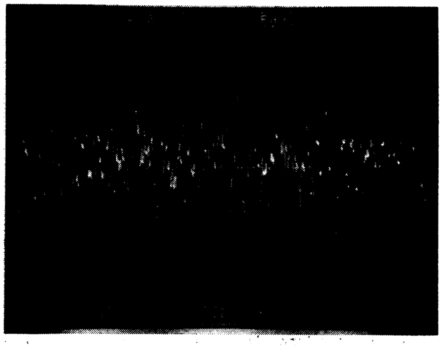
Typical Performance

0.1 Hz TO 10 Hz NOISE TEST CIRCUIT

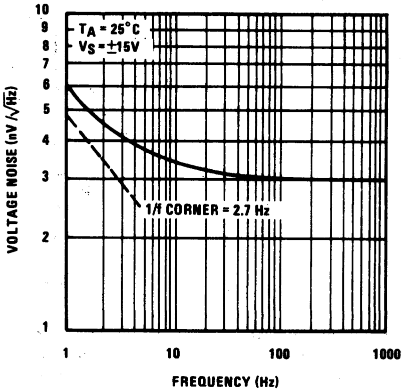

0.1 µF
100KΩ
10Ω
HA-5147
VOLTAGE GAIN = 50,000
2KΩ
4.7 µF
HA-OPO7
100K
0.1 µF
24.3K
4.3K
22 µF
2.2 µF
110K
SCOPE × 1
R_IN = 1MΩ

NOTE: All capacitor values are for non-polarized capacitors only.

0.1 Hz TO 10 Hz NOISE



VOLTAGE NOISE VERSUS FREQUENCY



HARRIS HA-5151/52/54

PRELIMINARY

Low Power Operational Amplifiers

Features

- Low Supply Current.......................... < 200μA/Amplifier
- Dual Supply Voltage Range...................... ±1V to ±15V
- Single Supply Voltage Range........................2V to 30V
- Full Power Bandwidth... 80KHz
- Low V_{OS} Drift..3μV/°C
- Low Noise .... 15nV/√Hz
- Dielectric Isolation

Applications

- Portable Instuments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Remote Sensor/Transmitter
- Battery Powered Equipment

Description

The HA-5151/52/54 series is a group of dielectrically isolated bipolar amplifiers designed to provide excellent AC performance while drawing less than 200μA of supply current per amplifier. These unity gain stable amplifiers are especially well suited for portable and lightweight equipment where available power is limited.

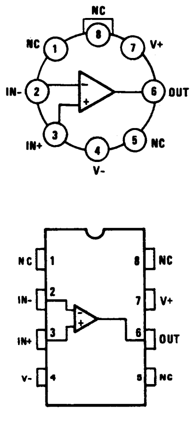
The HA-5151/52/54 series combines superior low power AC performance with DC precision not usually found in general purpose amplifiers. The DC performance is centered around low input offset voltage (0.5mV), low offset voltage drift (3μV/°C), and low input bias current (70nA). This is combined with a very low input noise voltage of 15nV/√Hz at 1KHz.

The AC performance of the HA-5151/52/54 series surpasses that of typical low power amplifiers with 4.5V/μsec slew rate and a full power bandwidth of 80KHz. This makes the HA-5151/52/54 series an excellent choice for virtually all audio processing applications as well as remote sensor/transmitter designs requiring both low power and high speed. The suitability of the HA-5151-/52/54 series for remote and low power operation is further enhanced by the wide range of supply voltages (±1V to ±15V) as well as single supply operation (2V to 30V).

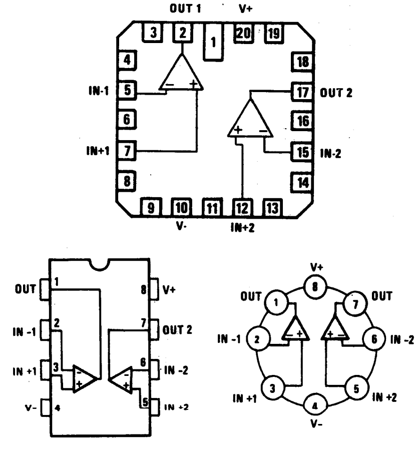
These amplifiers are available in singles (HA-5151, can or mini-dip), duals (HA-5152, can, mini-dip or 20 pin LCC) or quads (HA-5154, 14 pin dip or 20 pin LCC), as well as over both the commercial (0°C to +75°C) and military (-55°C to +125°C) temperature ranges. These amplifiers also carry industry standard pinouts which allow the HA-5151/52/54's to be interchangeable with most other operational amplifiers.

Pinouts

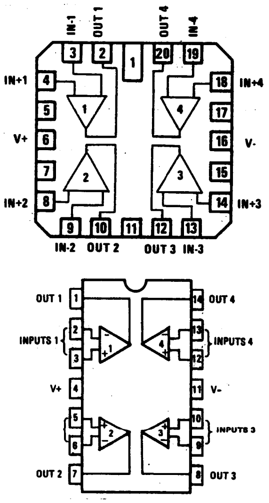
TOP VIEWS



HA-5151



HA-5152



HA-5154

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals........................40V
Differential Input Voltage...±7V
Output Current..S/C Protected
Internal Power Dissipation..500mW

Operating Temperature Range

HA-5151/52/54-5 .... $0^oC \leq T_A \leq +75^oC$
HA-5151/52/54-2 .... $-55^oC \leq T_A \leq +125^oC$
Storage Temp. Range................... $-65^oC \leq T_A \leq +150^oC$

Electrical Characteristics $V+ = 15V$, $V- = -15V$, $R_S = 100\Omega$, $C_L \leq 10pF$ unless otherwise specified.

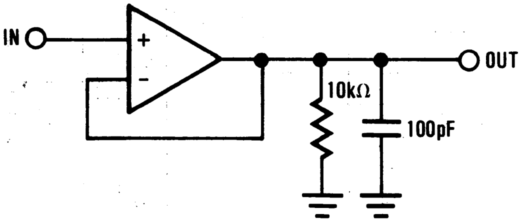
PARAMETER	TEMP	$-55^oC \leq T_A \leq +125^oC$			$0^oC \leq T_A \leq +75^oC$			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.5	2		2	3	mV
	Full			3			4	mV
Average Offset Voltage Drift	Full		3			3		μV/°C
Bias Current	+25°C		70	150		70	150	nA
	Full			250			250	nA
Offset Current	+25°C		10	30		10	30	nA
	Full			50			50	nA
Common Mode Range	Full	±10			±10			V
Differential Input Resistance	+25°C		1.5			1.5		mΩ
Input Noise Voltage (f = 1kHz)	+25°C		14.8			14.8		$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C		0.25			0.25		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2, 4)	+25°C	50K	100K		50K	100K		V/V
	Full	25K	50K		25K	50K		V/V
Common Mode Rejection Ratio (Note 7)	Full	80	105		80	105		dB
Bandwidth (Notes 2, 3)	+25°C		1.3			1.3		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 2)	Full	±10			±10			V
Full Power Bandwidth (Note 2, 4, 8)	+25°C		80			80		kHz
Output Current	+25°C		±3			±3		mA
TRANSIENT RESPONSE (Notes 2, 3)								
Rise Time	+25°C		300			300		ns
Slew Rate (Note 6)	+25°C	2	4.5		2	4.5		Vμs
Settling Time (Note 5)	+25°C		5			5		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		200	250		200	250	μA/Amp
	Full			275			275	μA/Amp
Power Supply Rejection Ratio (Note 9)	Full	80	105		80	105		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $R_L = 10k\Omega$
3. $C_L = 100pF$
4. $V_O = \pm 10V$
5. Settling Time is specified to 0.1% of final value for a 10V output step and $A_V = -1$.
6. Maximum input slew rate = 30V/μsec.
7. $V_{CM} = \pm 10V$.
8. Full Power Bandwidth is guaranteed by equation:
   $$\text{Full Power Bandwidth} = \frac{\text{Slew Rate}}{2 \pi \text{ V Peak}}$$
9. $\Delta V_S = \pm 5V$.

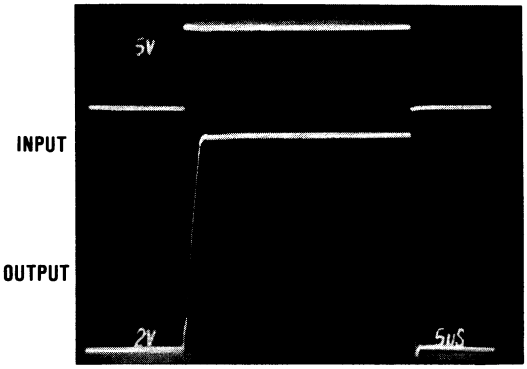
Test Circuits

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



LARGE SIGNAL RESPONSE

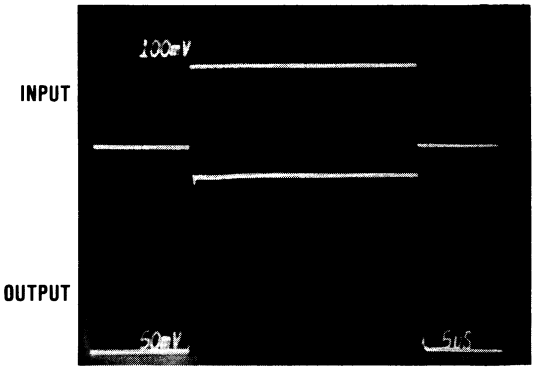
Vertical Scale: (Volts: Input = 5V/Div.)
(Volts: Output = 2V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



$+V_{SUPPLY} = +15V$, $-V_{SUPPLY} = -15V$

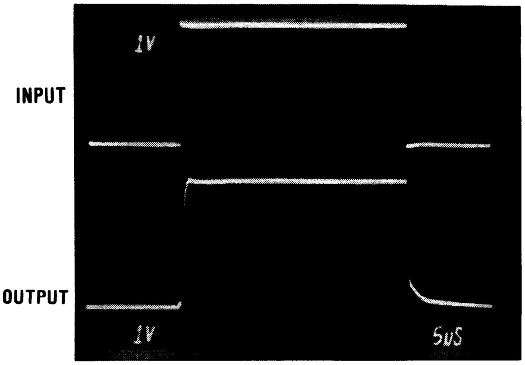
SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: Input = 100mV/Div.)
(Volts: Output = 50mV/Div.)
Horizontal Scale: (Time: 5μs/Div.)



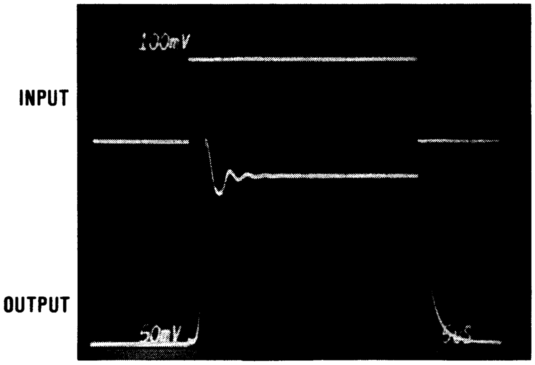
$+V_{SUPPLY} = +15$, $-V_{SUPPLY} = -15V$

Vertical Scale: (Volts: Input = 1V/Div.)
(Volts: Output = 1V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



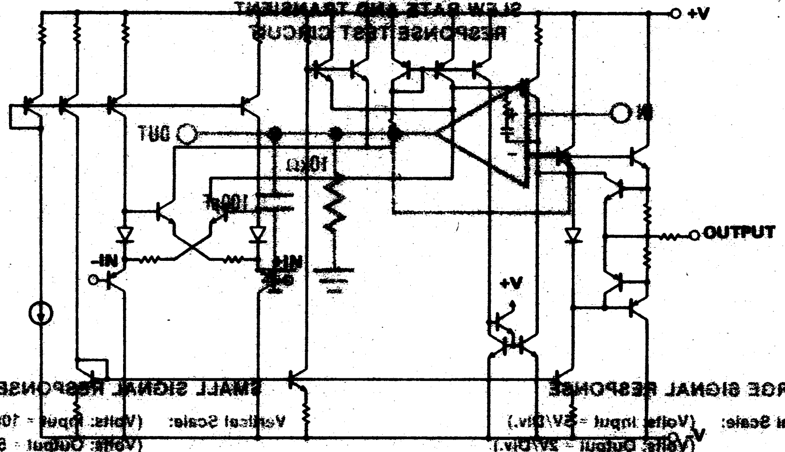
$+V_{SUPPLY} = +5V$, $-V_{SUPPLY} = 0V$

Vertical Scale: (Volts: Input = 100mV/Div.)
(Volts: Output = 50mV/Div.)
Horizontal Scale: (Time: 5μs/Div.)



$+V_{SUPPLY} = +5V$, $-V_{SUPPLY} = 0V$

Schematic


+V
OUTPUT
-IN
+IN
+V
V-

HARRIS

HA-5160/62

Wideband, JFET Input High Slew Rate, Uncompensated Operational Amplifier

FEATURES

• WIDE GAIN BANDWIDTH	100MHz
• HIGH SLEW RATE	120V/μs
• SETTLING TIME (0.2%)	280ns
• POWER BANDWIDTH	1000kHz
• OFFSET VOLTAGE	1.0mV
• BIAS CURRENT	20pA

APPLICATIONS

- VIDEO AND RF AMPLIFIERS
- DATA ACQUISITION
- PULSE AMPLIFIERS
- PRECISION SIGNAL GENERATION

DESCRIPTION

The HA-5160/5162 is a wideband, uncompensated, operational amplifier manufactured with FET/Bipolar technologies and dielectric isolation. This monolithic amplifier features superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. This device has excellent phase margin at a closed loop gain of 10 without external compensation.

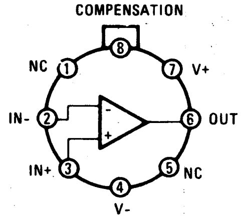
The HA-5160/5162 offers a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics, the HARRIS devices have nearly constant slew rate, bandwidth, and settling characteristics over the operating temperature range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. Note also that HARRIS specified all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

Complementing the HA-5160/5162's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and extremely high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications.* The HA-5160 provides excellent performance for applications which require both precision and high speed perfornance. The HA-5162 meets or exceeds the performance specifications of National's hybrid op amp, the LH0062.

* -2 denotes a range of -55°C to +125°C and -5 denotes a 0°C to +75°C range.

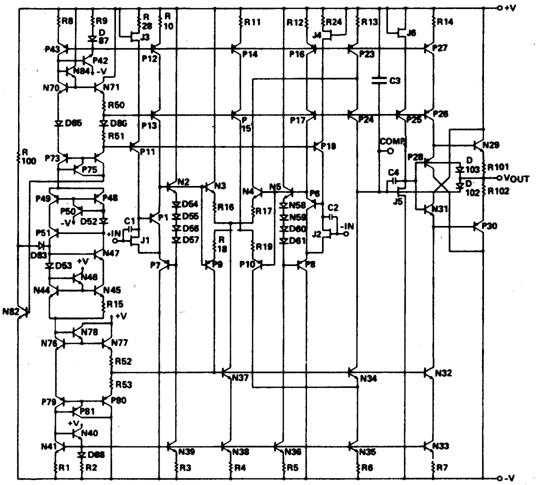
PINOUT

TOP VIEW


COMPENSATION
8
NC 1
7 V+
IN- 2
6 OUT
IN+ 3
5 NC
4
V-
-
+

Case connected to V-

SCHEMATIC


+V
-V
VOUT
COMP
+IN
-IN
R8
R9
R10
R11
R12
R13
R14
R24
R28
R50
R51
R100
R15
R16
R17
R18
R19
R52
R53
R101
R102
R1
R2
R3
R4
R5
R6
R7
J1
J2
J3
J4
J5
J6
C1
C2
C3
C4
P43
P42
N84
N70
N71
D85
D86
P73
P75
P49
P48
P50
D52
P51
D83
D53
N47
N46
N44
N45
N82
N78
N76
N77
P79
P80
P81
N40
N41
D88
P12
P13
P11
P14
P15
P16
P17
P18
P23
P24
P25
P26
P27
N29
P28
N31
P30
D103
D102
D87
N2
N3
N4
N5
P6
P1
P7
P9
P10
P8
D54
D55
D56
D57
N58
N59
D60
D61
N37
N34
N32
N39
N38
N36
N35
N33

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage	±40V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	675mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS V+ = +15V, V- = -15V

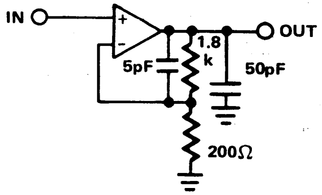
		HA-5160-2 -55°C to +125°C			HA-5160-5 0°C to +75°C			HA-5162-5 0°C to 75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	TYP	UNITS
INPUT CHARACTERISTICS											
*Offset Voltage	+25°C		1.0	3.0		1.0	3.0		3	15	mV
	Full		3.0	5.0		3.0	5.0		5	20	mV
Offset Voltage Average Drift	Full		10			20			20	35	μV/°C
*Bias Current	+25°C		20	50		20	50		20	65	pA
	Full		5	10			10			10	nA
*Offset Current	+25°C		2	10		2	10		2	10	pA
	Full		2	5		2	5		2	5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±11		V
TRANSFER CHARACTERISTICS											
*Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		25K	100K		V/V
	Full	60K	100K		60K	100K		25K	75K		V/V
*Common Mode Rejection Ratio (Note 4)	Full	74	80		74	80		70	80		dB
Gain Bandwidth Product (A_V = 10)	Full		100			100			100		MHz
OUTPUT CHARACTERISTICS											
*Output Voltage Swing (Note 5)	+25°C	±10	±11		±10	±11		±10	±11		V
	Full	±10	±11		±10	±11		±10	±11		V
*Output Current (Note 6)	+25°C	±15	±22		±15	±22		±15	±22		mA
Full Power Bandwidth (Note 7)	+25°C		1000			1000			1000		kHz
Output Resistance (Note 8)	+25°C		50			50			50		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time (A_V = 10)	+25°C		20			20			20		ns
Slew Rate (A_V = 10)	+25°C	100	120		100	120		50	70		V/μs
Settling Time (Note 10)	+25°C		280			280			400		ns
POWER SUPPLY CHARACTERISTICS											
*Supply Current	Full		8.0	10		8.0	10		8.0	12	mA
*Power Supply Rejection Ratio (Note 11)	+25°C	74	86		74	86		70	86		dB

NOTES:

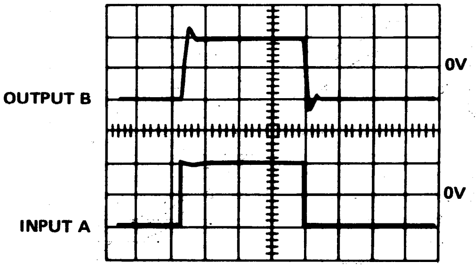
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$. $R_L = 2k$
4. $V_{CM} = \pm 10V$ DC.
5. $R_L = 2k$
6. $V_{OUT} = 0V$
7. $R_L = 2k$; Full power bandwidth guaranteed, based on slew rate measurement using $FPBW = \frac{SLEW\ RATE.}{2\pi V_{PEAK}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test Circuits section of the data sheet.
10. Settling Time is measured to 0.2% of final value for a 10 volt output step and $A_V = 10$.
11. $V_{SUPP} = \pm 10$ V.D.C. to ±20V DC.

TEST CIRCUITS

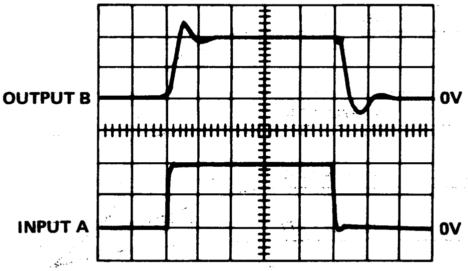
LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



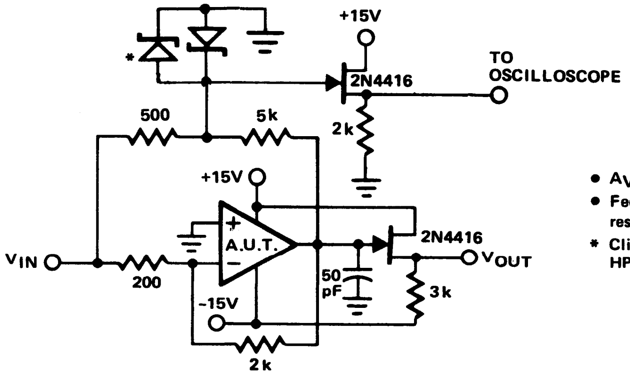
LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: A = 0.5V/Div., B = 5V/Div.)
Horizontal Scale: (Time: 500ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: A = 10mV/Div., B = 100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)



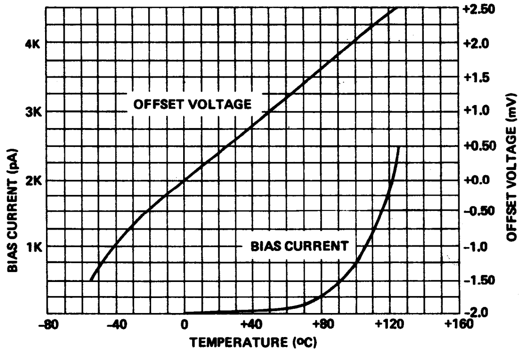
SETTLING TIME CIRCUIT



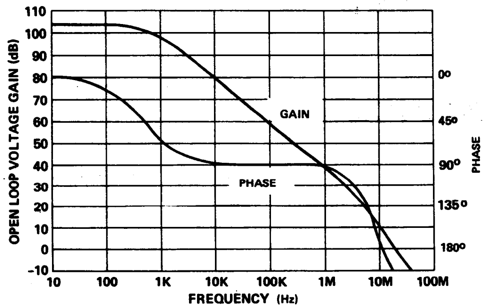
- $A_V = -10$
- Feedback and summing resistors should be 0.1%.
- * Clipping Diodes are optional. HP5082-2810 recommended.

PERFORMANCE CURVES

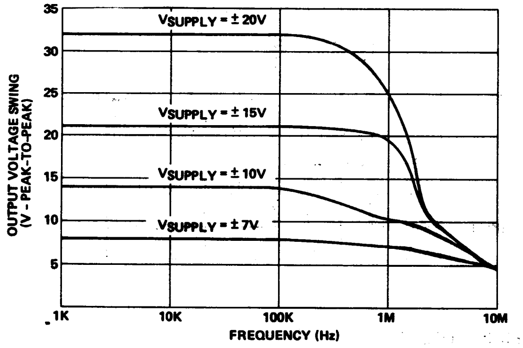
INPUT OFFSET VOLTAGE AND BIAS CURRENT VS. TEMPERATURE



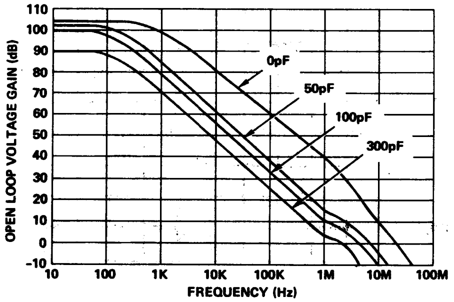
OPEN LOOP FREQUENCY RESPONSE



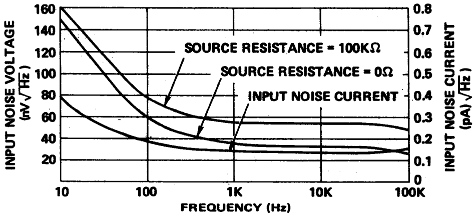
OUTPUT VOLTAGE SWING VS. FREQUENCY

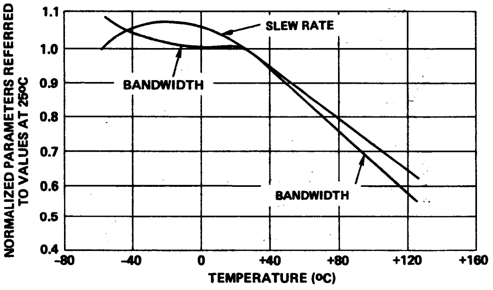


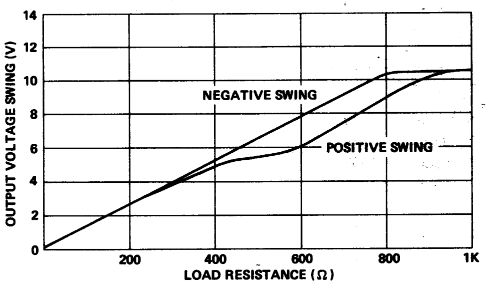
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS BANDWIDTH CONTROL CAPACITANCES

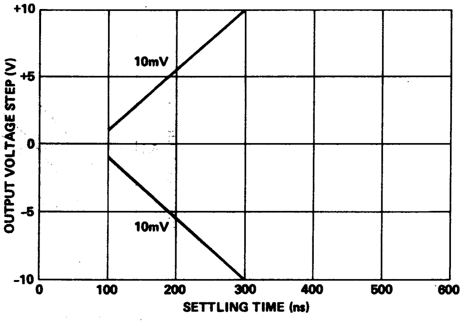


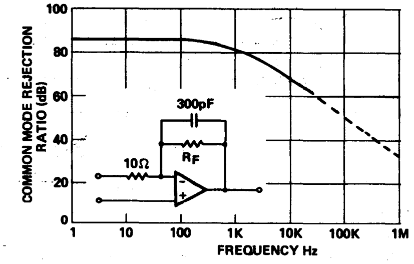
PERFORMANCE CURVES (Continued)


INPUT NOISE VOLTAGE AND NOISE CURRENT VS. FREQUENCY

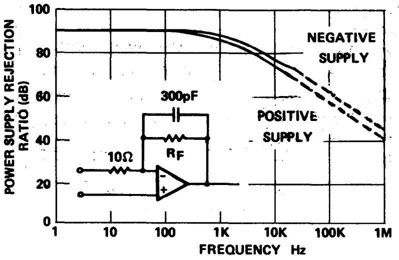

NORMALIZED AC PARAMETERS VS. TEMPERATURE


OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE

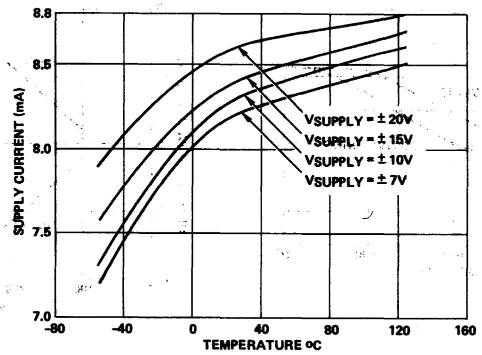

SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



COMMON MODE REJECTION RATIO VS. FREQUENCY



POWER SUPPLY REJECTION RATIO VS. FREQUENCY



POWER SUPPLY CURRENT VS. TEMPERATURE

APPLYING THE HA-5160/5162

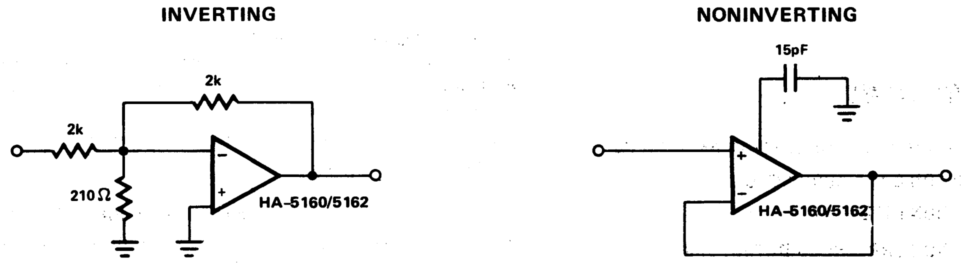
1. POWER SUPPLY DECOUPLING: Although not absolutely necessasry, it is recommended that all power supply lines be decoupled with 0.01 μF ceramic capacitors to ground decoupling capacitors should be located as near to the amplifier terminals as possible.

2. STABILITY: The phase margin of the HA-5160/5162 will be improved by connecting a small capacitor (>10pF) between the output and the inverting input of the device. This small capacitor compensates for the input capacitance of the FET.

3. CAPACITIVE LOADS: When driving large capacitive loads (>100pF), it is suggested that a small resistor (≈100Ω) be connected in series with the output of the device and inside the feedback loop.

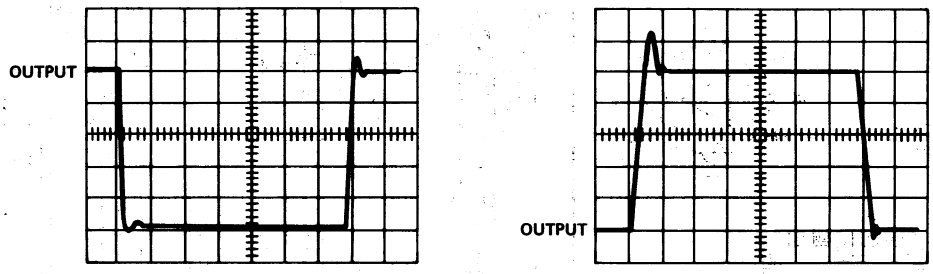
APPLICATIONS

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY *



*VALUES WERE DETERMINED EXPERIMENTALLY FOR OPTIMUM SPEED AND SETTLING TIME

VERTICAL SCALE: (VOLTS: 2V/DIV.)
HORIZONTAL SCALE: (TIME: 500ns/DIV.)



HARRIS

HA-5170

Precision JFET Input Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE	100μV
- LOW OFFSET VOLTAGE DRIFT	2μV/$^\circ$C
- LOW NOISE	10nV/$\sqrt{Hz}$
- HIGH OPEN LOOP GAIN	600K V/V
- WIDE BANDWIDTH	8MHz

APPLICATIONS

- HIGH GAIN INSTRUMENTATION AMPLIFIERS
- PRECISION DATA ACQUISITION
- PRECISION INTEGRATORS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

The Harris HA-5170 is a precision, JFET input, operational amplifier which features low noise, low offset voltage and low offset voltage drift. Constructed using FET/Bipolar technology, the Harris Dielectric Isolation (DI) process, and laser trimming this amplifier offers low input bias and offset currents. This operational amplifier design also completely eliminates the troublesome errors due to warm-up drift.

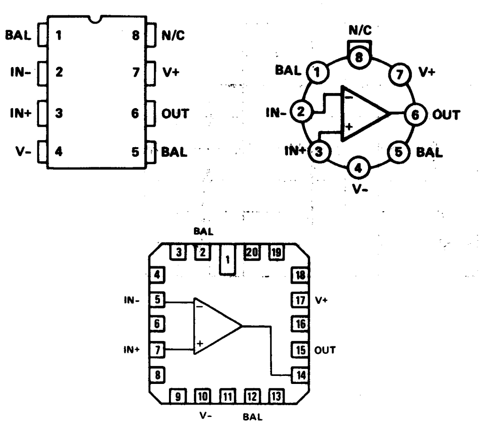
Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/μs slew rate and 8MHz bandwidth allow the designer to extend precision instrumentation applications in both speed and bandwidth. These characteristics make the HA-5170 well suited for precision integrator amplifier designs.

The superior input characteristics also make the HA-5170 ideally suited for transducer signal amplifiers, precision voltage followers and precision data acquisition systems.

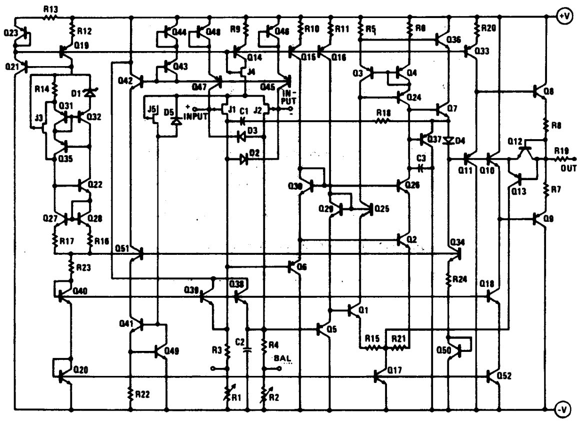
The HA-5170 is available in metal can (TO-99), 20 pin LCC, and both ceramic and epoxy mini-dip packages.

PINOUT

TOP VIEWS


BAL 1
IN- 2
IN+ 3
V- 4
8 N/C
7 V+
6 OUT
5 BAL
N/C 8
BAL 1
V+ 7
IN- 2
6 OUT
IN+ 3
5 BAL
4 V-
BAL
3 2 1 20 19
4 18
IN- 5
6 16
IN+ 7
8 14
17 V+
15 OUT
9 10 11 12 13
V- BAL

SCHEMATIC


+V
-V
R13
Q23
R12
Q19
Q21
R14
D1
J3
Q31
Q32
Q35
Q22
Q27
Q28
R17
R16
R23
Q40
Q20
Q42
Q44
Q48
Q43
Q47
J5
D5
INPUT
J1
C1
J2
D3
D2
R9
Q14
J4
Q46
Q45
IN-PUT
R10
Q15
R11
Q16
R5
R6
Q3
Q4
Q24
R18
Q7
Q37
D4
C3
Q36
R20
Q33
Q8
R8
Q12
R19
OUT
Q11
Q10
Q13
R7
Q9
Q30
Q29
Q26
Q25
Q2
Q34
Q51
Q6
Q39
Q38
Q41
Q49
R3
C2
R4
BAL
R22
R1
R2
Q5
Q1
R15
R21
Q50
Q17
R24
Q18
Q52

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated
Voltage Between V+ and V-Terminals 44.0V
Differential Input Voltage ± 30.0V
Output Short Circuit Duration Indefinite

Power Dissipation (Note 2) 675mW
Operating Temperature Range
HA-5170-2 $-55°C \leq T_A \leq +125°C$
HA-5170-5 $0°C \leq T_A \leq +75°C$
Storage Temperature Range $-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V

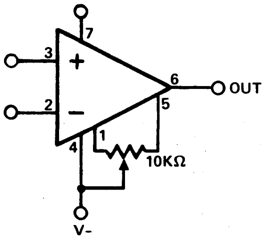
PARAMETER	TEMP.	HA-5170-2 MIN	HA-5170-2 TYP	HA-5170-2 MAX	HA-5170-5 MIN	HA-5170-5 TYP	HA-5170-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C Full		0.1	0.3 0.5		0.1	0.3 0.5	mV mV
Average Offset Voltage Drift (Note 3)	Full		2	5		2	5	μV/°C
Bias Current	+25°C Full		20 3	100 30		20 0.1	100 2	pA nA
Bias Current Average Drift	Full		3			3		pA/°C
Offset Current	+25°C Full		3	30 5		3	60 0.1	pA nA
Offset Current Average Drift	Full		0.3			0.3		pA/°C
Common Mode Range	Full	±10	+15.1 -12		±10	+15.1 -12		V
Differential Input Resistance	+25°C		6×10^{10}			6×10^{10}		Ω
Input Capacitance	+25°C		12			12		pF
Input Noise Voltage 0.1Hz to 10Hz (Note 3)	+25°C		0.5	5		0.5	5	μV_{p-p}
Input Noise Voltage Density (Note 3) f_0 = 10Hz f_0 = 100Hz f_0 = 1000Hz	+25°C		 20 12 10	 150 50 25		 20 12 10	 150 50 25	 nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$
Input Noise Current Density (Note 3) f_0 = 10Hz f_0 = 100Hz f_0 = 1000Hz	+25°C		 .05 .01 .01			 .05 .01 .01		 pA/$\sqrt{Hz}$ pA/$\sqrt{Hz}$ pA/$\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C Full	300K 200K	600K		300K 250K	600K		V/V V/V
Common Mode Rejection Ratio (Note 5)	Full	85	100		90	100		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	4	8		4	8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
Full Power Bandwidth (Note 7)	+25°C	80	120		80	120		kHz
Output Current (Note 8)	+25°C	±10			±10			mA
Output Resistance (Note 9)	+25°C		45			45		Ω
TRANSIENT RESPONSE								
Rise Time	+25°C		45	100		45	100	ns
Slew Rate	+25°C	5	8		5	8		V/μs
Settling Time (Note 10)	+25°C		1			1		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		1.9	2.5		1.9	2.5	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		90	105		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8 mW/°C for operation at ambient temperatures above +75°C.
3. Parameter is not 100% tested. 90% of all units meet or exceed these specifications.
4. $V_{OUT} = \pm 10V$; $R_L = 2k$.
5. $V_{CM} = \pm 10V$ D. C.
6. $R_L = 2k\Omega$.
7. R_L = 2k; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. V_{OUT} = 10V.
9. Output resistance measured under open loop conditions (f = 100Hz).
10. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
11. $V_{SUPP} = \pm 5V$ D. C. to $\pm 20V$ D. C.

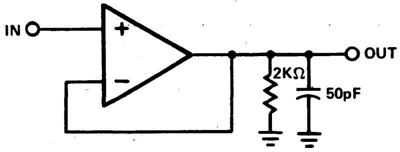
TEST CIRCUITS

V_{OS} ADJUSTMENT



7
3
+
2
−
6
OUT
5
1
4
10KΩ
V-

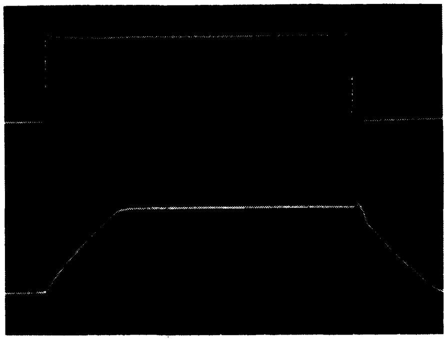
LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



IN
+
−
OUT
2KΩ
50pF

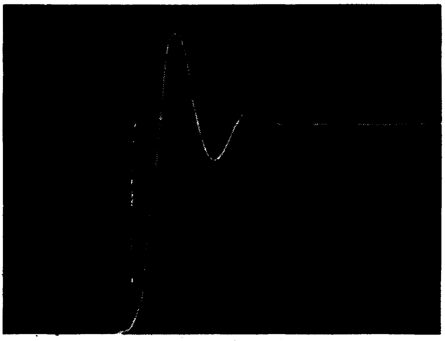
LARGE SIGNAL RESPONSE

VERTICAL SCALE: 5V/Div.
HORIZONTAL SCALE: 500ns/Div.

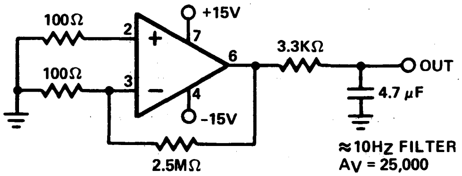


SMALL SIGNAL RESPONSE

VERTICAL SCALE: 10mV/Div.
HORIZONTAL SCALE: 100ns/Div.

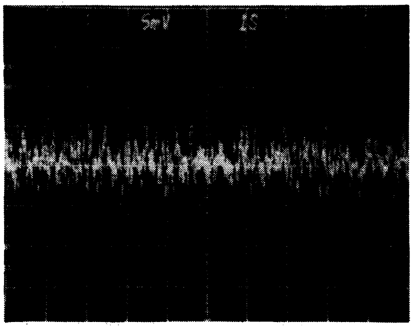


LOW FREQUENCY NOISE TEST CIRCUIT



100Ω
100Ω
2
3
+
−
+15V
7
6
4
-15V
3.3KΩ
OUT
4.7 μF
2.5MΩ
≈10Hz FILTER
AV = 25,000

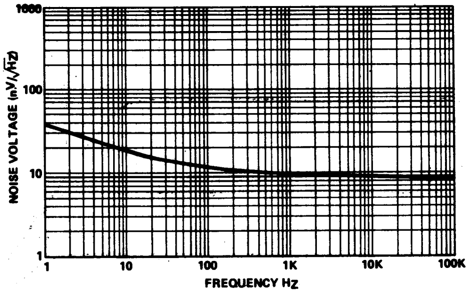
HA-5170 LOW FREQUENCY NOISE (0.1Hz To 10Hz)



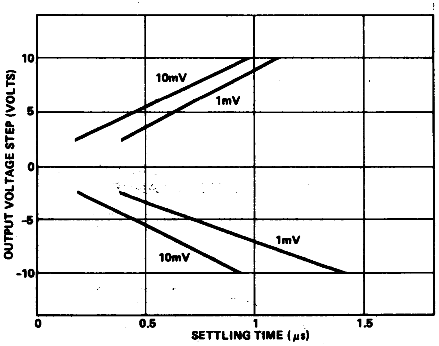
VERTICAL SCALE: 200nV/Div. (Noise Referred to Input)
5mVDiv. At Output, A_{VCL} = 25,000
HORIZONTAL SCALE: 1 Sec./Div.

PERFORMANCE CURVES

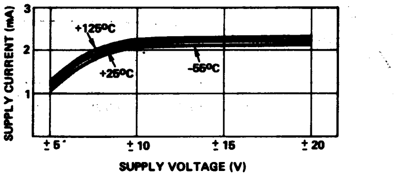
INPUT VOLTAGE NOISE VS. FREQUENCY



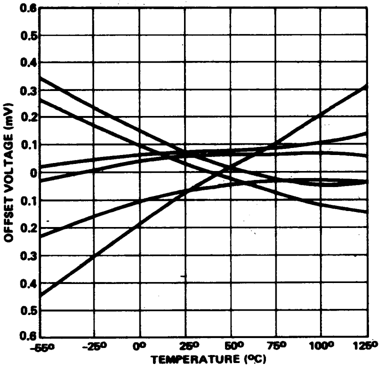
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



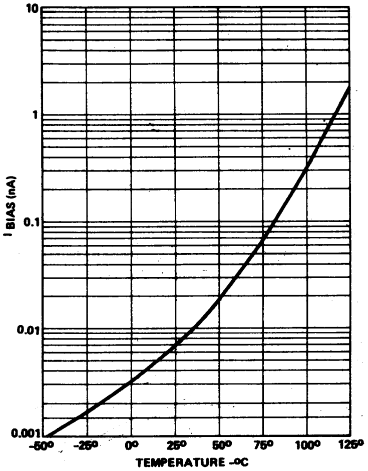
POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE & TEMPERATURE



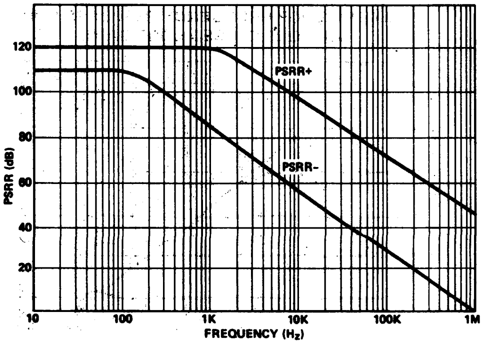
OFFSET VOLTAGE VS. TEMPERATURE DRIFT OF REPRESENTATIVE UNITS



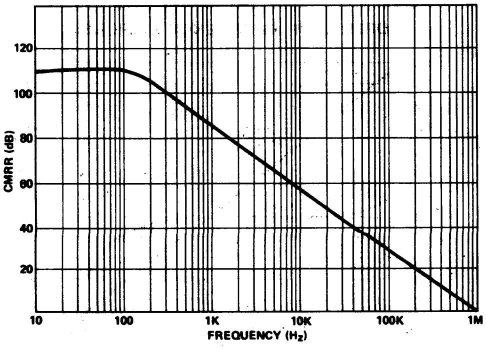
BIAS CURRENT VS. TEMPERATURE



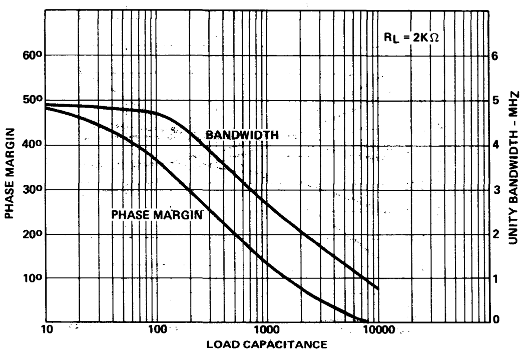
POWER SUPPLY REJECTION RATIO VS. FREQUENCY

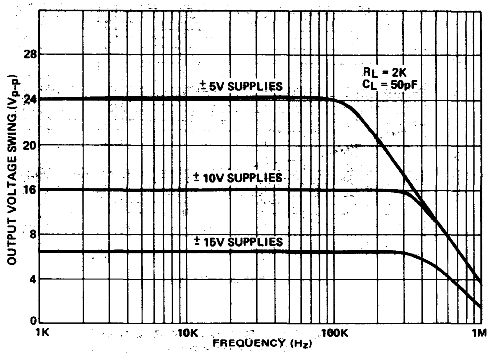


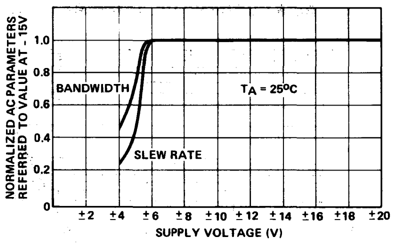
COMMON MODE REJECTION RATIO VS. FREQUENCY

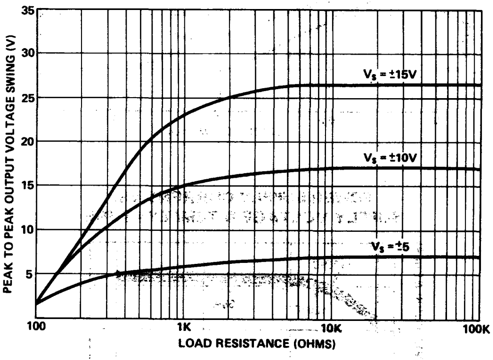


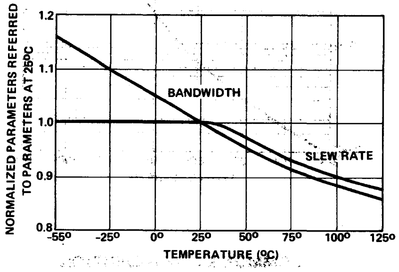
PERFORMANCE CURVES (Continued)

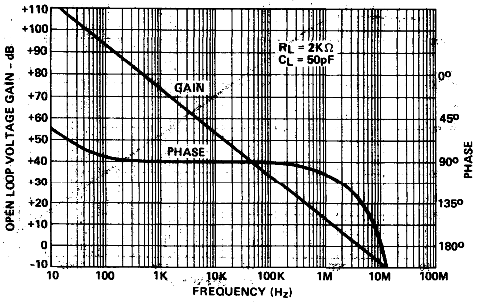

SMALL SIGNAL BANDWIDTH & PHASE MARGIN VS. LOAD CAPACITANCE

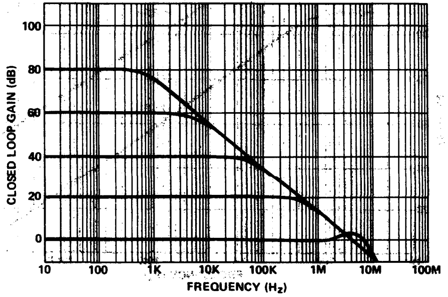

OUTPUT VOLTAGE SWING VS. FREQUENCY & SUPPLY VOLTAGE


NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE


MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE


NORMALIZED AC PARAMETERS VS. TEMPERATURE


OPEN LOOP FREQUENCY RESPONSE


CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS

HARRIS HA-5180/80A

Low Bias Current, Low Power JFET Input Operational Amplifier

FEATURES

• ULTRA LOW BIAS CURRENT	250fA
• LOW POWER SUPPLY CURRENT	0.8mA
• LOW OFFSET VOLTAGE	0.5mV (max.)
• BANDWIDTH	2 MHz
• SLEW RATE	7V/μs

APPLICATIONS

- ELECTROMETER AMPLIFIER DESIGNS
- PHOTO CURRENT DETECTORS
- PRECISION, LONG-TERM INTEGRATORS
- LOW DRIFT SAMPLE & HOLD CIRCUITS
- VERY HIGH IMPEDANCE BUFFERS
- HIGH IMPEDANCE BIOLOGICAL MICRO PROBES

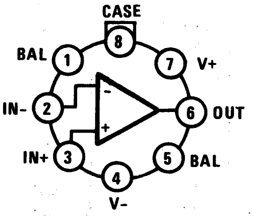
DESCRIPTION

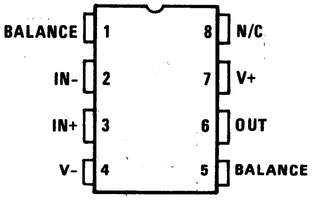
The HARRIS HA-5180/5180A is an ultra low input bias current, JFET input, monolithic operational amplifier which also features low power, low offset voltage and excellent AC characteristics. Employing FET/Bipolar construction coupled with dielectric isolation this operational amplifier offers the lowest input bias currents (250fA typ.) available in any monolithic operational amplifier. The HA-5180/5180A has another unique feature in which the offset bias current may be nulled by externally adjusting the offset voltage. For applications which require precision performance the HA-5180A offers an input offset voltage of 0.5 mV (max) while the HA-5180 offers 3 mV (max.)

The HA-5180/5180A also offers excellent AC performance not previously available in similar hybrid or monolithic op amp designs. The 2 MHz bandwidth and 7V/μs slew rate of the HA-5180/5180A extends the bandwidth and speed for applications such as very low drift sample and hold amplifiers and photo-current detectors. Other applications include use in electrometer designs, pH/Ion sensitive electrodes, low current oxygen sensors, long term precision integrators and very high impedance buffer measurement designs.

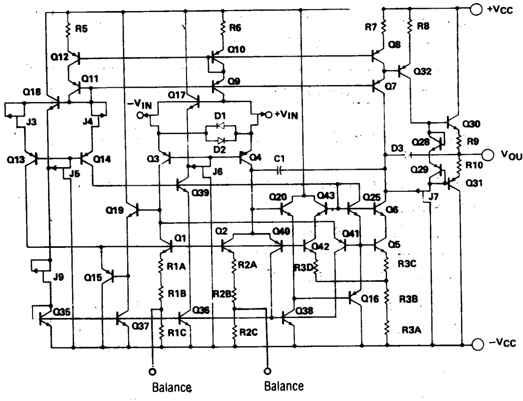
The HA-5180/5180A is packaged in an 8-pin (TO-99) can and an 8-lead cerdip and is pin compatible with most existing op amp configurations. The case of the TO-99 package is internally connected to pin 8 so that it may be connected to the same potential as the input. This feature helps minimize stray leakage to the case, helps shield the amplifier from external noise and reduces common mode input capacitance.

PINOUT


CASE
8
BAL 1
7 V+
IN- 2
-
+
6 OUT
IN+ 3
5 BAL
4
V-


BALANCE 1
IN- 2
IN+ 3
V- 4
8 N/C
7 V+
6 OUT
5 BALANCE

SCHEMATIC


+Vcc
R5
R6
R7
R8
Q10
Q8
Q12
Q11
Q32
Q9
Q7
Q18
Q17
-VIN
+VIN
D1
D2
J3
J4
Q30
D3
Q28
R9
VOUT
Q13
Q14
Q3
J6
Q4
C1
R10
Q29
Q31
J5
Q39
Q20
Q43
Q25
J7
Q19
Q6
Q1
Q2
Q40
Q41
Q42
Q5
J9
Q15
R1A
R2A
R3D
R3C
R1B
R2B
Q16
R3B
Q35
Q36
Q38
Q37
R1C
R2C
R3A
-Vcc
Balance
Balance

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated		Power Dissipation (Note 2)	300mW
Voltage Between V+ and V- Terminals	40V	Operating Temperature Range	
Differential Input Voltage	±40V	HA-5180/5180A-2	$-55°C \leq T_A \leq +125°C$
		HA-5180/5180A-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL RATINGS V+ = 15V, V- = -15V

PARAMETER	TEMP.	5180A-2			5180A-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.1	0.5		0.1	0.5	mV
	Full			1			1	mV
Average Offset Voltage Drift	Full		5			5		µV/°C
Bias Current (note 3)	+25°C		250	1000		250	1000	fA
	Full		100	500		6	30	pA
Offset Current (Note 3)	+25°C		30	200		30	200	fA
	Full		6	30		1	5	pA
Common Mode Range	Full	±10	±12		±10	±12		V
Differential Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Noise Voltage, 0.1Hz to 10Hz	+25°C		5			5		µVp-p
Input Noise Voltage Density	+25°C							
fo = 10Hz			200			200		$nV/\sqrt{Hz}$
fo = 100Hz			120			120		$nV/\sqrt{Hz}$
fo = 1000Hz			70			70		$nV/\sqrt{Hz}$
Input Noise Current (f=1kHz)	+25°C		0.01			0.01		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	200k	1M		200k	1M		V/V
	Full	150k			150k			V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110		90	110		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C		110			110		kHz
Output Current (Note 8)	+25°C	±10	±15		±10	±15		mA
Output Resistance (Note 9)	+25°C		25			25		Ω
TRANSIENT RESPONSE								
Overshoot	+25°C		30	50		30	50	%
Rise Time	+25°C		75			75		ns
Slew Rate	+25°C	4	7		4	7		V/µs
Settling Time (Note 10)	+25°C		2			2		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		0.7	1		0.8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		85	105		dB

ELECTRICAL RATINGS V+ = 15V, V- = -15V

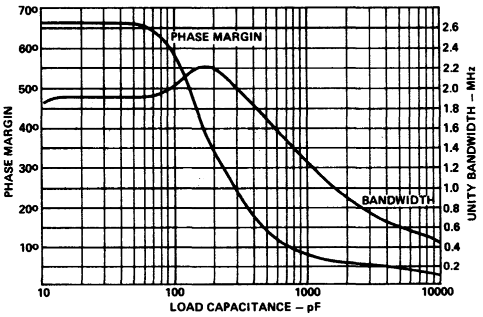
PARAMETER	TEMP.	5180-2			5180-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		1	3		1	3	mV
	Full			4			4	mV
Average Offset Voltage Drift	Full		5			5		µV/°C
Bias Current (Note 3)	+25°C		250	1000		250	1000	fA
	Full		100	500		6	30	pA
Offset Current (Note 3)	+25°C		30	200		30	200	fA
	Full		6	30		1	5	pA
Common Mode Range	Full	±10	±12		±10	±12		V
Differential Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Noise Voltage, 0.1Hz to 10Hz	+25°C		5			5		Vp-p
Input Noise Voltage Density	+25°C							
fo = 10Hz			200			200		$nV/\sqrt{Hz}$
fo = 100Hz			120			120		$nV/\sqrt{Hz}$
fo = 1000Hz			70			70		$nV/\sqrt{Hz}$
Input Noise Current (f=1kHz)	+25°C		0.01			0.01		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	200k	1M		200k	1M		V/V
	Full	150k			150k			V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110		90	110		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C		110			110		kHz
Output Current (Note 8)	+25°C	±10	±15		±10	±15		mA
Output Resistance (Note 9)	+25°C		25			25		Ω
TRANSIENT RESPONSE								
Overshoot	+25°C		30	50		30	50	%
Rise Time	+25°C		75			75		ns
Slew Rate	+25°C	4	7		4	7		V/µs
Settling Time (Note 10)	+25°C		2			2		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		0.7	1		0.8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		85	105		dB

NOTES:

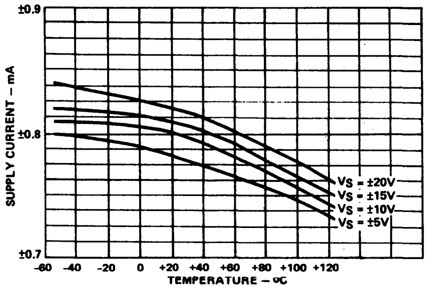
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.9 mW/°C for operation at ambient temperatures above +75°C.
3. This parameter is guaranteed by design and is not 100% tested.
4. $V_{OUT} = \pm 10V$; $R_L = 2k$. Gain dB = 20 log $_{10}$Av.
5. $V_{CM} = \pm 10V$ D.C.
6. $R_L = 2k$
7. $R_L = 2k$, $V_{peak} = 10V$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. $V_{OUT} = \pm 10V$.
9. Output resistance specified under open loop conditions (f = 100Hz)
10. Settling time is specified to 0.1% of final value for a 10V output step and $A_V = -1$.
11. $V_{SUPP} = \pm 5V$ D.C. to $\pm 20V$ D.C.

PERFORMANCE CURVES

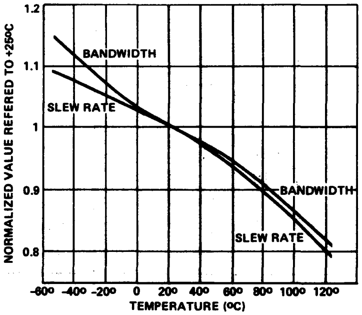
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



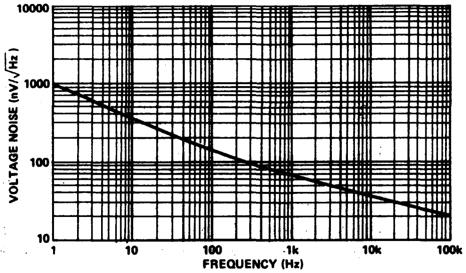
SUPPLY CURRENT VS. TEMPERATURE



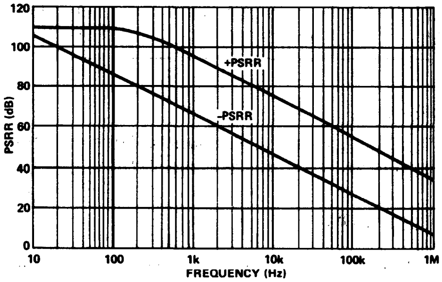
NORMALIZED AC PARAMETERS VS. TEMPERATURE



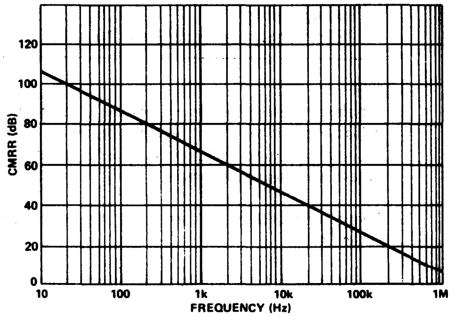
INPUT VOLTAGE NOISE VS. FREQUENCY



PSRR VS. FREQUENCY

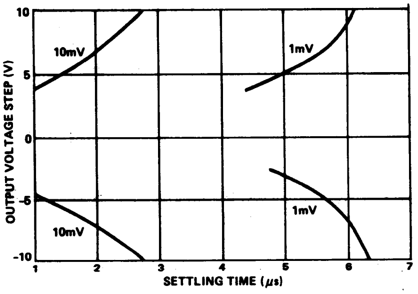


CMRR VS. FREQUENCY

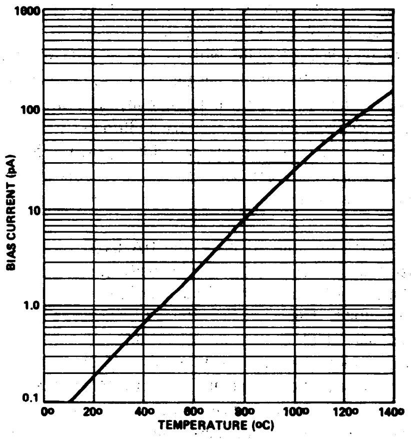


PERFORMANCE CURVES (Continued)

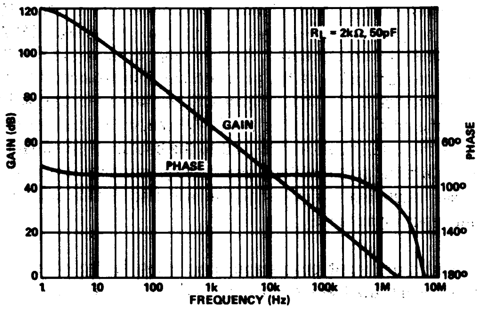
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



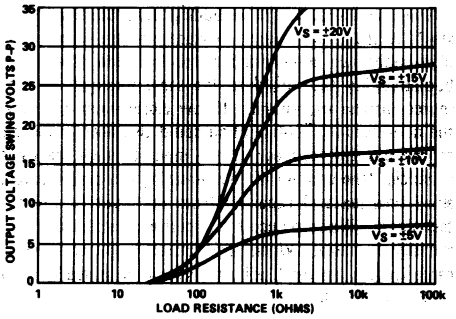
BIAS CURRENT VS. TEMPERATURE



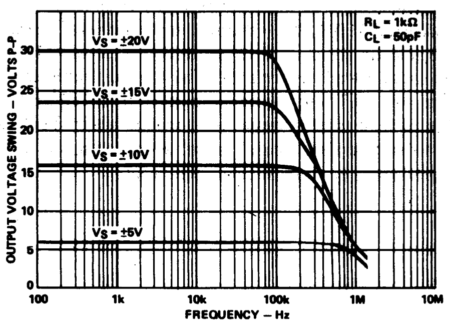
OPEN LOOP FREQUENCY RESPONSE



OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



OUTPUT VOLTAGE SWING VS. FREQUENCY



The HA-5180/5180A offers one of the lowest input bias currents of any monolithic operational amplifier and is ideal for use in applications for measuring signals from very high impedance or very low current sources. To fully utilize the capabilities of the HA-5180/5180A care should be taken to minimize noise pickup and current leakage paths with the use of shielding and guarding techniques and by placing the device as close as possible to the signal source. The small size and low quiesent current (possible battery operation) of the HA-5180/5180A allows easy installation at the signal source or inside a probe. The HA-5180/5180A is internally compensated and is capable of driving long signal cables which have several hundred pF capacitive loading.

If it is not possible to place the HA-5180 very close to the signal source then the use of shielded coaxial cable will offer the best isolation of the high impedance signal line from external noise sources. However, the effects of leakage, capacitance and vibrational noise should be taken into account when using coaxial cables. Leakage can be minimized by using cables with very high insulation resistance (such as polyethylene or Virgin Teflon). For example, the current to voltage converter circuit (as shown in Fig. 1) will eliminate leakage across the insulation of the cable by forcing the signal line to the same potential as the shield. This circuit also provides fast response to input signals because the cable capacitance is never forced to be charged or discharged. However, the cable capacitance directly increases the input capacitance of the circuit and could cause the circuit to become unstable; if so, adding capacitance across Rf will stablilize the circuit again. Leakage can also be reduced in the high-impedance non-inverting configuration (see Fig. 2) by bootstrapping the shield to the same potential as the signal source instead of ground. If low closed-loop gains are used, the non-inverting configuration could also become unstable due to the positive feedback to the input through the cable capacitance. One method of compensating this circuit is to place a small (low leakage) capacitor from the input to ground. This technique will also reduce the effective capacitance presented to the signal source. When large closed-loop gains and/or long cable lengths are used, a buffer should be added to the circuit to drive the shield.

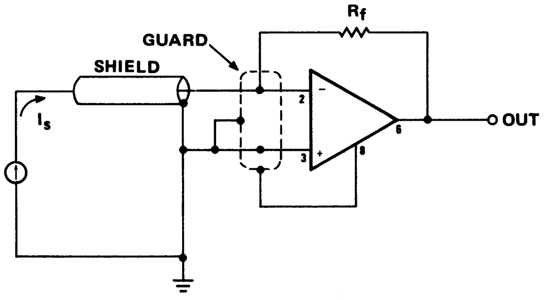


Figure 1. CURRENT TO VOLTAGE CONVERTER

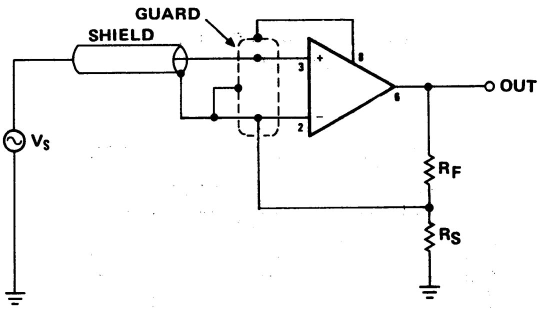


Figure 2. VERY HIGH IMPEDANCE NON-INVERTING AMPLIFIER

When using coaxial cable with the HA-5180 the cable should be kept as rigid and vibration free as possible. Frictional movement of the shield over the insulation can generate electrical charge which is picked up by the high impedance signal line as noise. Movement and bending of the cable can also cause charge. movement due to small changes in cable capacitance and capacitance to surrounding objects. Another source of noise currents is that which is generated by the movement of a conductor in a magnetic feild.

For lowest leakage at the device inputs either use a teflon IC socket or connect the signal line to the HA-5180/5180A inputs using teflon standoffs. A guard ring, as shown in Fig. 3, applied to both sides of the pc board and bootstrapped to the same potential as the input signal will minimize leakage paths across the pc board. Pin 8 of the TO-99 can, which is internally tied to the case, should also be tied to the bootstrap potential to help minimize noise pickup and leakage currents across the package insulation. This technique will also reduce common mode input capacitance.

Cleanliness of circuit boards and components is also important for achieving low leakage currents. Printed circuit boards and components should be thoroughly cleaned by using a low residue solvent such as TMC Freon, rinsed by deionized water and dried with nitrogen. The circuit board should be protected from high contamination and high humidity environments. A good quality conformal coating with low dielectric absorption provides the best protection from humidity and contamination.

Input protection is generally not necessary when designing with the HA-5180/5180A. Many electrometer type devices, especially CMOS, require elaborate zener protection schemes which may compromise overall performance. The Harris dielectric isolation process and JFET input design enables the HA-5180/5180A to withstand input signals several volts beyond either supply and large differential signals equal to the rail-to-rail supply voltage without damage or degradation of performance.

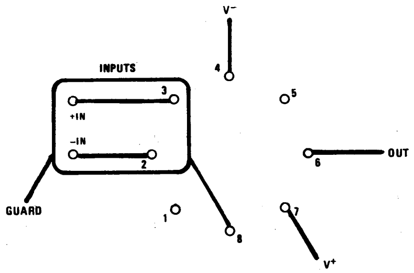

V⁻
4
INPUTS
3
+IN
−IN
2
5
6
OUT
GUARD
1
8
7
V⁺

Figure 3. GUARD RING EXAMPLE

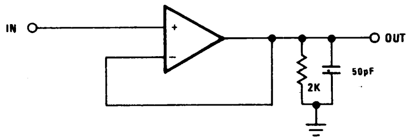

IN
+
−
OUT
2K
50pF

Figure 4. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT

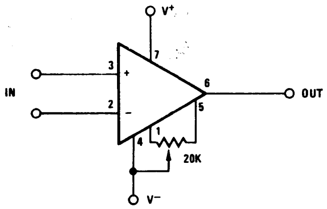
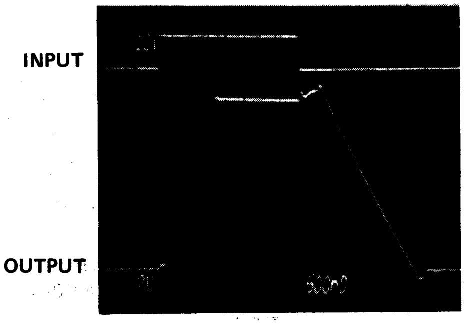

V⁺
7
3
+
IN
2
−
6
OUT
5
1
4
20K
V⁻

Figure 5. SUGGESTED OFFSET ADJUSTMENT CIRCUIT

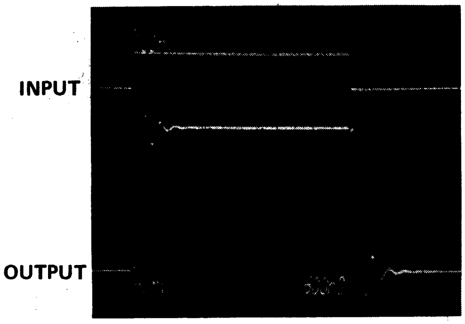
LARGE SIGNAL RESPONSE

VERTICAL SCALE (Volts: 5V/DIV INPUT)
(Volts: 2V/DIV OUTPUT)
HORIZONTAL SCALE (TIME: 500ns/DIV)



SMALL SIGNAL RESPONSE

VERTICAL SCALE (Volts: 100mV/DIV INPUT)
(Volts: 50mV/DIV OUTPUT)
HORIZONTAL SCALE (TIME: 500ns/DIV)



HARRIS HA-5190/95

Wideband, Fast Settling Operational Amplifier

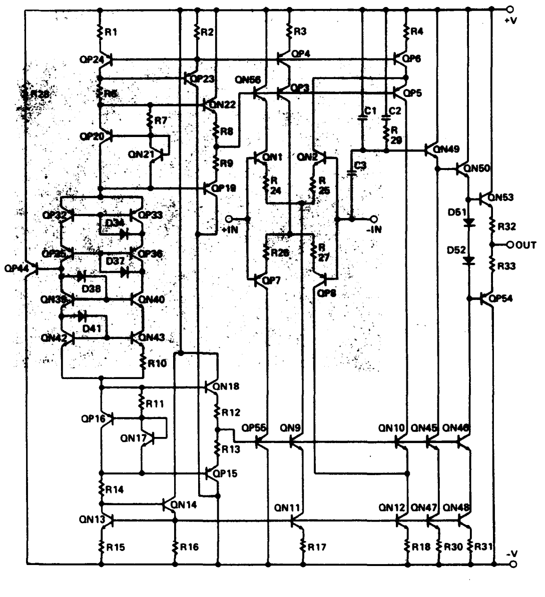
FEATURES

FAST SETTLING TIME	70ns
VERY HIGH SLEW RATE	200V/μs
WIDE GAIN-BANDWIDTH	150MHz
POWER BANDWIDTH	6.5MHz
LOW OFFSET VOLTAGE	3mV
INPUT VOLTAGE NOISE	6nV/√Hz
MONOLITHIC BIPOLAR CONSTRUCTION	

APPLICATIONS

- FAST, PRECISE D/A CONVERTERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- REPLACE COSTLY HYBRIDS

SCHEMATIC


+V
R1
R2
R3
R4
QP24
QP23
QN56
QP3
QP4
QP6
QP5
R5
R28
R7
QN22
R8
C1
C2
R29
QP20
QN21
R9
QN1
QN2
C3
QN49
QN50
QP19
R24
R25
QN53
+IN
-IN
D51
R32
OUT
D52
R33
QP54
QP32
QP33
D34
QP35
D37
QP36
QP44
D38
QN39
QN40
D41
QN42
QN43
R10
R26
R27
QP7
QP8
QN18
R11
R12
QP16
QN17
R13
QP55
QN9
QN10
QN45
QN46
QP15
R14
QN14
QN11
QN12
QN47
QN48
QN13
R15
R16
R17
R18
R30
R31
-V

GENERAL DESCRIPTION

HA-5190/5195 are monolithic operational amplifiers featuring an ultimate combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with dielectric isolation, these devices are capable of delivering an unparalleled 200V/μs slew rate with a settling time of 70ns (0.1%, 5V output step). These truly differential amplifiers are designed to operate at gains ≥ 5 without the need for external compensation. Other outstanding HA-5190/5195 features are 150MHz gain-bandwidth-product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 3mV offset voltage and 6.0nV input voltage noise (at 1kHz).

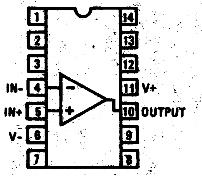
With 200V/μs slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. 150MHz gain-bandwidth-product, 6.5MHz power bandwidth, and 5mV offset voltage make HA-5190/5195 ideally suited for a variety of pulse and wideband video amplifier applications.

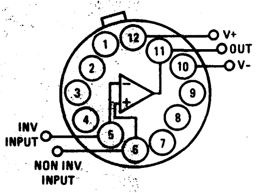
The HA-5190/5195 are available in metal can (TO-5), 20 pin LCC, and 14 pin ceramic packages.

At temperatures above +75°C, a heat sink is required for HA-5190. (See note 2). HA-5190 is specified over the -55°C to +125°C range while HA-5195 is specified from 0°C to +75°C.

PINOUTS

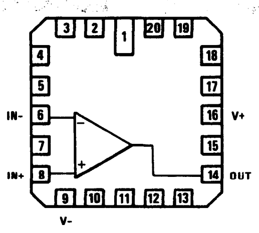
TOP VIEWS


1
2
3
4
5
6
7
14
13
12
11
10
9
8
IN-
IN+
V-
V+
OUTPUT


1
2
3
4
5
6
7
8
9
10
11
12
V+
OUT
V-
INV INPUT
NON INV INPUT

CASE TIED TO V-

LH0032 PINOUT


3
2
1
20
19
4
5
6
7
8
18
17
16
15
14
9
10
11
12
13
IN-
IN+
V+
OUT
V-

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals		35V
Differential Input Voltage		6V
Output Current		50mA (Peak)
Internal Power Dissipation (Note 2)		870mW (Cerdip); 1W (TO-8) Free Air
Operating Temperature Range:	(HA-5190)	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
	(HA-5195)	$0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range		$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; $R_L = 200$ ohms, unless otherwise specified.

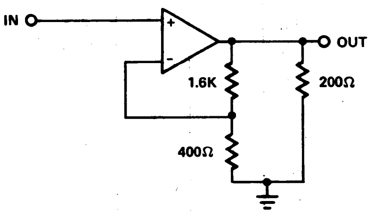
		HA-5190 -55°C to +125°C			HA-5195 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3.0	5.0		3.0	6	mV
	FULL			10.0			10.0	mV
Average Offset Voltage Drift	FULL		20			20		μV/°C
Bias Current	+25°C		5	15		5	15	μA
	FULL			20			20	μA
Offset Current	+25°C		1	4		1	4	μA
	FULL			6			6	μA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±5			±5			V
Input Noise Voltage (f = 1kHz, $R_g = 0\Omega$)	+25°C		6			6		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	74			74			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		150			150		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±5	±8		±5	±8		V
Output Current (Note 3)	+25°C	25	30		25	30		mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	5	6.5		5	6.5		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		13	18		13	18	ns
Overshoot	+25°C		8			8		%
Slew Rate	+25°C	160	200		160	200		V/μs
Settling Time:								
5V Step to 0.1%	+25°C		70			70		ns
5V Step to 0.01%	+25°C		100			100		ns
2.5V Step to 0.1%	+25°C		50			50		ns
2.5V Step to 0.01%	+25°C		80			80		ns
POWER REQUIREMENTS								
Supply Current	FULL		19	28		19	28	mA
Power Supply Rejection Ratio (Note 9)	FULL	70	90		70	90		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7mW/°C for operation at ambient temperatures above +75°c. Heat sinking required at temperatures above +75°c. T_{JA} = 115°C/W; T_{JC} = 35°C/W. Thermalloy model 6007 heat sink recommended.
3. $R_L = 200\Omega, C_L < 10pF, V0 = \pm 5V$
4. $V_{CM} = \pm 5V$.
5. $V_O = 90mV$.
6. $A_V = 10$.
7. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.
8. Refer to Test Circuits section of data sheet.
9. $V_{SUPPLY} = \pm 5$ VDC to ± 15 VDC

TEST CIRCUITS

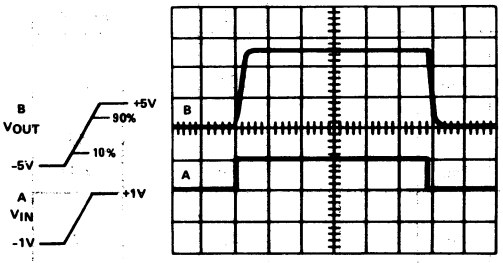
LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT*



AV = 5
*$C_L \leq 10pF$

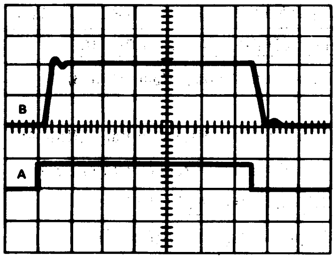
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A = 0.5V/Div., B = 4.0V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

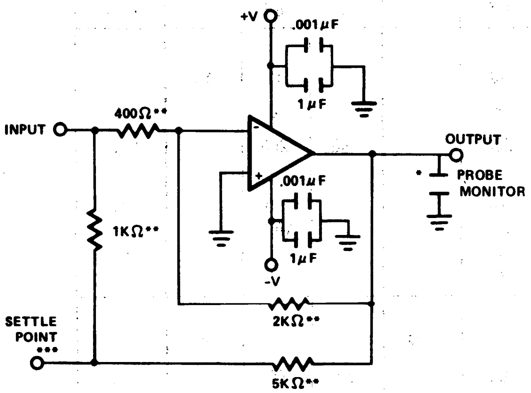


SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: A=50mV/Div., B=100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)



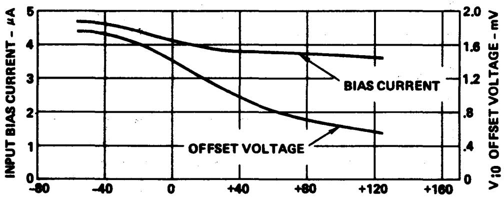
SETTLING TIME TEST CIRCUIT



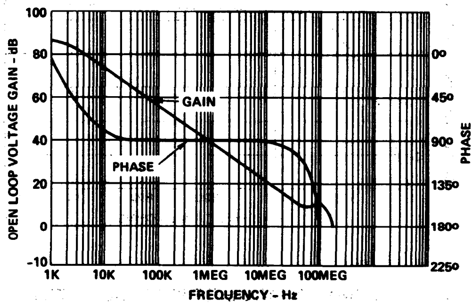
- * Load Capacitance should be less than 10pF.
- ** It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched.
- *** SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

PERFORMANCE CURVES

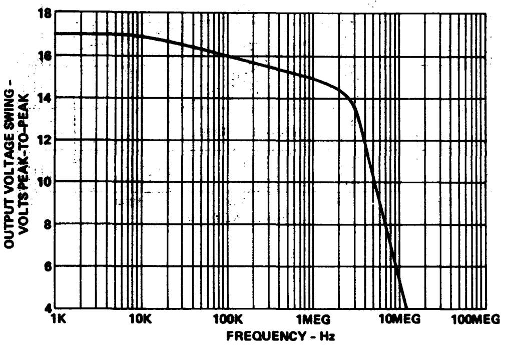
V+ = +15V, V- = -15V, T_A = +25°C unless otherwise stated.



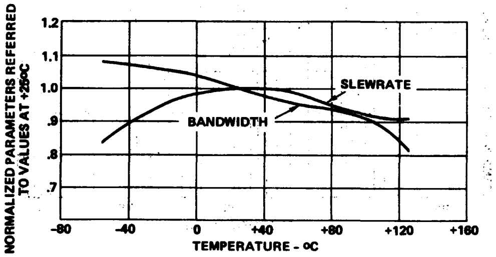
INPUT OFFSET VOLTAGE AND BIAS CURRENT VS. TEMPERATURE



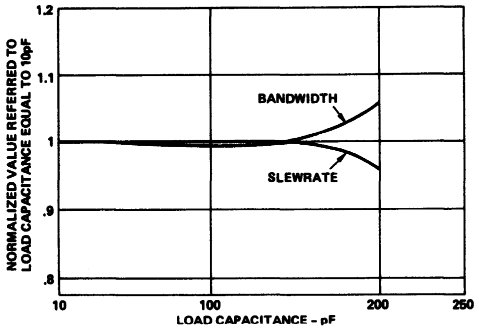
OPEN LOOP FREQUENCY RESPONSE



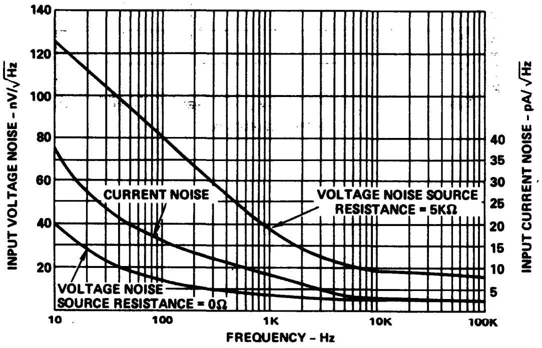
OUTPUT VOLTAGE SWING VS. FREQUENCY



NORMALIZED AC PARAMETERS VS. TEMPERATURE

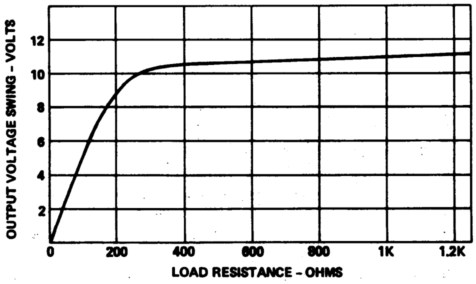


NORMALIZED AC PARAMETERS VS. LOAD CAPACITANCE

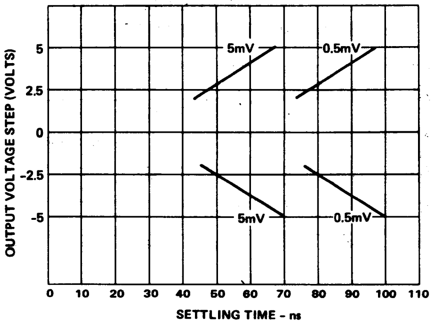


INPUT NOISE VOLTAGE AND NOISE CURRENT VS. FREQUENCY

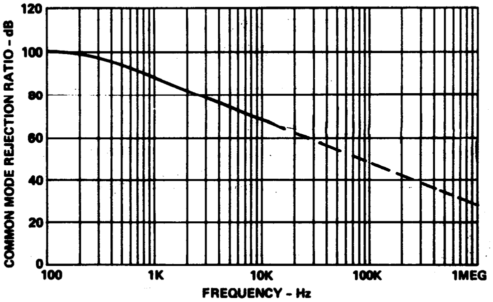
OUTPUT VOLTAGE SWING
VS. LOAD RESISTANCE



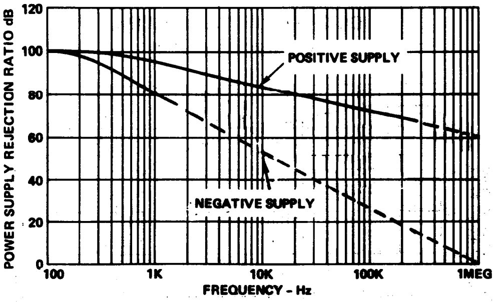
SETTLING TIME FOR VARIOUS
OUTPUT STEP VOLTAGES



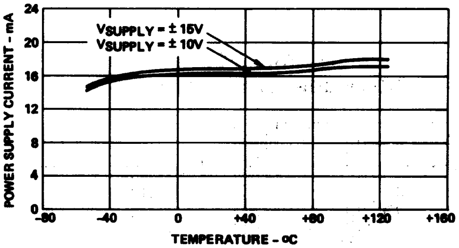
COMMON MODE REJECTION RATIO
VS. FREQUENCY



POWER SUPPLY REJECTION
RATIO VS. FREQUENCY



POWER SUPPLY CURRENT
VS. TEMPERATURE



APPLYING THE HA-5190/5195

1. **POWER SUPPLY DECOUPLING:** Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. **STABILITY CONSIDERATIONS:** HA-5190/5195 is stable at gains ≥ 5. Gains < 5 are covered elsewhere in this data sheet. Feedback resistors should be of carbon composition located as near to the input terminals as possible.

3. **WIRING CONSIDERATIONS:** Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.

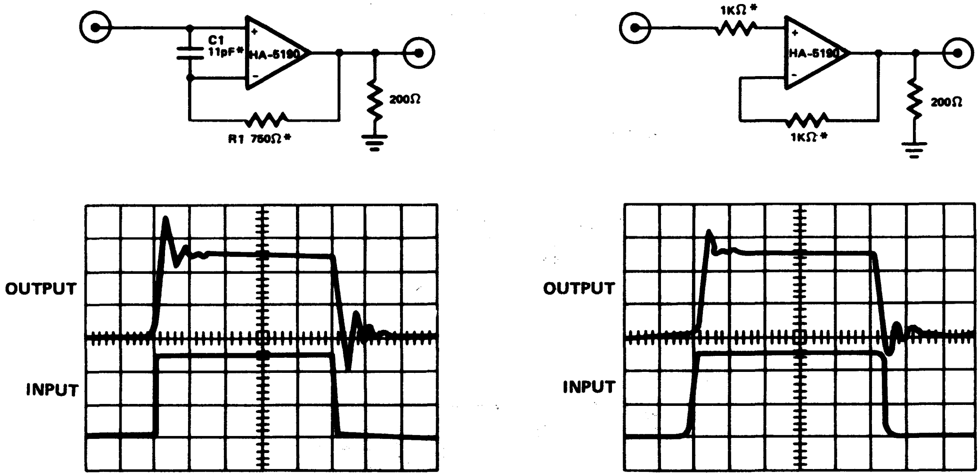
4. **OUTPUT SHORT CIRCUIT:** HA-5190/5195 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device.

5. **HEAVY CAPACITIVE LOADS:** When driving heavy capacitive loads (≥100pF) a small resistor (≈100Ω) should be conected in series with the output and inside the feedback loop.

APPLICATIONS

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY

NONINVERTING

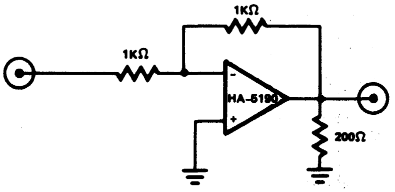


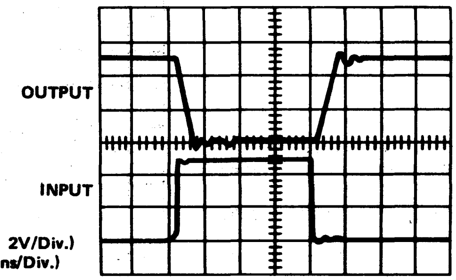
Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

* Values were determined experimentally for optimum speed and settling time.

R1 and C1 should be optimized for each particular application to ensure best overall frequency response.

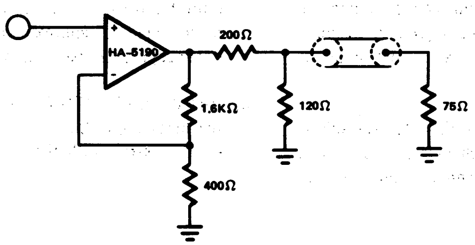
INVERTING



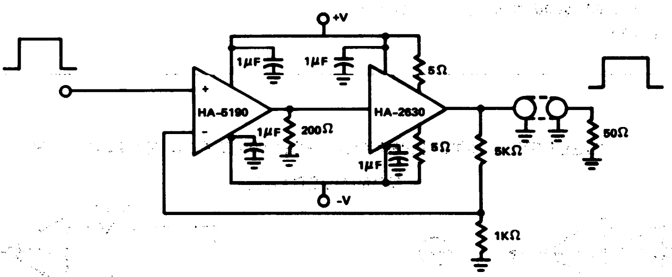


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (50ns/Div.)

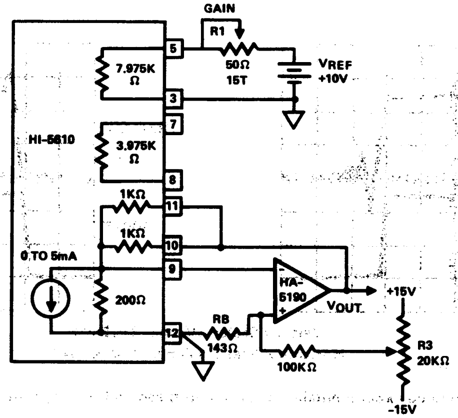
VIDEO PULSE AMPLIFIER/75Ω COAXIAL DRIVER

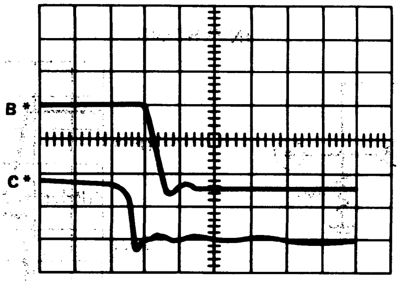

HA-5190
200Ω
1.6KΩ
120Ω
75Ω
400Ω

VIDEO PULSE AMPLIFIER COAXIAL LINE DRIVER


+V
1µF
1µF
5Ω
HA-5190
1µF
200Ω
HA-2630
5Ω
1µF
-V
5KΩ
50Ω
1KΩ

FAST DAC OUTPUT BUFFER


GAIN
R1
5
50Ω
15T
VREF
+10V
7.975K Ω
3
7
HI-5610
3.975K Ω
8
1KΩ
11
1KΩ
10
0 TO 5mA
9
200Ω
HA-5190
VOUT
+15V
RB
143Ω
12
100KΩ
R3
20KΩ
-15V



Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 50ns/Div.)

B = V_{OUT} C = DIGITAL INPUT

* Time delay between B and C represents total time delay for 0V to +5V full scale coded change.

HARRIS

HV-1000/1000A

Induction Motor Energy Saver

FEATURES

- OPERATES DIRECTLY OFF 120V/240V AC LINE – NO POWER SUPPLY REQUIRED
- 50Hz OR 60Hz OPERATION
- PRODUCES POWER SAVINGS FROM 10% TO 50% FOR MOTORS WITH LIGHT OR VARIABLE LOADS
- SCR OUTPUT STAGE TRIGGERS TRIAC DIRECTLY
- LOAD ANTICIPATOR SENSES SHOCK LOADS AND RESPONDS INSTANTLY WITH FULL POWER
- WITHSTANDS LINE SURGES TO 3500V
- CAUSES MOTOR TO RUN QUIETER, COOLER
- CAN BE MOUNTED INSIDE MOTOR
- NEEDS ONLY 3 RESISTORS, 3 CAPACITORS AND A TRIAC TO ASSEMBLE COMPLETE CONTROLLER

APPLICATIONS

- MACHINE TOOLS
- INDUSTRIAL SEWING MACHINES
- HEAT PUMPS
- PRESSES
- CONVEYORS
- DISC PACK DRIVES
  - ► ANY APPLICATION WHERE FOR SOME OF THE TIME THE MOTOR IS DRIVING LESS THAN ITS RATED LOAD

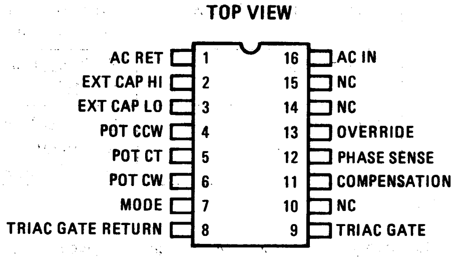
DESCRIPTION

The HV-1000 and HV-1000A are energy saving, induction motor, control circuits designed to reduce the power consumed by single phase induction motors. HV-1000 is for 120V AC use and HV-1000A for 240V AC use.

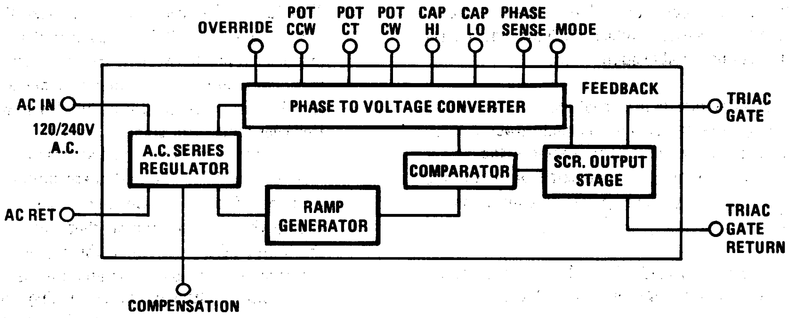
The controller circuit senses the load on the motor and then controls a TRIAC to apply reduced voltage to lightly loaded motors, full voltage to heavily loaded motors.

The HV-1000/1000A are available in a 16 lead plastic DIP. Ideal for mounting inside induction motors, they can also be mounted in a heat sunk circuit box for external, after market application.

PINOUT


TOP VIEW
AC RET 1
EXT CAP HI 2
EXT CAP LO 3
POT CCW 4
POT CT 5
POT CW 6
MODE 7
TRIAC GATE RETURN 8
16 AC IN
15 NC
14 NC
13 OVERRIDE
12 PHASE SENSE
11 COMPENSATION
10 NC
9 TRIAC GATE

FUNCTIONAL DIAGRAM


OVERRIDE
POT CCW
POT CT
POT CW
CAP HI
CAP LO
PHASE SENSE
MODE
AC IN
120/240V A.C.
AC RET
PHASE TO VOLTAGE CONVERTER
FEEDBACK
A.C. SERIES REGULATOR
COMPARATOR
SCR. OUTPUT STAGE
RAMP GENERATOR
TRIAC GATE
TRIAC GATE RETURN
COMPENSATION

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Input Voltage (With 5k Input Resistor)	3500V_{PEAK}	Storage Temperature	-40°C to +100°C
Input Voltage (Without Input Resistor)	±400V_{PEAK}	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	500mW	Output Current (10 microsecond Pulse)	500mA
Operating Temperature Range	0°C to +75°C		

ELECTRICAL CHARACTERISTICS See Note (a)

HV-1000/1000A using its internal power factor settings (pins 4, 5, 6, 7 shorted together). See Figure 1 for definition of θc, the current zero crossing, and θt, the TRIAC trigger point. Frequency = both 50Hz and 60Hz unless otherwise stated.

PARAMETER	DEFINITION	MIN	TYP	MAX	UNITS
Skew (b)	Difference Between Positive and Negative θt for $\theta c = 32°$	0	±6.5		Degrees
Load Anticipator Trip Point (60Hz Operation)	Value of θc at which Load Anticipator Trips at 60Hz	16	23		Degrees
Load Anticipator (c) Trip Point (50Hz Operation)	Value of θc at which Load Anticipator Trips at 50Hz	13	19		Degrees
Full Load Power Factor Setting	Value of θc at which $\theta c = \theta t$	39	43	47	Degrees
Full Load Power Factor (d)	Power Factor when $\theta c = \theta t$	.68	.73	.77	Power Factor
No Load Power Factor Setting	Value of θc when $\theta t = 146°$		32		Degrees
Maximum Input Voltage	Breakover Voltage of Input Protection SCRs	400	500		V_{PEAK}
Current Drain	RMS Input Current to chip (Pin 16)			2.0	mA RMS
Maximum Output Voltage	Breakover Voltage of Output Stage with Input to Chip Biased Normally with AC Power	600	800		V_{PEAK}

NOTES:

(a) No guarantee of power savings can be given since the savings achieved depend entirely on the motor and its application. However, for a completely unloaded motor driving only a flywheel or a pulley, power savings of 50% are typical. It is not uncommon to observe savings of as much as 80%. In all applications the percentage of power saved will depend on how much of the time the motor runs lightly loaded. Harris Application Note 542 covers the subject of selecting suitable applications.

(b) The presence of skew results in partial rectification of the AC power through the motor and reduced power savings. The skew numbers shown here may decrease the power savings of an unloaded motor as indicated on a rotating wheel type, electric, utility power meter by approximately 10% maximum.

The skew is greatest at no load ($\theta c = 32°$) and decreases linearly to zero as the motor approaches full load.

(c) The effect of a shock load is to shift θc (the current zero crossing) temporarily closer to the voltage zero crossing. If the shock is severe enough to perturb θc all the way back to the load anticipator trip point, the HV-1000 will discontinuously switch (trip) to full power. The anticipator trip point is increased by the absolute value of an external potentiometer, 10k ohms increasing it about 6 degrees. A circuit utilizing an external potentiometer is shown in Figure 6.

(d) This full load power factor is typical of a wide variety of U.S., single phase, 60Hz, capacitor start induction motors of power levels between ¼ HP and 1 HP. Many other motors, both larger and smaller and operating at 50Hz, can also be driven satisfactorily by this power factor setting. However, there are some motors for which this full load power factor setting is not satisfactory, being either too high or too low. To suit these motors, a potentiometer must be added as shown in Figure 6. The potentiometer should then be adjusted so that full voltage is applied to the motor ($\theta c = \theta t$) when the motor is fully loaded. An oscilloscope and a dynamometer are required to do this setup precisely, although other loading means can be substituted for a dynamometer, if none is available. The absolute value of the potentiometer determines the range of adjustment, a 5k potentiometer giving a much larger range of adjustment than a 1k potentiometer.

THEORY OF OPERATION

Induction motors run at a speed which depends primarily on the supply frequency, little on voltage. They draw almost a constant current regardless of the load – the motor responds to load with a change in power factor. Thus, a lightly loaded motor wastes energy by heating its windings with inductive current. The HV-1000/1000A measures the load using the current phase angle and then saves power by applying to the motor only sufficient voltage to drive the load.(1) The voltage is adjusted by TRIAC phase control.

The controller chip triggers a TRIAC which is in series with the motor. This varies the RMS voltage across the motor. The resulting voltage waveform across the motor is shown at the top of Figure 1. A motor can be characterized by the relation between the two parameters θc and θt, shown in Figure 1 for a typical motor. At point A, the motor is running fully loaded with full voltage applied, as it was designed. At point B, the motor is running lightly loaded with voltage reduced to the point of stalling. The function of the controller is to force the motor to operate along the load line AB, rather than AC which it does naturally. Figure 2 shows an example of the typical power savings which results when the controller chip is incorporated in a motor.

The key features of the circuit are firstly that all analog processing is carried out with the circuitry running entirely on 50Hz – 60Hz alternating current. Direct current is not used at all. Secondly it is integrated using dielectric isolation, with junction breakdowns of 400V. Junctions are stacked in both the input regulator and the SCR output stage so that the composite breakdown voltage of these stages is ±800V.

The analog processing which achieves the control function is explained conceptually in Figure 3. At any given load condition, the controller tries to force the motor current phase θc to a pre-programmed set phase. The phase to voltage converter measures the difference between the set phase and θc, and increments a pedestal voltage at a rate proportional to the difference, delaying the trigger point θt, where a reference ramp intersects the pedestal. The delayed triggering reduces the voltage applied to the motor, decreasing the motor winding current so that θc is forced to the set phase by the modulation of θt. The set phase is itself a slow function of θt, which produces the sloping controller characteristic fo Figure 1. This is achieved via the feedback path from the output stage to the phase to voltage converter.

An additional feature of the phase to voltage converter is the load anticipator. If θc is typically more than 0.42ms less than the set phase for 60Hz operation, which means the motor has received a sudden heavy load, the full line voltage is immediately applied to the motor. This allows the motor to respond at once to a step function load. If the load is abruptly removed, the controller cuts back the voltage applied to the motor over a time period set by the external time constant capacitor. This mechanism is described in more detail in Harris Application Note 542.

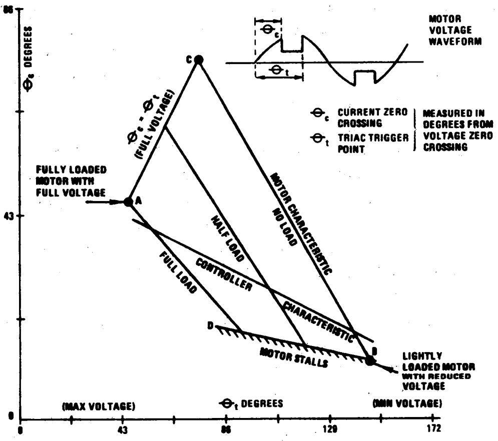


FIGURE 1

Voltage Waveform Characteristics of a TRIAC Controlled Induction Motor

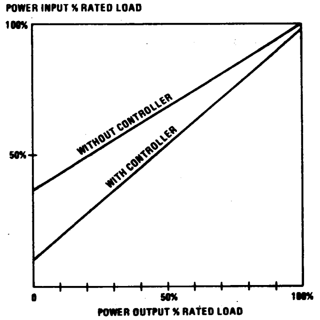


FIGURE 2

Power Savings as a Function of Load for a 1/3 HP Motor

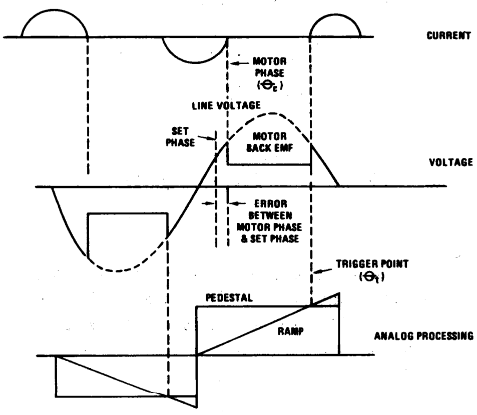


FIGURE 3

Relation of the Voltage and Current Waveforms to the Analog Processing Function

---

(1) This circuit principle was first described by F. J. Nola in U.S. Pat. 4052648.

Improvement of the efficiency of single phase induction motors may be achieved in two ways. For motors which drive a steady load equal to their rated capacity, the best method is to use a run capacitor with an auxiliary winding. This causes the internal field structure of the motor to resemble that of a three phase motor, an inherently more efficient arrangement. However, if a capacitor run motor is used to drive less than its rated load, its power consumption will usually be greater than a motor without a run capacitor. If this is the case for a significant fraction of the time, a run capacitor is not effective for improving efficiency. By contrast an electronic energy saving motor controller produces significant improvements in efficiency for lightly loaded motors, and is therefore, the best choice for motors which spend a significant part of their time lightly loaded. Electronic energy saving controllers are useful for machine tools, industrial sewing machines, heat pumps, presses, conveyors, disc pack drives, and commercial washing machines; in other words for any application where the load on the motor is either variable or ill defined. Run capacitors are useful for refrigerators, air conditioners, and ventilation fans – all applications where the load on the motor is steady and well defined. An electronic energy saving controller should not be applied in a circumstance where a motor is driving a constant, steady load equal to its rated load. In this circumstance the power dissipated in the TRIACs may actually increase the total power usage. However, it sometimes happens that induction motors are relatively conservatively designed, and the real power capability of the motor is greater than that stated. This may come about, for instance, because the motor may have been designed to operate with worst case low line voltage, say, 100V for a nominal 115V motor. In such a circumstance, an electronic energy saving controller can produce useful savings, because in reality, the conservative design of the motor is causing it to be operating at less than its full capability. This circumstance can be tested experimentally by connecting a power meter to the motor and then adjusting the set power factor with a potentiometer on the controller circuit to test whether reduced power consumption can be obtained. Once set up in this way, the controller will continue to give the motor just sufficient voltage to drive the load in hand, even if the line voltage drifts high. In other words, the energy saving controller also acts as a line voltage regulator. This is especially beneficial in areas where the line voltage fluctuates, since high line voltage can cause an induction motor to consume excessive amounts of power. For more information see Harris Application Note 542 "Using the HV-1000 Induction Motor Energy Saver".

APPLICATION CIRCUITS

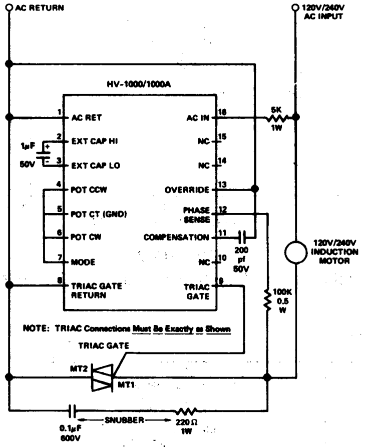

AC RETURN
120V/240V AC INPUT
HV-1000/1000A
1 AC RET
2 EXT CAP HI
3 EXT CAP LO
4 POT CCW
5 POT CT (GND)
6 POT CW
7 MODE
8 TRIAC GATE RETURN
16 AC IN
15 NC
14 NC
13 OVERRIDE
12 PHASE SENSE
11 COMPENSATION
10 NC
9 TRIAC GATE
1µF 50V
5K 1W
200 pf 50V
120V/240V INDUCTION MOTOR
100K 0.5 W
NOTE: TRIAC Connections Must Be Exactly as Shown
TRIAC GATE
MT2
MT1
SNUBBER
0.1µF 600V
220Ω 1W

FIGURE 4
Basic Application Circuit for the HV-1000

Basic Circuit

Figure 4 shows the basic application circuit for HV-1000. This circuit would be suitable for a 1/2 HP motor. For smaller or larger motors, the time constant capacitor (between pins 2 and 3) and snubber capacitor should be scaled in proportion to the size of the motor.

Operation with a Motor Switch

We recommend that the HV-1000 circuit should be permanently wired to the motor so that HV-1000 and motor are switched together. However, if this is not possible and a switch has to be placed in series with the motor between the motor and HV-1000, the circuit of Figure 5 should be used. The 0.01 μF (600V) capacitor keeps the phase sense property of HV-1000 alive while the switch is open, ensuring a smooth start-up when the switch is closed.

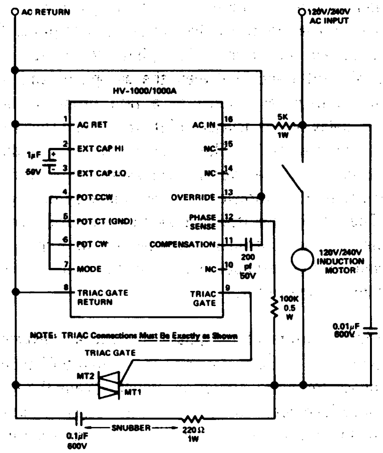

AC RETURN
120V/240V AC INPUT
HV-1000/1000A
1 AC RET
2 EXT CAP HI
3 EXT CAP LO
4 POT CCW
5 POT CT (GND)
6 POT CW
7 MODE
8 TRIAC GATE RETURN
16 AC IN
15 NC
14 NC
13 OVERRIDE
12 PHASE SENSE
11 COMPENSATION
10 NC
9 TRIAC GATE
1µF 50V
5K 1W
200 pf 50V
120V/240V INDUCTION MOTOR
100K 0.5 W
0.01µF 600V
NOTE: TRIAC Connections Must Be Exactly as Shown
TRIAC GATE
MT2
MT1
SNUBBER
0.1µF 600V
220Ω 1W

FIGURE 5
Application Circuit with Switch on Motor

To Adjust the Phase Setting

When it is required to adjust the full load, power factor setting, a potentiometer should be added as shown in Figure 6. The larger the absolute value of the potentiometer, the greater the range of adjustment. 1k ohms is recommended as a starting point if potentiometer adjustment is required. Adding the potentiometer also increases sensitivity of the load anticipator, a 10k potentiometer advances the anticipator trip point by 6 degrees. In general the smallest absolute value of potentiometer that covers the desired range of adjustment should be used. 10k ohms is the maximum potentiometer value normally needed.

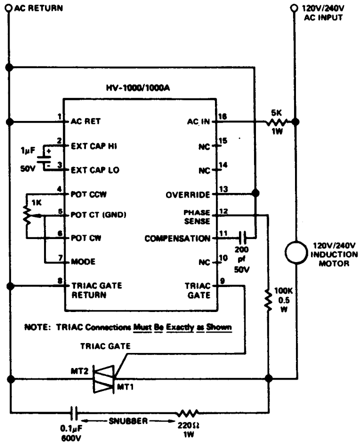

AC RETURN
120V/240V AC INPUT
HV-1000/1000A
1 AC RET
2 EXT CAP HI
3 EXT CAP LO
4 POT CCW
5 POT CT (GND)
6 POT CW
7 MODE
8 TRIAC GATE RETURN
16 AC IN
15 NC
14 NC
13 OVERRIDE
12 PHASE SENSE
11 COMPENSATION
10 NC
9 TRIAC GATE
5K 1W
1µF 50V
1K
200 pf 50V
120V/240V INDUCTION MOTOR
100K 0.5 W
NOTE: TRIAC Connections Must Be Exactly as Shown
TRIAC GATE
MT2
MT1
0.1µF 600V
SNUBBER
220Ω 1W

FIGURE 6
Application Circuit for HV-1000/1000A with Potentiometer to get Increased Anticipator Sensitivity and Adjustable Phase Setting

Electronic Override

Pin 13 is a TTL logic input which commands full output power. It can be activated with a switch as shown in Figure 7. The diode between pins 13 and 1 needs 5V capability, it is to prevent negative potentials being applied to pin 13.

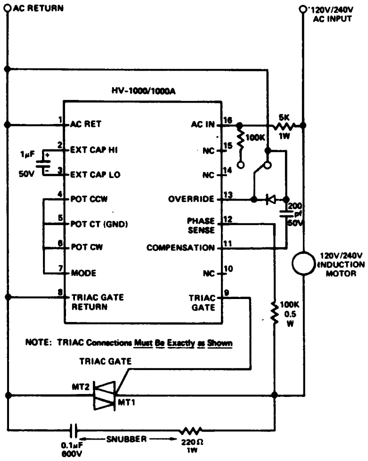

AC RETURN
120V/240V AC INPUT
HV-1000/1000A
1 AC RET
2 EXT CAP HI
3 EXT CAP LO
4 POT CCW
5 POT CT (GND)
6 POT CW
7 MODE
8 TRIAC GATE RETURN
16 AC IN
15 NC
14 NC
13 OVERRIDE
12 PHASE SENSE
11 COMPENSATION
10 NC
9 TRIAC GATE
100K
5K 1W
1µF 50V
200 pf 50V
120V/240V INDUCTION MOTOR
100K 0.5 W
NOTE: TRIAC Connections Must Be Exactly as Shown
TRIAC GATE
MT2
MT1
0.1µF 600V
SNUBBER
220Ω 1W

FIGURE 7
Application Circuit for HV-1000/1000A Illustrating Electronic Override

NOTES:

(a) Stability: A small number of motors, primarily amongst the larger (above 1 HP) single phase motors may not necessarily run in a stable fashion with the application circuit of Figure 4. The symptoms are irregular vibration and repeated jerky application of full power to the motor. An oscilloscope placed in differential mode across pins 2 and 3 will show rapid fluctuations in voltage instead of the steady voltage levels characteristic of control equilibrium. This and similar effects are described in Harris Application Note 542. The problem is helped by increasing the inertia on the shaft (e.g., adding a flywheel), by increasing the time constant capacitor and sometimes by adding a potentiometer and adjusting it for smaller power savings. If all these measures fail it may be that a special application circuit will be needed as described in Application Note 542. The effect is dependent on which company manufactured the motor.

(b) Selection of components: The TRIAC used should have a current rating which allows the locked motor current of the motor (often three or more times the run current) to be conducted for as long as this may persist. Normally heat sinking will be required to conduct away the heat of the TRIAC. The 5k input resistor only performs a useful purpose during voltage surges in excess of 600V. When this happens, internal crowbar clamps on chip between pins 1 and 16 break over and momentarily conduct about an ampere, causing thousands of volts to be dropped across the 5k resistor. For this reason the physically large size of a 1W resistor is needed, otherwise the terminals of the resistor would arc over. The time constant capacitor between pins 2 and 3 is normally chosen to be the smallest value that will allow the motor to run in a stable fashion. If it is chosen too large, the HV-1000 will not throttle back the voltage as quickly, if the load suddenly decreases. This effect reduces the power savings.

ANALOG

CMOS Analog Switches

3

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Standard Products Packaging Availability 3-3

Analog Switches Glossary 3-4

Selection Guide 3-5

Product Information 3-6

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

		Page
HI-200	Dual SPST CMOS Analog Switch	3-6
HI-201	Quad SPST CMOS Analog Switch	3-12
HI-201HS	High Speed Quad SPST CMOS Analog Switch	3-18
HI-300 thru 307	CMOS Analog Switches	3-27
HI-381/384/387/390	CMOS Analog Switches	3-32
HI-5040 thru 5051	CMOS Analog Switches	3-37
HI-5046A and HI-5047A	CMOS Analog Switches	3-37

Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H I 7 - 0200 - 5

PREFIX:
H (HARRIS)

FAMILY:
A — Analog
C — Communications
D — Digital
F — Filters
I — Interface
M — Memory
V — Analog, High Voltage
Y — Analog Hybrids

PACKAGE:
1 — Dual-In-Line, Ceramic
2 — Metal Can
3 — Dual-In Line, Plastic
4 — Leadless Carriers
5 — LCC Hybrid
7 — Mini-DIP, Ceramic
0 — Chip Form

PART NUMBER

TEMPERATURE:
1 — 0°C to +200°C ✻
2 — -55°C to +125°C
4 — -25°C to +85°C
5 — 0°C to +75°C
6 — 100% +25°C Probe (Dice Only)
7 — Dash-7 High Reliability Commercial Product. 0°C to +75°C
8 — Dash-8 Program HA2-2520-8 (Example only)
9 — -40°C to +85°C

✻ Special high temperature testing available on certain product types. Consult factory for availability.

Standard Products Packaging Availability

PACKAGE	PLASTIC DIP 3-		CERAMIC DIP 1-							CERAMIC MINI DIP 7-				METAL CAN 2-					SURFACE MOUNT LCC 4-	SURFACE MOUNT PLCC 4P-
TEMPERATURE	-5	-7	-1	-2	-4	-5	-7	-8	-9	-2	-4	-5	-8	-1	-2	-4	-5	-8	-8	-5
DEVICE NUMBER																				
HI-200	X			X	X	X	X	X						X	X	X	X	X		
HI-201	X		X	X	X	X	X	X											X	
HI-201HS	X			X	X	X		X											X	
HI-300	X			X		X		X							X		X	X		
HI-301	X			X		X		X							X		X	X		
HI-302	X			X		X		X												
HI-303	X			X		X		X												
HI-304	X			X		X		X							X		X	X		
HI-305	X			X		X		X							X		X	X		
HI-306	X			X		X		X												
HI-307	X			X		X		X												
HI-381	X			X		X		X							X		X	X		
HI-384	X			X		X		X												
HI-387	X			X		X		X							X		X	X		
HI-390	X			X		X		X												
HI-5040	X			X		X		X												
HI-5041	X			X		X		X												
HI-5042	X			X		X		X												
HI-5043	X			X		X		X											X	
HI-5044	X			X		X		X												
HI-5045	X			X		X		X											X	
HI-5046	X			X		X		X												
HI-5046A	X			X		X		X												
HI-5047	X			X		X		X												
HI-5047A	X			X		X		X												
HI-5048	X			X		X		X												
HI-5049	X			X		X		X												
HI-5050	X			X		X		X												
HI-5051	X			X		X		X												

Analog Switches Glossary

ANALOG SIGNAL RANGE (± Vs) - The maximum safe input voltage range.

BREAK-BEFORE-MAKE-DELAY (tOPEN) - The elapsed time between the turn-off of one switch and the corresponding turn-on of another switch for a common change in logic state. This delay is measured between the 50% points of the output transitions.

CHANNEL INPUT CAPACITANCE (C_{SOFF}) The capacitance between the analog input and ground with the channel "OFF." This capacitance consists primarily of the source-body capacitance.

CHANNEL OUTPUT CAPACITANCE (C_{DOFF}) The capacitance between the analog output and ground with the channel "OFF". This capacitance consists of the sum of the drain-body capacitances.

CHANNEL OUTPUT CAPACITANCE (C_{DON}) - The capacitance between the analog output and ground with the channel "ON".

CHARGE INJECTION - The amount of charge transferred to a specified load capacitance due to the switch changing state.

CROSSTALK - The amount of cross coupling from an "OFF" analog input to the output of another "ON" channel output.

DIGITAL INPUT CAPACITANCE - The capacitance between a digital input and ground.

INPUT LOW LEAKAGE CURRENT (I_{AL}) - The current measured at the digital input with a logic low applied.

INPUT LOW THRESHOLD (V_{AL}) - The maximum allowable voltage that can be applied to the digital inputs and still be recognized by the device as a low input.

INPUT HIGH LEAKAGE CURRENT (I_{AH}) - The current measured at the digital input with a logic high applied.

INPUT HIGH THRESHOLD (V_{AH}) - The minimum voltage that can be applied to the digital inputs and still be recognized by the device as a high input.

INPUT TO OUTPUT CAPACITANCE (CD_{SOFF}) - The capacitance between the analog input and output when the channel is "OFF".

"OFF" INPUT LEAKAGE CURRENT (I_{SOFF}) - The current measured at the input of an "OFF" channel with a a specified voltage applied to both input and output. This current consists largely of the diode leakage current of the source- body junctions.

OFF ISOLATION - The feedthrough of an applied signal through an "OFF" switch to the output. This feedthrough occurs through the source-body and drain-body capacitances and has a greater effect at high frequencies.

"OFF" OUTPUT LEAKAGE CURRENT (I_{DOFF}) - The current measured at the output of an "OFF" channel with a specified voltage applied to both input and output. This current is due largely to the diode leakages of the drain-body junctions.

"ON" CHANNEL LEAKAGE CURRENT (I_{DON}) - The current flowing through the source-body and drain body junctions of the "ON" channel. This current is measured with a specified voltage applied to both the input and output.

"ON" RESISTANCE (R_{ON}) - The series "ON" channel resistance measured between the input and output terminals under a specified range of input voltages.

SUPPLY CURRENT (I_S) - The current required from the power supply to operate the switch in a no load condition.

SWITCH TURN "OFF" TIME (t_{OFF}) - The time required to deactivate an "ON" switch to an "OFF" state. This time is measured from the 50% point of the logic input change to the time the output reaches 10% of the initial value.

SWITCH TURN "ON" TIME (t_{ON}) - The time required to activate an "OFF" switch to an "ON" state. This time is measured for the 50% point of the logic input to the time the output reaches 90% of the final value.

Selection Guide

CMOS SWITCHES

FUNCTION	DEVICE	R_{ON} (Ω) (TYP)	$I_{D(OFF)}$(NA) (TYP)	$t_{(ON)}$(NS) (TYP)	$t_{(OFF)}$(NS) (TYP)	P_D (mW) (TYP)
SPST	HI-5040	50	0.5	370	280	1.5
2 x SPST	HI-200	55	1	240	180	15
	HI-300	35	0.04	210	160	1
	HI-304	35	0.04	210	160	0.3
	HI-381	35	0.04	210	160	1
	HI-5048	25	0.5	370	280	1.5
	HI-5041	50	0.5	370	280	1.5
4 x SPST	HI-201	55	1	180	155	15
	HI-201HS	30	0.3	30	40	120
SPDT	HI-301	35	0.04	210	160	1
	HI-305	35	0.04	210	160	0.3
	HI-387	35	0.04	210	160	1
	HI-5050	25	0.5	370	280	1.5
	HI-5042	50	0.5	370	280	1.5
2 x SPDT	HI-303	35	0.04	210	160	1
	HI-307	35	0.04	210	160	0.3
	HI-390	35	0.04	210	160	1
	HI-5051	25	0.5	370	280	1.5
	HI-5043	50	0.5	370	280	1.5
DPST	HI-5044	50	0.5	370	280	1.5
2 x DPST	HI-302	35	0.04	210	160	1
	HI-306	35	0.04	210	160	0.3
	HI-384	35	0.04	210	160	1
	HI-5049	25	0.5	370	280	1.5
	HI-5045	50	0.5	370	280	1.5
DPDT	HI-5046A	25	0.5	370	280	1.5
	HI-5046	50	0.5	370	280	1.5
4PST	HI-5047A	25	0.5	370	280	1.5
	HI-5047	50	0.5	370	280	1.5

NOTE: All data represents typical room temperature specifications at ±15V supplies. For guaranteed and tested specifications, consult the device data sheet.

HARRIS

HI-200

Dual SPST CMOS Analog Switch

FEATURES

• ANALOG VOLTAGE RANGE	±15V
• ANALOG CURRENT RANGE	80mA
• TURN-ON TIME	240ns
• LOW R_{ON}	55Ω
• LOW POWER DISSIPATION	15mW
• TTL/CMOS COMPATIBLE	

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

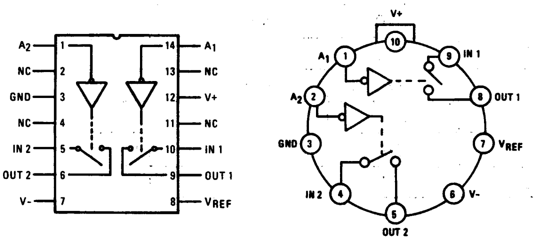
HI-200 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (240ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-200 operates without any applications problems induced by latch-up or SCR mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

HI-200 is available in DIP and metal (TO-100) cans. HI-200-2 is specified from -55°C to +125°C while HI-200-5 operates from 0°C to +75°C. HI-200 is functionally and pin compatible with other available "200 series" switches.

PINOUT

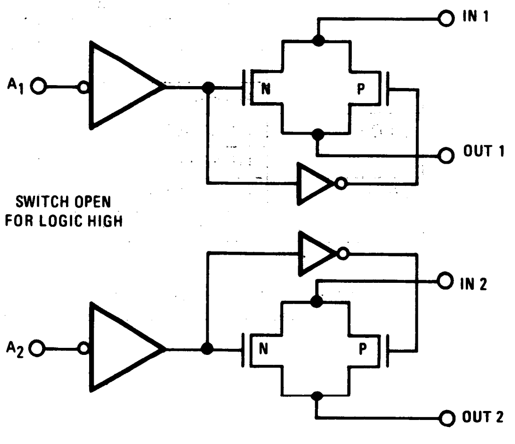
TOP VIEWS



A2
NC
GND
NC
IN 2
OUT 2
V-
1
2
3
4
5
6
7
14
13
12
11
10
9
8
A1
NC
V+
NC
IN 1
OUT 1
VREF
V+
10
A1
1
IN 1
9
A2
2
OUT 1
8
GND
3
7
VREF
IN 2
4
6
V-
5
OUT 2

CASE TIED TO V-

FUNCTIONAL DIAGRAM



IN 1
A1
N
P
OUT 1
SWITCH OPEN
FOR LOGIC HIGH
IN 2
A2
N
P
OUT 2

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	44V (±22)	Total Power Dissipation*	450mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	$+V_{Supply}$ +4V	HI-200-2	-55°C to +125°C
	$-V_{Supply}$ -4V	HI-200-4	-25°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-200-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 6mW/°C Above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified

Supplies = +15V, -15V; V_{REF} = Open; V_{AH}(Logic Level High) = 2.4V V_{AL}(Logic Level Low) = +0.8V

For Test Conditions, consult Performance Characteristics

		HI-200-2 -55°C to +125°C			HI-200-5** 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		72	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 6)	+25°C		1	5		1	50	nA
	Full		100	500		10	500	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 6)	+25°C		1	5		1	50	nA
	Full		100	500		10	500	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		1	5		1	50	nA
	Full		100	500		10	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	2.4			2.4			V
I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		60			60		ns
t_{on}, Switch on Time	+25°C		240	500		240		ns
t_{off}, Switch off Time	+25°C		330	500		500		ns
"Off Isolation" (Note 4)	+25°C		70			70		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, } Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, } Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)								
P_D, Power Dissipation	+25°C		15			15		mW
	Full			60			60	mW
I^+, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
I^-, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:

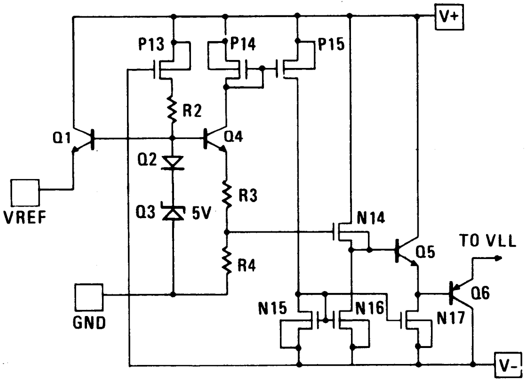
1. $V_{OUT} = \pm 10V$, I_{OUT} = 1mA
2. Digital Inputs are MOS gates - Typical Leakage is Less Than 1nA.
3. V_{AH} = 4.0V
4. V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = 3VRMS, f = 100kHz
5. V_A = +3V or V_A = 0V for Both Switches
6. Refer to leakage current measurement diagram on page 3-9

** Note: HI-200-4 has same specifications as HI-200-5 over the temperature range -20°C to +85°C.

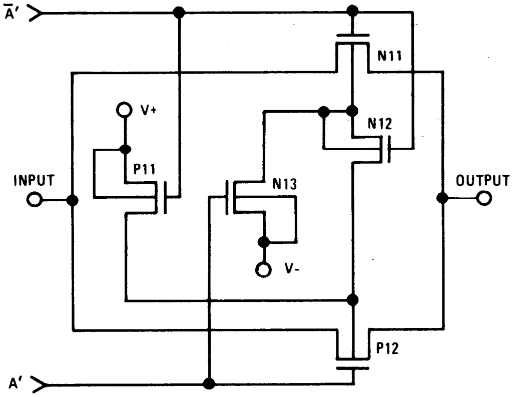
SCHEMATIC DIAGRAMS

TTL/CMOS
REFERENCE CIRCUIT

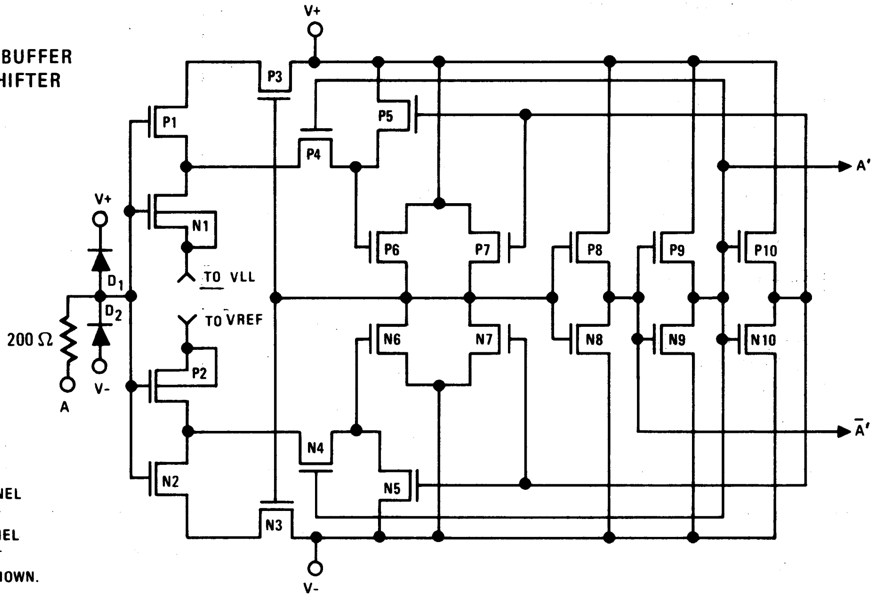
V-REF CELL


V+
P13
P14
P15
R2
Q1
Q4
Q2
R3
Q3
5V
VREF
N14
Q5
TO VLL
R4
Q6
GND
N15
N16
N17
V-

SWITCH CELL


A̅'
N11
V+
N12
P11
INPUT
N13
OUTPUT
V-
P12
A'

DIGITAL INPUT BUFFER
AND LEVEL SHIFTER


V+
P3
P1
P5
P4
A'
V+
N1
P6
P7
P8
P9
P10
D1
TO VLL
D2
TO VREF
200 Ω
N6
N7
N8
N9
N10
P2
V-
A
A̅'
N4
N2
N5
N3
V-

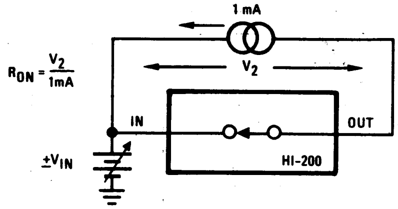
ALL N-CHANNEL
BODIES TO V-

ALL P-CHANNEL
BODIES TO V+

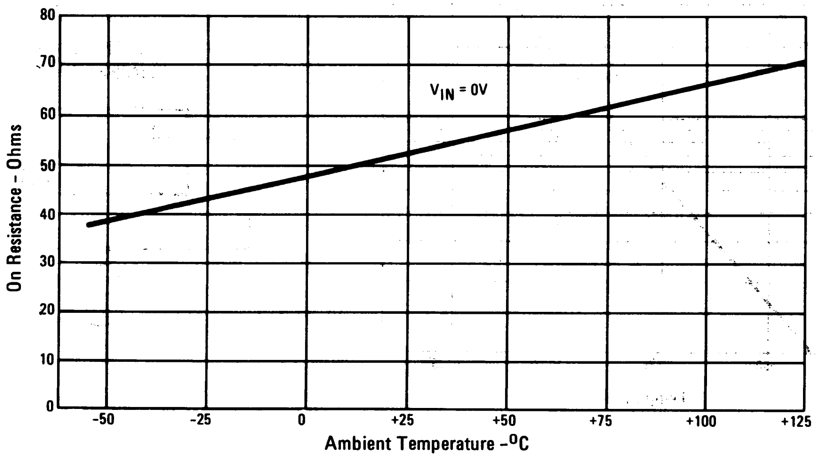
EXCEPT AS SHOWN.

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 2.4V$ $V_{AL} = 0.8V$ AND V_{REF} = OPEN).

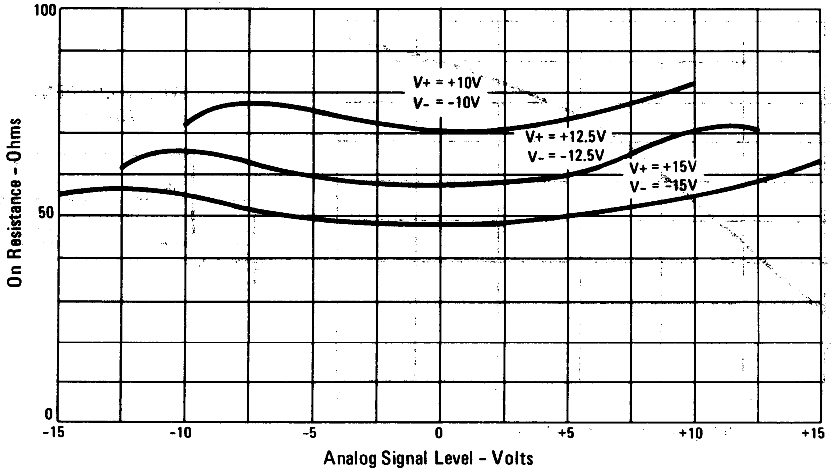
ON RESISTANCE vs. ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE


1 mA
$R_{ON} = \frac{V_2}{1mA}$
V_2
IN
OUT
HI-200
$\pm V_{IN}$

ON RESISTANCE vs. TEMPERATURE

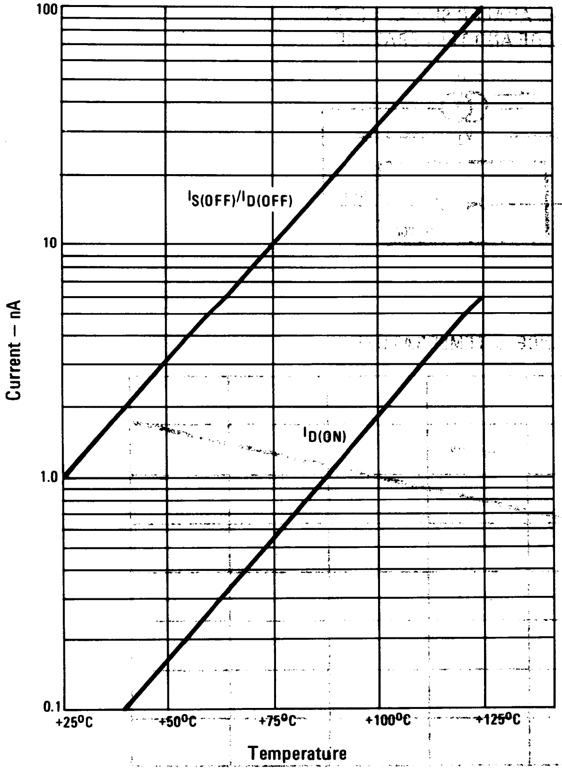


(HI-200) ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

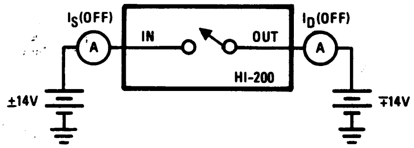


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (Continued)

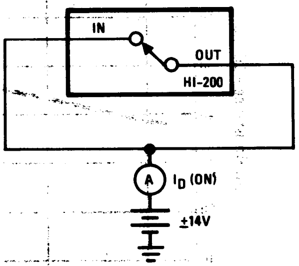
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-200)



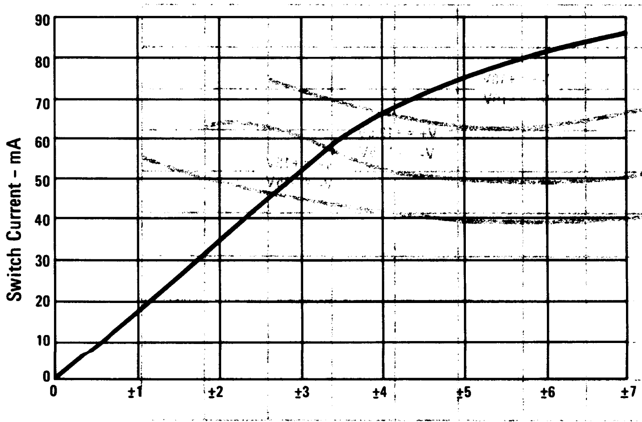
OFF LEAKAGE CURRENT vs. TEMPERATURE


$I_S(OFF)$
$I_D(OFF)$
A
IN
OUT
A
HI-200
±14V
∓14V

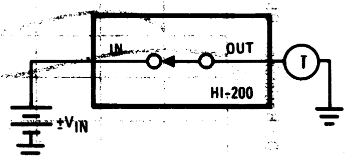
ON LEAKAGE CURRENT vs. TEMPERATURE


IN
OUT
HI-200
A
I_D (ON)
±14V

SWITCH CURRENT vs. VOLTAGE

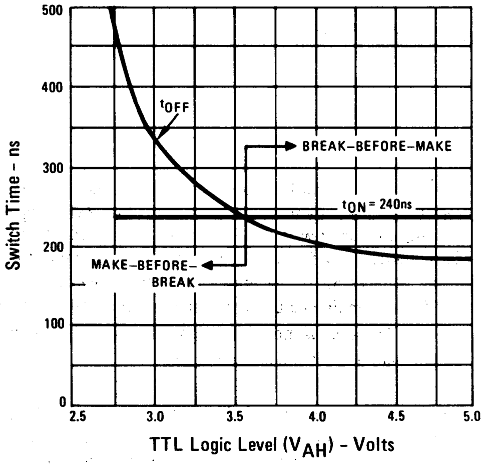


SWITCH CURRENT vs. VOLTAGE

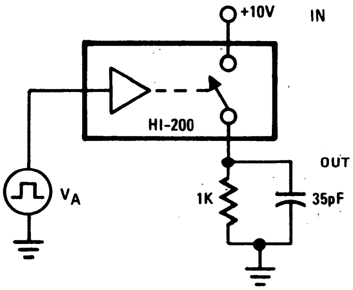

IN
OUT
HI-200
T
$\pm V_{IN}$

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (Continued)

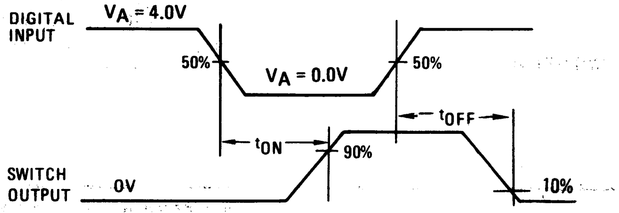
(HI-200)
SWITCH TIME vs. TTL LOGIC LEVEL



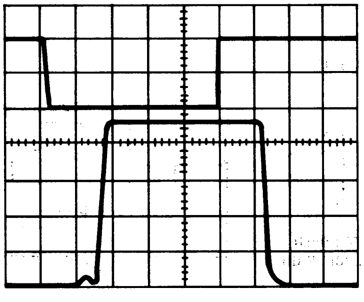
ON/OFF SWITCH TIME vs.
LOGIC LEVEL


+10V
IN
HI-200
OUT
V_A
1K
35pF

SWITCHING WAVEFORMS

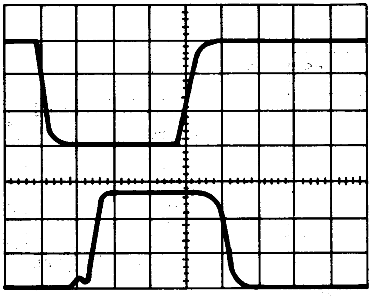

DIGITAL INPUT
V_A = 4.0V
50%
V_A = 0.0V
50%
t_{OFF}
t_{ON}
90%
SWITCH OUTPUT
0V
10%

t_{ON}, t_{OFF} (TTL INPUT)
V_{AH} = +4.0V



Top: TTL Input   Vertical: 2V/Div.
Bottom: Output   Horizontal: 200ns/Div.

t_{ON}, t_{OFF} (CMOS INPUT)
V_{REF} = OPEN, V_{AH} = +15V



Top: CMOS Input   Vertical: 5V/Div.
Bottom: Output   Horizontal: 200ns/Div.

HARRIS

HI-201

Quad SPST CMOS
Analog Switch

FEATURES

• ANALOG VOLTAGE RANGE	±15V
• ANALOG CURRENT RANGE	80mA
• TURN-ON TIME	185ns
• LOW R_{ON}	55 Ω
• LOW POWER DISSIPATION	15mW
• TTL/CMOS COMPATIBLE	

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

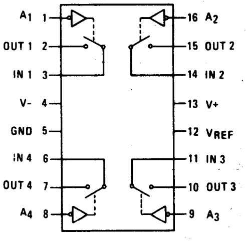
HI-201 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-201 operates without any applications problems induced by latch-up or SCR-mode phenomena.

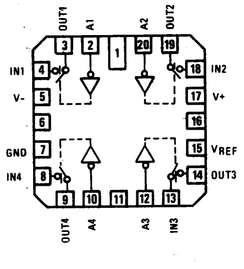
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

HI-201 is available in a 16 lead dual-in-line package and a 20 pin LCC package. HI-201-2 is specified from -55°C to +125°C while HI-201-5 operates from 0°C to +75°C. HI-201 is functionally and pin compatible with other available "200 series" switches.

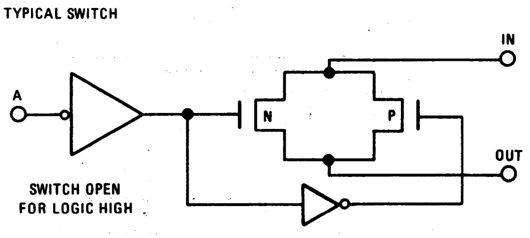
PIN OUT

TOP VIEWS


A1 1
OUT 1 2
IN 1 3
V- 4
GND 5
IN 4 6
OUT 4 7
A4 8
16 A2
15 OUT 2
14 IN 2
13 V+
12 VREF
11 IN 3
10 OUT 3
9 A3


OUT1
A1
A2
OUT2
3
2
1
20
19
IN1 4
V- 5
6
GND 7
IN4 8
18 IN2
17 V+
16
15 VREF
14 OUT3
9
10
11
12
13
OUT4
A4
A3
IN3

FUNCTIONAL DIAGRAM


TYPICAL SWITCH
A
IN
N
P
OUT
SWITCH OPEN
FOR LOGIC HIGH

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 4 and 13	44V (±22)
V_{REF} to Ground	+20V, -5V
Digital Input Voltage:	$V_{Supply}(+)$ +4V
	$V_{Supply}(-)$ -4V
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V
	$-V_{Supply}$ -2.0V

Total Power Dissipation*		750mW
Operating Temperature		
	HI-201-2	-55°C to +125°C
	HI-201-4	-25°C to +85°C
	HI-201-5	0°C to +75°C
Storage Temperature		-65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified :
Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V
For Test Conditions consult Performance Characteristics

		HI-201-2 -55°C to +125°C			HI-201-5 * 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		75	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 6)	+25°C		2	5		2	50	nA
	Full			500			250	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 6)	+25°C		2	5		2	50	nA
	Full			500			250	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		2	5		2	50	nA
	Full			500			250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	2.4			2.4			V
I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	µA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (Note 3)	+25°C		30			30		ns
t_{ON}, Switch ON Time	+25°C		185	500		185		ns
t_{OFF}, Switch OFF Time	+25°C		220	500		220		ns
"Off Isolation" (Note 4)	+25°C		80			80		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$ } Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$ } Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-to-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)								
P_D, Power Dissipation (Note 5)	+25°C		15			15		mW
	Full			60			60	mW
I+, Current (Pin 13)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
I-, Current (Pin 4)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

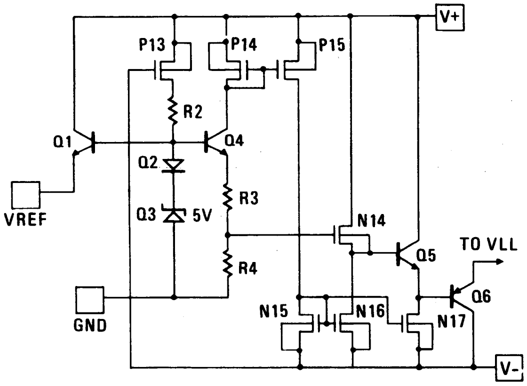
NOTES:
1. $V_{OUT} = \pm 10V$ I_{OUT} = 1mA
2. Digital Inputs are MOS gates - Typical Leakage is Less Than 1nA.
3. V_{AH} = 4.0V
4. V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = 3VRMS, f = 100kHz
5. V_A = +3V or V_A = 0V for All Switches
6. Refer to leakage current measurement diagram on page 3-15

* Note: HI-201-4 has same specifications as HI-201-5 over the temperature range -20°C to +85°C.

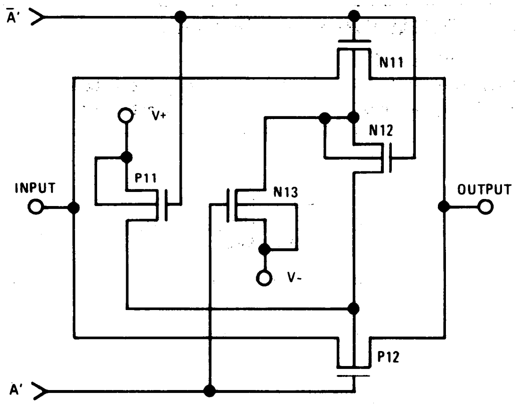
SCHEMATIC DIAGRAMS

TTL/CMOS
REFERENCE CIRCUIT

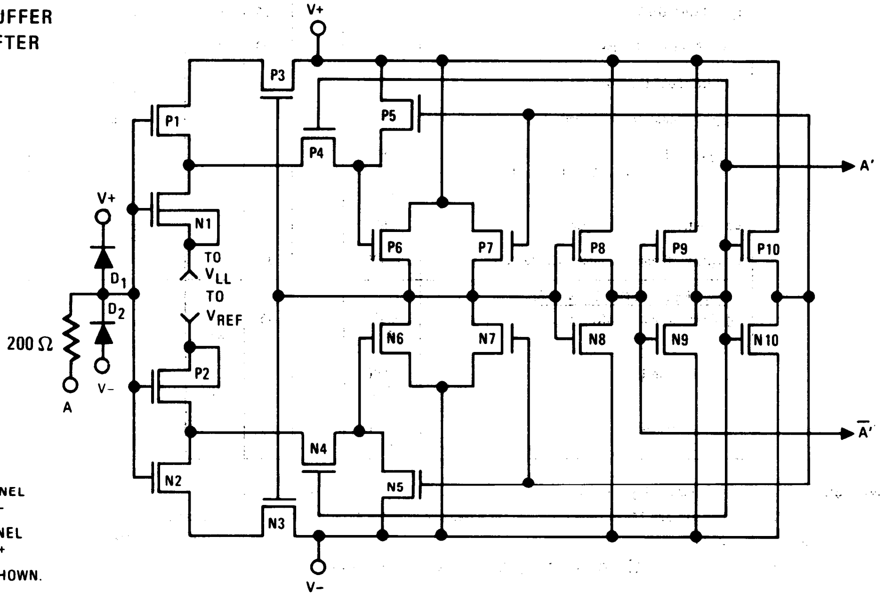
V-REF CELL


V+
P13
P14
P15
R2
Q1
Q4
Q2
R3
Q3
5V
VREF
N14
TO VLL
Q5
R4
Q6
GND
N15
N16
N17
V-

SWITCH CELL


Ā'
N11
V+
N12
P11
INPUT
N13
OUTPUT
V-
P12
A'

DIGITAL INPUT BUFFER
AND LEVEL SHIFTER


V+
P3
P1
P5
P4
A'
V+
N1
P6
P7
P8
P9
P10
TO
V_{LL}
D_1
D_2
TO
V_{REF}
200 Ω
N6
N7
N8
N9
N10
P2
V-
A
Ā'
N4
N2
N5
N3
V-

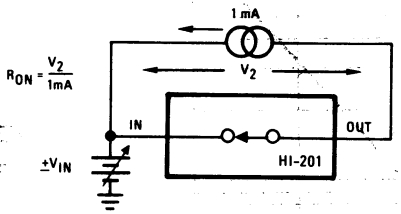
ALL N-CHANNEL
BODIES TO V-

ALL P-CHANNEL
BODIES TO V+

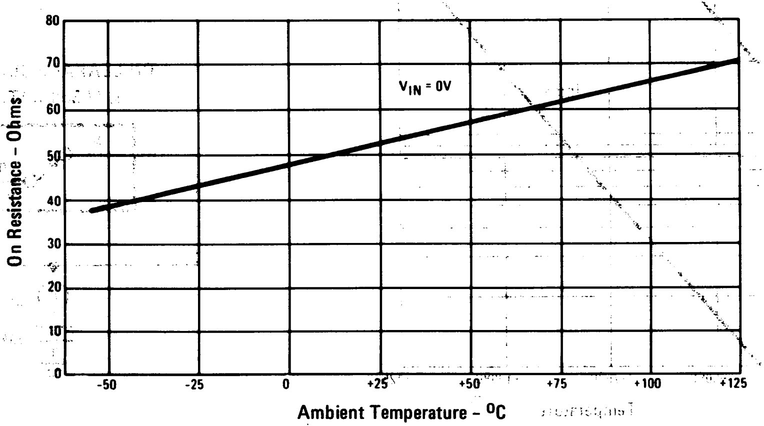
EXCEPT AS SHOWN.

(UNLESS OTHERWISE SPECIFIED $T_A = 25^{\circ}C$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 2.4V$ $V_{AL} = 0.8V$ AND V_{REF} = OPEN).

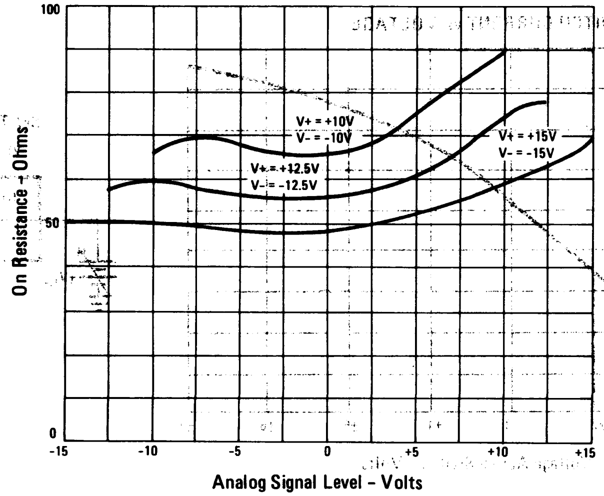
ON RESISTANCE vs. ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE


1 mA
$R_{ON} = \frac{V_2}{1mA}$
V_2
IN
OUT
HI-201
$\pm V_{IN}$

ON RESISTANCE vs. TEMPERATURE

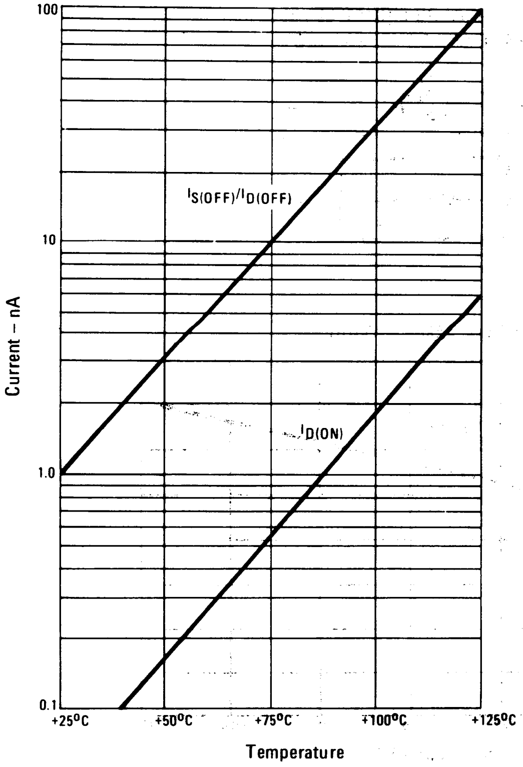


(HI-201)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

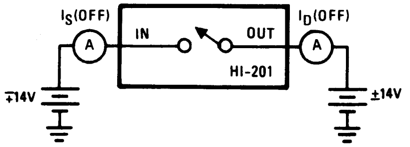


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (Continued)

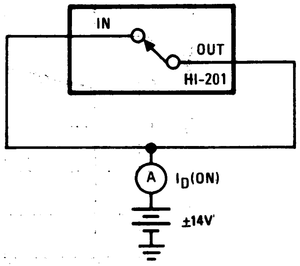
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-201)



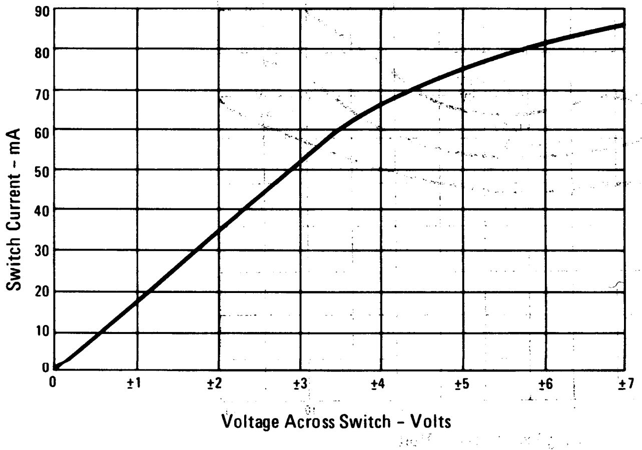
OFF LEAKAGE CURRENT vs. TEMPERATURE


I_S(OFF)
I_D(OFF)
A
IN
OUT
A
HI-201
∓14V
±14V

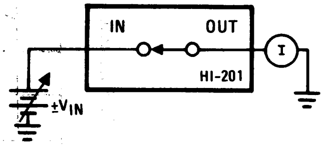
ON LEAKAGE CURRENT vs. TEMPERATURE


IN
OUT
HI-201
A
I_D(ON)
±14V

SWITCH CURRENT vs. VOLTAGE

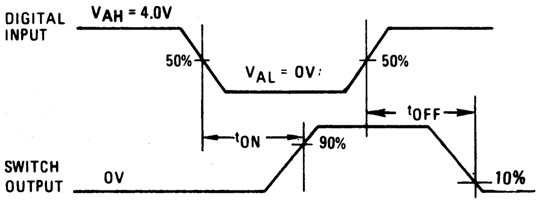


SWITCH CURRENT vs. VOLTAGE

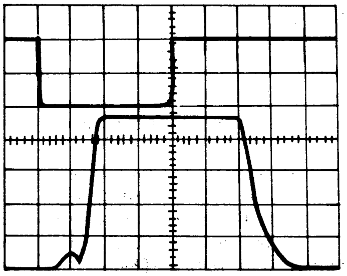

IN
OUT
HI-201
I
$\pm V_{IN}$

SWITCHING WAVEFORMS

LOGIC "0" = SWITCH ON

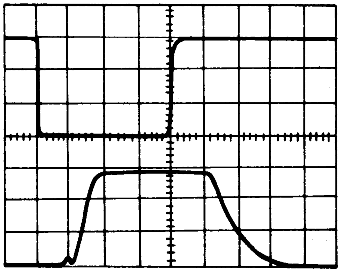

DIGITAL INPUT
V_{AH} = 4.0V
50%
V_{AL} = 0V
50%
t_{OFF}
t_{ON}
90%
SWITCH OUTPUT
0V
10%

t_{ON}, t_{OFF} (TTL INPUT)
V_{IN} = 4.0V



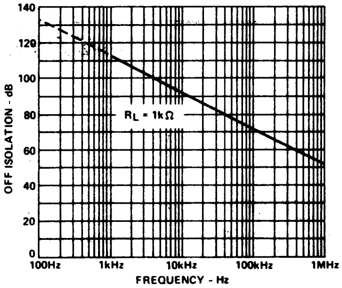
Top: TTL Input Horizontal: 100ns/Div.
Bottom: Output Vertical: 2V/Div.

t_{ON}, t_{OFF} (CMOS INPUT)
V_{REF} = OPEN, V_{IN} = +15V



Top: CMOS Input Vertical: 5V/Div.
Bottom: Output Horizontal: 100ns/Div.

OFF ISOLATION VS. FREQUENCY



HARRIS

HI-201HS

High Speed Quad SPST CMOS Analog Switch

FEATURES

• FAST SWITCHING TIMES	t_{on} = 30ns t_{off} = 40ns
• LOW ON RESISTANCE	30Ω
• PIN COMPATIBLE WITH STANDARD HI-201	
• WIDE ANALOG VOLTAGE RANGE (± 15V SUPPLIES)	±15V
• LOW CHARGE INJECTION (± 15V SUPPLIES)	10pC
• TTL COMPATIBLE	
• SYMMETRICAL SWITCHING	
ANALOG CURRENT RANGE	80mA

APPLICATIONS

- HIGH SPEED MULTIPLEXING
- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS
- INTEGRATOR RESET CIRCUITS

DESCRIPTION

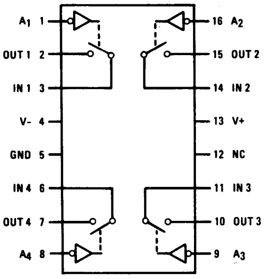
The HI-201HS is a monolithic CMOS Analog Switch featuring very fast switching speeds and low ON resistance. This integrated circuit consists of four independently selectable SPST switches and is pin compatible with the industry standard HI-201 switch.

Fabricated using silicon-gate technology and the Harris dielectric isolation process, this TTL compatible device offers improved performance over previously available CMOS analog switches. Featuring maximum switching times of 50ns, low ON resistance of 50Ω maximum, and a wide analog signal range, the HI-201HS is designed for any application where improved switching performance, particularly switching speed, is required. (A more detailed discussion on the design and application of the HI-201HS can be found in Application Note #543).

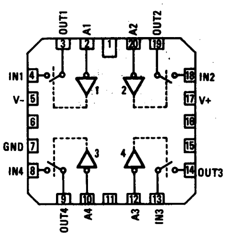
The HA-201HS is available in both plastic and ceramic 14 pin DIPs as well as a 20 pin LCC package. The HA-201HS-2 is specified over the temperature range from -55°C to +125°C and the -5 version from 0°C to +75°C. The HA-201HS-4 is also offered from -25°C to +85°C.

PINOUTS

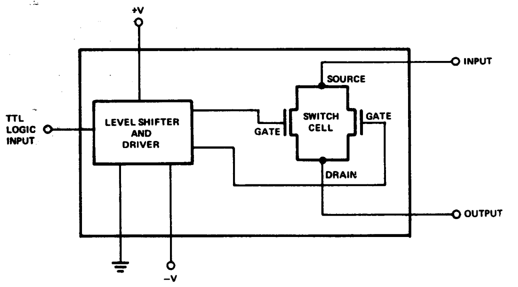
TOP VIEWS


A1 1
OUT1 2
IN1 3
V- 4
GND 5
IN4 6
OUT4 7
A4 8
16 A2
15 OUT2
14 IN2
13 V+
12 NC
11 IN3
10 OUT3
9 A3

LOGIC	SWITCH
0	ON
1	OFF


OUT1
A1
A2
OUT2
3
2
1
20
19
IN1 4
V- 5
6
GND 7
IN4 8
18 IN2
17 V+
16
15
14 OUT3
1
2
3
4
9
10
11
12
13
OUT4
A4
A3
IN3

FUNCTIONAL DIAGRAM


+V
INPUT
SOURCE
TTL LOGIC INPUT
LEVEL SHIFTER AND DRIVER
GATE
SWITCH CELL
GATE
DRAIN
OUTPUT
-V

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Between Pins 4 and 13)	36V
Digital Input Voltage (Pins 1, 8, 9, 16)	$+V_{SUPPLY}$ +4V $-V_{SUPPLY}$ -4V
Analog Input Voltage (One Switch) Pins 2, 3, 6, 7, 10, 11, 14, 15	$+V_{SUPPLY}$ +2.0V $-V_{SUPPLY}$ -2.0V

Total Power Dissipation (Note 2)	750mW
Maximum Junction Temperature	175°C
Operating Temperature	
HI-201HS-2	-55°C to +125°C
HI-201HS-4	-25°C to +85°C
HI-201HS-5	0°C to +75°C
Storage Temperature	-65°C to +150°C

ELECTRICAL CHARACTERISTICS Unless Otherwise Specified, Supplies = +15V, -15V; V_{AH} (Logic Level High) = 3.0V V_{AL} (Logic Level Low) = +0.8V, GND = 0V

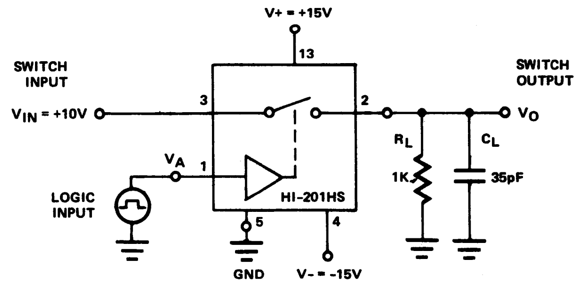
PARAMETER	TEMP.	HI-201HS-2			HI-201HS-5, -4			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 3)	+25°C		30	50		30	50	Ω
	Full			75			75	Ω
R_{ON} Match	+25°C		3			3		%
$I_{S(OFF)}$, Off Input Leakage Current	+25°C		.3	1		.3	1	nA
	Full			100			50	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C		.3	1		.3	1	nA
	Full			100			50	nA
$I_{D(ON)}$, On Leakage Current	+25°C		.1	1		.1	1	nA
	Full			100			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	+25°C	2.0			2.0			V
	Full	2.4			2.4			V
I_{AL}, Input Leakage Current (Low)	+25°C		200			200		μA
	Full			-500			-500	μA
I_{AH}, Input Leakage Current (High)(Note 9)	+25°C		20			20		μA
	Full			+40			+40	μA
SWITCHING CHARACTERISTICS								
t_{ON}, Switch ON Time (Note 4)	+25°C		30	50		30	50	ns
t_{OFF1}, Switch OFF Time (Note 4)	+25°C		40	50		40	50	ns
t_{OFF2}, Switch OFF Time (Note 4)	+25°C		150			150		ns
Output Settling Time 0.1%	+25°C		180			180		ns
"Off Isolation" (Note 5)	+25°C		72			72		dB
Crosstalk (Note 6)	+25°C		86			86		dB
Charge Injection (Note 7)	+25°C		10			10		pC
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		10			10		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		10			10		pF
$C_{D(ON)}$,	+25°C		30			30		pF
C_A, Digital Input Capacitance	+25°C		18			18		pF
$C_{DS(OFF)}$, Drain-to-Source Capacitance	+25°C		.5			.5		pF
POWER REQUIREMENTS (Note 8)								
P_D, Power Dissipation	+25°C		120			120		mW
	Full			240			240	mW
I^+, Current (Pin 13)	+25°C		4.5			4.5		mA
	Full			10.0			10.0	mA
I^-, Current (Pin 4)	+25°C		3.5			3.5		mA
	Full			6			6	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate 8mW/°C Above $T_A = +75^oC$
   $\theta_{jA} = 100^oC/W$ $\theta_{jC} = 32^oC/W$
3. $V_{OUT} = \pm 10V$, $I_{OUT} = 1mA$
4. $R_L = 1k\Omega$, $C_L = 35pF$, $V_{IN} = +10V$, $V_A = +3V$
   (See Switching Waveforms)
5. $V_A = 3V$, $R_L = 1K\Omega$, $C_L = 10pF$, $V_{IN} = 3$ VRMS, f = 100kHz
6. $V_A = 3V$, $R_L = 1K\Omega$, f = 100kHz, $V_{IN} = 3$ VRMS
7. $C_L = 1000pF$, $V_{IN} = 0V$, $R_{IN} = 0\Omega$
   $\Delta Q = C_L \times \Delta V_O$
8. $V_A = 3V$ or $V_A = 0$ for all switches
9. $V_A = 4V$

TEST CIRCUIT

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF1}, t_{OFF2})

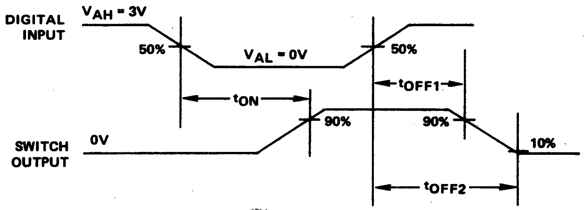

V+ = +15V
13
SWITCH INPUT
SWITCH OUTPUT
V_{IN} = +10V
3
2
V_O
V_A
1
R_L
C_L
1K
35pF
LOGIC INPUT
HI-201HS
5
4
GND
V- = -15V

$$V_O = V_{IN} \frac{R_L}{R_L + R_{ON}}$$

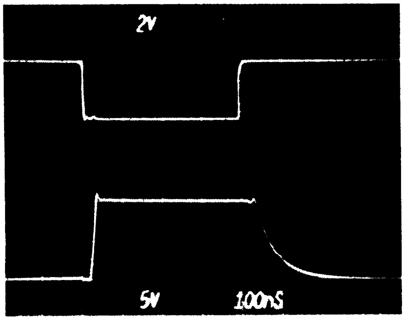
C_L INCLUDES $C_{FIXTURE} + C_{PROBE}$

SWITCHING WAVEFORMS

LOGIC "0" = SWITCH ON


DIGITAL INPUT
V_{AH} = 3V
50%
V_{AL} = 0V
50%
t_{OFF1}
t_{ON}
90%
90%
SWITCH OUTPUT
0V
10%
t_{OFF2}

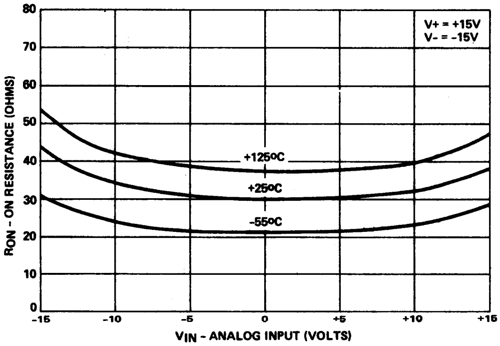
t_{ON}, t_{OFF}(TTL INPUT)
$V_{AH} = +3.0V$



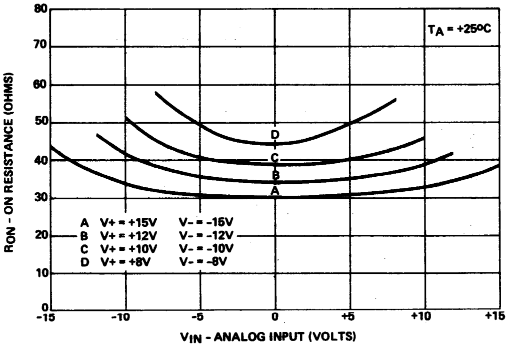
Top: TTL Input (2V/ON)
Bottom: Output (5V/Div.) Horizontal: 100ns/Div.

TYPICAL PERFORMANCE CURVES

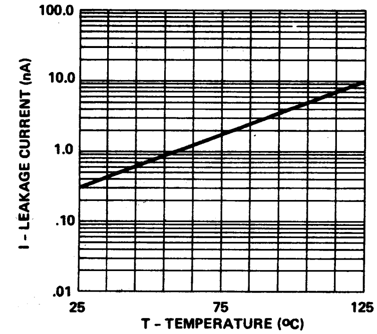
ON RESISTANCE vs ANALOG SIGNAL LEVEL AND TEMPERATURE



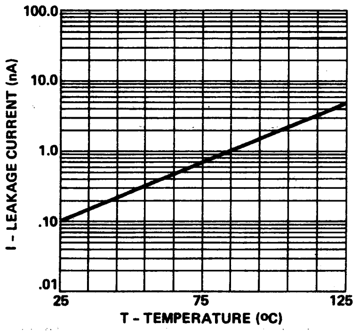
ON RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



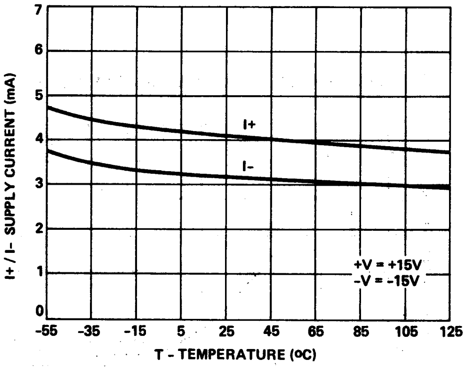
IS(OFF) or ID(OFF) vs TEMPERATURE *



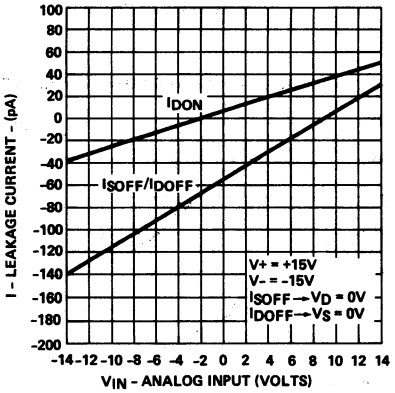
ID(ON) vs TEMPERATURE *



SUPPLY CURRENT vs TEMPERATURE



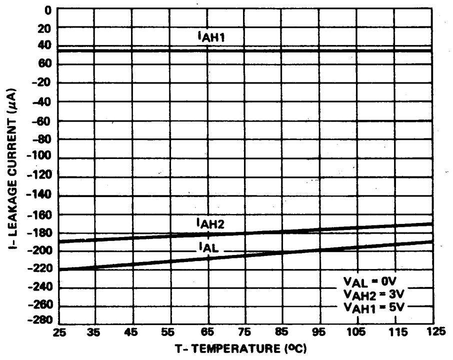
LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE



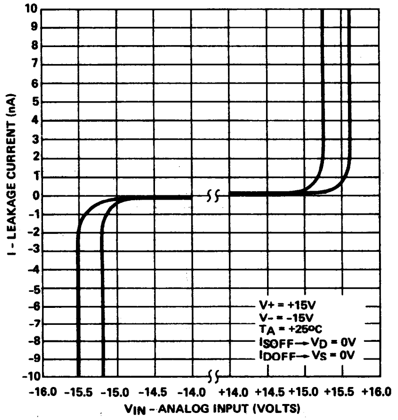
*THEORETICALLY, LEAKAGE CURRENT WILL CONTINUE TO DECREASE BELOW +25°C. BUT DUE TO ENVIRONMENTAL CONDITIONS, LEAKAGE MEASUREMENTS BELOW THIS TEMPERATURE ARE NOT REPRESENTATIVE OF ACTUAL SWITCH PERFORMANCE.

TYPICAL PERFORMANCE CURVES (Continued)

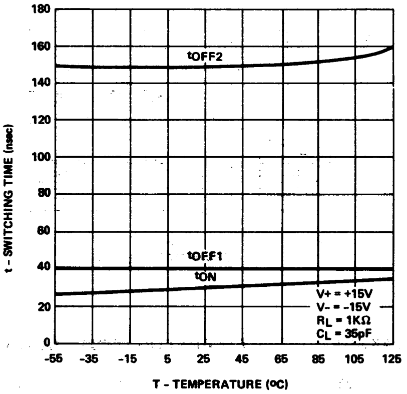
DIGITAL INPUT LEAKAGE CURRENT vs TEMPERATURE *



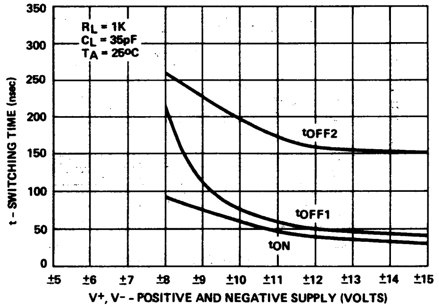
LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE ($V_{IN} \geq +14V$, $V_{IN} \leq -14V$)



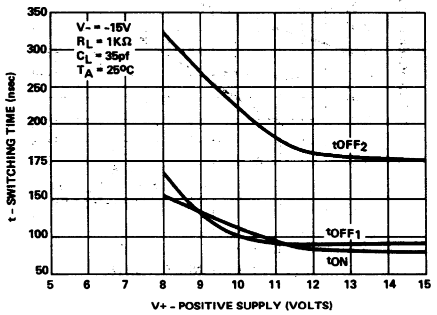
SWITCHING TIME vs TEMPERATURE



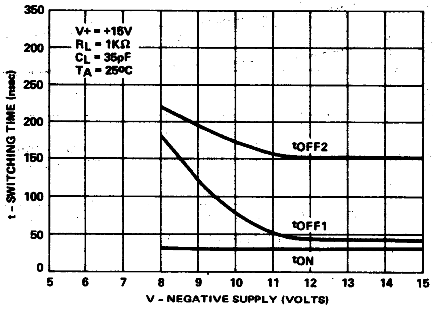
SWITCHING TIME vs POSITIVE AND NEGATIVE SUPPLY VOLTAGE



SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE

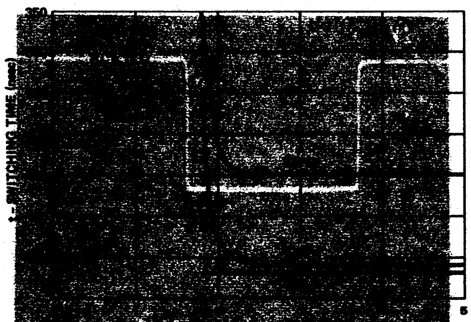


SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

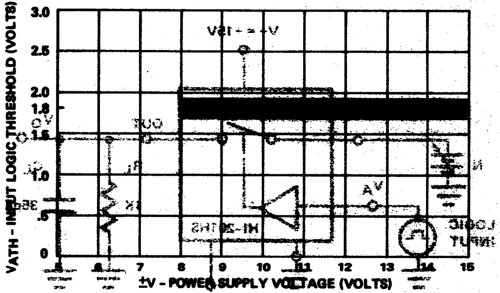


*THEORETICALLY, LEAKAGE CURRENT WILL CONTINUE TO DECREASE BELOW +25°C. BUT DUE TO ENVIRONMENTAL CONDITIONS, LEAKAGE MEASUREMENTS BELOW THIS TEMPERATURE ARE NOT REPRESENTATIVE OF ACTUAL SWITCH PERFORMANCE.

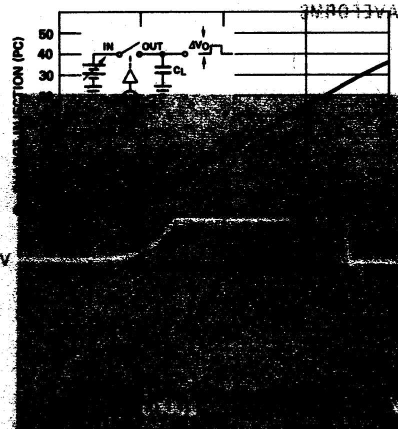
SWITCHING TIME vs INPUT LOGIC AMPLITUDE



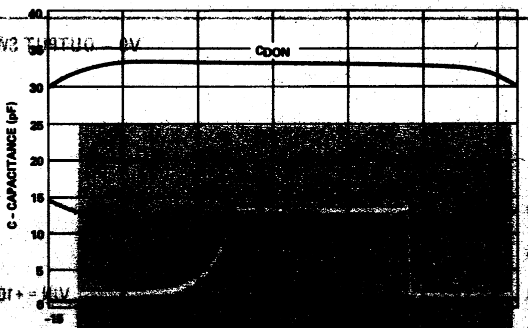
INPUT SWITCHING THRESHOLD vs POSITIVE AND NEGATIVE SUPPLY VOLTAGES

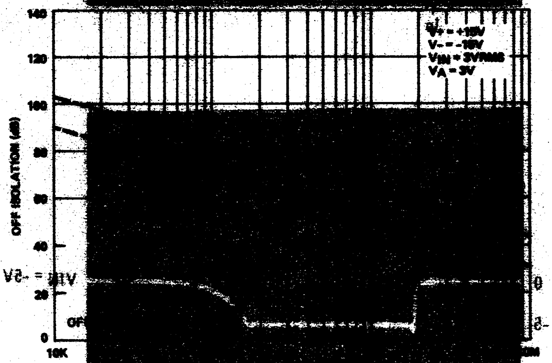


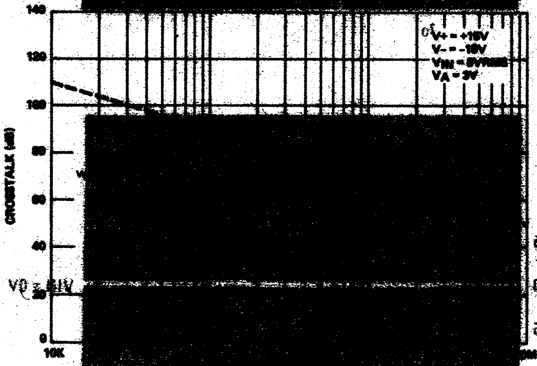
CHARGE INJECTION vs ANALOG INPUT



CAPACITANCE vs ANALOG INPUT



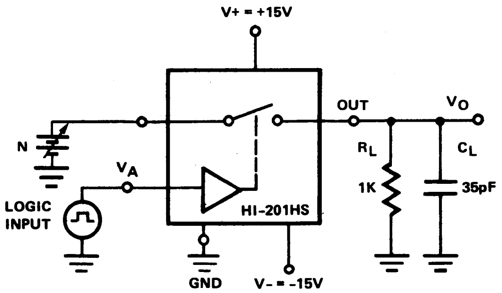




SWITCHING CHARACTERISTICS

SWITCHING CHARACTERISTICS vs INPUT VOLTAGE

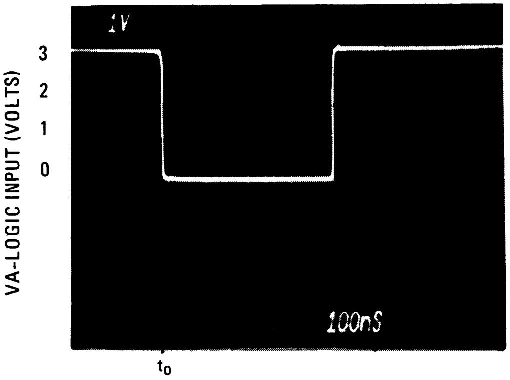
Typical delay, t_{ON}, t_{OFF}, settling time and switching transients in this circuit.



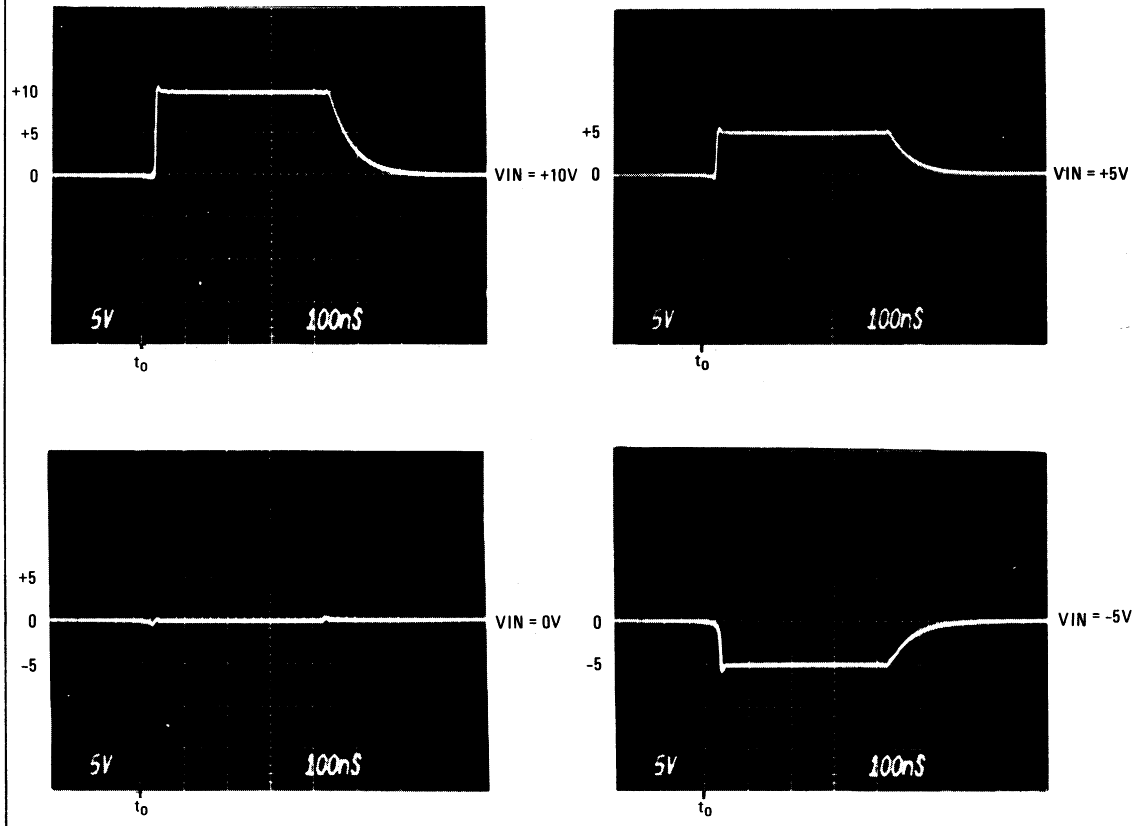
V+ = +15V
OUT
VO
N
VA
RL
CL
1K
35pF
LOGIC INPUT
HI-201HS
GND
V- = -15V

If R_L or C_L is increased, there will be corresponding increases in rise and/or fall RC times.

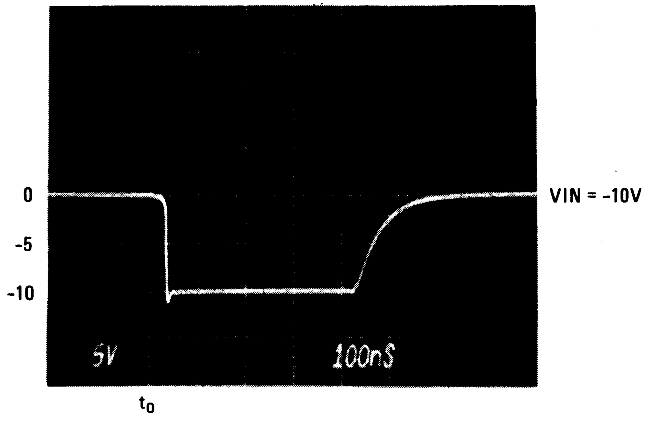
LOGIC INPUT



V0 – OUTPUT SWITCHING WAVEFORMS



V0 – OUTPUT SWITCHING WAVEFORMS



APPLICATION INFORMATION

LOGIC COMPATIBILITY

The HI-201HS is TTL compatible. Its logic inputs (Pins 1, 8, 9, 16) are designed to react to digital inputs which exceed a fixed, internally generated TTL switching threshold. The HI-201HS can also be driven with CMOS logic (0-15V), although the switch performance with CMOS logic will be inferior to that with TTL logic (0-5V).

The logic input design of the HI-201HS is largely responsible for its fast switching speed. It is a design which features a unique input stage consisting of complementary vertical PNP and NPN bipolar transistors. This design differs from that of the standard HI-201 product where the logic inputs are MOS transistors.

Although the new logic design enhances the switching speed performance, it also increases the logic input leakage currents. Therefore, the HI-201HS will exhibit larger digital input leakage currents in comparison to the standard HI-201 product.

CHARGE INJECTION

Charge injection is the charge transferred, through the internal gate-to-channel capacitances, from the digital logic input to the analog output. To optimize charge injection performance for the HI-201HS, it is advisable to provide a TTL logic input with fast rise and fall times.

If the power supplies are reduced from ±15V, charge injection will become increasingly dependent upon the digital input frequency. Increased logic input frequency will result in larger output error due to charge injection.

POWER SUPPLY CONSIDERATIONS

The electrical characteristics specified in this data sheet are guaranteed for power supplies of $\pm V_S = \pm 15V$. Power supply voltages less than ±15V will result in reduced switch performance. The following information is intended as a design aid only;

POWER SUPPLY VOLTAGES	SWITCH PERFORMANCE
$\pm 12 \leq \pm V_S$ $\pm 15V$	Minimal variation
$\pm V_S < \pm 12V$	Parametric variation becomes increasingly large (increased ON resistance, longer switching times).
$\pm V_S < \pm 10V$	Not recommended

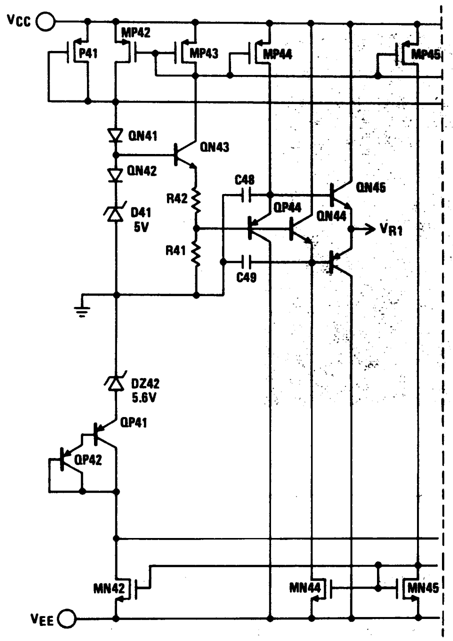
SINGLE SUPPLY

The switch operation of the HI-201HS is dependent upon an internally generated switching threshold voltage optimized for ± 15V power supplies. The HI-201HS does not provide the necessary internal switching threshold in a single supply system. Therefore, if single supply operation is required, the HI-300 series of switches is recommended. The HI-300 series will remain operational to a minimum +5V single supply.

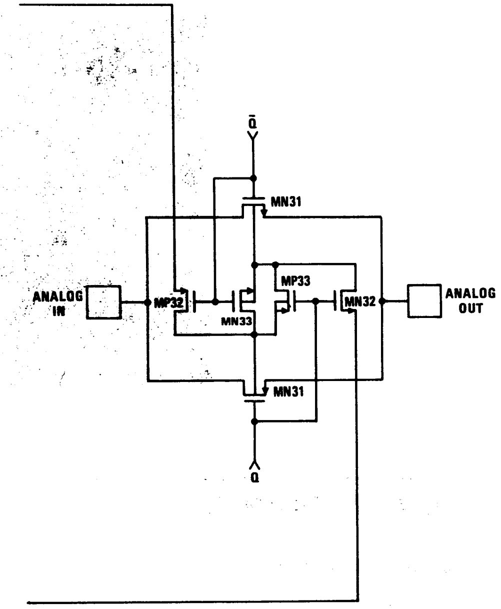
Switch performance will degrade as power supply voltage is reduced from optimum levels (± 15V). So it is recommended that a single supply design be thoroughly evaluated to ensure that the switch will meet the requirements of the application.

SCHEMATIC DIAGRAMS

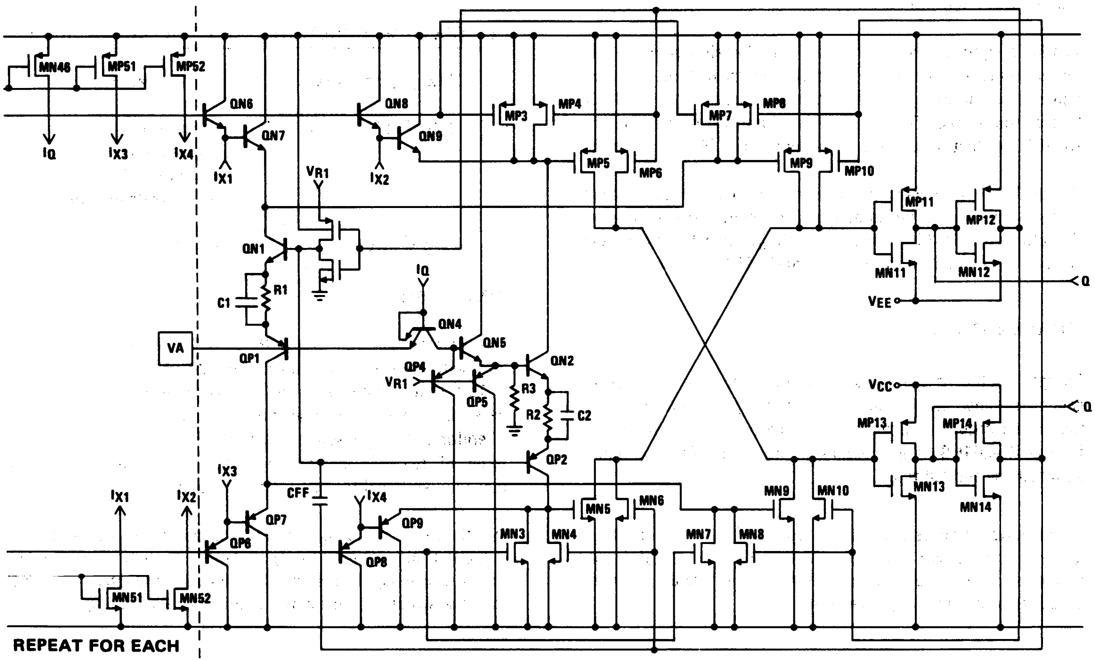
TTL/CMOS REFERENCE CIRCUIT


VCC
P41
MP42
MP43
MP44
MP45
QN41
QN43
QN42
R42
C48
QN45
D41
5V
QP44
QN44
VR1
R41
C49
DZ42
5.6V
QP41
QP42
MN42
MN44
MN45
VEE

SWITCH CELL


Q̄
MN31
ANALOG IN
MP32
MN33
MP33
MN32
ANALOG OUT
MN31
Q

DIGITAL INPUT AND LEVEL SHIFTER


MN46
MP51
MP52
IQ
IX3
IX4
QN6
QN7
IX1
QN8
QN9
IX2
VR1
MP3
MP4
MP5
MP6
MP7
MP8
MP9
MP10
MP11
MP12
MN11
MN12
VEE
Q
QN1
R1
C1
IQ
QN4
QN5
QN2
VA
QP1
QP4
VR1
QP5
R3
R2
C2
QP2
VCC
Q
MP13
MP14
MN13
MN14
IX3
IX1
IX2
CFF
IX4
QP7
QP6
QP9
QP8
MN3
MN4
MN5
MN6
MN7
MN8
MN9
MN10
MN51
MN52

REPEAT FOR EACH LEVEL SHIFTER

HARRIS

HI-300 thru HI-307

CMOS Analog Switches

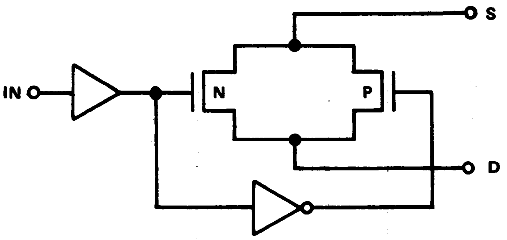
FEATURES

• ANALOG SIGNAL RANGE (± 15V SUPPLIES)	± 15V
• LOW LEAKAGE (TYP. @ 25°C)	40pA
• LOW LEAKAGE (TYP. @ 125°C)	1nA
• LOW ON RESISTANCE (TYP. @ 25°C)	35Ω
• BREAK-BEFORE-MAKE DELAY (TYP.)	60ns
• CHARGE INJECTION	30pC
• TTL, CMOS COMPATIBLE	
• SYMETRICAL SWITCH ELEMENTS	
• LOW OPERATING POWER (TYP. FOR HI-300 - 303)	1.0mW

APPLICATIONS

- SAMPLE AND HOLD i.e. LOW LEAKAGE SWITCHING
- OP AMP GAIN SWITCHING i.e. LOW ON RESISTANCE
- PORTABLE, BATTERY OPERATED CIRCUITS
- LOW LEVEL SWITCHING CIRCUITS
- DUAL OR SINGLE SUPPLY SYSTEMS

FUNCTIONAL DIAGRAM



TYPICAL SWITCH 300 SERIES

DESCRIPTION

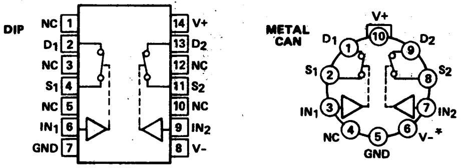
The HI-300 through HI-307 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These switches feature break-before-make switching, (HI-301, 303, 305 & 307 only), low and nearly constant ON resistance over the full analog signal range, and low power dissipation, (a few milliwatts for the HI-300-303, a few hundred microwatts for the HI-304-307).

The HI-300-303 are TTL compatible and have a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4.0V. The HI-304-307 switches are CMOS compatible and have a low state with an input less than 3.5V and a high state with an input greater than 11V. (See pinouts for switch conditions with a logic "1" input.)

All the devices are available in a 14 pin epoxy or ceramic DIP. The HI-300, 301, 304 and 305 are also available in a 10 pin metal can. Each of the switch types are available in either the -55°C to +125°C or 0°C to +75°C operating ranges.

PINOUTS (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

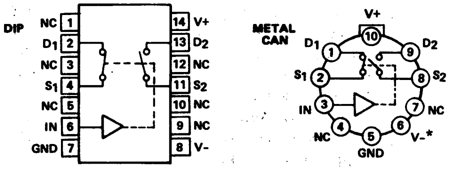
DUAL SPST HI-300 & HI-304
(TOP VIEWS)


DIP
NC 1
D1 2
NC 3
S1 4
NC 5
IN1 6
GND 7
14 V+
13 D2
12 NC
11 S2
10 NC
9 IN2
8 V-
METAL CAN
V+ 10
D1 1
D2 9
S1 2
S2 8
IN1 3
IN2 7
NC 4
GND 5
V-* 6

LOGIC	SWITCH
0	OFF
1	ON

*The substrate and case are internally tied to V−. (The case should not be used as the V− connection, however.)

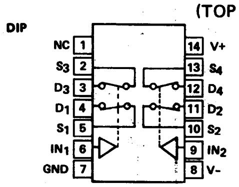
SPDT HI-301 & HI-305
(TOP VIEWS)


DIP
NC 1
D1 2
NC 3
S1 4
NC 5
IN 6
GND 7
14 V+
13 D2
12 NC
11 S2
10 NC
9 NC
8 V-
METAL CAN
V+ 10
D1 1
D2 9
S1 2
S2 8
IN 3
NC 7
NC 4
GND 5
V-* 6

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

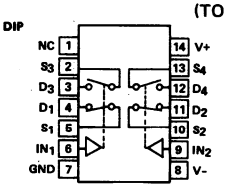
*The substrate and case are internally tied to V−. (The case should not be used as the V− connection, however.)

DUAL DPST HI-302 & HI-306
(TOP VIEW)


DIP
NC 1
S3 2
D3 3
D1 4
S1 5
IN1 6
GND 7
14 V+
13 S4
12 D4
11 D2
10 S2
9 IN2
8 V-

LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT HI-303 & HI-307
(TOP VIEW)


DIP
NC 1
S3 2
D3 3
D1 4
S1 5
IN1 6
GND 7
14 V+
13 S4
12 D4
11 D2
10 S2
9 IN2
8 V-

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

SPECIFICATIONS HI-300 - HI-307

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supplies	44V (±22V)
Digital Input Voltage	V^+ +4.0V V^- -4.0V
Analog Input Voltage	V^+ 1.5V V^- 1.5V

Total Power Dissipation		
	14 Pin Epoxy DIP	526mW
	14 Pin Ceramic DIP	588mW
	10 Pin Metal Can*	435mW

*Derate 6.9mW/0°C Above T_A = 70°C

Operating Temperature	HI-3XX-2	-55°C to +125°C
	HI-3XX-5	0°C to +75°C
Storage Temperature		-65°C to +150°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified; Supplies = +15V, -15V; V_{IN} = Logic Input.
HI-300-303 : V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V
HI-304-307 : V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V

PARAMETER	TEMP	-55°C to +125°C MIN	-55°C to +125°C TYP	-55°C to +125°C MAX	0°C to +75°C MIN	0°C to +75°C TYP	0°C to +75°C MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON} ON Resistance (Note 2)	+25°C		35	50		35	50	Ω
	Full		40	75		40	75	Ω
IS_{OFF} OFF Input Leakage Current (Note 3)	+25°C		0.04	1		0.04	5	nA
	Full		1	100		0.2	100	nA
ID_{OFF} OFF Output Leakage Current (Note 3)	+25°C		0.04	1		0.04	5	nA
	Full		1	100		0.2	100	nA
ID_{ON} ON Leakage Current (Note 4)	+25°C		0.03	1		0.03	5	nA
	Full		0.5	100		0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL} Input Low Level *	Full			0.8			0.8	V
V_{INH} Input High Level *	Full	4			4			V
V_{INL} Input Low Level **	Full			3.5			3.5	V
V_{INH} Input High Level **	Full	11			11			V
I_{INL} Input Leakage Current (Low) (Note 5)	Full			1			1	μA
I_{INH} Input Leakage Current (High) (Note 5)	Full			1			1	μA
SWITCHING CHARACTERISTICS								
t_{OPEN} Break-Before-Make Delay ***	+25°C		60			60		ns
t_{ON} Switch On Time *	+25°C		210	300		210	300	ns
t_{OFF} Switch Off Time *	+25°C		160	250		160	250	ns
t_{ON} Switch On Time **	+25°C		160	250		160	250	ns
t_{OFF} Switch Off Time **	+25°C		100	150		100	150	ns
Off Isolation (Note 6)	+25°C		60			60		dB
Charge Injection (Note 7)	+25°C		3			3		mV
CS_{OFF} Input Switch Capacitance	+25°C		16			16		pF
CD_{OFF} Output Switch Capacitance	+25°C		14			14		pF
CD_{ON} Output Switch Capacitance	+25°C		35			35		pF
C_{IN} (High) Digital Input Capacitance	+25°C		5			5		pF
C_{IN} (Low) Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
I+ Current * (Note 8)	+25°C		0.09	0.5		0.09	0.5	mA
	Full			1			1	mA
I- Current * (Note 8)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current * (Note 9)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current * (Note 9)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current ** (Note 10)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current ** (Note 10)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current ** (Note 11)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current ** (Note 11)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA

* HI-300 thru HI-303 Only; ** HI-304 thru HI-307 Only; *** HI-301, HI-303, HI-305, HI-307 Only

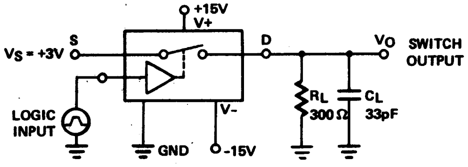
ELECTRICAL CHARACTERISTICS NOTES:

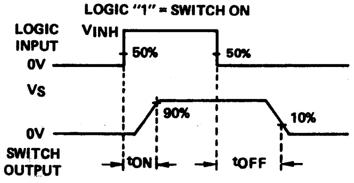
1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.
2. V_S = ± 10V, I_{OUT} = -10mA On resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V, V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. V_S = 1V_{RMS}, f = 500kHz, C_L = 15pF, R_L = 1k. C_L = $C_{FIXTURE}$ + C_{PROBE}, "Off Isolation" = 20logVS/VD.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. (HI-300 -303) Switches are symmetrical; S and D may be interchanged. Logic Drive = 15V (HI-304-307)
8. V_{IN} = 4V (one input) (all other inputs = 0V)
9. V_{IN} = 0.8V (all inputs).
10. V_{IN} = 15V (all inputs).
11. V_{IN} = 0V (all inputs).
12. To drive from DTL/TTL circuits, pull-up resistors to +5V supply are recommended.

TEST CIRCUITS

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

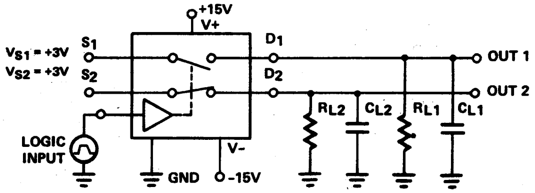
SWITCH TYPE	V_{INH}
HI-300 thru HI-303 HI-304 thru HI-307	4V 15V

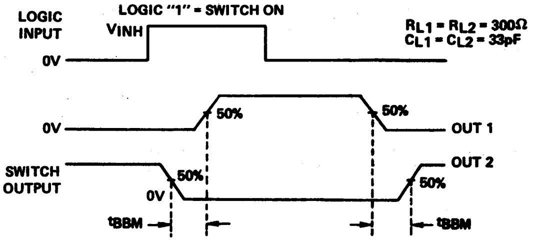

+15V
V+
S
D
Vo
SWITCH OUTPUT
VS = +3V
LOGIC INPUT
RL
300 Ω
CL
33pF
V-
GND
-15V


LOGIC "1" = SWITCH ON
LOGIC INPUT
VINH
50%
50%
0V
VS
90%
10%
0V
SWITCH OUTPUT
tON
tOFF

BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

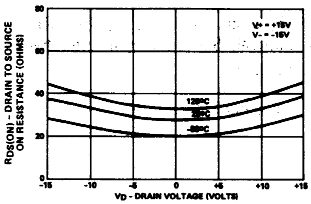
SWITCH TYPE	V_{INH}
HI-301, HI-303 HI-305, HI-307	5V 15V


+15V
V+
VS1 = +3V
VS2 = +3V
S1
S2
D1
D2
OUT 1
OUT 2
RL2
CL2
RL1
CL1
LOGIC INPUT
V-
GND
-15V

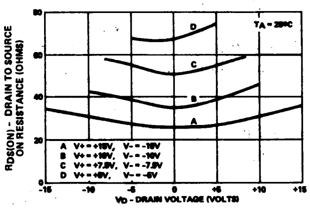

LOGIC "1" = SWITCH ON
LOGIC INPUT
VINH
0V
RL1 = RL2 = 300Ω
CL1 = CL2 = 33pF
50%
50%
0V
OUT 1
SWITCH OUTPUT
50%
OUT 2
50%
0V
tBBM
tBBM

TYPICAL PERFORMANCE CURVES

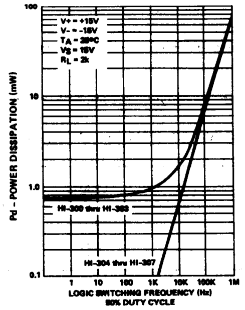
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



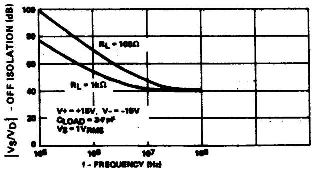
$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE



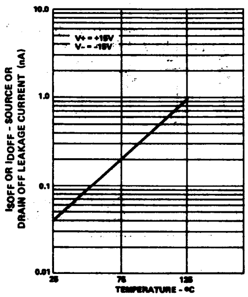
DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT



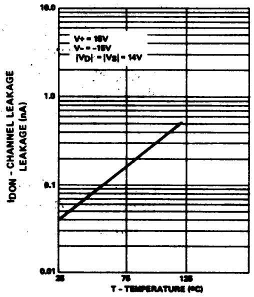
OFF ISOLATION VS. FREQUENCY



$I_{S(OFF)}$ OR $I_{D(OFF)}$ VS. TEMPERATURE *

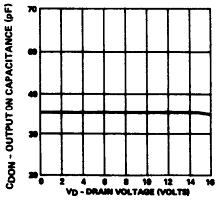


$I_{D(ON)}$ VS. TEMPERATURE *

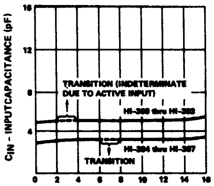


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

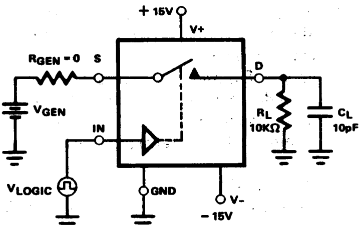
OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE



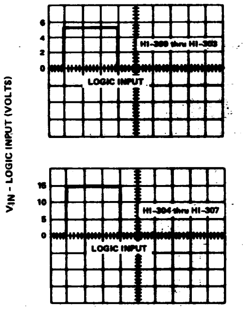
DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE

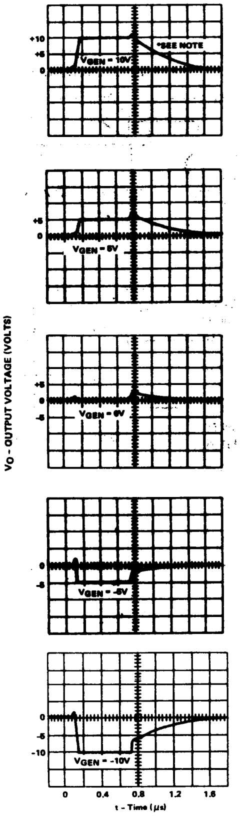


Typical delay, rise, fall, settling times, and switching transients in this circuit.



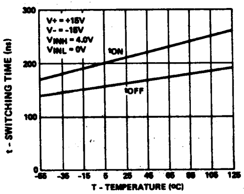
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



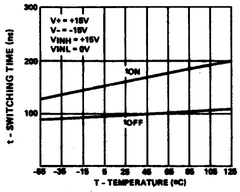


TYPICAL PERFORMANCE CURVES (Continued)

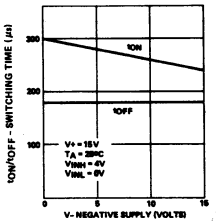
SWITCHING TIME VS. TEMPERATURE
HI-300 thru HI-303



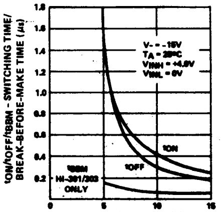
SWITCHING TIME VS. TEMPERATURE
HI-304 thru HI-307



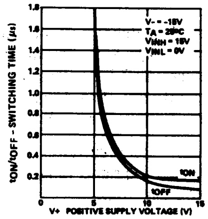
SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE
HI-300 thru HI-303



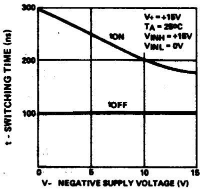
SWITCHING TIME AND BREAK BEFORE MAKE TIME VS. POSITIVE SUPPLY VOLTAGE
HI-300 thru HI-303



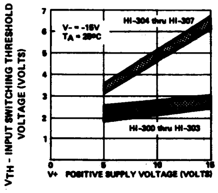
SWITCHING TIME VS. POSITIVE SUPPLY VOLTAGE
HI-304 thru HI-307



SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE
HI-304 thru HI-307

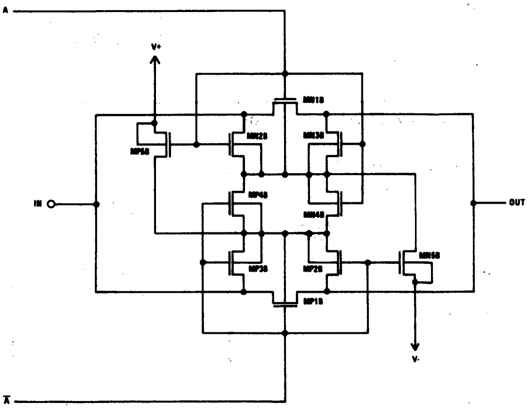


INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE
HI-300 thru HI-307

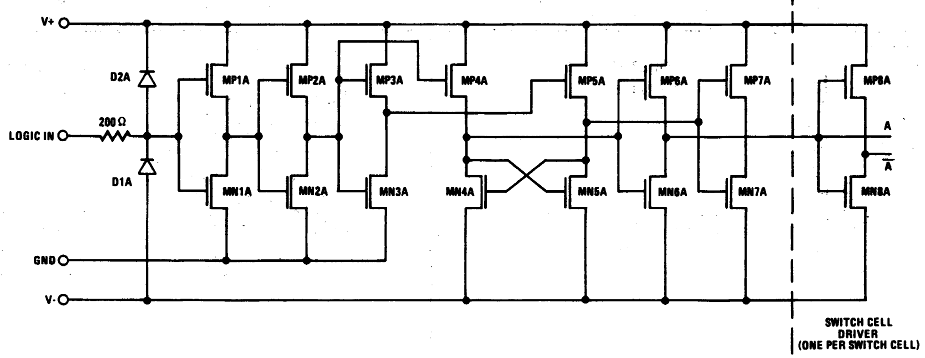


SCHEMATIC DIAGRAMS

SWITCH CELL


A
V+
MN1B
MN2B
MN3B
MP5B
IN
OUT
MP4B
MN4B
MP3B
MP2B
MN5B
MP1B
V-
$\overline{A}$

DIGITAL INPUT BUFFER AND LEVEL SHIFTER


V+
D2A
LOGIC IN
200 Ω
D1A
GND
V-
MP1A
MP2A
MP3A
MP4A
MP5A
MP6A
MP7A
MP8A
MN1A
MN2A
MN3A
MN4A
MN5A
MN6A
MN7A
MN8A
A
$\overline{A}$
SWITCH CELL DRIVER (ONE PER SWITCH CELL)

HARRIS

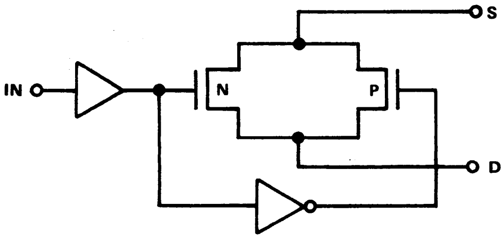
HI-381/384/387/390

CMOS Analog Switches

FEATURES

● ANALOG SIGNAL RANGE (±15V SUPPLIES)	±15V
● LOW LEAKAGE (TYP. @ 25°C)	40pA
● LOW LEAKAGE (TYP @ 125°C)	1nA
● LOW ON RESISTANCE (TYP. @ 25°C)	35Ω
● BREAK-BEFORE-MAKE DELAY (TYP.)	60ns
● CHARGE INJECTION	30pC
● TTL COMPATIBLE	
● SYMMETRICAL SWITCH ELEMENTS	
● LOW OPERATING POWER (TYP.)	1.0mW

FUNCTIONAL DIAGRAM



TYPICAL SWITCH - 300 SERIES

APPLICATIONS

- SAMPLE AND HOLD i.e. LOW LEAKAGE SWITCHING
- OP AMP GAIN SWITCHING i.e. LOW ON RESISTANCE
- PORTABLE BATTERY OPERATED CIRCUITS
- LOW LEVEL SWITCHING CIRCUITS
- DUAL OR SINGLE SUPPLY SYSTEMS

DESCRIPTION

The HI-381 through HI-390 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These devices are TTL compatible and are available in four switching configurations. (See device pinout for particular switching function with a logic "1" input.)

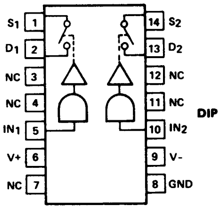
These switches feature low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

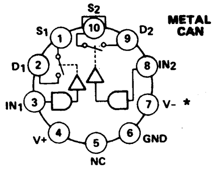
The HI-381 and HI-387 switches are available in a 14 pin epoxy or ceramic DIP or10 pin metal can. The HI-384 and HI-390 are available in a 16 pin epoxy or ceramic DIP. Each of the individual switch types are available in the -55°C to +125°C and 0°C to +75°C operating ranges.

PINOUTS (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

DUAL SPST HI-381

(TOP VIEWS)


S_1 1
D_1 2
NC 3
NC 4
IN_1 5
V+ 6
NC 7
8 GND
9 V-
10 IN_2
11 NC
12 NC
13 D_2
14 S_2
DIP

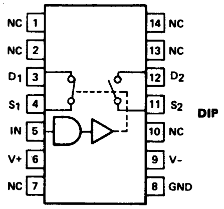

S_2
10
D_2
9
METAL CAN
S_1
1
D_1
2
8
IN_2
IN_1
3
7
V- *
V+
4
5
NC
6
GND

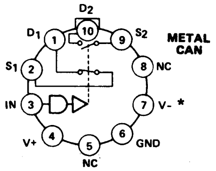
LOGIC	SW 1 SW 2
0	ON
1	OFF

*The substrate and case are internally tied to V–. (The case should not be used as the V– connection, however.)

SPDT HI-387

(TOP VIEWS)


NC 1
NC 2
D_1 3
S_1 4
IN 5
V+ 6
NC 7
8 GND
9 V-
10 NC
11 S_2
12 D_2
13 NC
14 NC
DIP

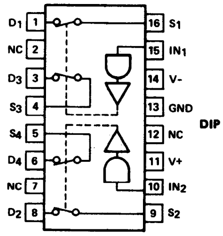

D_2
10
D_1
1
9
S_2
METAL CAN
S_1
2
8
NC
IN
3
7
V- *
V+
4
5
NC
6
GND

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*The substrate and case are internally tied to V–. (The case should not be used as the V– connection, however.)

DUAL DPST HI-384

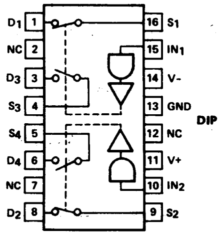
(TOP VIEW)


D_1 1
NC 2
D_3 3
S_3 4
S_4 5
D_4 6
NC 7
D_2 8
9 S_2
10 IN_2
11 V+
12 NC
13 GND
14 V-
15 IN_1
16 S_1
DIP

LOGIC	SW 1 - 4
0	OFF
1	ON

DUAL SPDT HI-390

(TOP VIEW)


D_1 1
NC 2
D_3 3
S_3 4
S_4 5
D_4 6
NC 7
D_2 8
9 S_2
10 IN_2
11 V+
12 NC
13 GND
14 V-
15 IN_1
16 S_1
DIP

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supplies	44V (±22)
Digital Input Voltage	V^++4.0V V^- -4.0V
Analog Input Voltage	V^++1.5V V^- -1.5V
Storage Temperature Range	-65°C to +150°C

Total Power Dissipation	
14 Pin Epoxy DIP	526mW
14 Pin Ceramic DIP	588mW
16 Pin Epoxy DIP	625mW
16 Pin Ceramic DIP	685mW
10 Pin Metal Can*	435mW
*Derate 6.9mW/°C above T_A = 70°C	
Operating Temperature	
HI-3XX-2	-55°C to +125°C
HI-3XX-5	0°C to +75°C

ELECTRICAL CHARACTERISITICS

Unless otherwise specified; Supplies = +15V, -15V; VIN = Logic Input, VIN for logic "1" = 4V, for logic 0 = .8V

		-55°C to +125°C			0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	FULL	-15		+15	-15		+15	V
R_{ON} ON Resistance (Note 2)	+25°C		35	50		35	50	Ω
	FULL		40	75		40	75	Ω
IS_{OFF} OFF Input Leakage Current (Note 3)	+25°C		.04	1		.04	5	nA
	FULL		1	100		0.2	100	nA
ID_{OFF} OFF Output Leakage Current (Note 3)	+25°C		.04	1		.04	5	nA
	FULL		1	100		0.2	100	nA
ID_{ON} ON Leakage Current (Note 4)	+25°C		.03	1		.03	5	nA
	FULL		0.5	100		0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL} Input Low Level	FULL			.8			.8	V
V_{INH} Input High Level	FULL	4			4			V
I_{INH} Input Leak. Current (High) (Note 5)	FULL			1			1	µA
I_{INL} Input Leak. Current (Low) (Note 5)	FULL			1			1	µA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (HI-387/390 only)	+25°C		60			60		ns
t_{ON}, Switch ON Time	+25°C		210	300		210	300	ns
t_{OFF}, Switch OFF Time	+25°C		160	250		160	250	ns
OFF Isolation (Note 6)	+25°C		60			60		dB
Charge Injection (Note 7)	+25°C		3			3		mV
CS_{OFF} Input Switch Capacitance	+25°C		16			16		pF
CD_{OFF} Output Switch Capacitance	+25°C		14			14		pF
CD_{ON} Output Switch Capacitance	+25°C		35			35		pF
C_{IN} (High) Digital Input Capacitance	+25°C		5			5		pF
C_{IN} (Low) Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
I+ Current (Note 8)	+25°C		.09	.5		.09	.5	mA
	FULL			1			1	mA
I- Current (Note 8)	+25°C		.01	10		.01	100	µA
	FULL			100				µA
I+ Current (Note 9)	+25°C		.01	10		.01	100	µA
	FULL			100				µA
I- Current (Note 9)	+25°C		.01	10		.01	100	µA
	FULL			100				µA

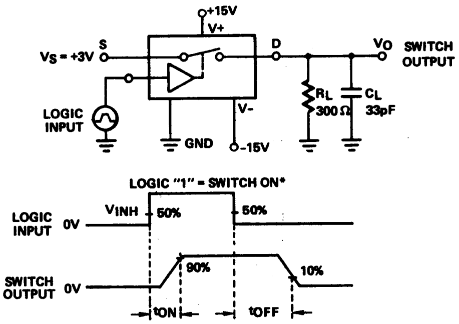
ELECTRICAL CHARACTERISTICS NOTES :

1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.
2. $V_S = \pm 10V$, $I_{OUT} = -10mA$ on resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V$, $V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, $C_L = 15pF$, $R_L = 1k$, $C_L = C_{FIXTURE} + C_{PROBE}$, "off isolation" = $20\log V_S/V_D$.
7. $V_S = 0V$, $C_L = 10{,}000pF$, Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged.
8. $V_{IN} = 4V$. (one input) (all other inputs = 0)
9. $V_{IN} = 0.8V$. (all inputs)
10. To drive from DTL/TTL circuits, pull-up resistors to +5V Supply are recommended.

TEST CIRCUITS

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

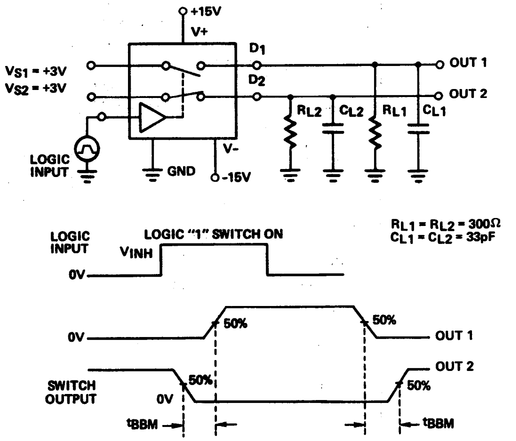
SWITCH TYPE	V_{INH}
HI-381 thru HI-390	5V


+15V
V+
S
D
V_S = +3V
V_O
SWITCH OUTPUT
LOGIC INPUT
R_L 300Ω
C_L 33pF
V-
GND
-15V
LOGIC "1" = SWITCH ON*
LOGIC INPUT
0V
V_{INH}
50%
50%
SWITCH OUTPUT
0V
90%
10%
t_{ON}
t_{OFF}

*Inverted logic for HI-381

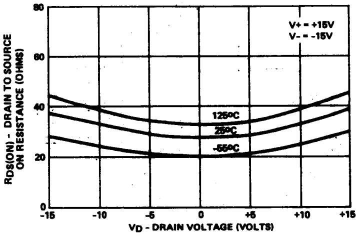
BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

SWITCH TYPE	V_{INH}
HI-387 and HI-390	5V

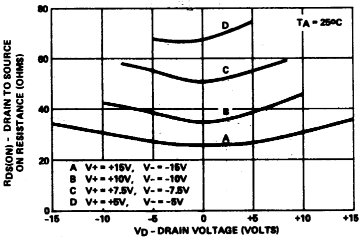

+15V
V+
D_1
D_2
V_{S1} = +3V
V_{S2} = +3V
OUT 1
OUT 2
R_{L2}
C_{L2}
R_{L1}
C_{L1}
LOGIC INPUT
GND
V-
-15V
LOGIC "1" SWITCH ON
V_{INH}
0V
$R_{L1} = R_{L2} = 300Ω$
$C_{L1} = C_{L2} = 33pF$
0V
50%
50%
OUT 1
OUT 2
SWITCH OUTPUT
0V
50%
50%
t_{BBM}
t_{BBM}

TYPICAL PERFORMANCE CURVES

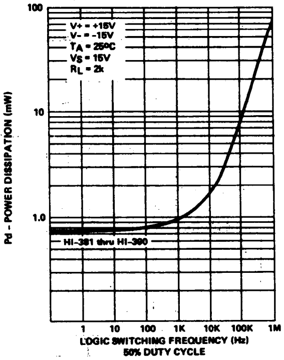
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



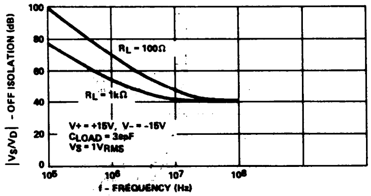
$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE



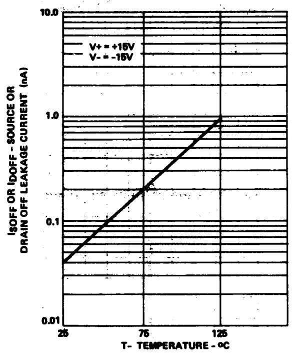
DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT



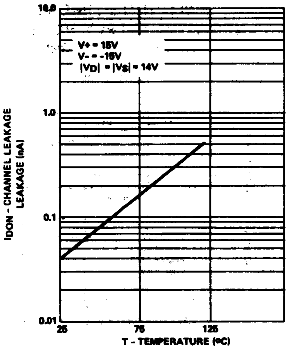
OFF ISOLATION VS. FREQUENCY



I_{SOFF} OR I_{DOFF} VS. TEMPERATURE*

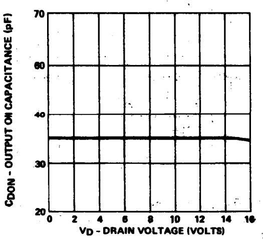


I_{DON} VS. TEMPERATURE*

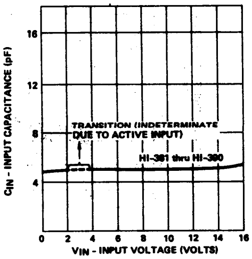


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE

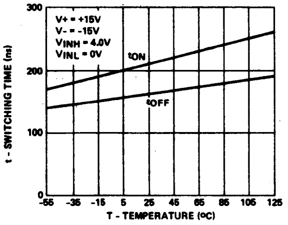


DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE

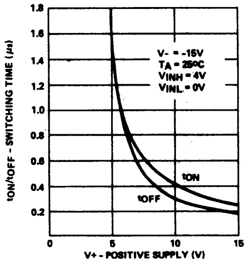


TYPICAL PERFORMANCE CURVES (Continued)

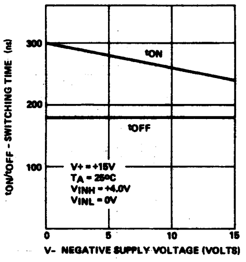
SWITCHING TIME VS. TEMPERATURE HI-381 thru HI-390



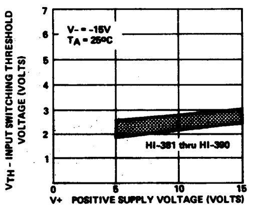
SWITCHING TIME VS. POSITIVE SUPPLY VOLTAGE HI-381 thru HI-390



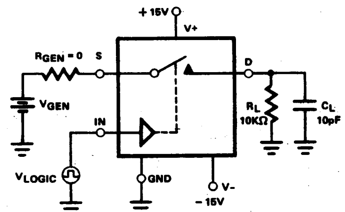
SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-381 thru HI-390



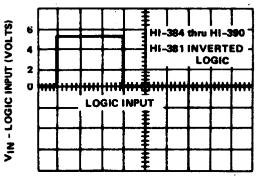
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-381 thru HI-390

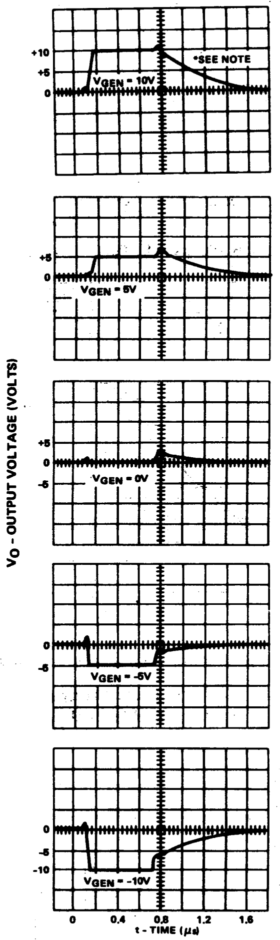


Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

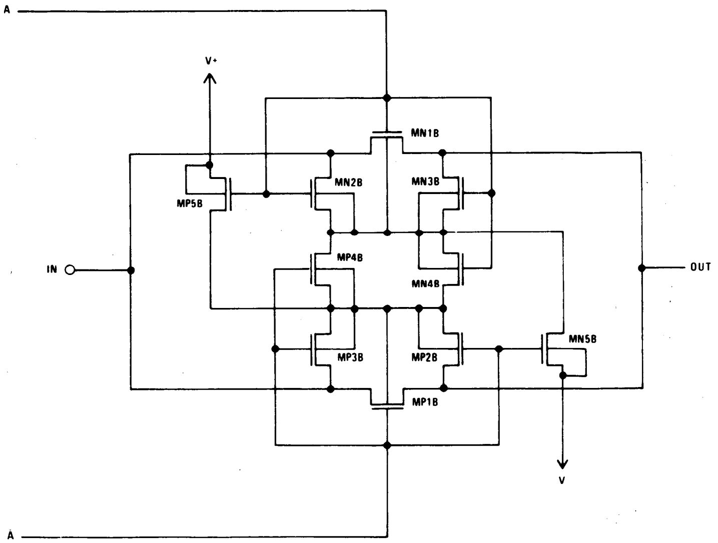




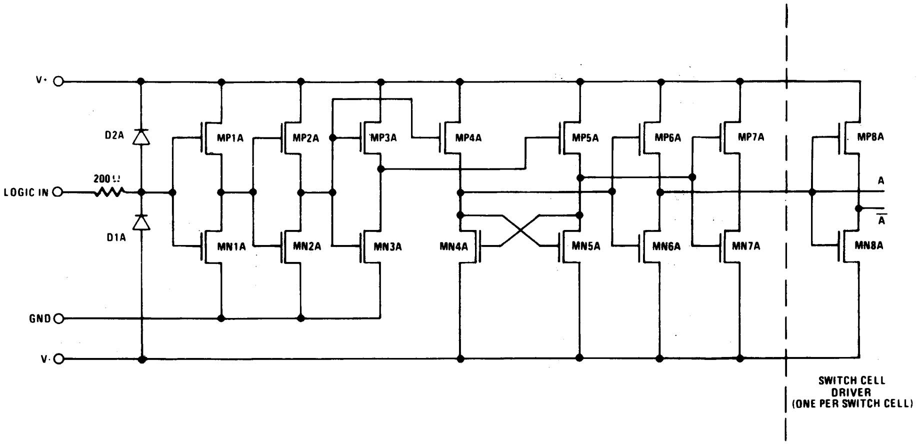
* NOTE: The turn-off time is primarily limited here by the RC time constant (100ns) of the load.

SCHEMATIC DIAGRAMS

SWITCH CELL


A
V+
MN1B
MP5B
MN2B
MN3B
IN
MP4B
OUT
MN4B
MN5B
MP3B
MP2B
MP1B
V-
Ā

DIGITAL INPUT BUFFER AND LEVEL SHIFTER


V+
D2A
200Ω
LOGIC IN
D1A
GND
V-
MP1A
MP2A
MP3A
MP4A
MP5A
MP6A
MP7A
MP8A
MN1A
MN2A
MN3A
MN4A
MN5A
MN6A
MN7A
MN8A
A
Ā
SWITCH CELL DRIVER (ONE PER SWITCH CELL)

HARRIS

HI-5040 thru HI-5051
HI-5046A
and HI-5047A

CMOS Analog Switches

FEATURES

WIDE ANALOG SIGNAL RANGE	±15V
LOW "ON" RESISTANCE (TYP)	25Ω
HIGH CURRENT CAPABILITY (TYP)	80mA
BREAK-BEFORE-MAKE SWITCHING	
TURN-ON TIME (TYP)	370ns
TURN-OFF TIME (TYP)	280ns
NO LATCH-UP	
INPUT MOS GATES ARE PROTECTED FROM ELECTROSTATIC DISCHARGE	
DTL, TTL, CMOS, PMOS COMPATIBLE	

APPLICATIONS

- HIGH FREQUENCY SWITCHING
- SAMPLE AND HOLD
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING

DESCRIPTION

This family of CMOS analog switches offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25 ohms for HI-5048 through HI-5051 and HI-5046A/5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at 25°C). This family of switches also features very low power operation (1.5mW at 25°C).

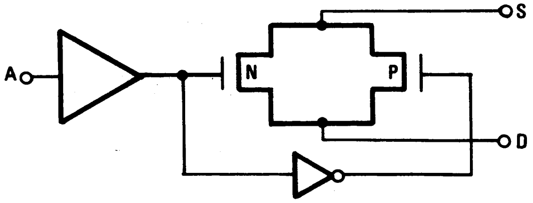
There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional diagram). All devices are available in 16 pin D.I.P. packages. The HI-5040/5050 switches can directly replace IH-5040 series devices and are functionally compatible with the DG 180/190 family. Each switch type is available in the -55°C to +125°C and 0°C to +75°C performance grades.

FUNCTIONAL DESCRIPTION

PART NUMBER	TYPE	R_{ON}
HI-5040	SPST	75Ω
HI-5041	DUAL SPST	75Ω
HI-5042	SPDT	75Ω
HI-5043	DUAL SPDT	75Ω
HI-5044	DPST	75Ω
HI-5045	DUAL DPST	75Ω
HI-5046	DPDT	75Ω
HI-5046A	DPDT	30Ω
HI-5047	4PST	75Ω
HI-5047A	4PST	30Ω
HI-5048	DUAL SPST	30Ω
HI-5049	DUAL DPST	30Ω
HI-5050	SPDT	30Ω
HI-5051	DUAL SPDT	30Ω

FUNCTIONAL DIAGRAM

TYPICAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ -V^-)	36V
V_R to Ground	V^+, V^-
Digital and Analog Input Voltage	V^+ +4V V^- -4V
Analog Current (S to D)	80mA
Total Power Dissipation*	450mW
Operating Temperature	
HI-50XX-2	-55°C to +125°C
HI-50XX-5	0°C to +75°C
Storage Temperature	-65°C to +150°C

*Derate 6mW/°C above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified

Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 3.0V; V_{AL} (Logic Level Low) = +0.8V, V_L = +5V

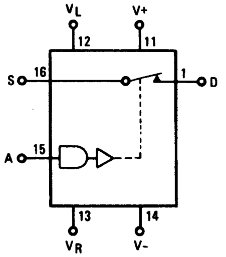
For Test Conditions, consult Performance Characteristics

		-55°C to +125°C			0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15		+15	-15		+15	V
Ron,"ON" Resistance (Note 1a)	+25°C		50			50		Ω
	Full			75			75	Ω
Ron,"ON"Resistance (Note 1b)	+25°C		25			25		Ω
	Full			50			50	Ω
Ron, Channel-to-Channel Match (Note 1a)	+25°C		2	10		2	10	Ω
Ron, Channel-to-Channel Match (Note 1b)	+25°C		1	5		1	5	Ω
$I_{S(OFF)} = I_{D(OFF)}$, Off Input or Output Leakage Current	+25°C		0.8			0.8		nA
	Full		100	500		100	500	nA
$I_{D(ON)}$, On Leakage Current	+25°C		0.01			0.01		nA
	Full		2	500		2	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
I_A, Input Leakage Current (High or Low)	Full		.01	1.0		.01	1.0	μA
SWITCHING CHARACTERISTICS								
t_{on}, Switch "ON" Time	+25°C		370	1000		370	1000	ns
t_{off}, Switch "OFF" Time	+25°C		280	500		280	500	ns
Charge Injection (Note 2)	+25°C		5	20		5		mV
"OFF Isolation" (Note 3)	+25°C	75	80			80		dB
"Crosstalk" (Note 3)	+25°C	80	88			88		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		11			11		pF
$C_{D(OFF)}$,	+25°C		11			11		pF
Output Switch Capacitance								
$C_{D(ON)}$,	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS\ (OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS								
P_D, Quiescent Power Dissipation	+25°C		1.5			1.5		mW
I^+, +15V Quiescent Current	Full			0.3			0.5	mA
I^-, -15V Quiescent Current	Full			0.3			0.5	mA
I_L, +5V Quiescent Current	Full			0.3			0.5	mA
I_R, Gnd Quiescent Current	Full			0.3			0.5	mA

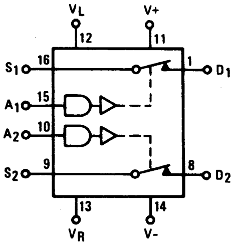
NOTES:
1. V_{OUT} = ±10V, I_{OUT} = 1mA
   a) For HI-5040 thru HI-5047
   b) For HI-5048 thru HI-5051, HI-5046A/5047A
2. V_{IN} = 0V, C_L = 10,000pF
3. R_L = 100Ω, f= 100 KHz, V_{IN} = 2 V_{PP}, C_L=5pF

SWITCH FUNCTIONS SWITCH STATES ARE FOR LOGIC "1" INPUT

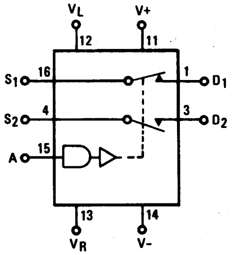
SPST
HI-5040 (75Ω)


VL
V+
12
11
S
16
1
D
A
15
13
14
VR
V-

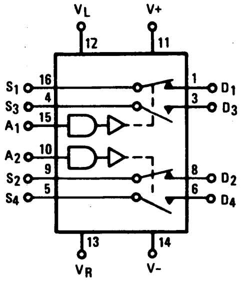
DUAL SPST
HI-5041 (75Ω)


VL
V+
12
11
S1
16
1
D1
A1
15
A2
10
S2
9
8
D2
13
14
VR
V-

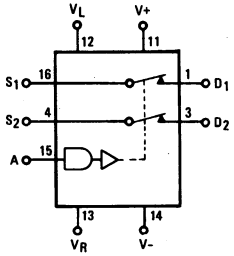
SPDT
HI-5042 (75Ω)


VL
V+
12
11
S1
16
1
D1
S2
4
3
D2
A
15
13
14
VR
V-

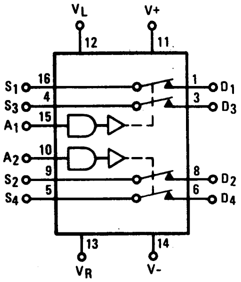
DUAL SPDT
HI-5043 (75Ω)


VL
V+
12
11
S1
16
1
D1
S3
4
3
D3
A1
15
A2
10
S2
9
8
D2
S4
5
6
D4
13
14
VR
V-

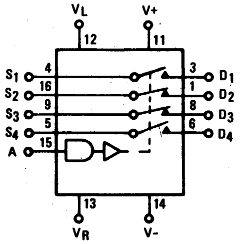
DPST
HI-5044 (75Ω)


VL
V+
12
11
S1
16
1
D1
S2
4
3
D2
A
15
13
14
VR
V-

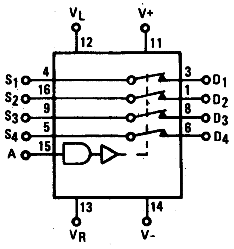
DUAL DPST
HI-5045 (75Ω)


VL
V+
12
11
S1
16
1
D1
S3
4
3
D3
A1
15
A2
10
S2
9
8
D2
S4
5
6
D4
13
14
VR
V-

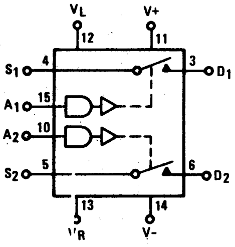
DPDT
HI-5046 (75Ω)
HI-5046A (30Ω)


VL
V+
12
11
S1
4
3
D1
S2
16
1
D2
S3
9
8
D3
S4
5
6
D4
A
15
13
14
VR
V-

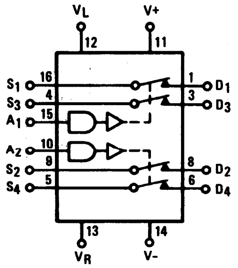
4PST
HI-5047 (75Ω)
HI-5047A (30Ω)


VL
V+
12
11
S1
4
3
D1
S2
16
1
D2
S3
9
8
D3
S4
5
6
D4
A
15
13
14
VR
V-

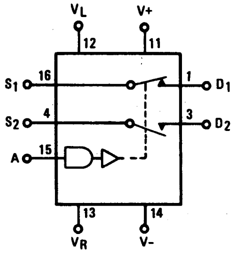
DUAL SPST
HI-5048 (30Ω)


VL
V+
12
11
S1
4
3
D1
A1
15
A2
10
S2
5
6
D2
13
14
VR
V-

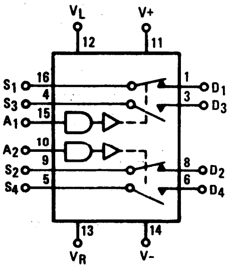
DUAL DPST
HI-5049 (30Ω)


VL
V+
12
11
S1
16
1
D1
S3
4
3
D3
A1
15
A2
10
S2
9
8
D2
S4
5
6
D4
13
14
VR
V-

SPDT
HI-5050 (30Ω)


VL
V+
12
11
S1
16
1
D1
S2
4
3
D2
A
15
13
14
VR
V-

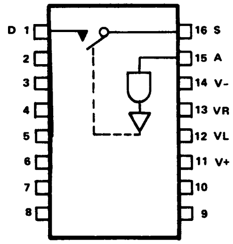
DUAL SPDT
HI-5051 (30Ω)


VL
V+
12
11
S1
16
1
D1
S3
4
3
D3
A1
15
A2
10
S2
9
8
D2
S4
5
6
D4
13
14
VR
V-

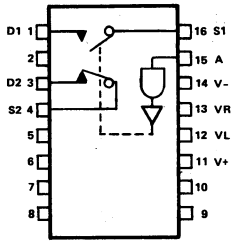
PIN CONFIGURATIONS SWITCH STATES ARE FOR LOGIC "0" INPUT

SINGLE CONTROL

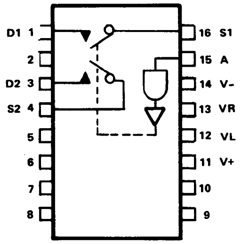
SPST
HI-5040 (75Ω)


D 1
2
3
4
5
6
7
8
16 S
15 A
14 V-
13 VR
12 VL
11 V+
10
9

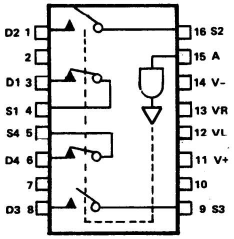
SPDT
HI-5042 (75Ω)
HI-5050 (25Ω)


D1 1
2
D2 3
S2 4
5
6
7
8
16 S1
15 A
14 V-
13 VR
12 VL
11 V+
10
9

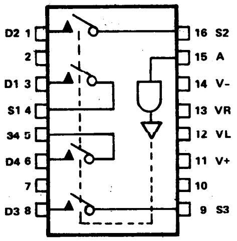
DPST
HI-5044 (75Ω)


D1 1
2
D2 3
S2 4
5
6
7
8
16 S1
15 A
14 V-
13 VR
12 VL
11 V+
10
9

DPDT
HI-5046 (75Ω)
HI-5046A (25Ω)

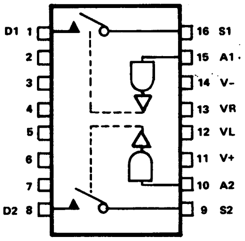

D2 1
2
D1 3
S1 4
S4 5
D4 6
7
D3 8
16 S2
15 A
14 V-
13 VR
12 VL
11 V+
10
9 S3

4 SPST
HI-5047 (75Ω)
HI-5047A (25Ω)

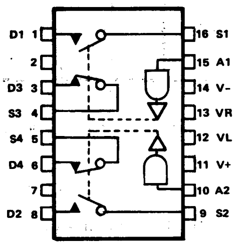

D2 1
2
D1 3
S1 4
S4 5
D4 6
7
D3 8
16 S2
15 A
14 V-
13 VR
12 VL
11 V+
10
9 S3

DUAL CONTROL

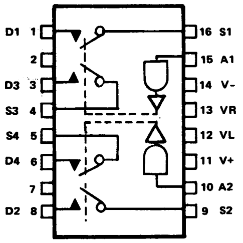
DUAL SPST
HI-5041 (75Ω)


D1 1
2
3
4
5
6
7
D2 8
16 S1
15 A1
14 V-
13 VR
12 VL
11 V+
10 A2
9 S2

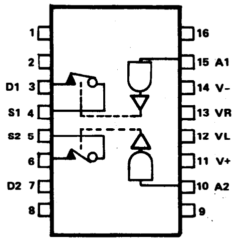
DUAL SPDT
HI-5043 (75Ω)
HI-5051 (25Ω)


D1 1
2
D3 3
S3 4
S4 5
D4 6
7
D2 8
16 S1
15 A1
14 V-
13 VR
12 VL
11 V+
10 A2
9 S2

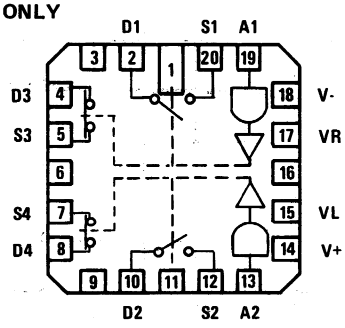
DUAL DPST
HI-5045 (75Ω)
HI-5049 (25Ω)


D1 1
2
D3 3
S3 4
S4 5
D4 6
7
D2 8
16 S1
15 A1
14 V-
13 VR
12 VL
11 V+
10 A2
9 S2

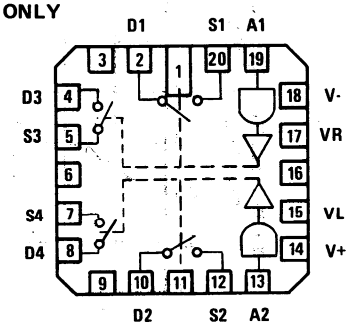
DUAL SPST
HI-5048 (25Ω)


1
2
D1 3
S1 4
S2 5
6
D2 7
8
16
15 A1
14 V-
13 VR
12 VL
11 V+
10 A2
9

HI-5043 ONLY


D1
S1
A1
3
2
1
20
19
D3
4
S3
5
6
S4
7
D4
8
18
V-
17
VR
16
15
VL
14
V+
9
10
11
12
13
D2
S2
A2

HI-5045 ONLY

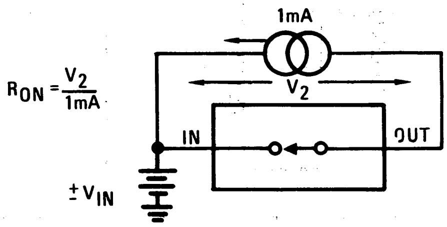

D1
S1
A1
3
2
1
20
19
D3
4
S3
5
6
S4
7
D4
8
18
V-
17
VR
16
15
VL
14
V+
9
10
11
12
13
D2
S2
A2

Note: Unused pins may be internally connected.

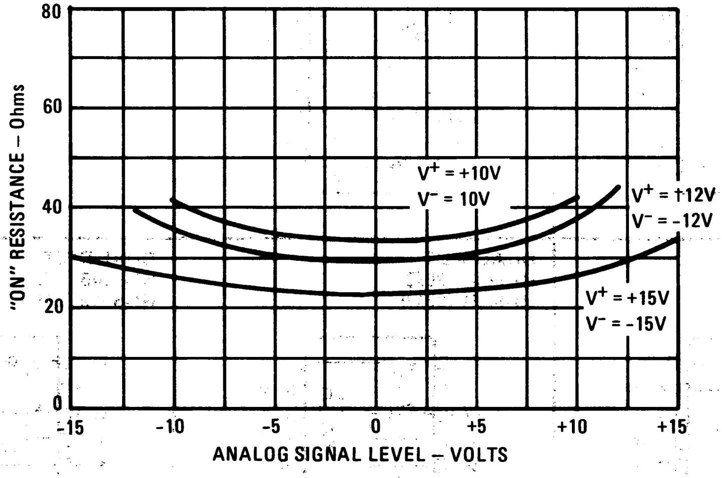
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, $V_R = 0V$, $V_{AH} = 3.0V$ and $V_{AL} = 0.8V$

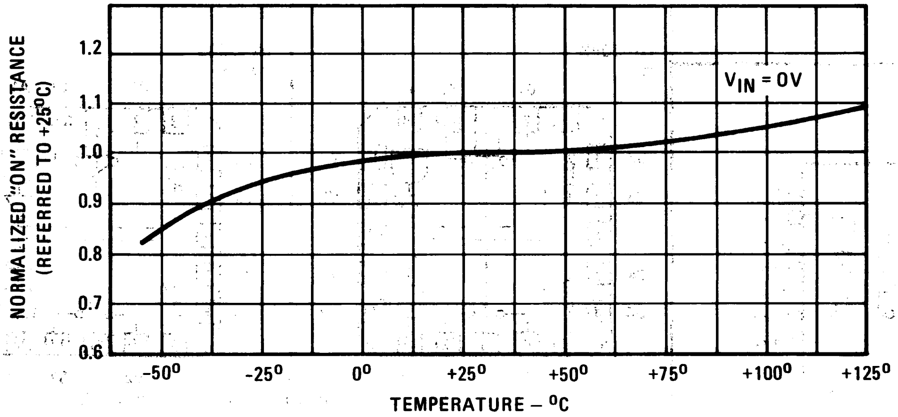
ON RESISTANCE vs. ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE



"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

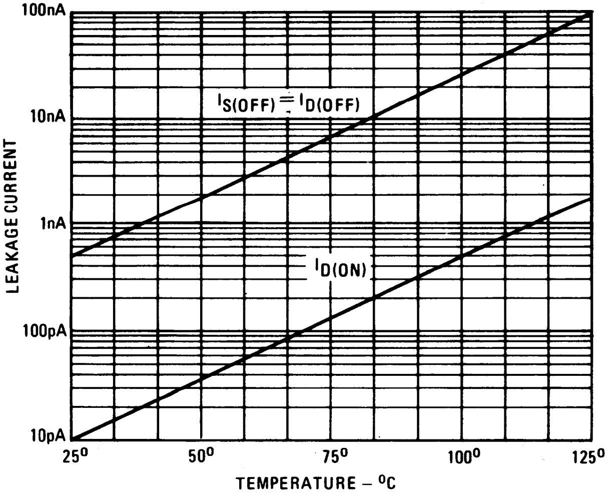


NORMALIZED "ON" RESISTANCE vs. TEMPERATURE

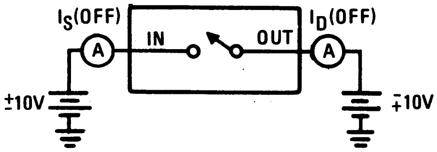


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

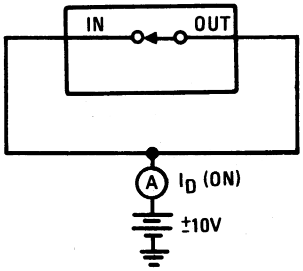
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



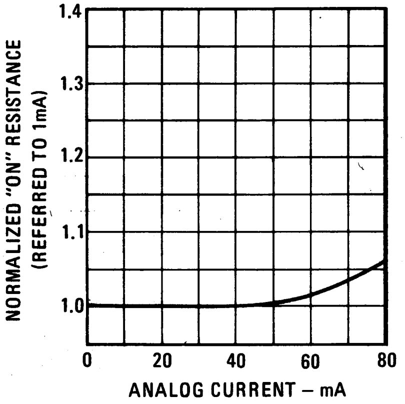
OFF LEAKAGE CURRENT vs. TEMPERATURE


I_S(OFF)
I_D(OFF)
IN
OUT
A
A
±10V
∓10V

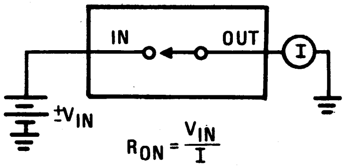
ON LEAKAGE CURRENT vs. TEMPERATURE


IN
OUT
A
I_D (ON)
±10V

NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT

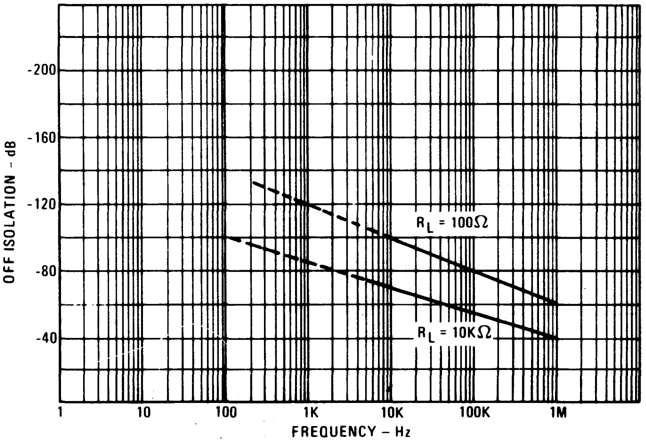


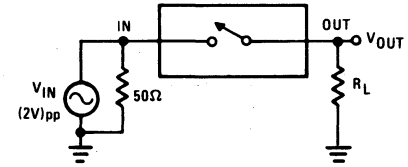
"ON" RESISTANCE vs. ANALOG CURRENT


IN
OUT
I
±V_{IN}
$R_{ON} = \frac{V_{IN}}{I}$

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS *(continued)*

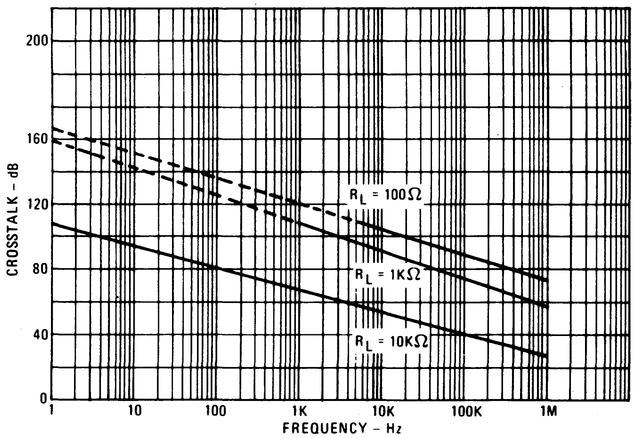
"OFF" ISOLATION vs. FREQUENCY

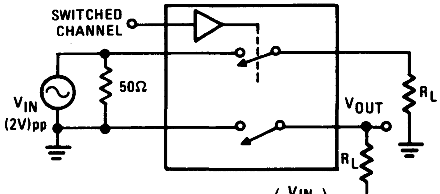



IN
OUT
V_{OUT}
V_{IN}
(2V)pp
50Ω
R_L

"OFF" ISOLATION = $20 \log\left(\frac{V_{IN}}{V_{OUT}}\right)$

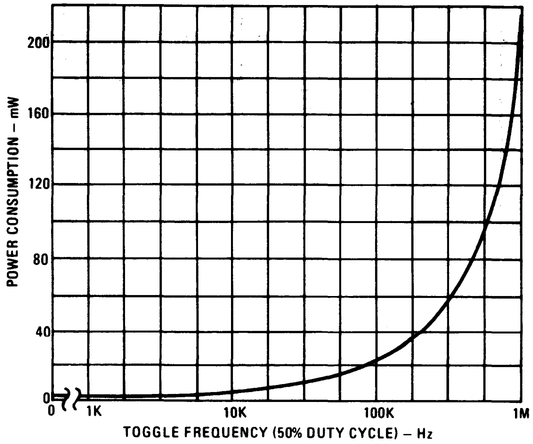
CROSSTALK vs. FREQUENCY

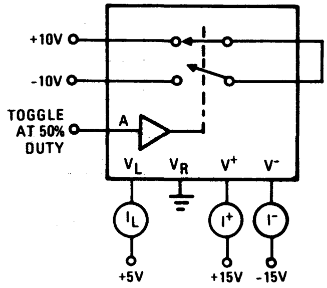



SWITCHED CHANNEL
V_{IN}
(2V)pp
50Ω
V_{OUT}
R_L
R_L

"CROSSTALK" = $20 \log\left(\frac{V_{IN}}{V_{OUT}}\right)$

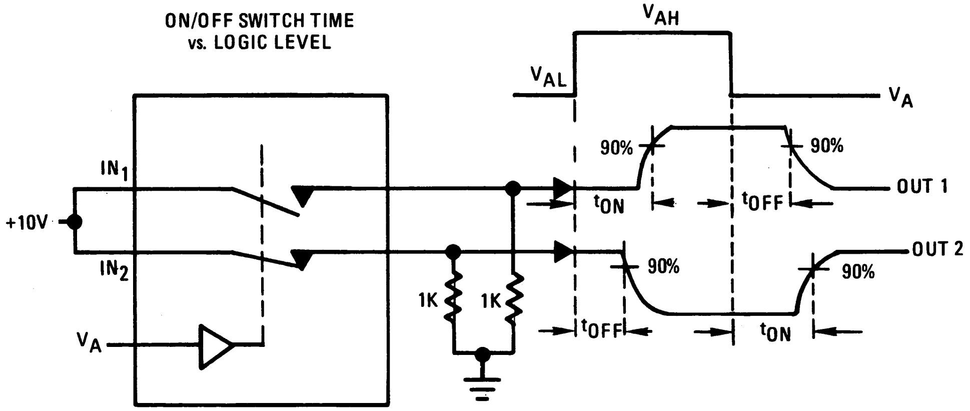
POWER CONSUMPTION vs. FREQUENCY

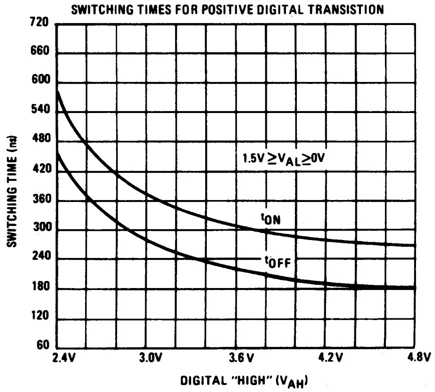


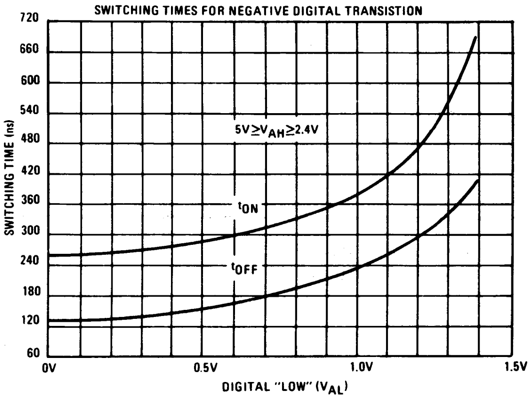

+10V
-10V
TOGGLE AT 50% DUTY
A
V_L
V_R
V^+
V^-
I_L
I^+
I^-
+5V
+15V
-15V

SWITCHING CHARACTERISTICS

ON/OFF SWITCH TIME
vs. LOGIC LEVEL

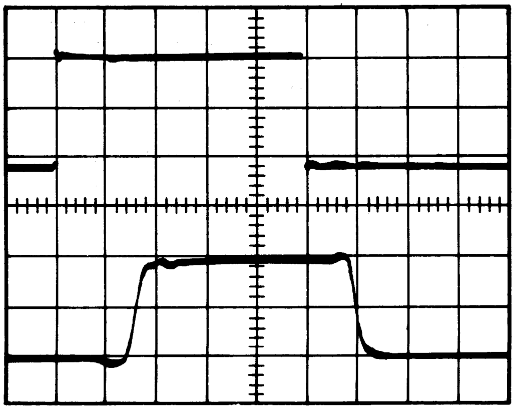

VAH
VAL
VA
IN1
IN2
+10V
VA
1K
1K
90%
90%
OUT 1
tON
tOFF
90%
90%
OUT 2
tOFF
tON





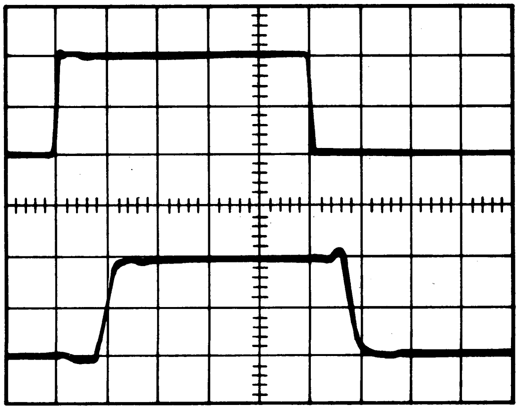
SWITCHING WAVEFORMS

TOP: TTL INPUT (1V/DIV)
V_{AH} = 3V, V_{AL} = 0.8V
BOTTOM: OUTPUT (5V/DIV)



200ns/DIV

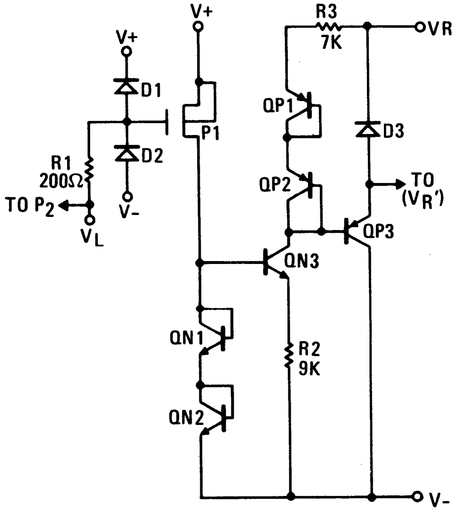
TOP: CMOS INPUT (5V/DIV)
V_{AH} = 10V, V_{AL} = 0V
BOTTOM: OUTPUT (5V/DIV



200ns/DIV

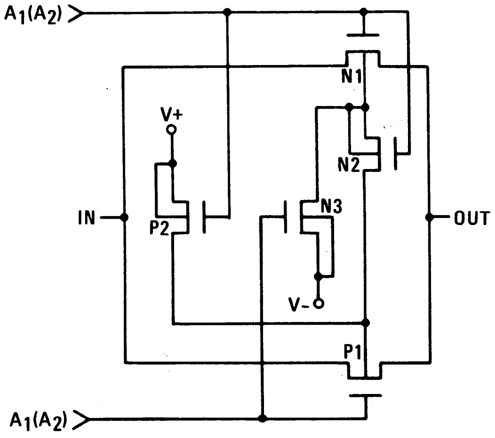
SCHEMATIC DIAGRAMS

TTL/CMOS
REFERENCE CIRCUIT*

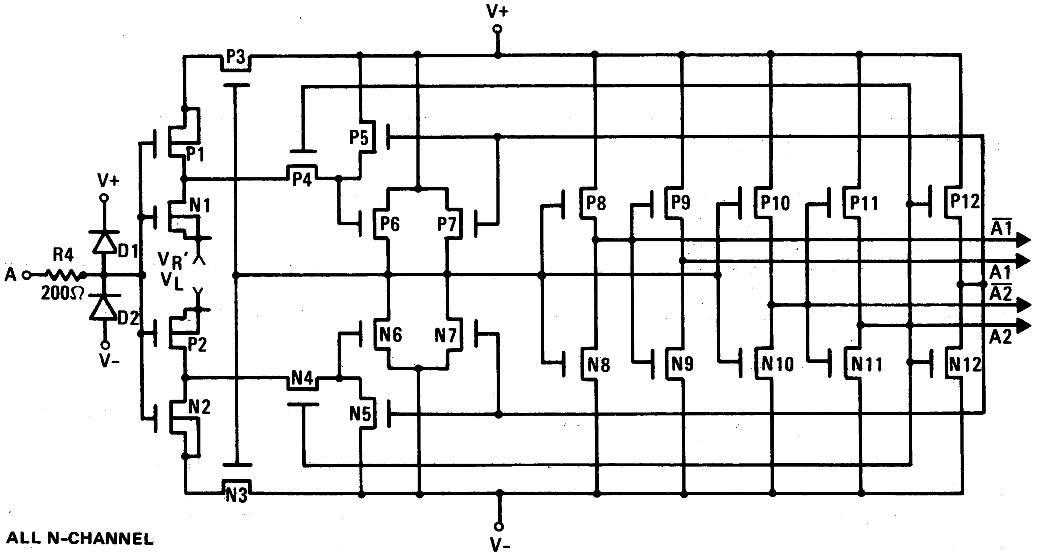

V+
V+
D1
D2
R1
200Ω
TO P_2
V_L
V-
P1
R3
7K
VR
QP1
QP2
D3
TO
(V_R')
QP3
QN3
QN1
QN2
R2
9K
V-

*Connect V^+ to V_L for minimizing power consumption when driving from CMOS circuits

SWITCH CELL


$A_1(A_2)$
N1
V+
N2
IN
P2
N3
OUT
V-
P1
$A_1(A_2)$

DIGITAL INPUT BUFFER
AND LEVEL SHIFTER


V+
P3
P1
P5
P4
P6
P7
P8
P9
P10
P11
P12
V+
D1
N1
R4
A
200Ω
V_R'
V_L
D2
P2
V-
$\overline{A1}$
A1
$\overline{A2}$
A2
N6
N7
N8
N9
N10
N11
N12
N4
N5
N2
N3
V-

ALL N-CHANNEL
BODIES TO V-

ALL P-CHANNEL
BODIES TO V+

EXCEPT AS SHOWN

ANALOG

Multiplexers

4

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ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

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HI-506LA/HI-507LA [illegible]

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HI-524 4 Channel Video Multiplexer 4-42

HI-539 Monolithic, 4 Channel, Low Level, Differential Multiplexer 4-47

HI-546/HI-547 Single 16/Differential 8 Channel CMOS Analog Multiplexers with Active Overvoltage Protection 4-56

HI-548/HI-549 Single 8/Differential 4 Channel CMOS Analog Multiplexers with Active Overvoltage Protection 4-62

HI-1818A/1828A Low On Resistance Single 8/Differential 4 Channel CMOS Analog Multiplexers 4-68

HY-9595/9596 Differential 8-Bit/Single 16-Bit Multiplexer with Programmable Gain Amplifier 4-72

Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H I 1 - 0506 - 5

PREFIX:
H (HARRIS)

FAMILY:
- A — Analog
- C — Communications
- D — Digital
- F — Filters
- I — Interface
- M — Memory
- V — Analog, High Voltage
- Y — Analog Hybrids

PACKAGE:
- 1 — Dual-In-Line, Ceramic
- 3 — Dual-In Line, Plastic
- 4 — Leadless Carriers (LCC)
- 4P — Plastic Leaded Chip Carrier (PLCC)
- 5 — LCC Hybrid
- 7 — Mini-DIP, Ceramic
- 0 — Chip Form

PART NUMBER

TEMPERATURE:
- 1 — 0°C to +200°C*
- 2 — -55°C to +125°C
- 4 — -25°C to +85°C
- 5 — 0°C to +75°C
- 6 — 100% +25°C Probe (Dice Only)
- 7 — Dash-7 High Reliability Commercial Product. 0°C to +75°C
- 8 — Dash-8 Program
- 9 — -40°C to +85°C

* Special high temperature testing available on certain product types. Consult factory for availability.

Standard Products Packaging Availability

PACKAGE	PLASTIC DIP	CERAMIC DIP					SURFACE MOUNT	
							LCC	PLCC
TEMPERATURE	-5	-2	-4	-5	-7	-8	-8	-5
DEVICE NUMBER								
MULTIPLEXERS								
HI-0506	X	X	X	X	X	X	X	X
HI-0506A	X	X		X	X	X	X	
HI-0507	X	X	X	X	X	X	X	X
HI-0507A	X	X		X	X	X	X	
HI-0508	X	X	X	X	X	X	X	X
HI-0508A	X	X		X	X	X	X	
HI-0509	X	X	X	X	X	X	X	X
HI-0509A	X	X		X	X	X	X	
HI-0516	X	X		X		X	X	
HI-0518	X	X		X		X	X	
HI-0524	X	X		X		X	X	X
HI-0539	X	X		X		X	X	X
HI-1818A	X	X		X		X	X	X
HI-1828A	X	X		X		X	X	X
HI-0546	X	X	X	X	X	*	*	X
HI-0547	X	X	X	X	X	*	*	X
HI-0548	X	X	X	X	X	*	*	X
HI-0549	X	X	X	X	X	*	*	X

*Available as MIL-STD-883 Only.

CMOS MULTIPLEXERS

FUNCTION	DEVICE	FEATURE	TTL 'HIGH' MIN(V)	R_{ON}(Ω) (TYP)	I_D(OFF) (nA) (TYP)	t(ON) (ns) (TYP)	t(OFF) (ns) (TYP)	P_D(mW) (TYP)	ΔR_{ON} (TYP)	PAGE
4-Channel Differential	HI-1828A	Low R_{ON} Low Leakage	4.0	250	0.05	350	250	5	N/A	4-68
	HI-509	Low R_{ON}	2.4	180	0.3	250	250	23	5%	4-18
	HI-509A	Analog Input Overvoltage Protection	4.0	1.2K	0.3	300	300	7.5	N/A	4-25
	HI-549	Analog Input Overvoltage Protection with Low ΔR_{ON}	4.0	1.2K	0.3	300	300	7.5	7% Max	4-62
	HI-509LA Advanced	Address Latches and Overvoltage Protection	2.0	1K	2.0	500	500	40	N/A	4-31
8-Channel	HI-1818A	Low R_{ON} Low Leakage	4.0	250	0.1	350	250	5	N/A	4-68
	HI-508	Low R_{ON}	2.4	180	0.3	250	250	23	5%	4-18
	HI-508A	Analog Input Overvoltage Protection	4.0	1.2K	0.3	300	300	7.5	N/A	4-25
	HI-548	Analog Input Overvoltage Protection with Low ΔR_{ON}	4.0	1.2K	0.3	300	300	7.5	7% Max	4-62
	HI-508LA Advanced	Address Address Latches and Overvoltage Protection	2.0	1K	2.0	500	500	40	N/A	4-31
8-Channel Differential	HI-507	Low R_{ON}	2.4	180	0.3	250	250	30	5%	4-5
	HI-507A	Analog Input Overvoltage Protection	4.0	1.2K	0.3	300	300	7.5	N/A	4-11
	HI-547	Analog Input Overvoltage Protection with Low ΔR_{ON}	4.0	1.2K	0.3	300	300	7.5	7% Max	4-56
	HI-507LA Advanced	Address Latches and Overvoltage Protection	2.0	1K	2.0	500	500	60	N/A	4-17
16-Channel	HI-506	Low R_{ON}	2.4	180	0.3	250	250	30	N/A	4-5
	HI-506A	Analog Input Overvoltage Protection	4.0	1.2K	0.3	300	300	7.5	N/A	4-11
	HI-546	Analog Input Overvoltage Protection with Low ΔR_{ON}.	4.0	1.2K	0.3	300	300	7.5	7% Max	4-56
	HI-506LA Advanced	Address Latches and Overvoltage Protection	2.0	1K	4.0	500	500	60	N/A	4-17
8-Channel 4-Differential	HI-518 Low Leakage	High Speed	2.4	480	0.1	80	80	360	N/A	4-37
16-Channel 8-Differential	HI-516 Low Leakage	High Speed	2.4	620	0.035	100	80	525	N/A	4-32
4-Channel	HI-524	Video Bandwidth	2.4	700	0.2	180	180	540	N/A	4-42
4-Channel Differential	HI-539	Low Level Signals	4.0 R_{ON} = 4Ω	650 I_D(OFF) = .003	0.03	250	160	2.5	0.6%	4-47
8-Differential	HY-9595 Advanced	Input Overvoltage Protected, Latched Programmable Gain	4.0	1.2K	0.3	TBD	TBD	TBD	N/A	4-72
16-Channel	HY-9596 Advanced	Input 0V Protected, Latched Programmable Gain	4.0	1K	0.3	TBD	TBD	TBD	N/A	4-72

HI-506/507

Single 16/Differential 8 Channel CMOS Analog Multiplexer

Features

- **Low On Resistance (Typ.)................180Ω**
- **Wide Analog Signal Range.............±15 V**
- **TTL/CMOS Compatible.......2.4 V (Logic "1")**
- **Access Time (Typ.)...................250 ns**
- **44 V Maximum Power Supply**
- **Break-Before-Make Switching**
- **No Latch-up**
- **Replaces DG506A/DG506AA and DG507A/DG507AA**

Applications

- **Data Acquisition Systems**
- **Precision Instrumentation**
- **Demultiplexing**
- **Selector Switch**

Description

These monolithic CMOS multiplexers each include an array of sixteen analog switches, a digital decode circuit for channel selection, voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

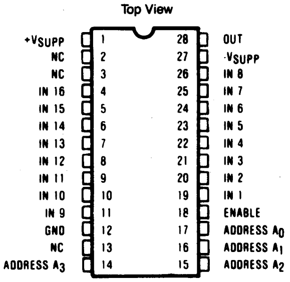
The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latchup. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (See Application Note 521). With the low ON resistance (180Ω typical), this allows low static error, fast channel switching rates, and fast settling.

The switching threshold for each digital input is established by an internal +5 V reference, providing a guaranteed minimum 2.4 V for "1" and maximum 0.8 V for "0". This allows direct interface without pullup resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and diode clamp to each supply.

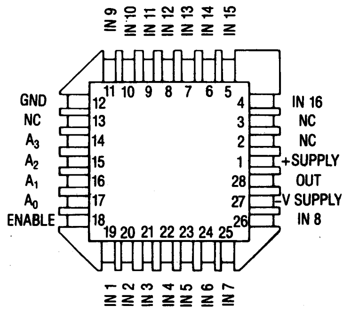
The HI-506 is a sixteen channel single-ended multiplexer, and the HI-507 is an eight channel differential version. Each device is available in a 28 pin ceramic or plastic DIP, a 28 pin ceramic LCC or 28 pin plastic LCC (PLCC) package. The recommended supply voltage is ±15 V, and reasonable performance is available down to ±7 V. If input overvoltage protection is needed, the HI-506A/507A multiplexers are recommended. For further information see Application Notes 520 and 521.

The HI-506/507 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in specify the "−8" suffix. For MIL-STD-883 compliant parts, request the 506/883 or 507/883 data sheet.

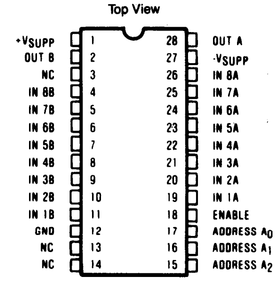
Pinouts


Top View
+VSUPP 1
NC 2
NC 3
IN 16 4
IN 15 5
IN 14 6
IN 13 7
IN 12 8
IN 11 9
IN 10 10
IN 9 11
GND 12
NC 13
ADDRESS A3 14
28 OUT
27 -VSUPP
26 IN 8
25 IN 7
24 IN 6
23 IN 5
22 IN 4
21 IN 3
20 IN 2
19 IN 1
18 ENABLE
17 ADDRESS A0
16 ADDRESS A1
15 ADDRESS A2

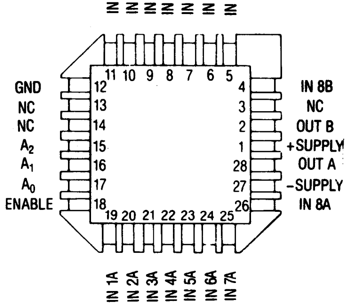
HI1-506 (ceramic)
HI3-506 (plastic)


IN 9
IN 10
IN 11
IN 12
IN 13
IN 14
IN 15
11 10 9 8 7 6 5
GND 12
NC 13
A3 14
A2 15
A1 16
A0 17
ENABLE 18
4 IN 16
3 NC
2 NC
1 +SUPPLY
28 OUT
27 -V SUPPLY
26 IN 8
19 20 21 22 23 24 25
IN 1
IN 2
IN 3
IN 4
IN 5
IN 6
IN 7

HI4-506 (LCC)
HI4P506 (PLCC)

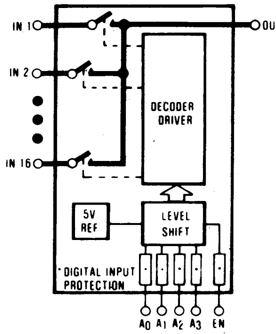

Top View
+VSUPP 1
OUT B 2
NC 3
IN 8B 4
IN 7B 5
IN 6B 6
IN 5B 7
IN 4B 8
IN 3B 9
IN 2B 10
IN 1B 11
GND 12
NC 13
NC 14
28 OUT A
27 -VSUPP
26 IN 8A
25 IN 7A
24 IN 6A
23 IN 5A
22 IN 4A
21 IN 3A
20 IN 2A
19 IN 1A
18 ENABLE
17 ADDRESS A0
16 ADDRESS A1
15 ADDRESS A2

HI1-507 (ceramic)
HI3-507 (plastic)

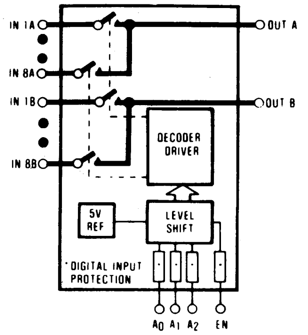

IN 1B
IN 2B
IN 3B
IN 4B
IN 5B
IN 6B
IN 7B
11 10 9 8 7 6 5
GND 12
NC 13
NC 14
A2 15
A1 16
A0 17
ENABLE 18
4 IN 8B
3 NC
2 OUT B
1 +SUPPLY
28 OUT A
27 -SUPPLY
26 IN 8A
19 20 21 22 23 24 25
IN 1A
IN 2A
IN 3A
IN 4A
IN 5A
IN 6A
IN 7A

HI4-507 (LCC)
HI4P507 (PLCC)

Functional Diagrams


IN 1
IN 2
IN 16
OUT
DECODER DRIVER
5V REF
LEVEL SHIFT
DIGITAL INPUT PROTECTION
A0 A1 A2 A3 EN

HI-506


IN 1A
IN 8A
IN 1B
IN 8B
OUT A
OUT B
DECODER DRIVER
5V REF
LEVEL SHIFT
DIGITAL INPUT PROTECTION
A0 A1 A2 EN

HI-507

ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{Supply}(+)$ to $V_{Supply}(-)$ 44 V
$V_{Supply}(+)$ to GND 22 V
$V_{Supply}(-)$ to GND 25 V
Digital Input Overvoltage:
V_{EN}, V_A $\left\{ \begin{array}{ll} V_{Supply}(+) & +4\text{ V} \\ V_{Supply}(-) & -4\text{ V} \end{array} \right\}$
or 20 mA, whichever occurs first.
Analog Signal Overvoltage (Note 7)
V_D, V_S $\left\{ \begin{array}{ll} V_{Supply}(+) & +2\text{ V} \\ V_{Supply}(-) & -2\text{ V} \end{array} \right\}$

Continuous Current, S or D: 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max): 40 mA
Power Dissipation* (Cerdip) 1.96 W
Operating Temperature Range:
HI-506/507-2,-8 −55°C to +125°C
HI-506/507-4 −25°C to +85°C
HI-506/507-5 0°C to +75°C
Storage Temperature Range −65°C to +150°C

*Derate 19.6 mW/°C above T_A =75°C

ELECTRICAL CHARACTERISTICS Unless Otherwise Specified:

Supplies= +15 V, −15 V; V_{AH}(Logic Level High) = +2.4 V, V_{AL} (Logic Level Low) = +0.8 V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-506/HI-507 −2, −8			HI-506/507 −4, −5			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	−15		+15	−15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		180	300		180	400	Ω
	Full			400			500	Ω
$\triangle R_{ON}$, (Any Two Channels)	+25°C		5			5		%
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-506	Full			300			300	nA
HI-507	Full			200			200	nA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-506	Full			300			300	nA
HI-507	Full			200			200	nA
*I_{DIFF} Differential Off Output Leakage Current (HI-507 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold	Full			+0.8			+0.8	V
*V_{AH},, Input High Threshold	Full	+2.4			+2.4			V
*I_A, Input Leakage Current (High or Low) (Note 4)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Delay (ON)	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		250	500		250		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		2.4			2.4		μs
"Off Isolation" (Note 5)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506	+25°C		44			44		pF
HI-507	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.08			0.08		pF
POWER REQUIREMENTS								
*I+, Current, Pin 1 (Note 6)	Full		1.5	3.0		1.5	3.0	mA
*I−, Current Pin 27 (Note 6)	Full		0.4	1.0		0.4	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at −55°C.

TRUTH TABLES

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507

A_2	A_1	A_0	EN	ON CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

NOTES:

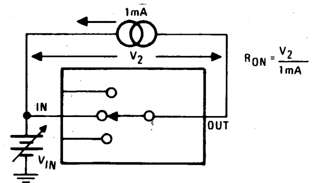
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} ±10V, I_{OUT} -1mA.
3. 10nA is the practical lower limit for high speed measurement in the production test environment.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
5. V_{EN} 0.8V, R_L 1K, C_L 15pF, V_S 7V_{RMS}, f 100kHz. Worst case isolation occurs on channel 8B due to proximity of the output pins.
6. V_{EN}, V_A 0V or 2.4V.
7. Signal voltage at any analog input or output (S or D) will be clamped to the supply rail by internal diodes. Limit the resulting current as shown under Absolute Maximum Ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the Harris HI-506A/507A multiplexers are recommended.

Performance Characteristics and Test Circuits

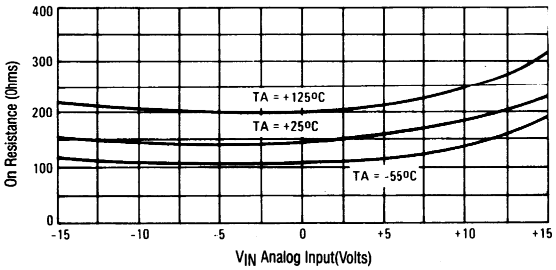
Unless Otherwise Specified; $T_A = 25°C$, $V_{Supply} = \pm 15$ V, $V_{AH} = 2.4$ V, $V_{AL} = 0.8$ V.

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

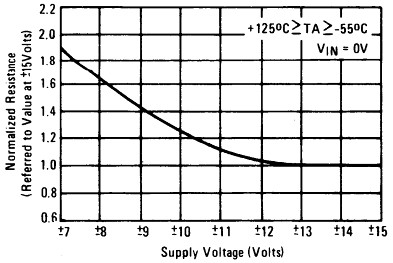
TEST CIRCUIT NO. 1


1mA
V2
RON = V2/1mA
IN
OUT
VIN

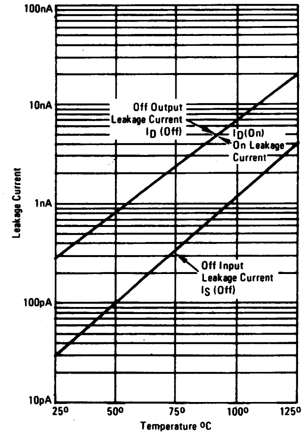
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



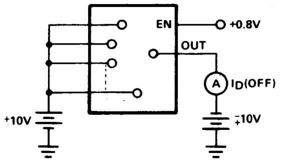
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



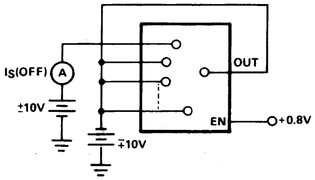
LEAKAGE CURRENT VS. TEMPERATURE



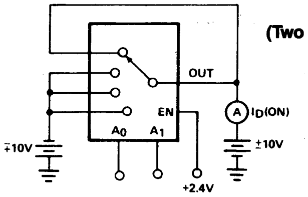
TEST CIRCUIT NO. 2*


EN
+0.8V
OUT
A
ID(OFF)
+10V
∓10V

TEST CIRCUIT NO. 3*

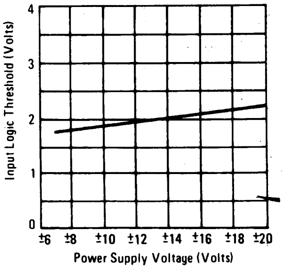

OUT
IS(OFF)
A
±10V
EN
+0.8V
∓10V

TEST CIRCUIT NO. 4*

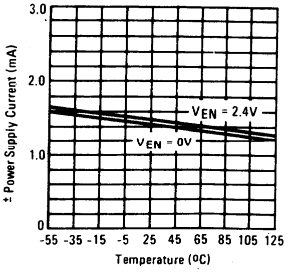

OUT
EN
A
ID(ON)
A0
A1
∓10V
±10V
+2.4V

***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for I_D(OFF) +10 V/−10 V and −10 V/+10 V.)**

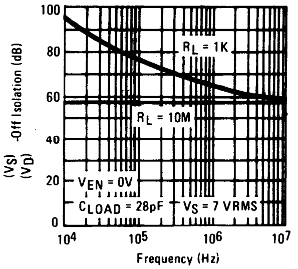
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE

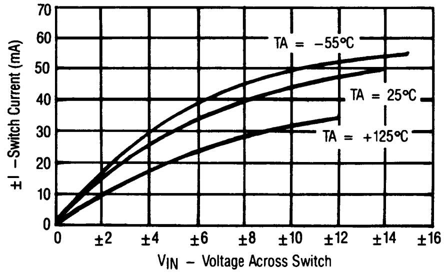


OFF ISOLATION vs. FREQUENCY



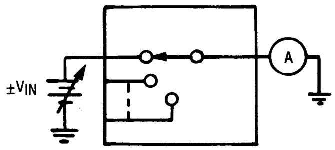
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE



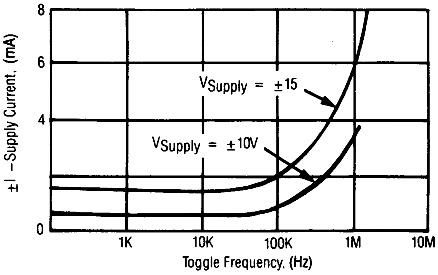
TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

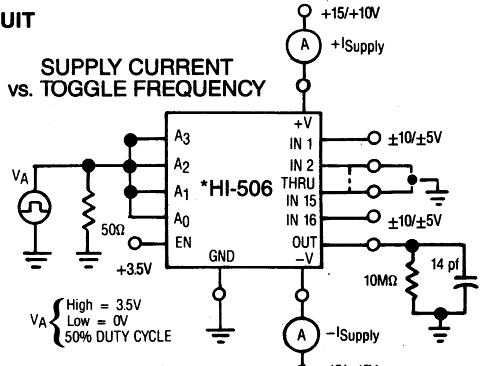


TEST CIRCUIT NO. 6

SUPPLY CURRENT vs. TOGGLE FREQUENCY



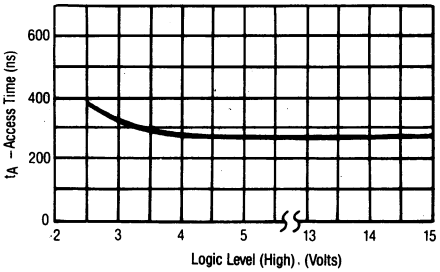
SUPPLY CURRENT vs. TOGGLE FREQUENCY


+15/+10V
A
+I_{Supply}
+V
A_3
A_2
A_1
A_0
EN
*HI-506
IN 1
IN 2 THRU IN 15
IN 16
OUT
–V
GND
±10/±5V
±10/±5V
V_A
50Ω
+3.5V
14 pf
10MΩ
V_A High = 3.5V Low = 0V 50% DUTY CYCLE
A
–I_{Supply}
–15/–10V

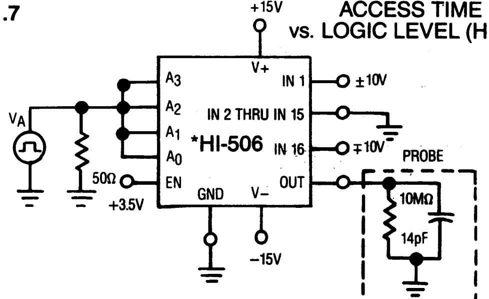
*Similar connection for HI-507

TEST CIRCUIT NO .7

ACCESS TIME VS. LOGIC LEVEL (HIGH)

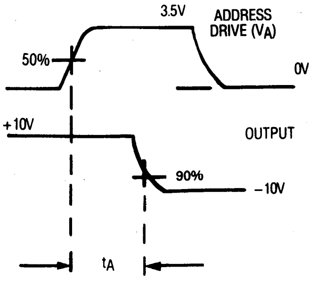


ACCESS TIME vs. LOGIC LEVEL (HIGH)

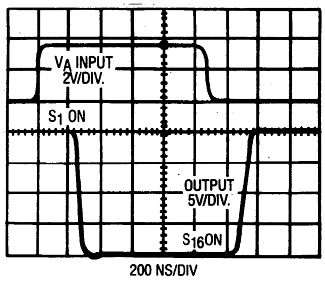

+15V
V+
A_3
A_2
A_1
A_0
EN
*HI-506
IN 1
IN 2 THRU IN 15
IN 16
OUT
GND
V–
±10V
∓10V
PROBE
10MΩ
14pF
V_A
50Ω
+3.5V
–15V

*Similar connection for HI-507

Switching Waveforms

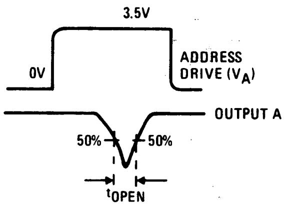

3.5V
ADDRESS DRIVE (V_A)
50%
0V
+10V
OUTPUT
90%
–10V
t_A

ACCESS TIME

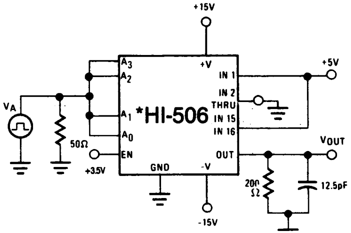


Switching Waveforms (continued)

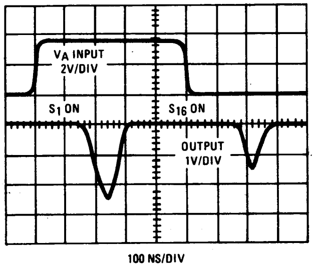
TEST CIRCUIT NO. 8


3.5V
0V
ADDRESS DRIVE (V_A)
OUTPUT A
50%
50%
t_{OPEN}

BREAK-BEFORE-MAKE DELAY (t_{OPEN})

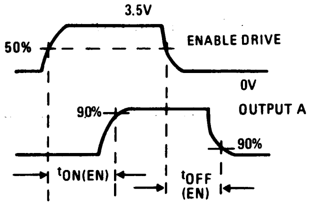

+15V
A_3
A_2
A_1
A_0
EN
+V
IN 1
IN 2 THRU IN 15
IN 16
OUT
GND
-V
*HI-506
+5V
V_{OUT}
V_A
50Ω
+3.5V
200 Ω
12.5pF
-15V

BREAK-BEFORE-MAKE DELAY(t_{OPEN})

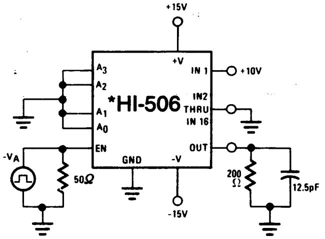


*Similar connection for HI-507

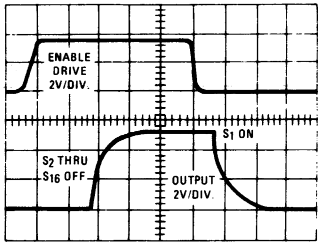
TEST CIRCUIT NO. 9


3.5V
50%
ENABLE DRIVE
0V
90%
OUTPUT A
90%
$t_{ON(EN)}$
t_{OFF} (EN)

ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)


+15V
A_3
A_2
A_1
A_0
EN
+V
IN 1
IN2 THRU IN 16
OUT
GND
-V
*HI-506
+10V
$-V_A$
50Ω
200 Ω
12.5pF
-15V

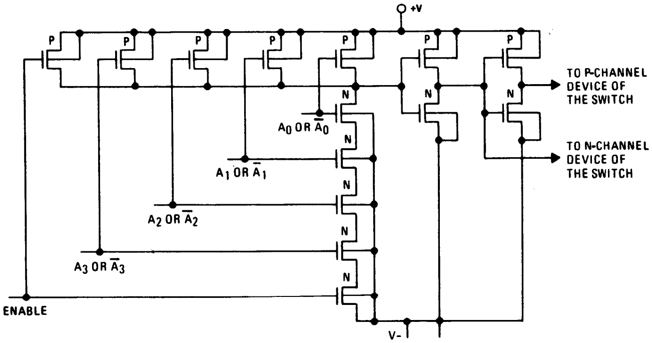
ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)



*Similar connection for HI-507

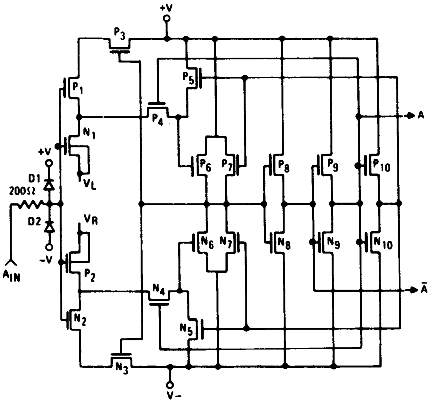
Schematic Diagrams

ADDRESS DECODER


+V
P
N
TO P-CHANNEL DEVICE OF THE SWITCH
TO N-CHANNEL DEVICE OF THE SWITCH
A_0 OR $\overline{A_0}$
A_1 OR $\overline{A_1}$
A_2 OR $\overline{A_2}$
A_3 OR $\overline{A_3}$
ENABLE
V-

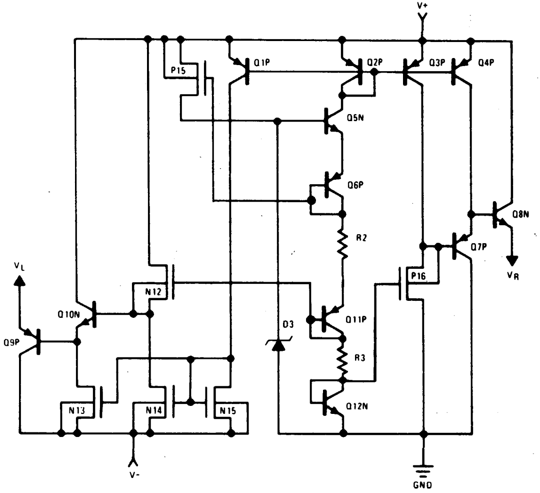
Delete A_3 or $\overline{A_3}$ Input for HI-507

ADDRESS INPUT BUFFER LEVER SHIFTER

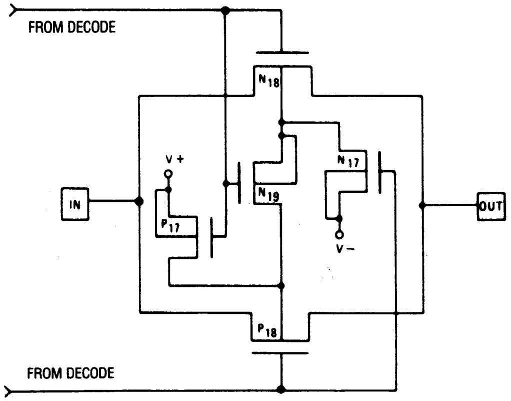

+V
P_3
P_1
P_5
P_4
N_1
+V
V_L
D_1
200Ω
D_2
V_R
-V
A_{IN}
P_2
P_6
P_7
P_8
P_9
P_{10}
N_6
N_7
N_8
N_9
N_{10}
N_4
N_5
N_2
N_3
V-
A
$\overline{A}$

All N-Channel Bodies to V−
All P-Channel Bodies to V+
Unless Otherwise Indicated

TTL REFERENCE CIRCUIT


V+
P15
Q1P
Q2P
Q3P
Q4P
Q5N
Q6P
R2
Q8N
Q7P
VR
P16
VL
N12
Q10N
Q9P
D3
Q11P
R3
Q12N
N13
N14
N15
V-
GND

MULTIPLEX SWITCH


FROM DECODE
N18
V +
N17
IN
N19
OUT
P17
V −
P18
FROM DECODE

Die Characteristics

Transistor Count		421	
Die Size		110 x 83 mils	
Thermal Constants	θja	51°C/W	For Ceramic DIP
	θjc	20°C/W	
Tie Substrate to:		$-V_{Supply}$	
Process:		CMOS-DI	

HI-506A/507A

Single 16/Differential 8 Channel
CMOS Analog Multiplexer with Active Overvoltage Protection

Features

- **Analog Overvoltage Protection . . . . 70 Vpp**
- **No Channel Interaction During Overvoltage**
- **ESD Resistant . . . . >4,000 Volts**
- **44 V Maximum Power Supply**
- **Fail Safe with Power Loss (No Latchup)**
- **Break-Before-Make Switching**
- **Analog Signal Range . . . . ±15 V**
- **Access Time (Typical) . . . . 500 ns**
- **Standby Power (Typical) . . . . 7.5 mW**

Applications

- **Data Acquisition**
- **Industrial Controls**
- **Telemetry**

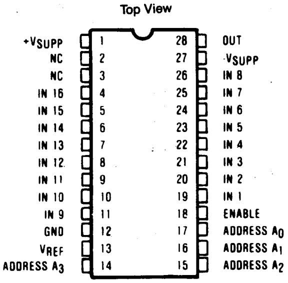
Description

The HI-506A and HI-507A are analog multiplexers with Active Overvoltage Protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-506A and HI-507A ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The 506A is a 16 channel device and the 507A is an 8 channel differential version. If input overvoltage protection is not needed, the HI-506 and HI-507 multiplexers are recommended. For further information see Application Notes 520 and 521.

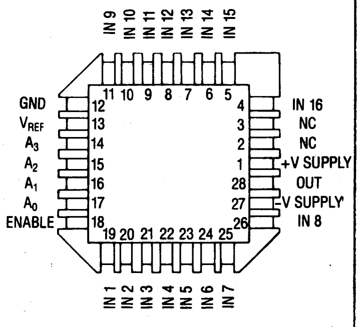
Each device is available in a 16 pin plastic or ceramic DIP, a 20 pin ceramic LCC package.

The HI-506A/507A are offered in both commercial and military grades. Additional Hi-Rel screening including 160 hour burn-in is specified by the "–8" suffix.

Pinouts

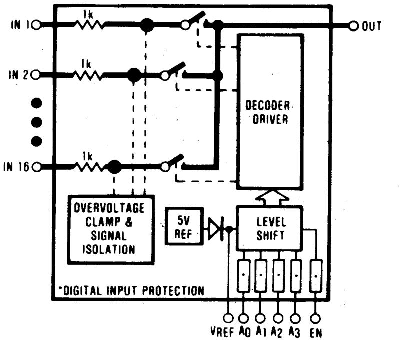

Top View
+VSUPP 1
NC 2
NC 3
IN 16 4
IN 15 5
IN 14 6
IN 13 7
IN 12 8
IN 11 9
IN 10 10
IN 9 11
GND 12
VREF 13
ADDRESS A3 14
28 OUT
27 -VSUPP
26 IN 8
25 IN 7
24 IN 6
23 IN 5
22 IN 4
21 IN 3
20 IN 2
19 IN 1
18 ENABLE
17 ADDRESS A0
16 ADDRESS A1
15 ADDRESS A2

HI1-506A (ceramic)
HI3-506A (plastic)

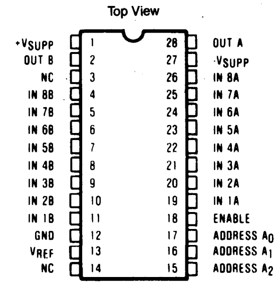

IN 9
IN 10
IN 11
IN 12
IN 13
IN 14
IN 15
11 10 9 8 7 6 5
GND 12
VREF 13
A3 14
A2 15
A1 16
A0 17
ENABLE 18
4 IN 16
3 NC
2 NC
1 +V SUPPLY
28 OUT
27 -V SUPPLY
26 IN 8
19 20 21 22 23 24 25
IN 1
IN 2
IN 3
IN 4
IN 5
IN 6
IN 7

HI4-506A (LCC)

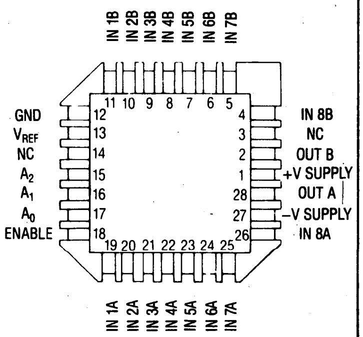
Functional Diagrams


IN 1
1k
OUT
IN 2
1k
IN 16
1k
DECODER DRIVER
OVERVOLTAGE CLAMP & SIGNAL ISOLATION
5V REF
LEVEL SHIFT
*DIGITAL INPUT PROTECTION
VREF A0 A1 A2 A3 EN

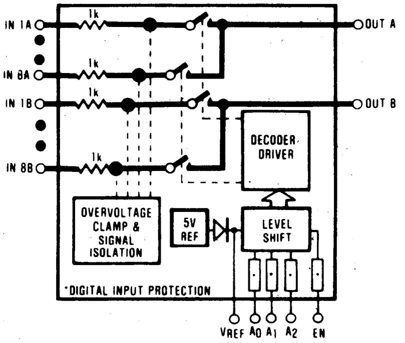
HI-506A


Top View
+VSUPP 1
OUT B 2
NC 3
IN 8B 4
IN 7B 5
IN 6B 6
IN 5B 7
IN 4B 8
IN 3B 9
IN 2B 10
IN 1B 11
GND 12
VREF 13
NC 14
28 OUT A
27 -VSUPP
26 IN 8A
25 IN 7A
24 IN 6A
23 IN 5A
22 IN 4A
21 IN 3A
20 IN 2A
19 IN 1A
18 ENABLE
17 ADDRESS A0
16 ADDRESS A1
15 ADDRESS A2

HI1-507A (ceramic)
HI3-507A (plastic)


IN 1B
IN 2B
IN 3B
IN 4B
IN 5B
IN 6B
IN 7B
11 10 9 8 7 6 5
GND 12
VREF 13
NC 14
A2 15
A1 16
A0 17
ENABLE 18
4 IN 8B
3 NC
2 OUT B
1 +V SUPPLY
28 OUT A
27 -V SUPPLY
26 IN 8A
19 20 21 22 23 24 25
IN 1A
IN 2A
IN 3A
IN 4A
IN 5A
IN 6A
IN 7A

HI4-507A (LCC)


IN 1A
1k
OUT A
IN 8A
1k
IN 1B
1k
OUT B
IN 8B
1k
DECODER DRIVER
OVERVOLTAGE CLAMP & SIGNAL ISOLATION
5V REF
LEVEL SHIFT
*DIGITAL INPUT PROTECTION
VREF A0 A1 A2 EN

HI-507A

HI-506A/507A Specifications

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supply Pins	44 V
V_{REF} to Ground, V+ to Ground	22 V
V− to Ground	25 V

Digital Input Overvoltage:

V_{EN}, V_A $\left\{ \begin{array}{ll} V_{Supply}(+) & +4\text{ V} \\ V_{Supply}(-) & -4\text{ V} \end{array} \right\}$

or 20 mA, whichever occurs first.

Analog Input Overvoltage:

V_S $\left\{ \begin{array}{ll} V_{Supply}(+) & +20\text{ V} \\ V_{Supply}(-) & -20\text{ V} \end{array} \right\}$

Continous Current, S or D:	20 mA
Peak Current, S or D (Pulsed at 1 msec, 10% duty cycle max):	40 mA
Power Dissipation* (Cerdip)	2.0 W
Operating Temperature Range:	
HI-506A/507A-2,-8	−55°C to +125°C
HI-506A/507A-5	0°C to +75°C
Storage Temperture Range	−65°C to +150°C

*Derate 20.0 mW/°C above T_A =75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: Supplies = +15 V, −15 V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0 V; V_{AL} (Logic Level Low) = + 0.8 V. For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	HI-506A/HI-507A -2, -8 MIN.	HI-506A/HI-507A -2, -8 TYP.	HI-506A/HI-507A -2, -8 MAX.	HI-506A/507A -5 MIN.	HI-506A/507A -5 TYP.	HI-506A/507A -5 MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	−15		+15	−15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-506A	Full			300			300	nA
HI-507A	Full			200			200	nA
*I_D (OFF), with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-506A	Full			300			300	nA
HI-507A	Full			200			200	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-507A Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold TTL Drive	Full			0.8			0.8	V
*V_{AH}, Input High Threshold (Note 8)	Full	4.0			4.0			V
V_{AL} MOS Drive (Note 9)	+25°C			0.8			0.8	V
V_{AH}	+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		0.5			0.5		μs
	Full			1.0			1.0	μs
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		3.5			3.5		μs
"Off Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506A	+25°C		50			50		pF
HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current Pin 1 (Note 7)	Full		0.5	2.0		0.5	2.0	mA
*I−, Current Pin 27 (Note 7)	Full		0.02	1.0		0.02	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at −55°C.

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	ON CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

NOTES:

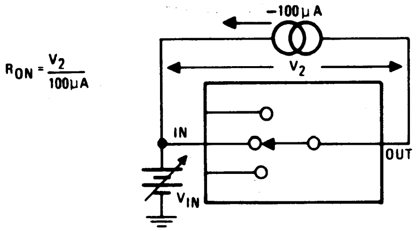
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = −100 μA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33 V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1 nA at 25°C.
6. V_{EN} = 0.8 V. R_L = 1 K, C_L = 15 pF, V_S = 7 V_{RMS}, f = 100 kHz. Worst case isolation occurs on channel 8B due to proximity of the output pins.
7. V_{EN}, V_A = 0 V or 4.0 V.
8. To drive from DTL/TTL Circuits, 1 kΩ pull-up resistors to +5.0 V supply are recommended.
9. V_{REF} = +10 V.

Performance Characteristics and Test Circuits

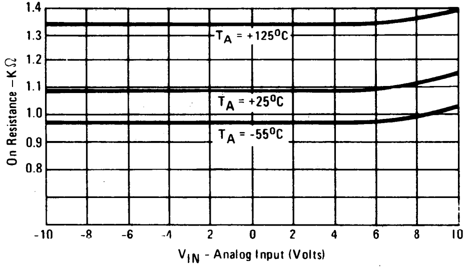
Unless Otherwise Specified: T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V And V_{Ref} = Open.

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

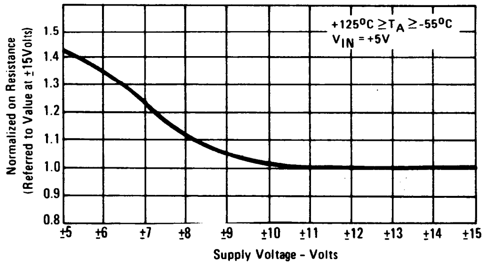
TEST CIRCUIT NO. 1


$R_{ON} = \frac{V_2}{100\mu A}$
−100μ A
V_2
IN
OUT
V_{IN}

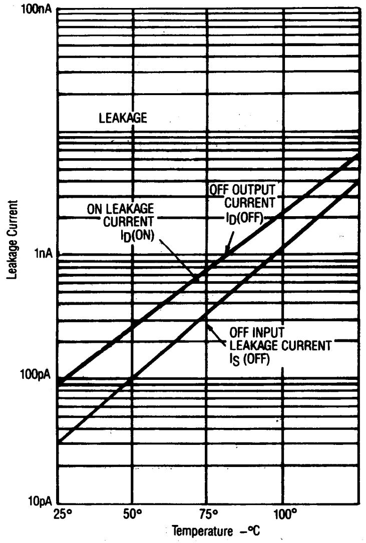
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



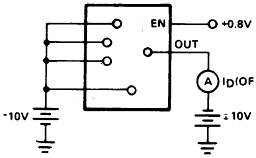
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



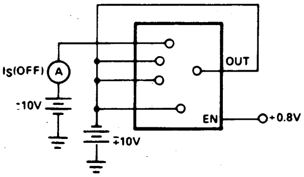
LEAKAGE CURRENT VS. TEMPERATURE



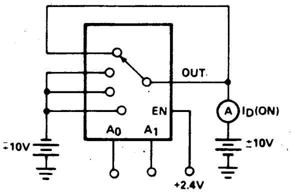
TEST CIRCUIT NO. 2*


EN
+0.8V
OUT
I_D(OFF)
·10V
±10V

TEST CIRCUIT NO. 3*

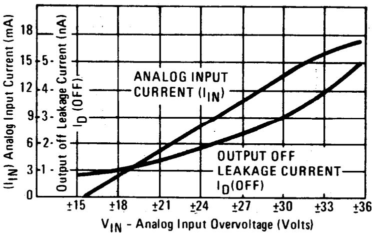

I_S(OFF)
OUT
±10V
EN
+0.8V
±10V

TEST CIRCUIT NO. 4*


OUT
EN
A_0
A_1
I_D(ON)
±10V
±10V
+2.4V

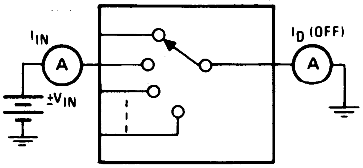
***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for I_D(OFF): +10 V/−10 V and −10 V/+10 V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

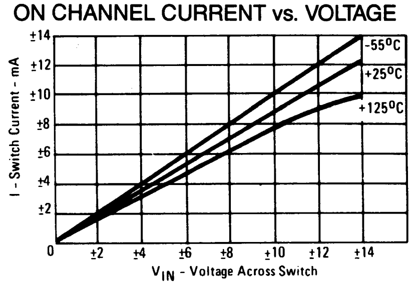


TEST CIRCUIT NO. 5

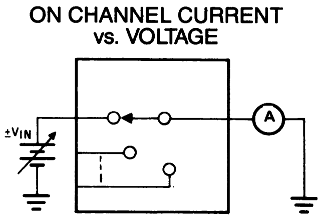
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

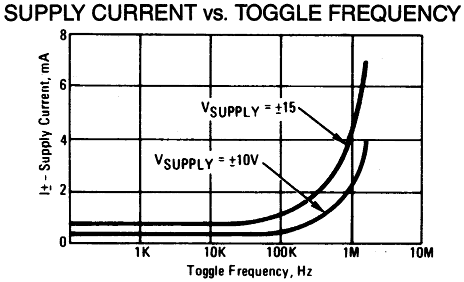

I_{IN}
I_D (OFF)
±V_{IN}

Performance Characteristics and Test Circuits (continued)

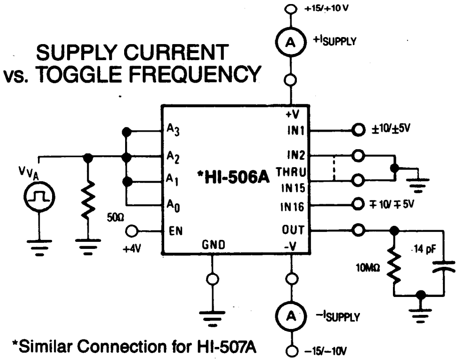

ON CHANNEL CURRENT vs. VOLTAGE

TEST CIRCUIT NO. 6

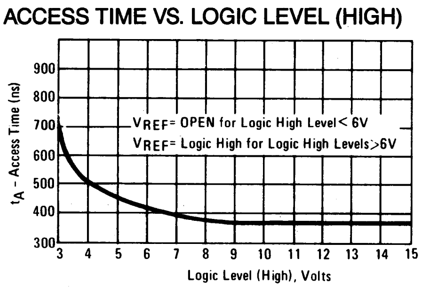

ON CHANNEL CURRENT vs. VOLTAGE


SUPPLY CURRENT vs. TOGGLE FREQUENCY

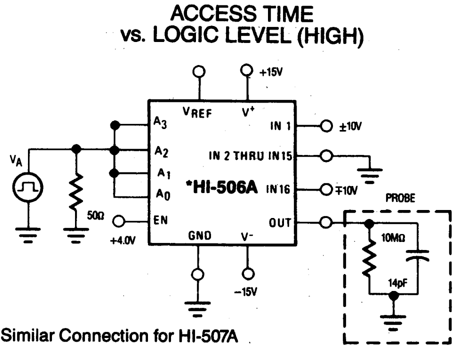
TEST CIRCUIT NO. 7


SUPPLY CURRENT vs. TOGGLE FREQUENCY
+15/+10 V
A
$+I_{SUPPLY}$
+V
IN1
±10/±5V
A_3
A_2
A_1
A_0
V_{V_A}
*HI-506A
IN2
THRU
IN15
IN16
∓10/∓5V
50Ω
EN
+4V
GND
OUT
-V
14 pF
10MΩ
A
$-I_{SUPPLY}$
−15/−10V

*Similar Connection for HI-507A

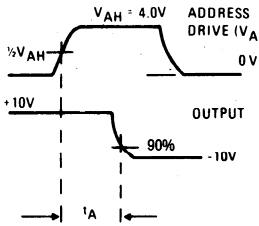

ACCESS TIME VS. LOGIC LEVEL (HIGH)

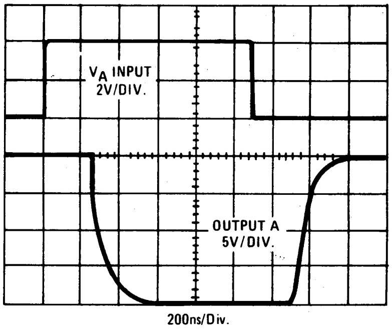
TEST CIRCUIT NO. 8


ACCESS TIME vs. LOGIC LEVEL (HIGH)
+15V
V_{REF}
V^+
A_3
IN 1
±10V
V_A
A_2
IN 2 THRU IN15
A_1
A_0
*HI-506A
IN16
∓10V
PROBE
50Ω
EN
+4.0V
GND
V^-
OUT
10MΩ
14pF
−15V

*Similar Connection for HI-507A

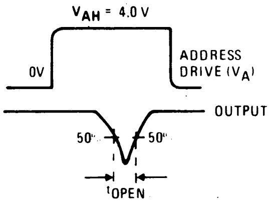
Switching Waveforms


V_{AH} = 4.0V
ADDRESS DRIVE (V_A)
½V_{AH}
0 V
+10V
OUTPUT
90%
-10V
t_A

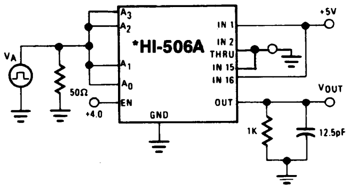


Switching Waveforms (continued)

TEST CIRCUIT NO. 9

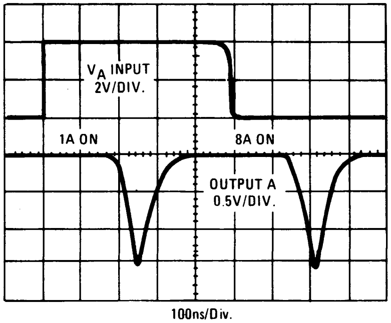

V_{AH} = 4.0 V
0V
ADDRESS DRIVE (V_A)
OUTPUT
50%
50%
t_{OPEN}

BREAK-BEFORE-MAKE DELAY (tOPEN)


A_3
A_2
A_1
A_0
EN
*HI-506A
IN 1
IN 2 THRU IN 15
IN 16
OUT
GND
+5V
V_A
50Ω
+4.0
V_{OUT}
1K
12.5pF

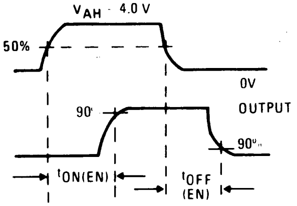
*Similar Connection for HI-507A

BREAK-BEFORE-MAKE DELAY(tOPEN)

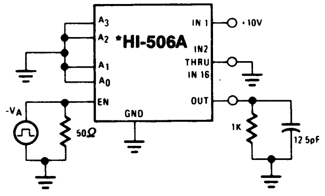


TEST CIRCUIT NO. 10

ENABLE DRIVE

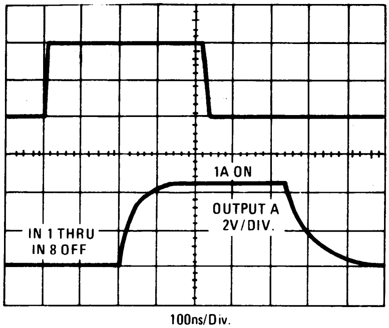

V_{AH} 4.0 V
50%
0V
OUTPUT
90%
90%
$t_{ON(EN)}$
$t_{OFF(EN)}$

ENABLE DELAY (tON(EN),tOFF(EN))

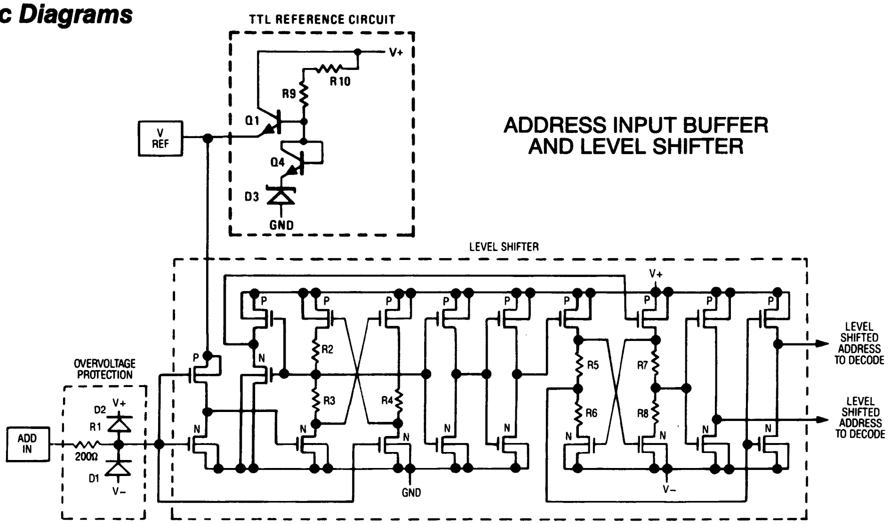

A_3
A_2
A_1
A_0
EN
*HI-506A
IN 1
IN2 THRU IN 16
OUT
GND
+10V
$-V_A$
50Ω
1K
12.5pF

*Similar Connection for HI-507A

ENABLE DELAY (tON(EN),tOFF(EN))



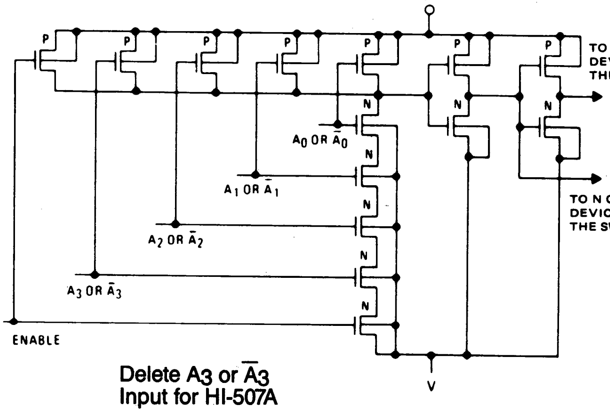
Schematic Diagrams


TTL REFERENCE CIRCUIT
V+
R10
R9
Q1
V REF
Q4
D3
GND
LEVEL SHIFTER
V+
P
N
R2
R3
R4
R5
R6
R7
R8
OVERVOLTAGE PROTECTION
D2
V+
R1
200Ω
D1
V−
ADD IN
GND
V−
LEVEL SHIFTED ADDRESS TO DECODE
LEVEL SHIFTED ADDRESS TO DECODE

ADDRESS INPUT BUFFER AND LEVEL SHIFTER

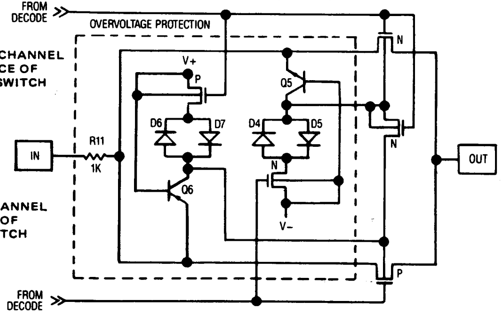
Schematic Diagrams (continued)

ADDRESS DECODER


V+
P
N
TO P CHANNEL DEVICE OF THE SWITCH
TO N CHANNEL DEVICE OF THE SWITCH
A_0 OR $\bar{A}_0$
A_1 OR $\bar{A}_1$
A_2 OR $\bar{A}_2$
A_3 OR $\bar{A}_3$
ENABLE
V

Delete A3 or $\overline{A}3$
Input for HI-507A

MULTIPLEX SWITCH


FROM DECODE
OVERVOLTAGE PROTECTION
V+
P
N
Q5
D6
D7
D4
D5
R11
1K
IN
Q6
V-
OUT
FROM DECODE

Die Characteristics

Transistor Count		485	
Die Size		161 x 85 mils	
Thermal Constants	θja	50°C/W	For Ceramic DIP
	θjc	18°C/W	
Tie Substrate to:		−VSupply	
Process:		CMOS-DI	

HARRIS

HI-506LA/HI-507LA

ADVANCED

Single 16/Differential 8 Channel CMOS Analog Multiplexers with Latches and Overvoltage Protection

Features

- **Analog Overvoltage protection**
- **Resettable Latches ($\overline{RS}$)**
- **TTL/DTL and CMOS Compatible**
- **Failsafe for conditions of Overvoltage & Loss of Power**
- **No SCR Latch-up**
- **Break-before-make switching**
- **Microprocessor Bus compatible**
- **Very low leakage-I_D(off)$\leq$4nA (typ)**
- **Acess time-t_A = 500nS (typ)**
- **Minimum write pulse width ($\overline{WR}$) = 300nS**
- **OFF isolation = -100dB, typ @ 10Kz**

Description

These monolithic CMOS multiplexers feature on-board address latches, plus overvoltage protection for the analog inputs and the output as well. Each model includes digital inputs for channel selection and an Enable input for device selection under program control. In addition, Write ($\overline{WR}$) and Reset ($\overline{RS}$) inputs allow the program to store or clear the channel address.

The overvoltage performance of these multiplexers is particularly useful in redundant systems, where the inputs and output must present a high inpedance when power is off. This is achieved by a switch cell with three MOSFET's in series rather than the conventional transmission gate design.

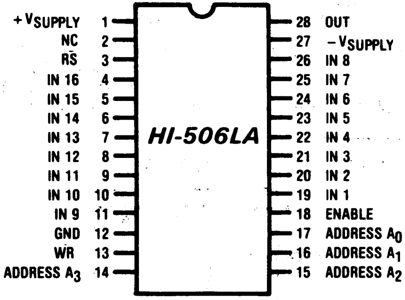
Each channel can withstand overvoltage to ±25VDC with respect to ground with power ON or OFF. An OFF channel remains OFF in the presence of overvoltage. If the channel is ON, output voltage is clamped below the supply rail, which protects the load circuit.

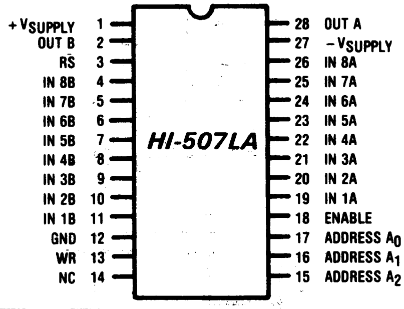
The HI-506LA offers 16 single-ended channels, and the HI-507LA is an 8 channel differential version. The recommended supply voltages are ±15V, though operation at reduced levels or with a single supply may also be inplemented. The package is a 28 pin ceramic or plastic DIP.

Each product is specified for the commercial temperature range (0°C to +75°C,-5 suffix) and the military range (-55°C to +125°C,-2 suffix). For MIL-STD-883 conpliant parts, request the 506LA/883 or 507LA/883 data sheet.

Pinout

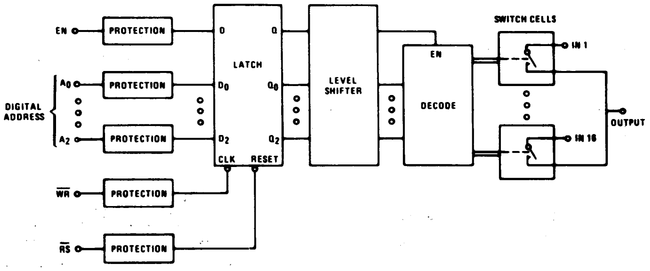
TOP VIEWS


+VSUPPLY 1
NC 2
RS 3
IN 16 4
IN 15 5
IN 14 6
IN 13 7
IN 12 8
IN 11 9
IN 10 10
IN 9 11
GND 12
WR 13
ADDRESS A3 14
HI-506LA
28 OUT
27 -VSUPPLY
26 IN 8
25 IN 7
24 IN 6
23 IN 5
22 IN 4
21 IN 3
20 IN 2
19 IN 1
18 ENABLE
17 ADDRESS A0
16 ADDRESS A1
15 ADDRESS A2

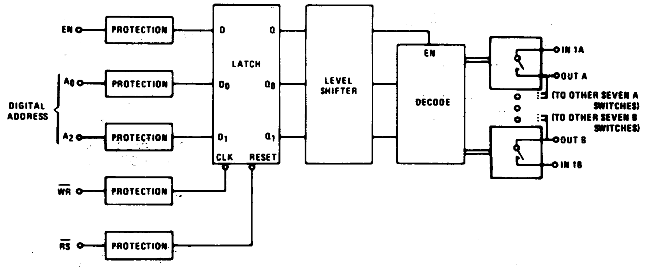

+VSUPPLY 1
OUT B 2
RS 3
IN 8B 4
IN 7B 5
IN 6B 6
IN 5B 7
IN 4B 8
IN 3B 9
IN 2B 10
IN 1B 11
GND 12
WR 13
NC 14
HI-507LA
28 OUT A
27 -VSUPPLY
26 IN 8A
25 IN 7A
24 IN 6A
23 IN 5A
22 IN 4A
21 IN 3A
20 IN 2A
19 IN 1A
18 ENABLE
17 ADDRESS A0
16 ADDRESS A1
15 ADDRESS A2

Functional Diagram

HI-506LA


EN
PROTECTION
A0
PROTECTION
DIGITAL ADDRESS
A2
PROTECTION
WR
PROTECTION
RS
PROTECTION
D
Q
LATCH
D0
Q0
D2
Q2
CLK
RESET
LEVEL SHIFTER
EN
DECODE
SWITCH CELLS
IN 1
IN 16
OUTPUT

HI-507LA


EN
PROTECTION
A0
PROTECTION
DIGITAL ADDRESS
A2
PROTECTION
WR
PROTECTION
RS
PROTECTION
D
Q
LATCH
D0
Q0
D1
Q1
CLK
RESET
LEVEL SHIFTER
EN
DECODE
IN 1A
OUT A
(TO OTHER SEVEN A SWITCHES)
(TO OTHER SEVEN B SWITCHES)
OUT B
IN 1B

DEVICE	FUNCTION	FEATURE	TTL "HIGH" MIN (V)	R_{ON}Ω (TYP)	$I_{D(OFF)}$ (nA) (TYP)	t(ON) (ns) (TYP)	t(OFF) (ns) (TYP)	PD(mW) (TYP)
HI-506LA	16-Channel	Address Latches and Overvoltage Protection	2.0	1K	4.0	500	500	60
HI-507LA	8-Channel Differential	Address Latches and Overvoltage Protection	2.0	1K	2.0	500	500	60

CAUTION: These devices are sensitive to electrostatic discharge. Proper I. C. handling procedures should be followed.

HARRIS

HI-508/509

Single 8/Differential 4 Channel CMOS Analog Multiplexer

Features

- R_{ON} 180Ω
- **Wide Analog Signal Range** .... ±15 V
- **TTL/CMOS Compatible** .... 2.4 V (Logic "1")
- **Fast Access** .... 250 ns
- **Fast Settling (0.01%)** .... 600 ns
- **44V Maximum Power Supply**
- **Break-Before-Make Switching**
- **No Latch-Up**
- **Replaces DG508A/DG508AA and DG509A/DG509AA**

Applications

- **Data Acquisition Systems**
- **Precision Instrumentation**
- **Demultiplexing**
- **Selector Switch**

Description

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (see Application Note 521). Combined with the low ON resistance (180Ω typical), these benefits allow low static error, fast channel switching rates, and fast settling.

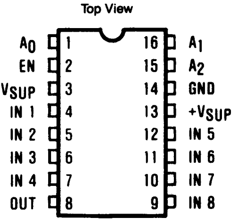
Switches are guaranteed to break-before-make, so that two channels are never shorted together.

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4 V for "1" and Maximum 0.8 V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

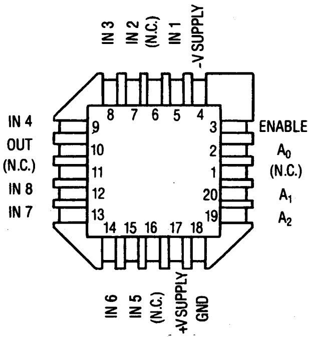
The HI-508 is an eight channel single-ended multiplexer, and the HI-509 is a four channel differential version. The recommended supply voltage is ±15 V; however, reasonable performance is available down to ±7 V. Each device is available in a 16 pin plastic or ceramic DIP, a 20 pin ceramic LCC or 20 pin plastic LCC (PLCC) package. If input overvoltage protection is needed, the HI-508A/509A multiplexers are recommended. For further information, see Application Notes 520 and 521.

The HI-508/509 is offered in both commercial and military grades, suitable for spacecraft/military applications. For additional HI-Rel screening including 160 hour burn-in, specify the "-8" suffix. For further information see Application Notes 520 and 521. For MIL-STD-883 compliant parts, request the 508/883 or 509/883 data sheet.

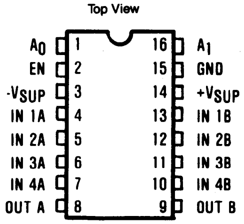
Pinouts


Top View
A0 1
EN 2
-VSUP 3
IN 1 4
IN 2 5
IN 3 6
IN 4 7
OUT 8
16 A1
15 A2
14 GND
13 +VSUP
12 IN 5
11 IN 6
10 IN 7
9 IN 8

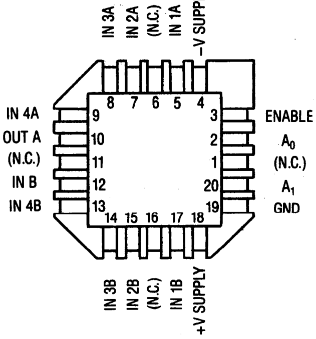
HI1-508 (ceramic)
HI3-508 (plastic)


IN 3
IN 2
(N.C.)
IN 1
-V SUPPLY
IN 4
OUT
(N.C.)
IN 8
IN 7
ENABLE
A0
(N.C.)
A1
A2
IN 6
IN 5
(N.C.)
+VSUPPLY
GND
8 7 6 5 4
9 10 11 12 13
3 2 1 20 19
14 15 16 17 18

HI4-508 (LCC)
HI4P508 (PLCC)

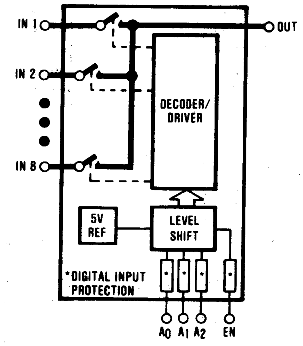

Top View
A0 1
EN 2
-VSUP 3
IN 1A 4
IN 2A 5
IN 3A 6
IN 4A 7
OUT A 8
16 A1
15 GND
14 +VSUP
13 IN 1B
12 IN 2B
11 IN 3B
10 IN 4B
9 OUT B

HI1-509 (ceramic)
HI3-509 (plastic)

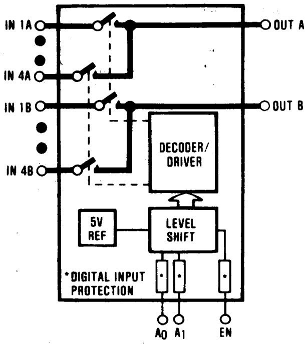

IN 3A
IN 2A
(N.C.)
IN 1A
-V SUPPLY
IN 4A
OUT A
(N.C.)
IN B
IN 4B
ENABLE
A0
(N.C.)
A1
GND
IN 3B
IN 2B
(N.C.)
IN 1B
+V SUPPLY
8 7 6 5 4
9 10 11 12 13
3 2 1 20 19
14 15 16 17 18

HI4-509 (LCC)
HI4P509 (PLCC)

Functional Diagrams


IN 1
IN 2
IN 8
OUT
DECODER/ DRIVER
5V REF
LEVEL SHIFT
*DIGITAL INPUT PROTECTION
A0 A1 A2 EN

HI-508


IN 1A
IN 4A
IN 1B
IN 4B
OUT A
OUT B
DECODER/ DRIVER
5V REF
LEVEL SHIFT
*DIGITAL INPUT PROTECTION
A0 A1 EN

HI-509

ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{Supply}(+)$ to $V_{Supply}(-)$	44 V
$V_{Supply}(+)$ to GND	22 V
$V_{Supply}(-)$ to GND	25 V
Digital Input Overvoltage:	
$V_{EN}, V_A \begin{cases} V_{Supply}(+) & +4\text{ V} \\ V_{Supply}(-) & -4\text{ V} \end{cases}$	
or 20 mA, whichever occurs first.	
Analog Signal Overvoltage (Note 7)	
$V_D, V_S \begin{cases} V_{Supply}(+) & +2\text{ V} \\ V_{Supply}(-) & -2\text{ V} \end{cases}$	
Continuous Current, S or D:	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max):	40 mA
Power Dissipation* (Cerdip)	1.09 W
Operating Temperature Range:	
HI-508/509-2,-8	−55°C to +125°C
HI-508/509-4	−25°C to +85°C
HI-508/509-5	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

*Derate 10.9 mW/°C above T_A =75°C

ELECTRICAL CHARACTERISTICS Unless Otherwise Specified:

Supplies= +15 V, −15 V; V_{AH}(Logic Level High) = +2.4 V, V_{AL} (Logic Level Low) = +0.8 V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-508/HI-509 -2, -8 MIN.	TYP.	MAX.	HI-508/509 -4, -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	−15		+15	−15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		180	300		180	400	Ω
	Full			400			500	Ω
ΔR_{ON}, Any Two Channels	+25°C		5			5		%
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-508	Full			200			200	nA
HI-509	Full			100			100	nA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-508	Full			200			200	nA
HI-509	Full			100			100	nA
*I_{DIFF}, Differential Off Output Leakage Current (HI-509 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold	Full			0.8			0.8	V
*V_{AH},, Input High Threshold	Full	2.4			2.4			V
*I_A, Input Leakage Current (High or Low) (Note 4)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OPEN}, Break-Before-Make Interval	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Turn-On	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Turn-Off	+25°C		250	500		250		ns
	Full			1000			1000	ns
t_S, Settling Time to 0.1%	+25°C		360			360		ns
to 0.01%	+25°C		600			600		ns
"Off Isolation" (Note 5)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-508	+25°C		22			22		pF
HI-509	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		.08			.08		pF
POWER REQUIREMENTS								
*I+, Positive Supply Current (Note 6)	Full		1.5	2		1.5	2	mA
*I−, Negative Supply Current (Note 6))	Full		0.4	1		0.4	1	mA
P_D, Power Dissipation	Full			45			45	mW

*100% tested for Dash 8. Leakage currents not tested at −55°C.

TRUTH TABLES

HI-508

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

NOTES:

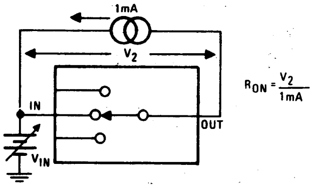
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = −1 mA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1 nA at 25°C.
5. V_{EN} = 0.8 V, R_L = 1 K, C_L = 15 pF, V_S = 7 V_{RMS}, f = 100 kHz. Worst case isolation occurs on channel 4 due to proximity of the output pins.
6. V_{EN}, V_A = 0 V or 2.4 V.
7. Signal voltage at any analog input or output (S or D) will be clamped to the supply rail by internal diodes. Limit the resulting current as shown under absolute maximum ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the HARRIS HI-508A/509A multiplexers are recommended.

Performance Characteristics and Test Circuits

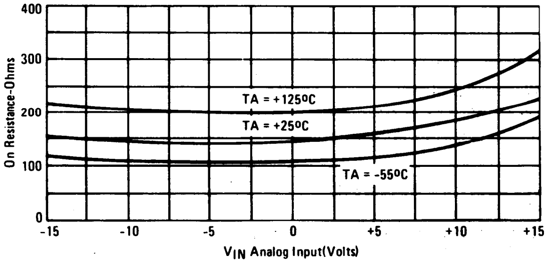
Unless Otherwise Specified; $T_A = 25°C$, $V_{Supply} = \pm 15$ V, $V_{AH} = 2.4$ V, $V_{AL} = 0.8$ V.

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

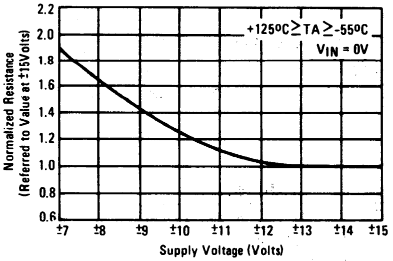
TEST CIRCUIT NO. 1


1mA
V2
IN
OUT
VIN
RON = V2 / 1mA

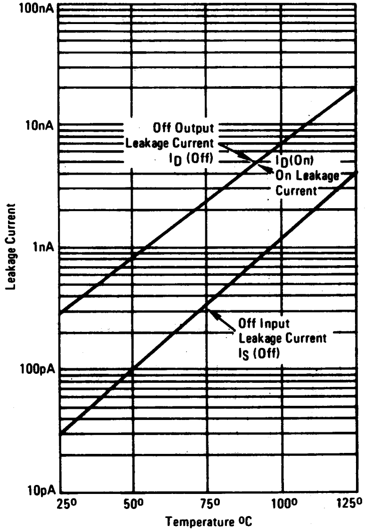
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



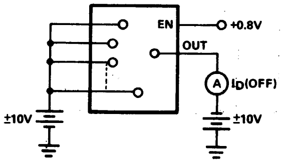
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



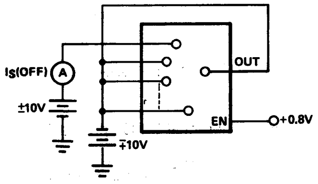
LEAKAGE CURRENT VS. TEMPERATURE



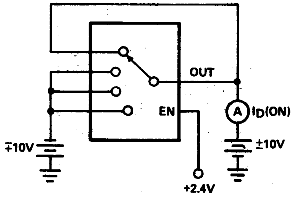
TEST CIRCUIT NO. 2*


EN
+0.8V
OUT
A
ID(OFF)
±10V
±10V

TEST CIRCUIT NO. 4*

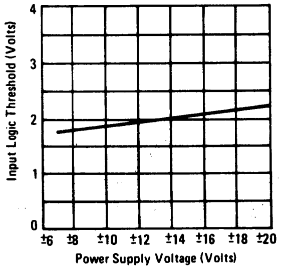

IS(OFF)
A
OUT
±10V
EN
+0.8V
∓10V

TEST CIRCUIT NO. 3*

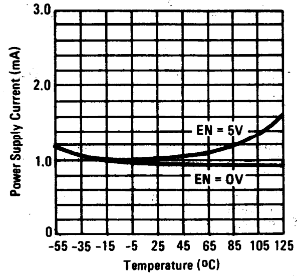

OUT
EN
A
ID(ON)
∓10V
±10V
+2.4V

***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for I_D(OFF): +10 V/−10 V and −10 V/+10 V.)**

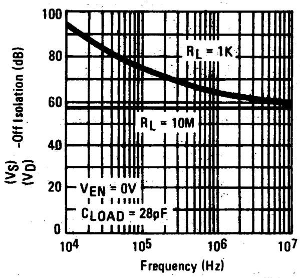
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE

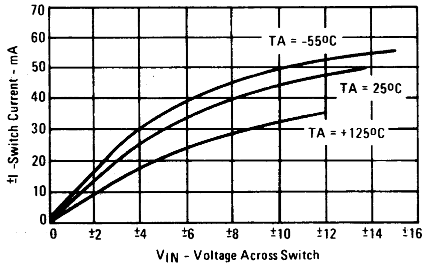


OFF ISOLATION vs. FREQUENCY



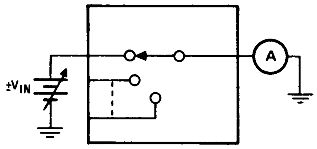
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE



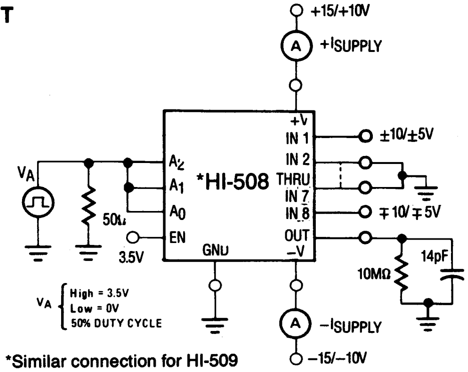
TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE



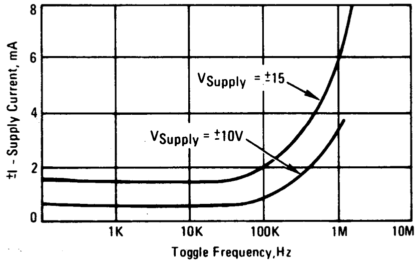
TEST CIRCUIT NO. 6

SUPPLY CURRENT vs. TOGGLE FREQUENCY


+15/+10V
A
+ISUPPLY
+V
IN 1
IN 2
THRU
IN 7
IN 8
OUT
-V
A2
A1
A0
EN
GND
*HI-508
±10/±5V
∓10/∓5V
14pF
10MΩ
VA
50Ω
3.5V
VA
High = 3.5V
Low = 0V
50% DUTY CYCLE
A
-ISUPPLY
-15/-10V

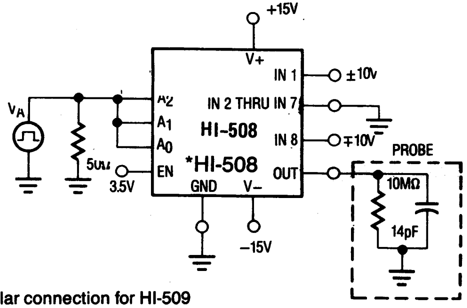
*Similar connection for HI-509

SUPPLY CURRENT vs. TOGGLE FREQUENCY



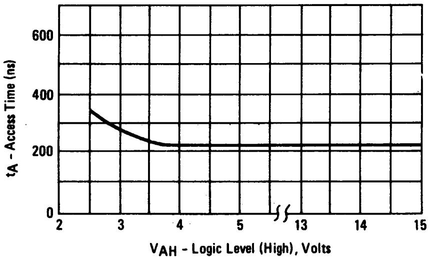
TEST CIRCUIT NO. 7

ACCESS TIME vs. LOGIC LEVEL (HIGH)

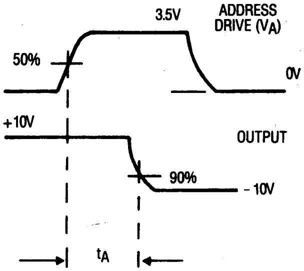

+15V
V+
IN 1
IN 2 THRU IN 7
IN 8
OUT
A2
A1
A0
EN
HI-508
*HI-508
GND
V-
±10V
∓10V
PROBE
10MΩ
14pF
VA
50Ω
3.5V
-15V

*Similar connection for HI-509

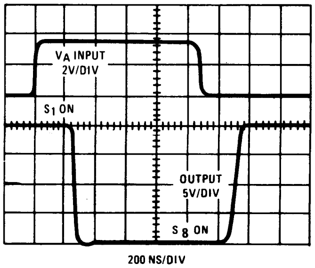
ACCESS TIME vs. LOGIC LEVEL (HIGH)



Switching Wav


3.5V
ADDRESS DRIVE (VA)
50%
0V
+10V
OUTPUT
90%
-10V
tA

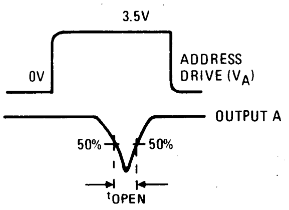
ACCESS TIME



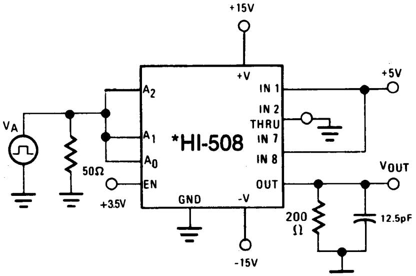
Switching Waveforms (continued)

TEST CIRCUIT NO. 8

ADDRESS DRIVE

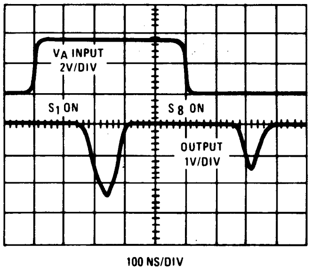

3.5V
0V
ADDRESS DRIVE (V_A)
OUTPUT A
50%
50%
t_{OPEN}

BREAK-BEFORE-MAKE DELAY (tOPEN)


+15V
+V
A_2
A_1
A_0
EN
*HI-508
IN 1
IN 2 THRU IN 7
IN 8
OUT
GND
-V
+5V
V_A
50Ω
+3.5V
V_{OUT}
200 Ω
12.5pF
-15V

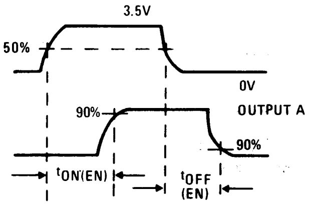
*Similar connection for HI-509

BREAK-BEFORE-MAKE DELAY(tOPEN)

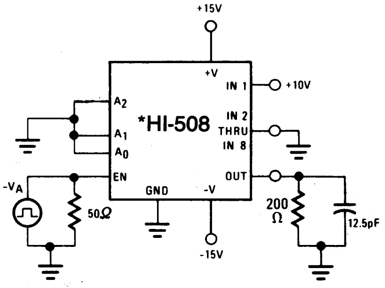


TEST CIRCUIT NO. 9

ENABLE DRIVE

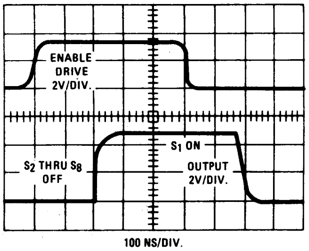

3.5V
50%
0V
90%
OUTPUT A
90%
$t_{ON(EN)}$
t_{OFF} (EN)

ENABLE DELAY (tON(EN),tOFF(EN))


+15V
+V
A_2
A_1
A_0
EN
*HI-508
IN 1
+10V
IN 2 THRU IN 8
OUT
GND
-V
$-V_A$
50Ω
200 Ω
12.5pF
-15V

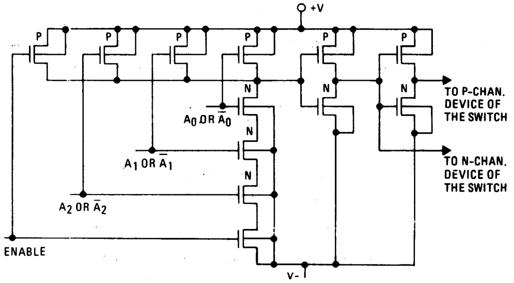
*Similar connection for HI-509

ENABLE DELAY (tON(EN),tOFF(EN))



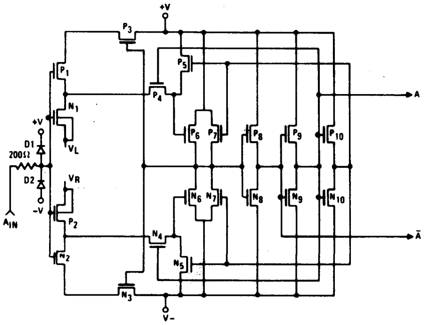
Schematic Diagrams

ADDRESS DECODER


+V
P
P
P
P
P
P
N
N
N
N
N
N
A_0 OR $\bar{A}_0$
A_1 OR $\bar{A}_1$
A_2 OR $\bar{A}_2$
ENABLE
V-
TO P-CHAN. DEVICE OF THE SWITCH
TO N-CHAN. DEVICE OF THE SWITCH

Delete A_2 or $\overline{A_2}$ Input for HI-509

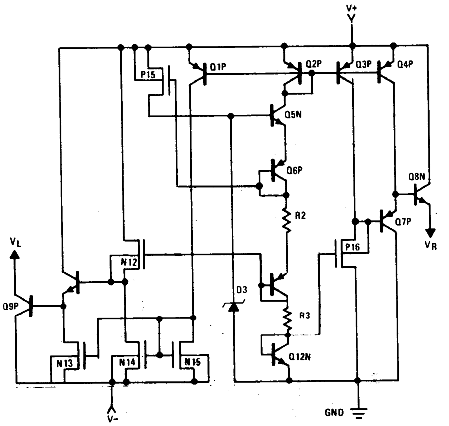
ADDRESS INPUT BUFFER LEVER SHIFTER


+V
P_3
P_1
P_5
P_4
N_1
P_6
P_7
P_8
P_9
P_{10}
+V
D1
200Ω
V_L
D2
V_R
N_6
N_7
N_8
N_9
N_{10}
-V
P_2
A_{IN}
N_4
N_2
N_5
N_3
V-
A
$\bar{A}$

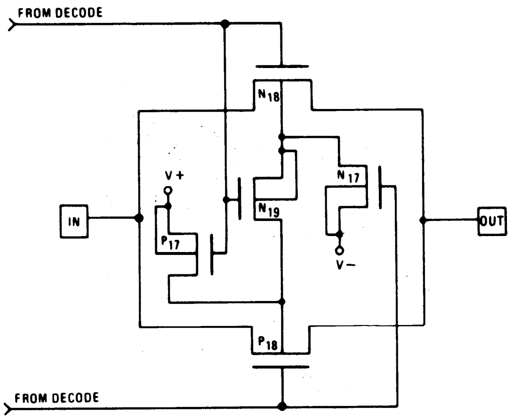
All N-Channel Bodies to V−
All P-Channel Bodies to V+ Unless Otherwise Indicated

Schematic Diagrams (continued)

TTL REFERENCE CIRCUIT

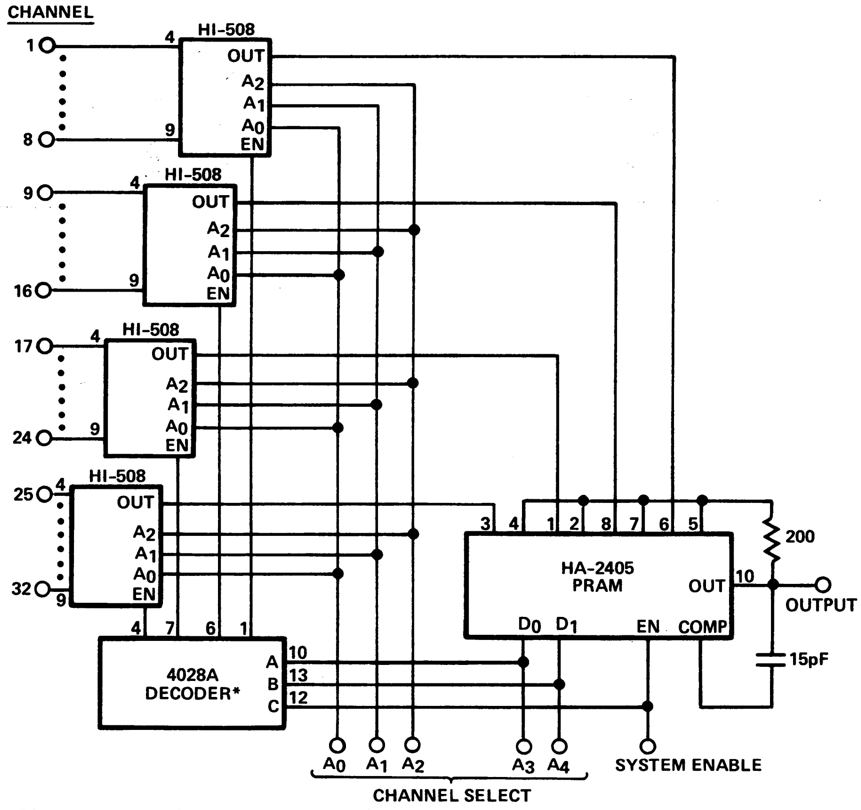

V+
P15
Q1P
Q2P
Q3P
Q4P
Q5N
Q6P
Q8N
R2
Q7P
V_R
V_L
N12
P16
Q9P
D3
R3
Q12N
N13
N14
N15
V-
GND

MULTIPLEX SWITCH


FROM DECODE
N_{18}
V+
N_{17}
IN
N_{19}
OUT
P_{17}
V−
P_{18}
FROM DECODE

Applications

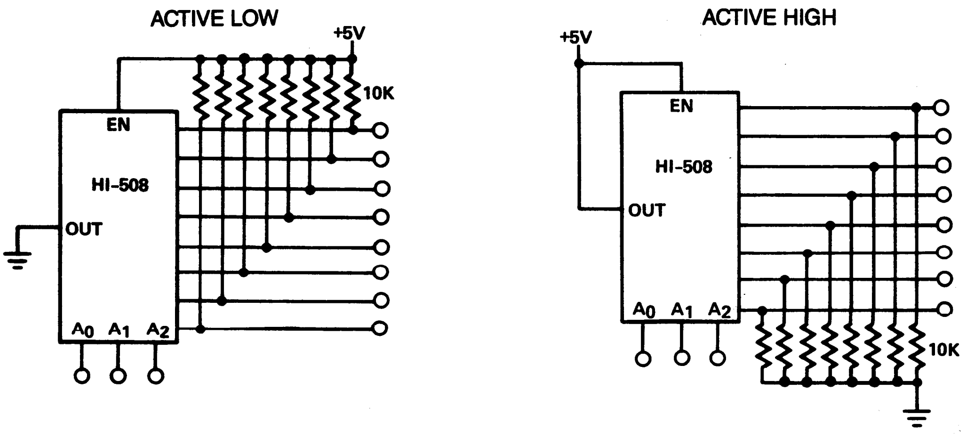
32 CHANNEL BUFFERED MULTIPLEXER


CHANNEL
1
8
4
9
HI-508
OUT
A_2
A_1
A_0
EN
9
16
17
24
25
32
4028A
DECODER*
A
B
C
10
13
12
4
7
6
1
3
4
1
2
8
7
6
5
HA-2405
PRAM
OUT
10
D_0
D_1
EN
COMP
200
OUTPUT
15pF
A_0
A_1
A_2
A_3
A_4
CHANNEL SELECT
SYSTEM ENABLE

*Optional; Provides Greater Isolation for AC Signals.

Applications (continued)

ONE OF 8 DECODER


ACTIVE LOW
+5V
10K
EN
HI-508
OUT
A0 A1 A2
ACTIVE HIGH
+5V
EN
HI-508
OUT
A0 A1 A2
10K

Die Characteristics

Transistor Count		243	
Die Size		86 x 79 mils	
Thermal Constants	θ_{ja}	92°C/W	For Ceramic Dip
	θ_{jc}	37°C/W	
Tie Substrate to:		$-V_{Supply}$	
Process:		CMOS - DI	

HARRIS

HI-508A/509A

Single 8/Differential 4 Channel
CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- **Analog Overvoltage Protection. . . . . 70 Vpp**
- **No Channel Interaction During Overvoltage**
- **ESD Resistant. . . . . >4,000 Volts**
- **44 V Maximum Power Supply**
- **Fail Safe with Power Loss (No Latchup)**
- **Break-Before-Make Switching**
- **Analog Signal range. . . . . ±15 V**
- **Access Time (Typical). . . . . 500 ns**
- **Standby Power (Typical). . . . . 7.5 mW**

Applications

- **Data Acquisition**
- **Industrial Controls**
- **Telemetry**

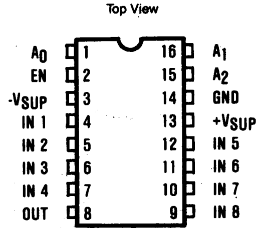
Description

The HI-508A and 509A are analog multiplexers with Active Overvoltage Protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-508A and HI-509A ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The 508A is an 8 channel device and the 509A is a 4 channel differential version. If input overvoltage protection is not needed, the HI-508 and HI-509 multiplexers are recommended. For further information see Application Notes 520 and 521.

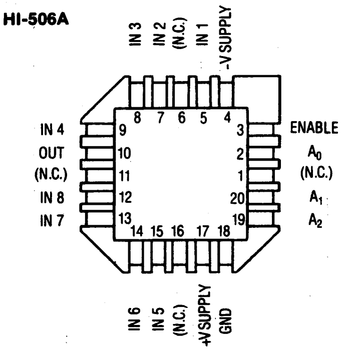
Each device is available in a 16 pin plastic or ceramic DIP, a 20 pin ceramic LCC package.

The HI-508A/509A are offered in both commercial and military grades. Addition Hi-Rel screening including 160 hour burn-in is specified by the "−8" suffix.

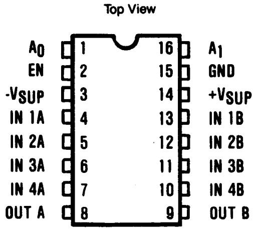
Pinouts


Top View
A0 1
EN 2
-VSUP 3
IN 1 4
IN 2 5
IN 3 6
IN 4 7
OUT 8
16 A1
15 A2
14 GND
13 +VSUP
12 IN 5
11 IN 6
10 IN 7
9 IN 8

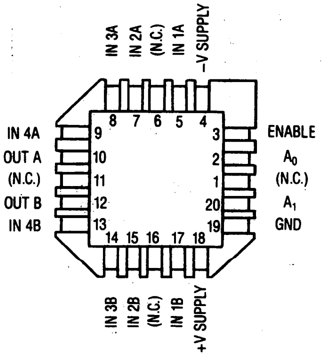
HI1-508A (ceramic)
HI3-508A (plastic)


HI-506A
IN 3
IN 2
(N.C.)
IN 1
-V SUPPLY
8 7 6 5 4
IN 4 9
OUT 10
(N.C.) 11
IN 8 12
IN 7 13
3 ENABLE
2 A0
1 (N.C.)
20 A1
19 A2
14 15 16 17 18
IN 6
IN 5
(N.C.)
+VSUPPLY
GND

HI4-508A (LCC)

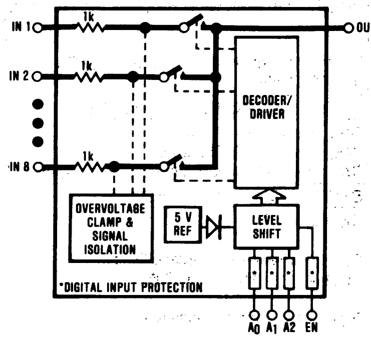

Top View
A0 1
EN 2
-VSUP 3
IN 1A 4
IN 2A 5
IN 3A 6
IN 4A 7
OUT A 8
16 A1
15 GND
14 +VSUP
13 IN 1B
12 IN 2B
11 IN 3B
10 IN 4B
9 OUT B

HI1-509A (ceramic)
HI3-509A (plastic)

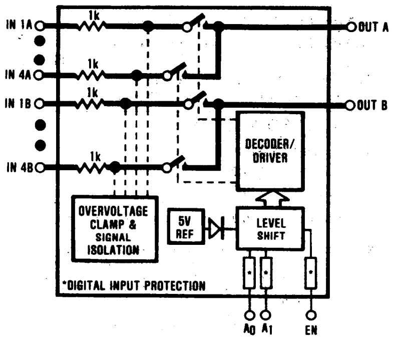

IN 3A
IN 2A
(N.C.)
IN 1A
-V SUPPLY
8 7 6 5 4
IN 4A 9
OUT A 10
(N.C.) 11
OUT B 12
IN 4B 13
3 ENABLE
2 A0
1 (N.C.)
20 A1
19 GND
14 15 16 17 18
IN 3B
IN 2B
(N.C.)
IN 1B
+V SUPPLY

HI4-509A (LCC)

Functional Diagrams


IN 1
IN 2
IN 8
1k
1k
1k
OUT
DECODER/ DRIVER
OVERVOLTAGE CLAMP & SIGNAL ISOLATION
5 V REF
LEVEL SHIFT
*DIGITAL INPUT PROTECTION
A0 A1 A2 EN

HI-508A


IN 1A
IN 4A
IN 1B
IN 4B
1k
1k
1k
1k
OUT A
OUT B
DECODER/ DRIVER
OVERVOLTAGE CLAMP & SIGNAL ISOLATION
5V REF
LEVEL SHIFT
*DIGITAL INPUT PROTECTION
A0 A1 EN

HI-509A

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between Supply Pins	44 V
V+ to Ground	22 V
V− to Ground	25 V
Digital Input Overvoltage:	
V_{EN}, V_A $V_{Supply(+)}$	+4 V
$V_{Supply(-)}$	−4 V
or 20 mA, whichever occurs first.	
Analog Input Overvoltage:	
V_S $V_{Supply(+)}$	+20 V
$V_{Supply(-)}$	−20 V

Continuous Current, S or D:	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max):	40 mA
Power Dissipation* (CERDIP)	1.28 W
Operating Temperature Range:	
HI-508A/509A-2,-8	−55°C to +125°C
HI-508A/509A-5	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

*Derate 12.8 mW/°C above T_A=75°C

ELECTRICAL CHARACTERISTICS

Supplies= +15 V, −15 V; V_{AH} (Logic Level High) = +4.0 V, V_{AL}(Logic Level Low) = +0.8 V. (unless otherwise specified). For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-508A/HI-509A -2, -8 MIN.	TYP.	MAX.	HI-508A/509A -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	−15		+15	−15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-508A	Full			200			200	nA
HI-509A	Full			100			100	nA
*$I_{D(OFF)}$ with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				µA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-508A	Full			200			200	nA
HI-509A	Full			100			100	nA
I_{DIFF} Differential Off Output Leakage Current (HI-509A Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold (Note 8)	Full			0.8			0.8	V
*V_{AH}, Input High Threshold	Full	4.0			4.0			V
*I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	µA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		0.5			0.5		µs
	Full			1.0			1.0	µs
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		µs
(0.01%)	+25°C		3.5			3.5		µs
"OFF Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current (Note 7)	Full		0.5	2.0		0.5	2.0	mA
*I−, Current (Note 7)	Full		0.02	1.0		0.02	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at −55°C.

TRUTH TABLES

HI-508A

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

A_1	A_0	EN	ON CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

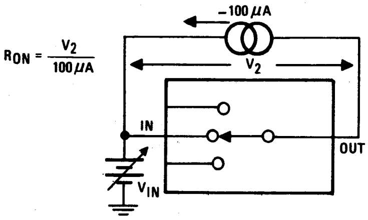
NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = −100µA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33 V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1 nA at 25°C.
6. V_{EN} = 0.8 V. R_L = 1 K, C_L = 15 pF, V_S = 7 V_{RMS}, f = 100 kHz. Worst Case isolation occurs on channel 4 due to proximity of the output pins.
7. V_{EN}, V_A = 0 V or 4.0 V.
8. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5.0 V supply are recommended.

Performance Characteristics and Test Circuits

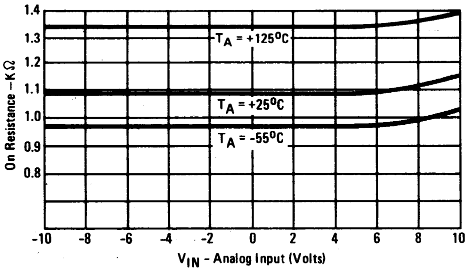
Unless Otherwise Specified T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V

TEST CIRCUIT NO. 1

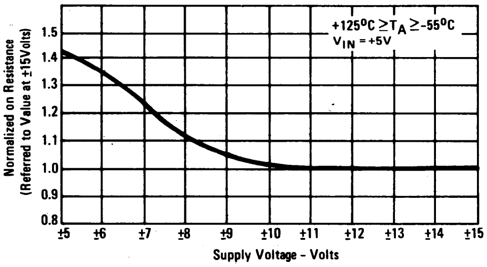
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE


$R_{ON} = \frac{V_2}{100 \mu A}$
−100 μA
V_2
IN
OUT
V_{IN}

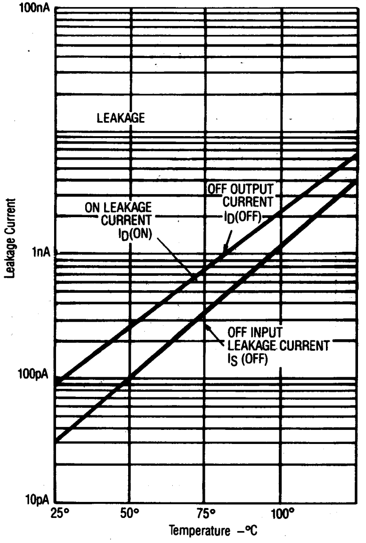
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



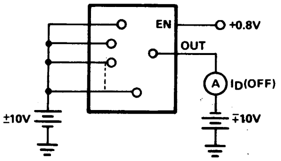
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



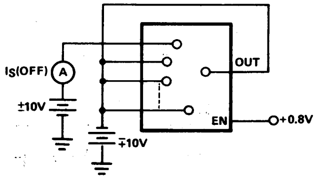
LEAKAGE CURRENT VS. TEMPERATURE



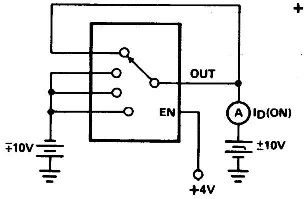
TEST CIRCUIT NO. 2*


EN
+0.8V
OUT
A
$I_D(OFF)$
±10V
∓10V

TEST CIRCUIT NO. 3*

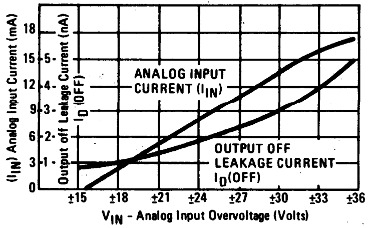

$I_S(OFF)$
A
±10V
OUT
EN
+0.8V
∓10V

TEST CIRCUIT NO. 4*


OUT
EN
A
$I_D(ON)$
∓10V
±10V
+4V

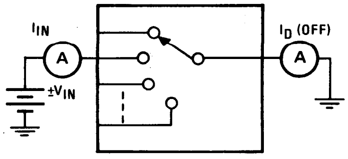
***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_D(OFF)$: +10 V/−10 V and −10 V/+10 V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



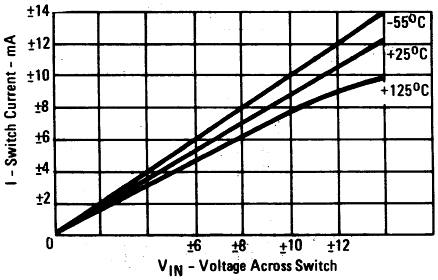
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS


I_{IN}
A
±V_{IN}
I_D (OFF)
A

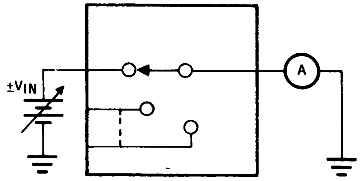
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

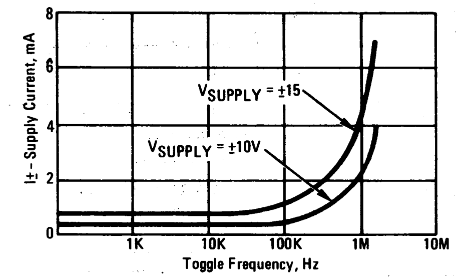


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

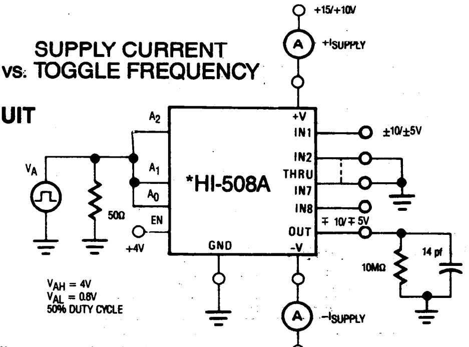


SUPPLY CURRENT vs. TOGGLE FREQUENCY



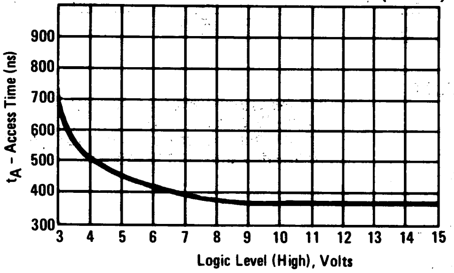
SUPPLY CURRENT vs. TOGGLE FREQUENCY

TEST CIRCUIT NO. 7


+15/+10V
A
$+I_{SUPPLY}$
+V
IN1
±10/±5V
IN2
THRU
IN7
IN8
∓ 10/∓ 5V
OUT
-V
A_2
A_1
A_0
EN
*HI-508A
GND
V_A
50Ω
+4V
14 pf
10MΩ
V_{AH} = 4V
V_{AL} = 0.8V
50% DUTY CYCLE
A
$-I_{SUPPLY}$
-15/-10V

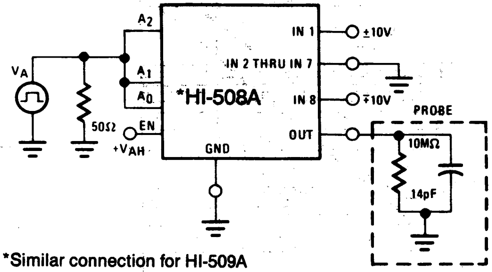
*Similar connection for HI-509A

ACCESS TIME VS. LOGIC LEVEL (HIGH)



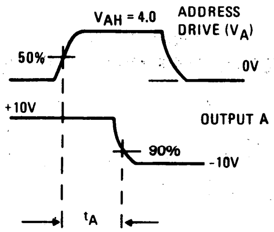
TEST CIRCUIT NO. 8

ACCESS TIME vs. LOGIC LEVEL (HIGH)

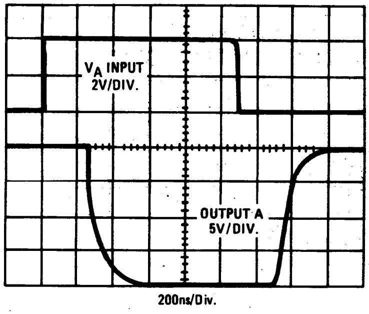

A_2
A_1
A_0
EN
*HI-508A
GND
IN 1
±10V
IN 2 THRU IN 7
IN 8
∓10V
OUT
PROBE
10MΩ
14pF
V_A
50Ω
$+V_{AH}$

*Similar connection for HI-509A

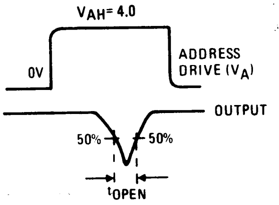
Switching Waveforms


V_{AH} = 4.0
ADDRESS DRIVE (V_A)
50%
0V
+10V
OUTPUT A
90%
-10V
t_A

ACCESS TIME

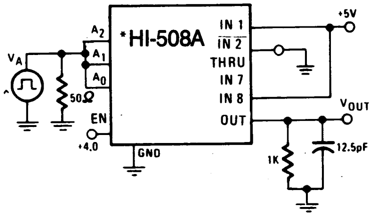


Switching Waveforms (continued)


V_{AH}= 4.0
0V
ADDRESS DRIVE (V_A)
OUTPUT
50%
50%
t_{OPEN}

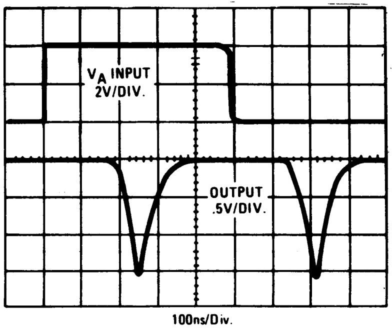
TEST CIRCUIT NO. 9

BREAK-BEFORE-MAKE DELAY(t_{OPEN})


*HI-508A
A_2
A_1
A_0
EN
+4.0
GND
IN 1
$\overline{IN\ 2}$
THRU
IN 7
IN 8
OUT
+5V
V_{OUT}
V_A
50Ω
1K
12.5pF

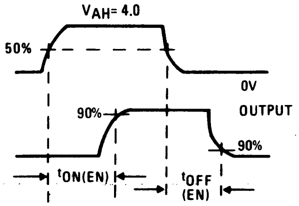
*Similar connection for HI-509A

BREAK-BEFORE-MAKE DELAY (t_{OPEN})

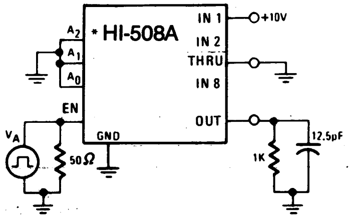


TEST CIRCUIT NO. 10

ENABLE DRIVE

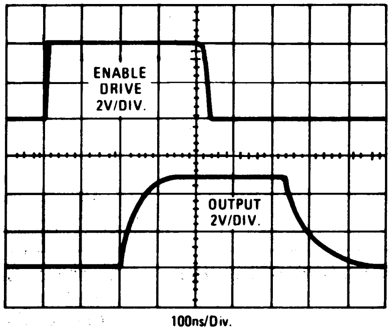

V_{AH}= 4.0
50%
0V
90%
OUTPUT
90%
$t_{ON(EN)}$
t_{OFF} (EN)

ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)

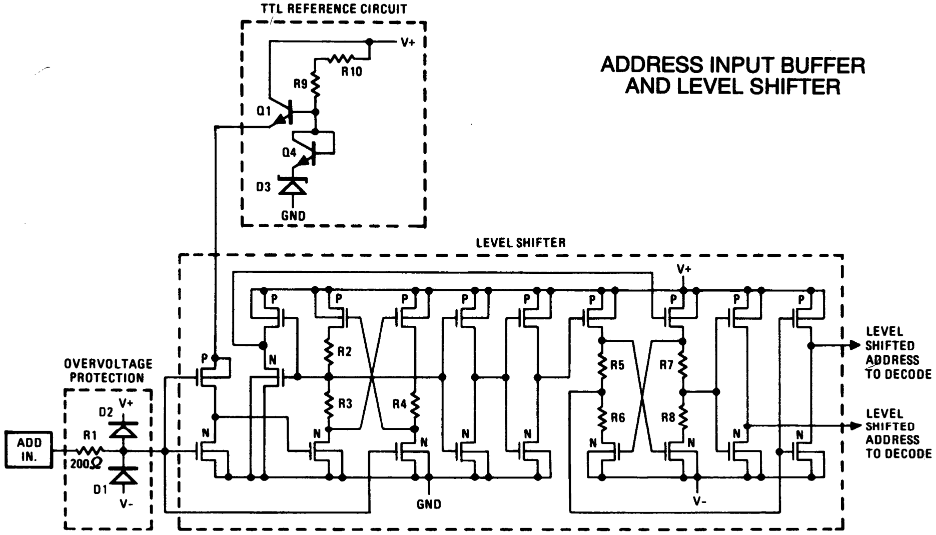

* HI-508A
A_2
A_1
A_0
EN
GND
IN 1
IN 2
THRU
IN 8
OUT
+10V
V_A
50Ω
1K
12.5pF

*Similar connection for HI-509A

ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)



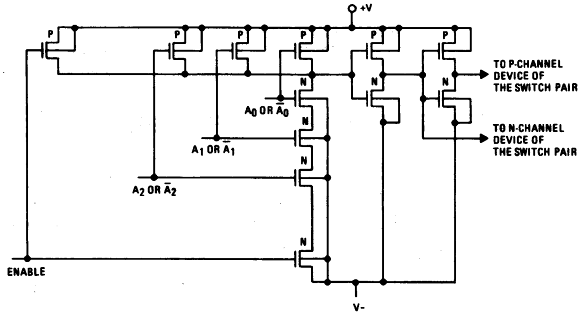
Schematic Diagrams


TTL REFERENCE CIRCUIT
V+
R10
R9
Q1
Q4
D3
GND
LEVEL SHIFTER
V+
P
N
R2
R3
R4
R5
R6
R7
R8
GND
V-
OVERVOLTAGE PROTECTION
D2
V+
R1
200Ω
D1
V-
ADD IN.
LEVEL SHIFTED ADDRESS TO DECODE
LEVEL SHIFTED ADDRESS TO DECODE

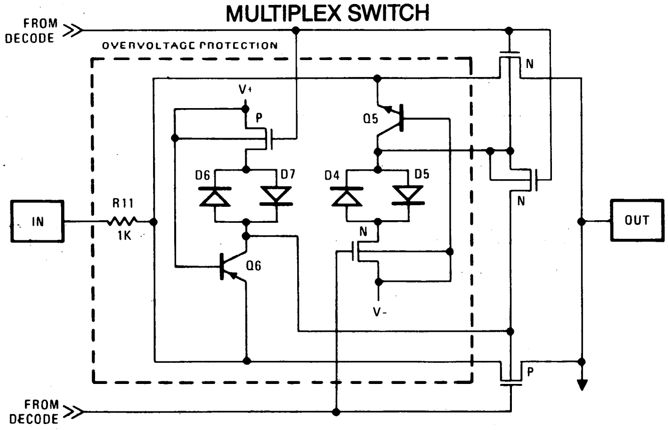
ADDRESS INPUT BUFFER AND LEVEL SHIFTER

Schematic Diagrams (continued)

ADDRESS DECODER


+V
P
N
A0 OR Ā0
A1 OR Ā1
A2 OR Ā2
ENABLE
TO P-CHANNEL DEVICE OF THE SWITCH PAIR
TO N-CHANNEL DEVICE OF THE SWITCH PAIR
V-

MULTIPLEX SWITCH


FROM DECODE
OVERVOLTAGE PROTECTION
V+
P
Q5
D6
D7
D4
D5
IN
R11
1K
Q6
N
V-
OUT
FROM DECODE

Die Characteristics

Transistor Count		253	
Die Size		116 x 79 mil	
Thermal Constants	θ_{ja}	78°C/W	For Ceramic Dip
	θ_{jc}	25°C/W	
Tie Substrate to:		$-V_{Supply}$	
Process:		CMOS - DI	

HARRIS

HI-508LA/HI-509LA

Single 8 Differential 4 Channel CMOS Analog Multiplexers With Latches and Overvoltage Protection

Features

- Analog Overvoltage protection
- Resettable Latches ($\overline{RS}$)
- TTL/DTL and CMOS Compatible
- Failsafe for conditions of Overvoltage & Loss of Power
- No SCR Latch-up
- Break-before-make switching
- Microprocessor Bus compatible
- Very low leakage - $I_{D(off)} \leq$ 2nA (typ)
- Access time - t_A = 500nS (typ)
- Minimum write pulse width ($\overline{WR}$) = 300 nS
- OFF isolation = −100dB, typ @ 10kHz

Description

These monolithic CMOS multiplexers feature on-board address latches, plus overvoltage protection for the analog inputs and the output as well. Each model includes digital inputs for channel selection and an Enable input for device selection under program control. In addition, Write ($\overline{WR}$) and Reset ($\overline{RS}$) inputs allow the program to store or clear the channel address.

The overvoltage performance of these multiplexers is particularly useful in redundant systems, where the inputs and output must present a high inpedance when power is off. This is achieved by a switch cell with three MOSFET's in series rather than the conventional transmission gate design.

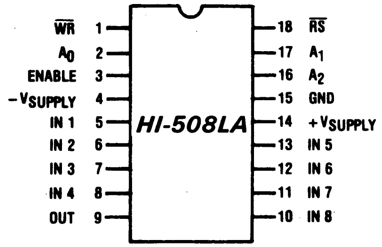
Each channel can withstand overvoltage to ±25VDC with respect to ground with power ON or OFF. An OFF channel remains OFF in the presence of overvoltage. If the channel is ON, output voltage is clamped below the supply rail, which protects the load circuit.

The HI-508LA offers 8 single-ended channels, and the HI-509LA is an 4 channel differential version. The recommended supply voltages are ±15V, though operation at reduced levels or with a single supply may also be inplemented. The package is an 18 pin ceramic or plastic DIP.

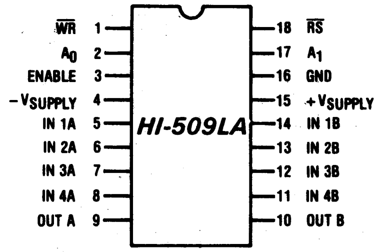
Each product is specified for the commercial temperature range (0°C to +75°C,-5 suffix) and the military range (-55°C to +125°C,-2 suffix). For MIL-STD-883 compliant parts, request the 508LA/883 or 509LA/883 data sheet.

Pinout

TOP VIEWS



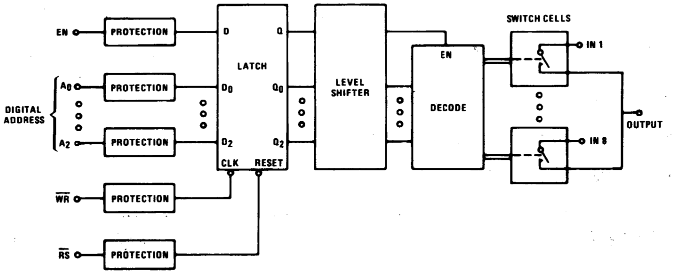
$\overline{WR}$ 1
A_0 2
ENABLE 3
$-V_{SUPPLY}$ 4
IN 1 5
IN 2 6
IN 3 7
IN 4 8
OUT 9
HI-508LA
18 $\overline{RS}$
17 A_1
16 A_2
15 GND
14 $+V_{SUPPLY}$
13 IN 5
12 IN 6
11 IN 7
10 IN 8



$\overline{WR}$ 1
A_0 2
ENABLE 3
$-V_{SUPPLY}$ 4
IN 1A 5
IN 2A 6
IN 3A 7
IN 4A 8
OUT A 9
HI-509LA
18 $\overline{RS}$
17 A_1
16 GND
15 $+V_{SUPPLY}$
14 IN 1B
13 IN 2B
12 IN 3B
11 IN 4B
10 OUT B

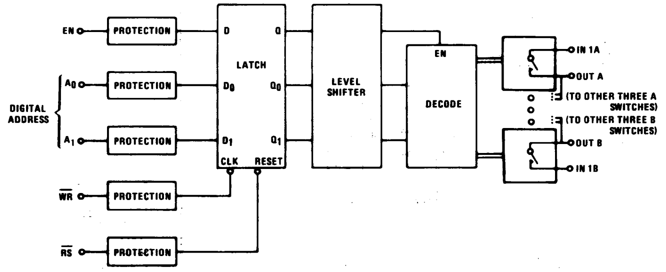
Functional Diagram

HI-508LA



EN
PROTECTION
D
Q
LATCH
DIGITAL ADDRESS
A_0
D_0
Q_0
A_2
D_2
Q_2
CLK
RESET
LEVEL SHIFTER
EN
DECODE
SWITCH CELLS
IN 1
IN 8
OUTPUT
$\overline{WR}$
$\overline{RS}$

HI-509LA



EN
PROTECTION
D
Q
LATCH
DIGITAL ADDRESS
A_0
D_0
Q_0
A_1
D_1
Q_1
CLK
RESET
LEVEL SHIFTER
EN
DECODE
IN 1A
OUT A
(TO OTHER THREE A SWITCHES)
(TO OTHER THREE B SWITCHES)
OUT B
IN 1B
$\overline{WR}$
$\overline{RS}$

DEVICE	FUNCTION	FEATURE	TTL "HIGH" MIN (V)	$R_{ON}\Omega$ (TYP)	$I_{D(OFF)}$ (nA) (TYP)	t(ON) (ns) (TYP)	t(OFF) (ns) (TYP)	P_D(mW) (TYP)
HI-508LA	8-Channel	Address Latches and Overvoltage Protection	2.0	1K	2.0	500	500	40
HI-509LA	4-Channel Differential	Address Latches and Overvoltage Protection	2.0	1K	1.0	500	500	40

CAUTION: These devices are sensitive to electrostatic discharge. Proper I. C. handling procedures should be followed.

HI-516

16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer

PRELIMINARY

FEATURES

ACCESS TIME (TYP)	100ns
SETTLING TIME (0.1%)	250ns
LOW LEAKAGE (TYP) I_S(OFF) I_D(OFF)	10pA 30pA
LOW CAPACITANCE (TYP) C_S OFF C_D OFF	2pF 18pF
HIGH OFF ISOLATION AT 500kHz	90dB
LOW CHARGE INJECTION	0.3pC
SINGLE ENDED TO DIFFERENTIAL SELECTABLE (SDS)	
LOGIC LEVEL SELECTABLE (LLS)	

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- INDUSTRIAL CONTROL

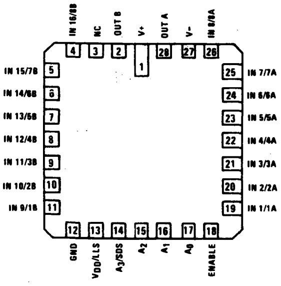
DESCRIPTION

The HI-516 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_3 enables the HI-516 to be user programmed either as a single ended 16-channel multiplexer by connecting 'out A' to 'out B' and using A_3 as a digital address input, or as an 8-channel differential multiplexer by connecting A_3 to the V^- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris dielectric isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I_D Off $<$ 100pA @ 25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

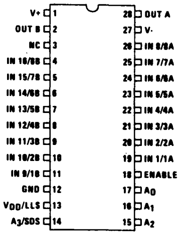
The HI-516 is available in a 28 lead dual-in-line package and a 28 lead LCC package (-8 only). It is offered in both commercial and military grades. for additional Hi-Rel screening including 160 hour burn-in, specify the -8 suffix.

PINOUT

TOP VIEWS



IN 16/8B
NC
OUT B
V+
OUT A
V-
IN 8/8A
4
3
2
1
28
27
26
IN 15/7B 5
IN 14/6B 6
IN 13/5B 7
IN 12/4B 8
IN 11/3B 9
IN 10/2B 10
IN 9/1B 11
25 IN 7/7A
24 IN 6/6A
23 IN 5/5A
22 IN 4/4A
21 IN 3/3A
20 IN 2/2A
19 IN 1/1A
12 GND
13 V_{DD}/LLS
14 A_3/SDS
15 A_2
16 A_1
17 A_0
18 ENABLE

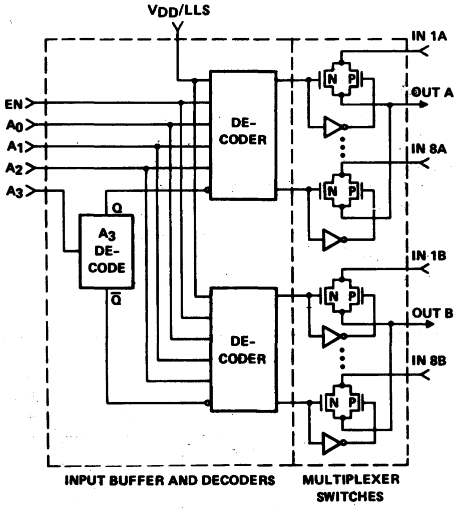


V+ 1
OUT B 2
NC 3
IN 16/8B 4
IN 15/7B 5
IN 14/6B 6
IN 13/5B 7
IN 12/4B 8
IN 11/3B 9
IN 10/2B 10
IN 9/1B 11
GND 12
V_{DD}/LLS 13
A_3/SDS 14
28 OUT A
27 V-
26 IN 8/8A
25 IN 7/7A
24 IN 6/6A
23 IN 5/5A
22 IN 4/4A
21 IN 3/3A
20 IN 2/2A
19 IN 1/1A
18 ENABLE
17 A_0
16 A_1
15 A_2

FUNCTIONAL DIAGRAM

A3 Decode

A_3	Q	$\overline{Q}$
H	H	L
L	L	H
V^-	L	L



V_{DD}/LLS
IN 1A
OUT A
IN 8A
EN
A_0
A_1
A_2
A_3
DE-CODER
Q
A_3 DE-CODE
$\overline{Q}$
N
P
IN 1B
OUT B
IN 8B
DE-CODER
INPUT BUFFER AND DECODERS
MULTIPLEXER SWITCHES

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:
TTL { $-6V < V_{AH} < +6V$
A3 V_{SUPPLY} (-) -2V
CMOS { V_{SUPPLY}(+) +2V
GND -2V
Analog Input Voltage:
V_S { V_{SUPPLY}(+) +2V
V_{SUPPLY}(-) -2V

Voltage Between Supply Pins 33V
Total Power Dissipation * (Cerdip) 2000mW
Operating Temperature Ranges:
HI-516-2,-8 -55°C to +125°C
HI-516-5 0°C to 75°C
Storage Temperature Range -65°C to 150°C

*Derate 20mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 1)

		-55°C to +125°C			0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range (Note 2)	Full	-14		+14	-15		-15	V
R_{ON}, On Resistance (Note 3)	+25°C		620	750		620	750	Ω
	Full			1,000			1,000	Ω
I_S (OFF), Off Input Leakage Current	+25°C		0.01			0.01		nA
	Full			50			50	nA
I_D(OFF), Off Output Leakage Current	+25°C		0.03			0.03		nA
	Full			100			100	nA
I_D(ON), On Channel Leakage Current	+25°C		0.04			0.04		nA
	Full			100			100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AH} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AL} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full			1			1	μA
I_{AL} Current (Low)	Full			25			25	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		100	150		100	150	ns
	Full			200			200	ns
t_{OPEN}, Break before make delay	+25°C		20			20		ns
t_{ON}(EN), Enable Delay (ON)	+25°C		100	150		100		ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		80	150		80		ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		ns
Charge Injection (Note 4)	+25°C		0.3			0.3		pC
Off Isolation (Note 5)	+25°C		90			90		dB
C_S(OFF), Channel Input Capacitance	+25°C		2			2		pF
C_D(OFF), Channel Output Capacitance	+25°C		18			18		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS}(OFF), Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
PD, Power Dissipation	Full		525			525		mW
I^+, Current (Note 6)	Full			25			30	mA
I^-, Current (Note 6)	Full			25			30	mA

NOTES:
1. V_{DD}/LLS pin = open or grounded for TTL Compatibility
V_{DD}/LLS pin = V_{DD} for CMOS Compatibility
2. At temperatures above 90°C, care must be taken to assure V_S remains at least 1.0V below the V_{SUPPLY} for proper operation.
3. $V_{IN} = \pm 10V$, $I_{OUT} = -100\mu A$
4. $V_{IN} = 0V$, $C_L = 100pF$, Enable input pulse = 3V, f = 500kHz.
5. $V_{EN} = 0.8V$, $V_S = 3V_{RMS}$, f = 500kHz, $C_L = 40pF$, $R_L = 1k$, Pin 3 grounded.
6. $V_{EN} = +2.4V$

TRUTH TABLES

HI-516 USED AS A 16-CHANNEL MULTIPLEXER OR
8 CHANNEL DIFFERENTIAL MULTIPLEXER *

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	NONE	NONE
H	L	L	L	L	1A	NONE
H	L	L	L	H	2A	NONE
H	L	L	H	L	3A	NONE
H	L	L	H	H	4A	NONE
H	L	H	L	L	5A	NONE
H	L	H	L	H	6A	NONE
H	L	H	H	L	7A	NONE
H	L	H	H	H	8A	NONE
H	H	L	L	L	NONE	1B
H	H	L	L	H	NONE	2B
H	H	L	H	L	NONE	3B
H	H	L	H	H	NONE	4B
H	H	H	L	L	NONE	5B
H	H	H	L	H	NONE	6B
H	H	H	H	L	NONE	7B
H	H	H	H	H	NONE	8B

* For 16-Channel single-ended function, tie 'out A' to 'out B', for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

HI-516 USED AS A DIFFERENTIAL
8-CHANNEL MULTIPLEXER

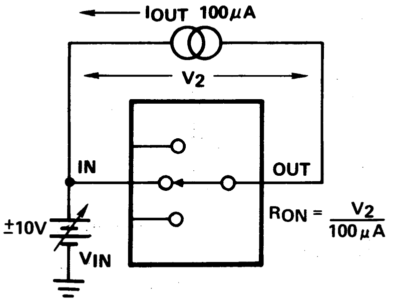
A_3 CONNECT TO V^- SUPPLY				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

DIE CHARACTERISTICS

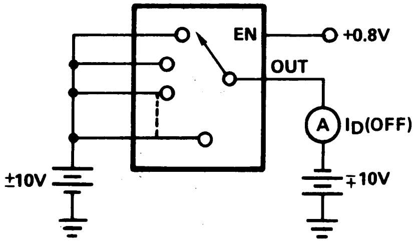
Transistor Count		647	
Die Size		90 x 147 mils	
Thermal Constants	θ_{ja}	$50^oC/W$	For Ceramic DIP
	θ_{jc}	$18^oC/W$	
Tie Substrate to:		$-V_{Supply}$	
Process:		CMOS - DI	

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

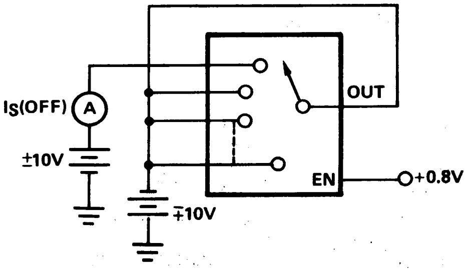
TEST CIRCUIT NO. 1
ON RESISTANCE vs. INPUT SIGNAL LEVEL


I_{OUT} 100µA
V_2
IN
OUT
±10V
V_{IN}
$R_{ON} = \frac{V_2}{100\mu A}$

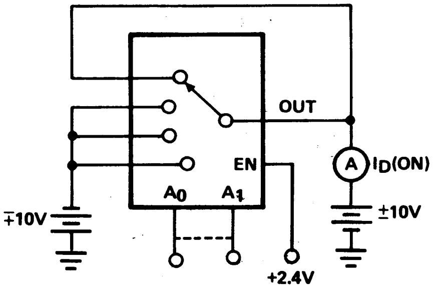
TEST CIRCUIT NO. 2*


EN
+0.8V
OUT
A
$I_{D(OFF)}$
±10V
∓10V

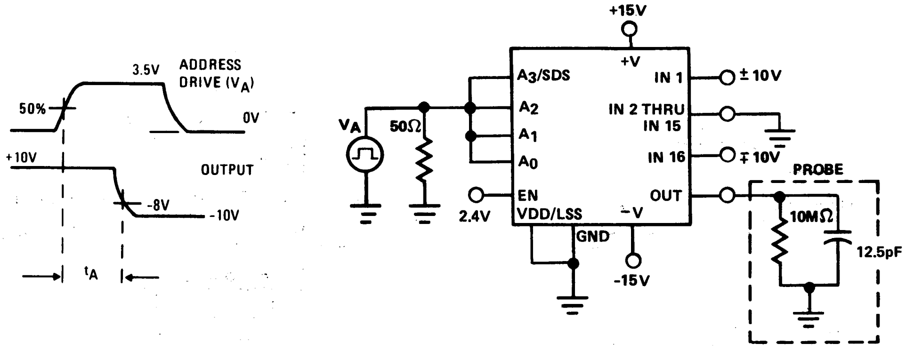
TEST CIRCUIT NO. 3*


$I_{S(OFF)}$
A
±10V
OUT
EN
+0.8V
∓10V

TEST CIRCUIT NO. 4*


OUT
A
$I_{D(ON)}$
EN
A_0
A_1
∓10V
±10V
+2.4V

TEST CIRCUIT NO. 5
ACCESS TIME

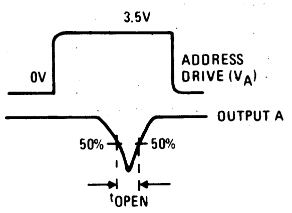

3.5V
ADDRESS DRIVE (V_A)
50%
0V
+10V
OUTPUT
-8V
-10V
t_A
+15V
+V
A_3/SDS
A_2
A_1
A_0
EN
VDD/LSS
IN 1
IN 2 THRU IN 15
IN 16
OUT
-V
GND
±10V
∓10V
V_A
50Ω
2.4V
-15V
PROBE
10MΩ
12.5pF

*Two measurements per channel: +10V/-10V and -10V/+10V.
(Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V)

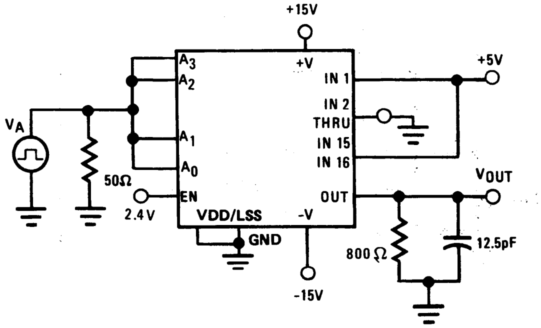
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (Continued)

TEST CIRCUIT NO. 6

ENABLE DRIVE

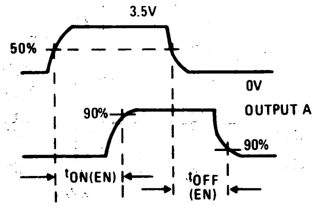

3.5V
0V
ADDRESS DRIVE (V_A)
OUTPUT A
50%
50%
t_{OPEN}

BREAK-BEFORE MAKE DELAY (t_{OPEN})

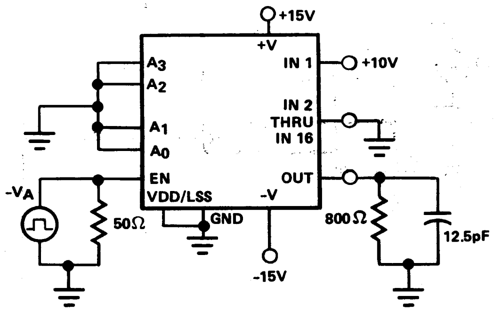

+15V
A_3
A_2
A_1
A_0
EN
+V
IN 1
IN 2 THRU IN 15
IN 16
OUT
VDD/LSS
-V
GND
V_A
50Ω
2.4V
+5V
V_{OUT}
800Ω
12.5pF
-15V

TEST CIRCUIT NO. 7

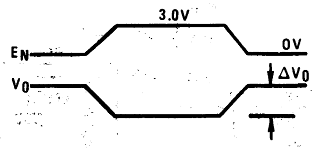
ENABLE DRIVE


3.5V
50%
0V
90%
OUTPUT A
90%
$t_{ON(EN)}$
$t_{OFF(EN)}$

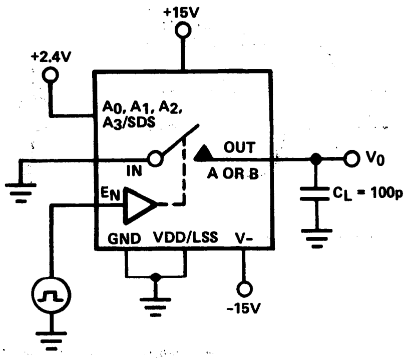
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)


+15V
+V
A_3
A_2
A_1
A_0
EN
VDD/LSS
IN 1
+10V
IN 2 THRU IN 16
OUT
-V
GND
$-V_A$
50Ω
800Ω
12.5pF
-15V

TEST CIRCUIT NO. 8
CHARGE INJECTION TEST CIRCUIT


3.0V
EN
0V
V_0
ΔV_0

ΔV_0 IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $Q = C_L \times \Delta V_0$.


+15V
+2.4V
A_0, A_1, A_2, A_3/SDS
IN
OUT
A OR B
EN
GND
VDD/LSS
V-
V_0
C_L = 100pF
-15V

HARRIS

HI-518

8 Channel/Differential
4 Channel CMOS High Speed Analog Multiplexer

FEATURES

• ACCESS TIME (TYP)		80ns
• SETTLING TIME (0.1%)		250ns
• LOW LEAKAGE (TYP)	I_S (OFF)	5pA
	I_D (OFF)	15pA
• LOW CAPACITANCE (TYP)	C_S (OFF)	2pF
	C_D (OFF)	10pF
• HIGH OFF ISOLATION AT 500kHz		86dB
• LOW CHARGE INJECTION		0.3pC
• SINGLE ENDED TO DIFFERENTIAL SELECTABLE (SDS)		
• LOGIC LEVEL SELECTABLE (LLS)		

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- TELEMETRY
- INDUSTRIAL CONTROL

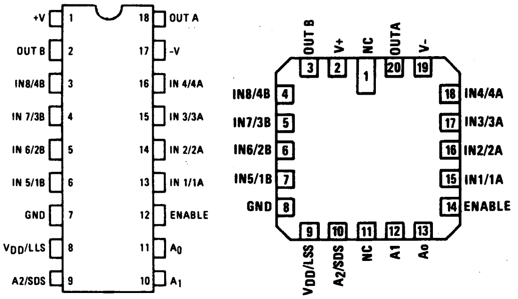
DESCRIPTION

The HI-518 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_2 enables the HI-518 to be user programmed either as a single ended 8-channel multiplexer by connection 'out A' to 'out B' and using A_2 as a digital address input, or as a 4-channel differential multiplexer by connecting A_2 to the V- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris dielectric isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I_D Off $<$ 100pA@25°C) and fast settling (t_{SETTLE}=800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

The HI-518 is available in an 18 lead dual-in-line package and a 20 lead LCC package (-8 only). It is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

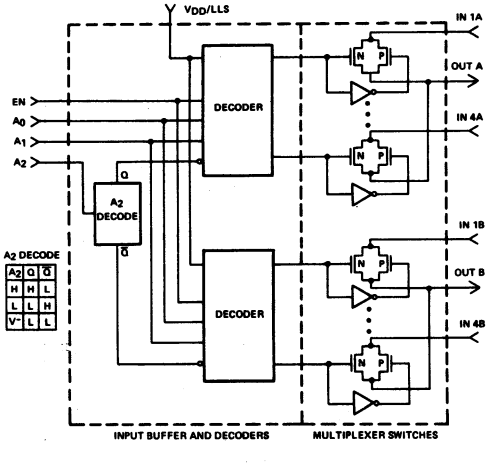
PINOUT

TOP VIEWS



+V 1
OUT B 2
IN8/4B 3
IN 7/3B 4
IN 6/2B 5
IN 5/1B 6
GND 7
VDD/LLS 8
A2/SDS 9
18 OUT A
17 -V
16 IN 4/4A
15 IN 3/3A
14 IN 2/2A
13 IN 1/1A
12 ENABLE
11 A0
10 A1
OUT B 3
V+ 2
NC 1
OUTA 20
V- 19
IN8/4B 4
IN7/3B 5
IN6/2B 6
IN5/1B 7
GND 8
18 IN4/4A
17 IN3/3A
16 IN2/2A
15 IN1/1A
14 ENABLE
9 VDD/LSS
10 A2/SDS
11 NC
12 A1
13 A0

FUNCTIONAL DIAGRAM



VDD/LLS
EN
A0
A1
A2
DECODER
DECODER
A2 DECODE
Q
Q̄
A2 DECODE
A2 Q Q̄
H H L
L L H
V- L L
N P
IN 1A
OUT A
IN 4A
IN 1B
OUT B
IN 4B
INPUT BUFFER AND DECODERS
MULTIPLEXER SWITCHES

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:

TTL	$-6V < V_{AH} < +6V$	
	A2 V_{SUPPLY} (-)	-2V
CMOS	V_{SUPPLY}(+)	+2V
	GND	-2V

Analog Input Voltage:

V_S	V_{SUPPLY}(+)	+2V
	V_{SUPPLY}(-)	-2V

Voltage Between Supply Pins	33V
Total Power Dissipation * (Cerdip)	1.19mW
Operating Temperature Ranges:	
HI-518-2,-8	-55°C to +125°C
HI-518-5	0°C to 75°C
Storage Temperature Range	-65°C to 150°C

*Derate 11.9mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = Gnd. (Note 1).

PARAMETER	TEMP	-55°C to +125°C			0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS								
V_S Analog Signal Range (Note 2)	Full	-14		+14	-15		+15	V
R_{ON} On Resistance (Note 3)	+25°C		480	750		480	750	Ω
	Full			1000			1000	Ω
I_S (OFF) Off Input Leakage Current	+25°C		.005			0.05		nA
	Full			50		0.60	50	nA
I_D (OFF) Off Output Leakage Current	+25°C		.015			0.10		nA
	Full			50			50	nA
I_D (ON) On Channel Leakage Current	+25°C		.015			0.10		nA
	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AL} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full			1			1	μA
I_{AL} Input Leakage Current (Low)	Full			20			20	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		80	125		80	125	ns
	Full			150			150	ns
t_{OPEN}, Break before make Delay	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		80	150		80	150	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		60	125		60	125	ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		ns
Charge Injection (Note 4)	+25°C		0.3			0.3		pC
Off Isolation (Note 5)	+25°C		86			86		dB
C_S (OFF) Channel Input Capacitance	+25°C		2			2		pF
C_D (OFF) Channel Output Capacitance	+25°C		10			10		pF
C_A, Digital Input Capacitance	+25°C		3			3		pF
CDS (OFF) Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		360	450		360	540	mW
I+, Current (Note 6)	Full		12	15		12	18	mA
I^-, Current (Note 6)	Full		12	15		12	18	mA

1. V_{DD}/LLS Pin = Open or Grounded ed for TTL compatibility. V_{DD}/LLS for CMOS compatibility.
2. At temperatures above 90°C, care must be taken to assure V_S remains at least 1.0V below the V_{SUPPLY}.
3. $V_{IN} = \pm 10V$, $I_{OUT} = -100\mu A$.
4. $V_{IN} = 0V$, $C_L = 100pF$, Enable Input pulse = 3V, f = 500kHz.
5. $C_L = 40pF$, $R_L = 1k$. Due to the pin to pin capacitance between IN 8/4B (Pin 3) and Out B (Pin 2) channel 8/4B exhibits 60dB of Off Isolation under the above test conditions.
6. $V_{EN} = +2.4V$.

TRUTH TABLES

HI-518 USED AS 8 CHANNEL MULTIPLEXER OR
4 CHANNEL DIFFERENTIAL MULTIPLEXER

USE A_2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	NONE
H	L	L	H	2A	NONE
H	L	H	L	3A	NONE
H	L	H	H	4A	NONE
H	H	L	L	NONE	1B
H	H	L	H	NONE	2B
H	H	H	L	NONE	3B
H	H	H	H	NONE	4B

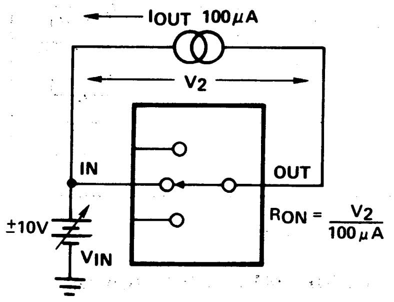
HI-518 USED AS DIFFERENTIAL
4 CHANNEL MULTIPLEXER

A_2 CONNECT TO V^- SUPPLY			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	NONE	NONE
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

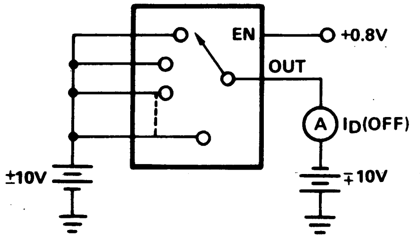
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

TEST CIRCUIT NO. 1

ON RESISTANCE vs. INPUT SIGNAL LEVEL



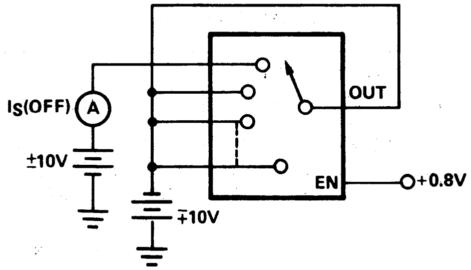
TEST CIRCUIT NO. 2*



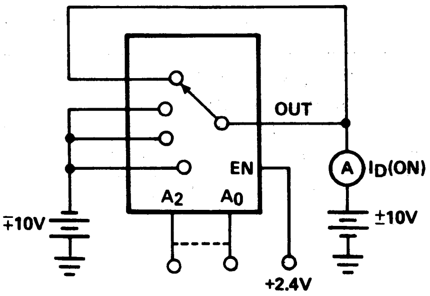
*Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for I_D(OFF): +10V/-10V and +10V/-10V)

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (Continued)

TEST CIRCUIT NO. 3*


$I_S(OFF)$
A
±10V
∓10V
OUT
EN
+0.8V

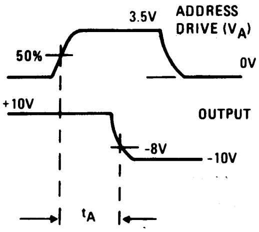
TEST CIRCUIT NO. 4*

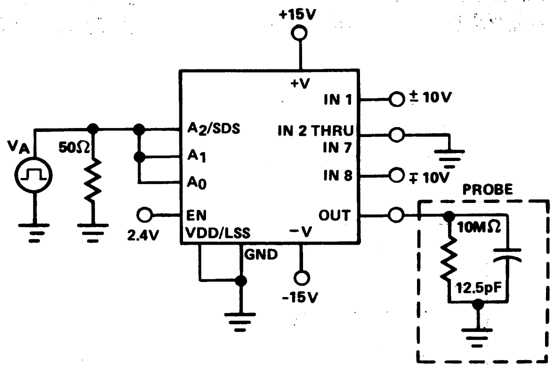

OUT
EN
A_2
A_0
∓10V
+2.4V
A
$I_D(ON)$
±10V

*Two measurements per channel: +10V/-10V and -10V/+10V.
(Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V)

TEST CIRCUIT NO. 5

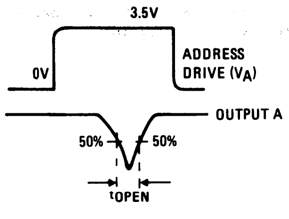
ACCESS TIME



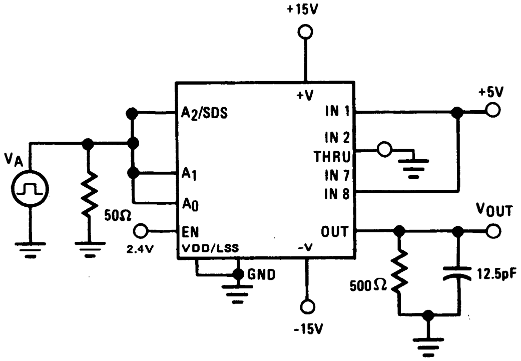

+15V
+V
IN 1
± 10V
A_2/SDS
IN 2 THRU IN 7
A_1
A_0
IN 8
∓ 10V
V_A
50Ω
EN
2.4V
VDD/LSS
OUT
−V
GND
-15V
PROBE
10MΩ
12.5pF

TEST CIRCUIT NO. 6

ENABLE DRIVE

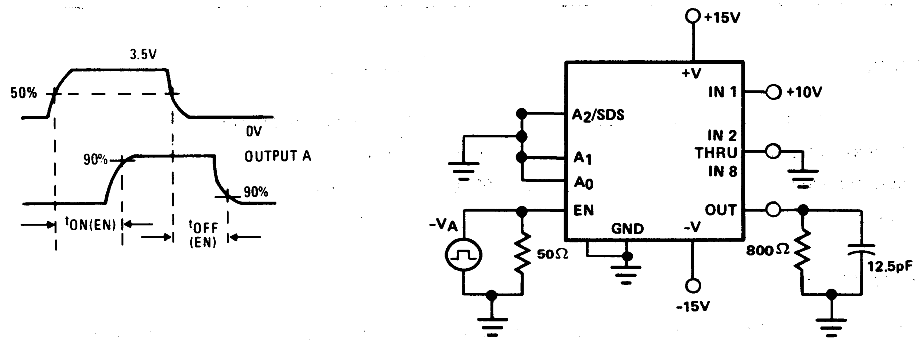


BREAK-BEFORE MAKE DELAY (t_{OPEN})


+15V
+V
A_2/SDS
IN 1
+5V
IN 2 THRU IN 7
IN 8
V_A
A_1
A_0
50Ω
EN
2.4V
VDD/LSS
OUT
V_{OUT}
-V
GND
500Ω
12.5pF
-15V

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (Continued)

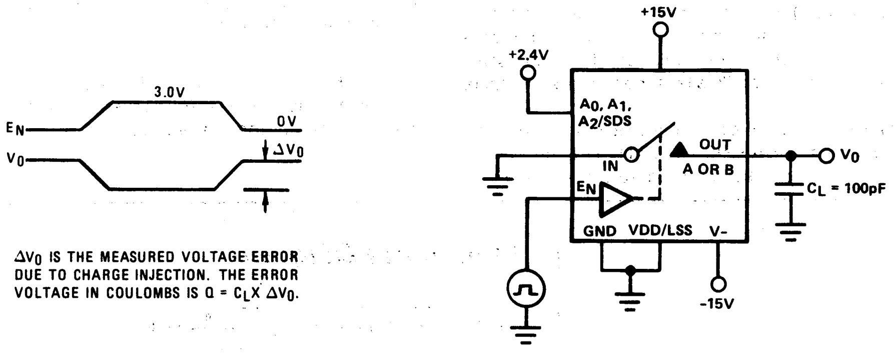
TEST CIRCUIT NO. 7


3.5V
50%
0V
OUTPUT A
90%
90%
$t_{ON(EN)}$
$t_{OFF(EN)}$
+15V
+V
IN 1
+10V
A2/SDS
IN 2
THRU
IN 8
A1
A0
EN
OUT
-VA
GND
-V
50Ω
800Ω
12.5pF
-15V

ENABLE DRIVE

ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

TEST CIRCUIT NO. 8
CHARGE INJECTION TEST CIRCUIT


3.0V
EN
0V
V0
ΔV0
+15V
+2.4V
A0, A1,
A2/SDS
OUT
IN
A OR B
EN
V0
CL = 100pF
GND
VDD/LSS
V-
-15V

ΔV_0 IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $Q = C_L \times \Delta V_0$.

DIE CHARACTERISTICS

Transistor Count		356	
Die Size		90 x 93 mils	
Thermal Constants	θ_{ja}	84°C/W	For Ceramic Dip
	θ_{jc}	25°C/W	
Tie Substrate to:		$-V_{Supply}$	
Process:		CMOS - DI	

HARRIS HI-524

4 Channel Wideband and Video Multiplexer

Features

- **Crosstalk (10 MHz) .... < -60dB**
- **Fast Access Time 150ns**
- **Fast Settling Time 200ns**
- **TTL Compatible**

Applications

Wideband Switching

- **Radar**
- **TV Video**
- **ECM**

Description

The HI-524 is a four channel CMOS analog multiplexer designed to process single-ended signals with bandwidths up to 10MHz. The chip includes a 1 of 4 decoder for channel selection and an Enable input to inhibit all channels (chip select).

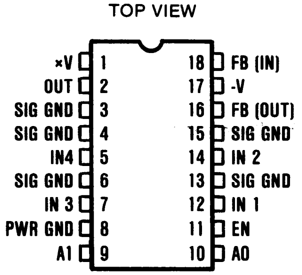
Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure that Crosstalk is less than -60dB at 10MHz.

The HI-524 is designed to operate into a wideband buffer amplifier such as the HARRIS HA-2541. The multiplexer chip includes two "on" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel R_{ON} resistance, to minimize the amplifier V_{OS} and its variation with temperature.

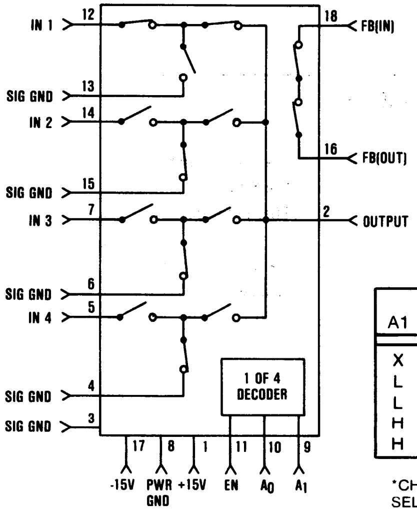
The HI-524 is well suited to the rapid switching of video and other wideband signals in telemetry, instrumentation, radar and video systems. It is packaged in an 18 pin ceramic or plastic DIP and operates on ±15V supplies.

The HI-524 is offered in both commercial and military grades. For aditional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

Pinout


TOP VIEW
+V 1
OUT 2
SIG GND 3
SIG GND 4
IN4 5
SIG GND 6
IN 3 7
PWR GND 8
A1 9
18 FB (IN)
17 -V
16 FB (OUT)
15 SIG GND
14 IN 2
13 SIG GND
12 IN 1
11 EN
10 A0

Functional Diagram


IN 1 12
SIG GND 13
IN 2 14
SIG GND 15
IN 3 7
SIG GND 6
IN 4 5
SIG GND 4
SIG GND 3
18 FB(IN)
16 FB(OUT)
2 OUTPUT
1 OF 4 DECODER
17 -15V
8 PWR GND
1 +15V
11 EN
10 A_0
9 A_1

TRUTH TABLE

A1	A0	EN	ON CHANNEL
X	X	L	NONE
L	L	H	1*
L	H	H	2
H	L	H	3
H	H	H	4

*CHANNEL 1 IS SHOWN SELECTED IN THE DIAGRAM

HI-524 Specifications

Absolute Maximum Ratings

Digital Input Overvoltage:
$-6V < VAH < +6V$

Analog Input (V_S) or Output (V_O)

$+V_{SUPPLY}$ +2V
$-V_{SUPPLY}$ -2V

Voltage Between Supply	33V
Either Supply to Ground	16.5V
Total Power Dissipation* (Ceramic)	1.23W

Operating Temperature Range

HI-524-2, -8	-55°C to +125°C
HI-524-5	0°C to 75°C
Storage Temp. Range	-65°C to 150°C

*Derate 12.3mW/°C above 75°C

Electrical Characteristics (Unless otherwise specified) Supplies = +15V, -15V; VAH (Logic Level High) = +2.4V, V_{AL} = (Logic Level Low) = +0.8V; V_{EN} = +2.4V

PARAMETER	TEMP	HI-524-2, -8 -55°C to +125°C			HI-524-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS								
VS, Analog Signal Range	Full	-10		+10	-10		+10	V
R_{ON}, On Resistance (Note 1)	+25°C		700			700		Ω
	Full			1.5K			1.5K	Ω
I_S (OFF), Off Input Leakage Current (Note 2)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current (Note 2)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (ON), On Channel Leakage Current (Note 2)	+25°C		0.7			0.7		nA
	Full			50			50	nA
3dB Bandwidth: (Note 3)	+25°C		16			16		MHz
	Full		11			13		MHz
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	µA
A_L Current (Low)	Full		4	25		4	25	µA
SWITCHING CHARACTERISTICS								
t_A, Access Time (Note 4)	+25°C		150	300		150	300	ns
t_{OPEN}, Break before make delay (Note 4)	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON), R_L = 500Ω	+25°C		180	300		180		ns
t_{OFF} (EN), Enable Delay (OFF), R_L =500Ω	+25°C		180	250		180		ns
Settling Time (0.1%) (Note 4)	+25°C		200			200		ns
(0.01%)	+25°C		600			600		ns
Crosstalk (Note 5)	+25°C		-65			-65		dB
C_S(OFF), Channel Input Capacitance	+25°C		4			4		pF
C_D(OFF),Channel Output Capacitance	+25°C		10			10		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		540			540		mW
I+, Current (Note 6)	Full		18	25		18	25	mA
I-, Current (Note 6)	Full		18	25		18	25	mA

NOTES:

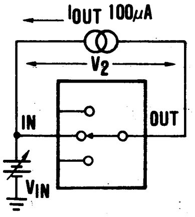
1. $V_{IN} = \pm 10V$; $I_{OUT} = 100\mu A$ (See Test Circuits # 1)
2. $V_O = \pm 10V$; $VS = \pm 10V$ (See Test Circuits # 2,3,4,)
3. MUX output is buffered with HA-5033 amplifier
4. (See Test Circuit #5)
5. V_{IN} = 10MHz, 3Vp-p on one channel, with any other channel selected. (Worst case is channel 3 selected with input on channel 4). MUX output is buffered with HA-2541 as shown in Applications section. Terminate all channels with 75Ω.
6. Supply currents vary less than 0.5mA for switching rates from DC to 2MHz.

HI-524 Performance Characteristics and Test Circuits

ON RESISTANCE

(Unless otherwise specified $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$)

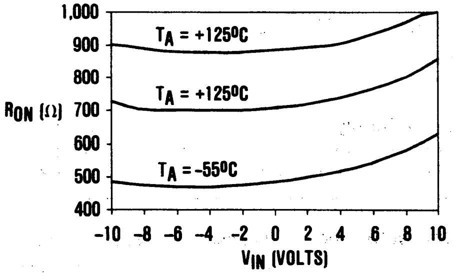
TEST CIRCUIT NO. 1



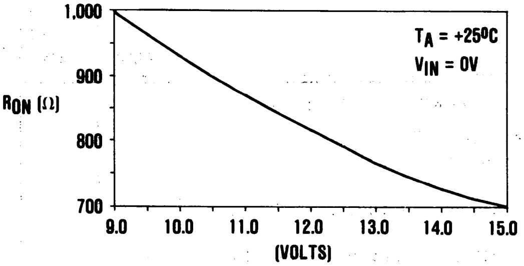
I_{OUT} 100μA
V_2
IN
OUT
V_{IN}

$$R_{ON} = \frac{V2}{100\mu A}$$

ON RESISTANCE vs. ANALOG INPUT VOLTAGE

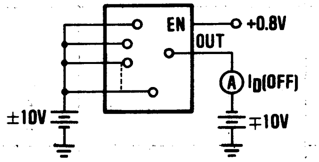


ON RESISTANCE vs. SUPPLY VOLTAGE



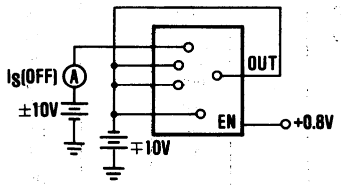
LEAKAGE CURRENT

TEST CIRCUIT NO. 2*



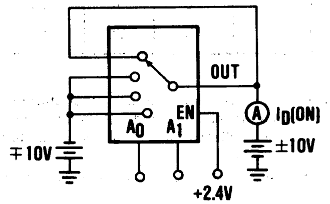
EN
+0.8V
OUT
$I_D(OFF)$
±10V
∓10V

TEST CIRCUIT NO. 3*



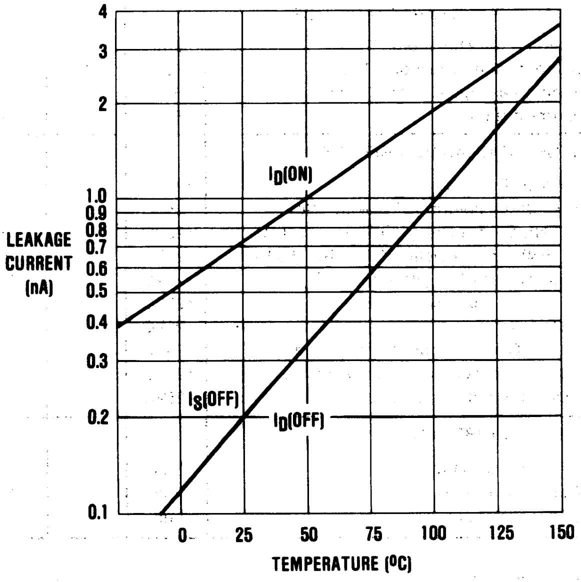
$I_S(OFF)$
±10V
OUT
EN
+0.8V
∓10V

TEST CIRCUIT NO. 4*



OUT
EN
A_0
A_1
$I_D(ON)$
∓10V
±10V
+2.4V

LEAKAGE CURRENT vs. TEMPERATURE

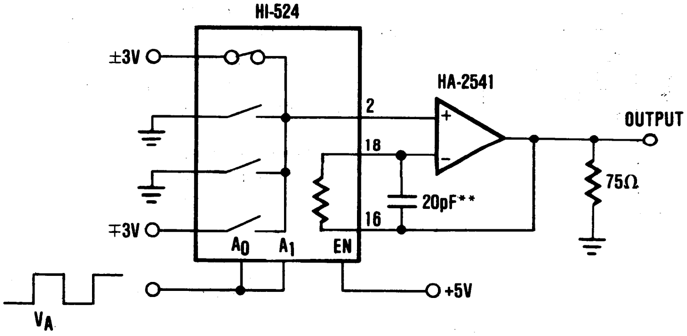


* Two measurements per channel:
+10V/-10V and -10V/+10V
(Two measurements per device for $I_D(OFF)$:
+10V/-10V and -10V/+10V.)

Performance Characteristics and Test Circuits (Continued)

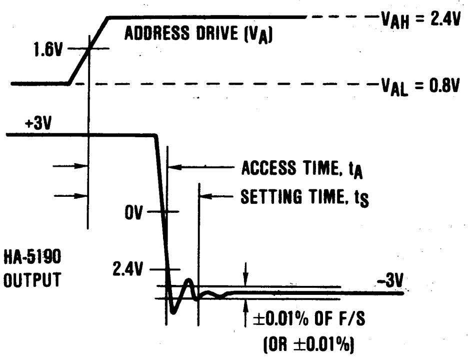
TEST CIRCUIT NO. 5

SETTLING TIME
ACCESS TIME
BREAK-BEFORE-MAKE DELAY *

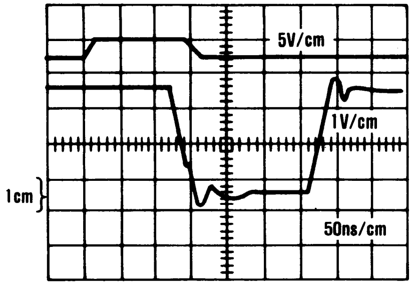

HI-524
±3V
∓3V
A0
A1
EN
2
18
16
HA-2541
+
−
OUTPUT
75Ω
20pF**
+5V
VA

* This test requires channel inputs 1 and 4 at the same level.
** Capacitor value may be selected to optimize AC performance.

(Use Differential comparator plug-in on scope for settling time measurement)

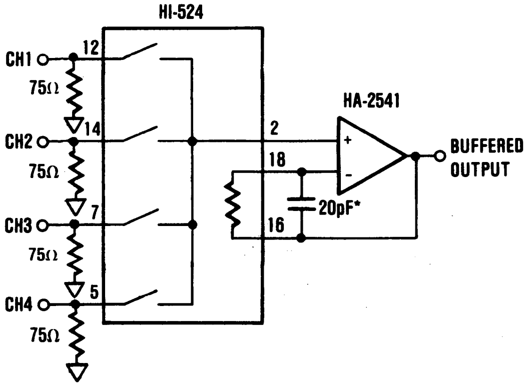

ADDRESS DRIVE (VA)
VAH = 2.4V
1.6V
VAL = 0.8V
+3V
ACCESS TIME, tA
SETTING TIME, tS
0V
HA-5190
OUTPUT
2.4V
-3V
±0.01% OF F/S
(OR ±0.01%)

ACCESS TIME



Applications

Often it is desirable to buffer the HI-524 output, to avoid loading errors due to the channel "ON" resistance:



* Capacitor value may be selected to optimize AC performance.

The buffer amplifier should offer sufficient bandwidth and slew rate to avoid degradation of the anticipated signals. For video switching, the HA-5033 and HA-2542 offer good performance plus ±100mA output current for driving coaxial cables. For general wideband applications, the HA-2541 offers the convenience of unity gain stability plus 90ns settling (to ±0.1%) and ±10V output swing. Also, the HI-524 includes a feedback resistance for use with the HA-2541. This resistance matches and tracks the channel "ON" resistance, to minimize offset voltage due to the buffer's bias currents.

Note that the on-chip feedback element between pins 16 and 18 includes two switches in series, to simulate a channel resistance. These switches open for V_{EN} = Low. This allows two or more HI-524's to operate into one HA-2541, with their feedback elements connected in parallel. Thus, only the selected multiplexer provides feedback, and the amplifier remains stable.

All HI-524 package pins labeled 'SIG GND' (pins 3, 4, 6, 13, 15) should be externally connected to signal ground for best crosstalk performance.

Bypass capacitors (0.1 to 1.0μF) are recommended from each HI-524 supply pin to power ground (pins 1 and 17 to pin 8). Locate the buffer amplifier near the HI-524 so the two capacitors may bypass both devices.

If an analog input 1V or greater is present when supplies are off, a low resistance is seen from that input to a supply line. (For example, the resistance is approximately 160Ω for an input of -3V.) Current flow may be blocked by a diode in each supply line, or limited by a resistor in series with each channel. The best solution, of course, is to arrange that no digital or analog inputs are present when the power supplies are off.

Die Characteristics

Transistor Count		599	
Die Size		146 x 88.6 mils	
Thermal Constants	θ_{ja}	81°C/W	For Ceramic DIP
	θ_{jc}	22°C/W	
Tie Substrate to:		$-V_{Supply}$	
Process:		Linear SiGate CMOS-DI	

HI-539

Monolithic, Four Channel, Low Level, Differential Multiplexer

FEATURES

- DIFFERENTIAL PERFORMANCE, TYP.:
  - LOW ΔR_{ON}, +125°C 5.5Ω
  - LOW $\Delta I_{D(ON)}$, +125°C 0.6nA
  - LOW Δ(CHARGE INJECTION) 0.1pC
  - LOW CROSSTALK -120dB
- SETTLING TIME, ±0.01% 900ns
- WIDE SUPPLY RANGE ±5V TO ±18V
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- LOW LEVEL DATA ACQUISITION
- PRECISION INSTRUMENTATION
- TEST SYSTEMS

DESCRIPTION

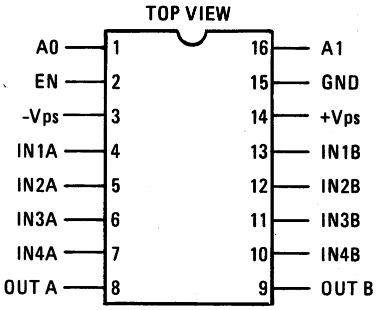
The Harris HI-539 is a monolithic, four channel, differential multiplexer. Two digital inputs are provided for channel selection, plus an Enable input to disconnect all channels.

Performance is guaranteed for each channel over the range ± 10V, but is optimized for low level differential signals. Leakage current, for example, which varies slightly with input voltage, has its distribution centered at zero for zero input volts.

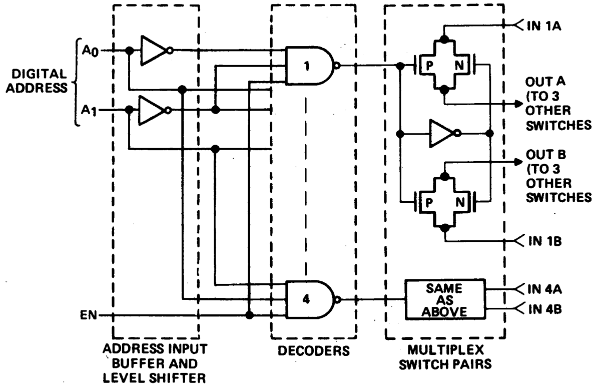
In most monolithic multiplexers, the net differential offset due to thermal effects becomes significant for low level signals. This problem is minimized in the HI-539 by symmetrical placement of critical circuitry with respect to the few heat producing devices.

The HI-539 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. Supply voltages are ± 15V and power consumption is only 2.5mW. The package is a 16 pin ceramic or plastic DIP.

PINOUT


TOP VIEW
A0 1
EN 2
-Vps 3
IN1A 4
IN2A 5
IN3A 6
IN4A 7
OUT A 8
16 A1
15 GND
14 +Vps
13 IN1B
12 IN2B
11 IN3B
10 IN4B
9 OUT B

FUNCTIONAL DIAGRAM


DIGITAL ADDRESS
A0
A1
EN
1
4
P
N
IN 1A
OUT A (TO 3 OTHER SWITCHES)
OUT B (TO 3 OTHER SWITCHES)
IN 1B
SAME AS ABOVE
IN 4A
IN 4B
ADDRESS INPUT BUFFER AND LEVEL SHIFTER
DECODERS
MULTIPLEX SWITCH PAIRS

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between Supply Pins (V_{ps+}, V_{ps-})	40V
Voltage from either Supply to Ground	20V
Analog Input Voltage, V_S	$V_{ps-} \leq V_S \leq V_{ps+}$
Digital Input Voltage, V_A	$V_{ps-} \leq V_A \leq V_{ps+}$
Storage Temperature Range	-65°C to +150°C

Internal Power Dissipation*	(Ceramic)	1265mW
Operating Temperature Range		
	HI-539-2, -8	-55°C to +125°C
	HI-539-4	-25°C to +85°C
	HI-539-5	0°C to +75°C

*Derate 12.65mW°C above 75°C.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = ± 15V, V_{EN} = +4.0V, V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V.
See the Performance Characteristics Section for test circuits and conditions.
Selected parameters are defined in the Definitions Section.

PARAMETER	TEMP	HI-539-2, -8		HI-539-4, -5		UNITS
		TYP	MAX (MIN)	TYP	MAX (MIN)	
ANALOG CHANNEL CHARA'S						
V_S, Analog Signal Range	Full		(-10)/+10		(-10)/+10	V
R_{ON}, On Resistance V_{IN} = 0V	+25°C	650	850	650	850	Ω
V_{IN} = ± 10V	+25°C	700	900	700	900	Ω
V_{IN} = 0V	Full	950	1.3K	800	1K	Ω
V_{IN} = ± 10V	Full	1.1k	1.4k	900	1.1k	Ω
ΔR_{ON} [Side A - Side B]						
V_{IN} = 0V	+25°C	4.0	24	4.0	24	Ω
V_{IN} = ± 10V	+25°C	4.5	27	4.5	27	Ω
V_{IN} = 0V	Full	4.75	28	4.0	24	Ω
V_{IN} = ± 10V	Full	5.5	33	4.5	27	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 1)						
Condition 0V	+25°C	30	200	30	200	pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{S(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3	100	3	100	pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 1)						
Condition 0V	+25°C	30	200	30	200	pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{D(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3	100	3	100	pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(ON)}$, On Channel Leakage Current (Note 1)						
Condition 0V	+25°C	50	200	50	200	pA
Condition ± 10V	+25°C	150		150		pA
Condition 0V	Full	5	25	0.5	2.5	nA
Condition ± 10V	Full	6	40	0.8	4.0	nA
$\Delta I_{D(ON)}$ [Side A - Side B]						
Condition 0V	+25°C	10	100	10	100	pA
Condition ± 10V	+25°C	30		30		pA
Condition 0V	Full	0.5	5	0.05	0.5	nA
Condition ± 10V	Full	0.6	6	0.08	0.8	nA
ΔV_{OS}, Differential Offset Voltage	+25°C	0.02		0.02		μV
	Full	0.70		0.08		μV

SPECIFICATIONS (Continued)

PARAMETER	TEMP	HI-539-2, -8 TYP	HI-539-2, -8 MAX (MIN)	HI-539-4, -5 TYP	HI-539-4, -5 MAX (MIN)	UNITS
DIGITAL INPUT CHARACTERISTICS						
V_{AL}, Input Low Threshold	Full		0.8		0.8	V
V_{AH}, Input High Threshold	Full		(4.0)		(4.0)	V
I_{AH}, Input Leakage Current (High)	Full		1		1	μA
I_{AL}, Input Leakage Current (Low)	Full		1		1	μA
SWITCHING CHARACTERISTICS						
T_A, Access Time	+25°C Full	250	750 1,000	250	750 1,000	ns ns
T_{open}, Break-Before-Make Delay	+25°C Full	85	(30) (30)	85	(30) (30)	ns ns
$T_{ON(EN)}$, Enable Delay On	+25°C Full	250	750 1,000	250	750 1,000	ns ns
$T_{OFF(EN)}$, Enable Delay Off	+25°C Full	160	650 900	160	650 900	ns ns
Settling Time, to ±0.01%	+25°C	0.9		0.9		μs
Charge Injection (Output)	Full	3		3		pC
Δ Charge Injection (Output)	Full	0.1		0.1		pC
Charge Injection (Input)	Full	10		10		pC
Differential Crosstalk (Note 3)	+25°C	124		124		dB
Single Ended Crosstalk (Note 3)	+25°C	100		100		dB
$C_{S(OFF)}$, Channel Input Capacitance	Full	5		5		pF
$C_{D(OFF)}$, Channel Output Capacitance	Full	7		7		pF
$C_{D(ON)}$, Channel On Output Capacitance	Full	17		17		pF
C_{DS}, Input to Output Capacitance (Note 4)	Full	0.08		0.08		pF
C_A, Digital Input Capacitance	Full	3		3		pF
POWER REQUIREMENTS						
P_D, Power Dissipation	+25°C Full	2.5	 45	2.5	 45	mW mW
I+ Current	+25°C Full	0.150	 2.0	0.150	 2.0	mA mA
I- Current	+25°C Full	0.001	 1.0	0.001	 1.0	mA mA
±V, Supply Voltage Range	Full	±15	(±5)/±18	±15	(±5)/±18	V

NOTES

1. See Test Circuits #2, 3, 4. The condition ±10V means:

$I_{S(OFF)}$ and $I_{D(OFF)}$: (V_S = +10V, V_D = -10V), then
(V_S = -10V, V_D = +10V)
$I_{D(ON)}$: (+10V, then -10V)

2. ΔV_{OS} (Exclusive of thermocouple effects) = $R_{ON}\,\Delta I_{D(ON)} + I_{D(ON)}\,\Delta R_{ON}$.

See Applications section for discussion of additional V_{OS} error.

3. V_{IN} = 1kHz, $15V_{p-p}$ on all but the selected channel. See Test Circuit #9.

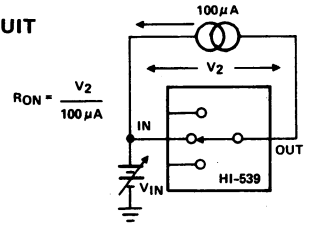
4. Calculated from typical Single-Ended Crosstalk performance.

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = +4V$ AND $V_{AL} = +0.8V$)

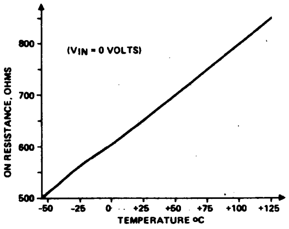
ON RESISTANCE MEASUREMENT

TEST CIRCUIT NO. 1

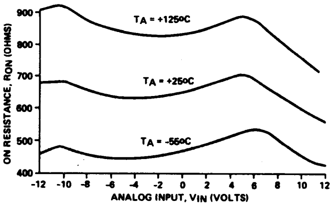


100µA
V2
$R_{ON} = \frac{V_2}{100\mu A}$
IN
OUT
HI-539
VIN

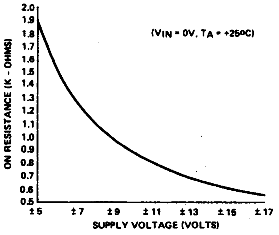
ON RESISTANCE vs. TEMPERATURE



ON RESISTANCE vs. ANALOG INPUT VOLTAGE

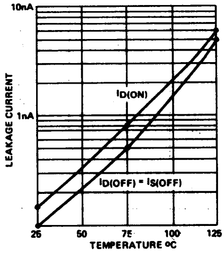


NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

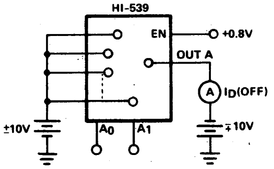


LEAKAGE CURRENT

LEAKAGE CURRENT vs. TEMPERATURE



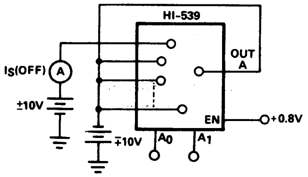
TEST CIRCUIT NO. 2*



HI-539
EN
+0.8V
OUT A
A
ID(OFF)
±10V
∓10V
A0
A1

(Similar connections for side "B")

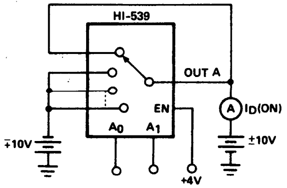
TEST CIRCUIT NO. 3*



HI-539
IS(OFF)
A
±10V
∓10V
OUT A
EN
+0.8V
A0
A1

(Similar connections for side "B")

TEST CIRCUIT NO. 4*



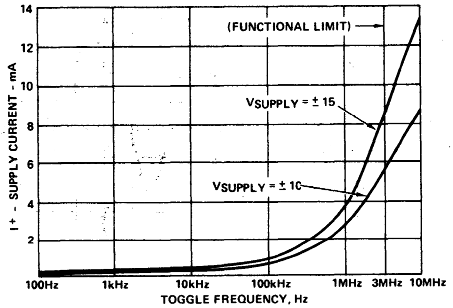
HI-539
OUT A
EN
A
ID(ON)
∓10V
±10V
A0
A1
+4V

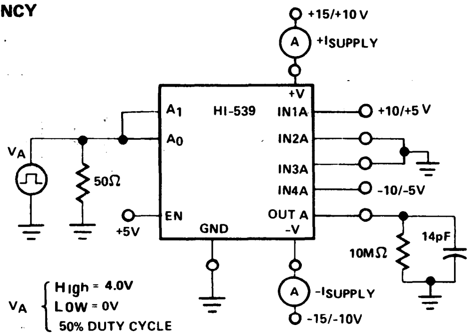
(Similar connections for side "B")

***Three measurements = +10V/-10V, -10V/+10V, and 0V**

TEST CIRCUITS (Continued)

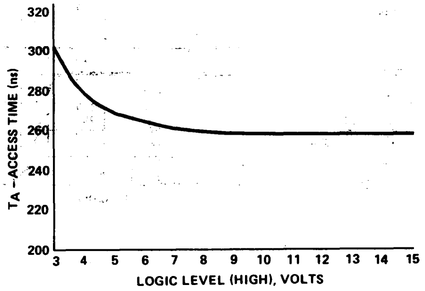
TEST CIRCUIT
NO. 5
SUPPLY CURRENT vs. TOGGLE FREQUENCY

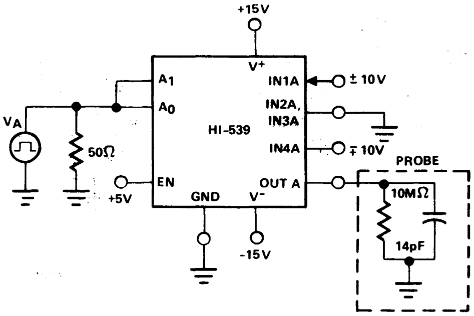



+15/+10 V
A
+ISUPPLY
+V
A1
HI-539
IN1A
+10/+5 V
A0
IN2A
IN3A
IN4A
-10/-5V
VA
50Ω
EN
+5V
GND
OUT A
-V
10MΩ
14pF
A
-ISUPPLY
-15/-10V
VA High = 4.0V
LOW = 0V
50% DUTY CYCLE

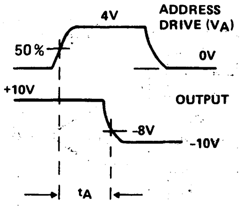
(SIMILAR CONNECTIONS FOR "B" SIDE)

TEST CIRCUIT
NO. 6
ACCESS TIME vs. LOGIC LEVEL (HIGH)

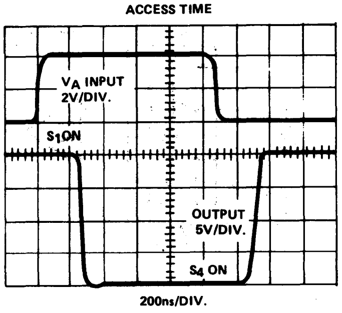



+15V
V+
A1
IN1A
± 10V
A0
IN2A, IN3A
HI-539
VA
50Ω
IN4A
∓ 10V
PROBE
EN
OUT A
+5V
GND
V-
10MΩ
14pF
-15V

(SIMILAR CONNECTIONS FOR "B" SIDE)

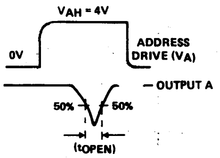

4V
ADDRESS DRIVE (VA)
50%
0V
+10V
OUTPUT
-8V
-10V
tA

Example: t_A for 4V logic level

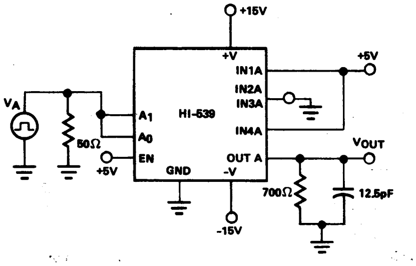


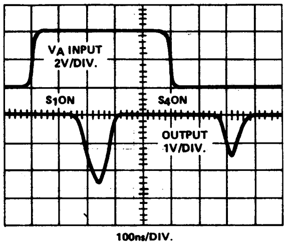
TEST CIRCUIT
NO. 7

ADDRESS DRIVE


V_{AH} = 4V
0V
ADDRESS DRIVE (V_A)
— OUTPUT A
50%
50%
(t_{OPEN})

BREAK-BEFORE-MAKE DELAY (t_{OPEN})

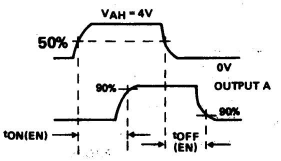

+15V
+V
IN1A
+5V
IN2A
IN3A
V_A
A1
HI-539
A0
IN4A
50Ω
EN
+5V
GND
OUT A
-V
V_{OUT}
700Ω
12.5pF
-15V



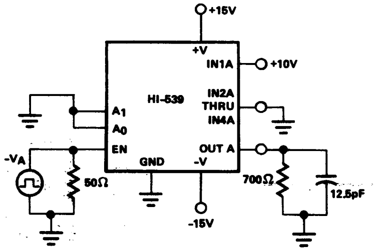
(SIMILAR CONNECTION FOR "B" SIDE)

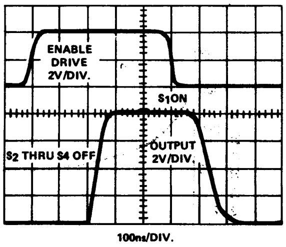
TEST CIRCUIT
NO. 8

ENABLE DRIVE


V_{AH} = 4V
50%
0V
90%
OUTPUT A
90%
$t_{ON(EN)}$
t_{OFF} (EN)

ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

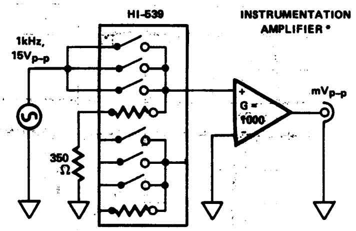

+15V
+V
IN1A
+10V
HI-539
IN2A
THRU
IN4A
A1
A0
EN
-V_A
50Ω
GND
OUT A
-V
700Ω
12.5pF
-15V



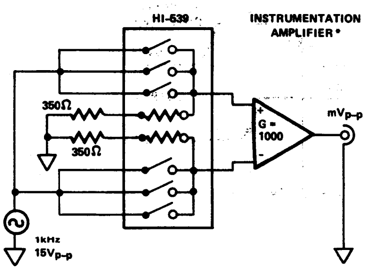
(SIMILAR CONNECTION FOR "B" SIDE)

TEST CIRCUIT
NO. 9

SINGLE-ENDED CROSSTALK


HI-539
INSTRUMENTATION
AMPLIFIER *
1kHz,
$15V_{p-p}$
G = 1000
mV_{p-p}
350 Ω

DIFFERENTIAL CROSSTALK


HI-539
INSTRUMENTATION
AMPLIFIER *
350Ω
350Ω
G = 1000
mV_{p-p}
1kHz
$15V_{p-p}$

* AD606 OR BB3630, FOR EXAMPLE

DEFINITIONS

CHARGE INJECTION – Charge (in pC) transferred, during a transition between channels, through the internal gate-to-channel capacitance. The resulting voltage error varies inversely with the output (or input) capacitance.

CROSSTALK – Signal at the multiplexer output, coupling though the C_{DS} capacitance of an OFF channel. Amplitude is proportional to source resistance for the ON channel. See Test Circuit # 9 for single-ended and differential versions of crosstalk.

DIFFERENTIAL LEAKAGE CURRENT ($\Delta I_S(OFF)$, $\Delta I_D(OFF)$, $\Delta I_D(ON)$) – The absolute difference in leakage for the two sides of a channel.

DIFFERENTIAL OFFSET VOLTAGE (ΔV_{OS}) – Voltage between the multiplexer output terminals with both channel input terminals shorted to ground.

DIFFERENTIAL ON RESISTANCE (ΔR_{ON}) – The absolute difference in On Resistance for the two sides of a channel.

INPUT TO OUTPUT CAPACITANCE (C_{DS}) – Capacitance from one input terminal of a channel to the corresponding output of the multiplexer. This parameter is responsible for Crosstalk.

APPLICATIONS

GENERAL

The HI-539 accepts inputs in the range -15V to +15V, with performance guaranteed over the ±10V range. At these higher levels of analog input voltage it is comparable to the HI-509, and is plug-in compatible with that device (as well as the HI-509A). However, as mentioned earlier, the HI-539 was designed to introduce minimum error when switching low level inputs.

Special care is required in working with these low level signals. The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded, differential signal path is essential, especially to maintain a noise level below 50 μVrms.

LOW LEVEL SIGNAL TRANSMISSION

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area, to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only one tenth as much leakage capacitance to ground per foot. A key requirement for the transmission cable is that it presents a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in phase to both conductors, and may be rejected as common mode voltage by a differential amplifier connected to the multiplexer output.

Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

Table 1

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 oz. Cu.)	D.C. RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				AT 60Hz	AT 10kHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.37μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

WATCH SMALL ΔV ERRORS

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12 bits or more.

Table 1 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values of inductance.)

As an example, suppose the HI-539 is feeding a 12 bit converter system with an allowable error of ±1/2 LSB (±1.22mV). If the interface logic draws 100mA from the 5V supply, this current will produce 1.28mV across 6 inches of #24 wire; more than the error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

PROVIDE PATH FOR I_{BIAS}

The input bias current for any DC-coupled amplifier must have an external path back to the amplifier's power supply. No such path exists in Figure 1A, and consequently the amplifer output will remain in saturation.

A single large resistor (1MΩ to 10MΩ) from either signal line to power supply common will provide the required path, but a resistor on each line is necessary to preserve accuracy. A single pair of these bias current resistors on the HI-539 output may be used if their loading effect can be tolerated (each forms a voltage divider with R_{ON}). Otherwise, a resistor pair on each input channel of the multiplexer is required. The use of bias current resistors is acceptable only if one is confident that the sum of signal plus common-mode voltage will remain within the input range of the multiplexer/amplifier combination.

Another solution is to simply run a third wire from the low side of the signal source, as in Figure 1B. This wire assures a low common-mode voltage as well as providing the path for bias currents. Making the connection near the multiplexer will save wire, but it will also unbalance the line and reduce the amplifier's common-mode rejection.

DIFFERENTIAL OFFSET, ΔV_{OS}

There are two major sources of ΔV_{OS}. That part, due to the expression ($R_{ON}\ \Delta I_D(ON) + I_D(ON)\ \Delta R_{ON}$) becomes significant with increasing temperature, as shown in the Electrical Characteristics section. The other source of offset is the thermocouple effects due to dissimilar materials in the signal path. These include silicon, aluminum, tin, nickel-iron and (often) gold, just to exit the package.

For the thermocouple effects in the package alone, the constraint on ΔV_{OS} may be stated in terms of a limit on the difference in temperature for package pins leading to any channel of the HI-539. For example, a difference of 0.13°C produces a 5μV offset. Obviously, this ΔT effect can dominate the ΔV_{OS} parameter at any temperature unless care is taken in mounting the HI-539 package.

Temperature gradients across the HI-539 package should be held to a minimum in critical applications. Locate the HI-539 far from heat producing components, with any air currents flowing lengthwise across the package.

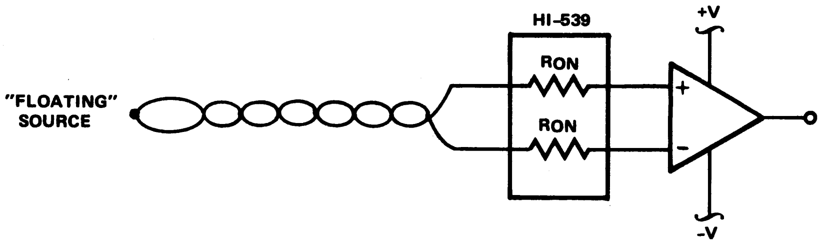

HI-539
+V
RON
RON
"FLOATING" SOURCE
+
-
-V

Figure 1A

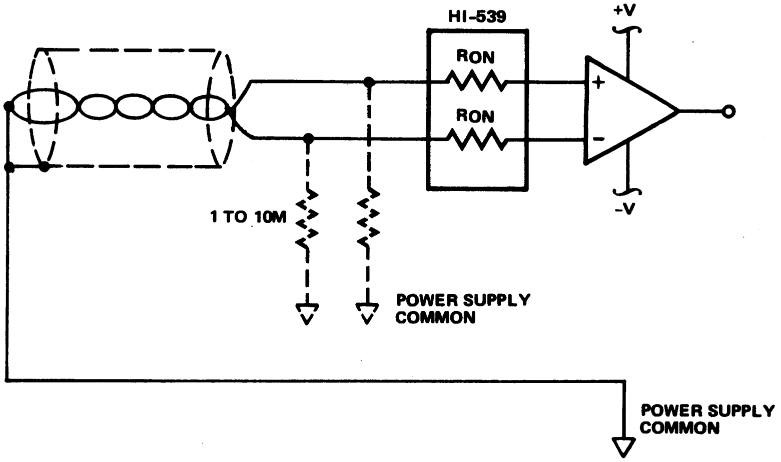

HI-539
+V
RON
RON
+
-
-V
1 TO 10M
POWER SUPPLY COMMON
POWER SUPPLY COMMON

Figure 1B

The amplifier in Figure 1A is unusable because its bias currents cannot return to the power supply. Figure 1B shows two alternative paths for these bias currents: either a pair of resistors, or (better) a third wire from the low side of the signal source.

DIE CHARACTERISTICS

Transistor Count		236
Die Size		92 x 100 mils
Thermal Constants	θ_{ja}	79°C/W
	θ_{jc}	26°C/W
Tie Substrate to:		$-V_{Supply}$
Process:		CMOS - DI

HARRIS

HI-546/547

Single 16/Differential 8 Channel CMOS Analog Multiplexer with Active Overvoltage Protection

Features

- **Analog Overvoltage Protection.........70 Vpp**
- **No Channel Interaction During Overvoltage**
- **ESD Resistant..................>4,000 Volts**
- **Guaranteed R_{ON} Matching**
- **44 V Maximum Power Supply**
- **Break-Before-Make Switching**
- **Analog Signal Range..................±15 V**
- **Access Time (Typical)................500 ns**
- **Standby Power (Typical)..............7.5 mW**

Applications

- **Data Acquisition**
- **Industrial Controls**
- **Telemetry**

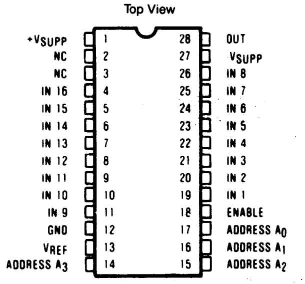
Description

The HI-546 and HI-547 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-546 and HI-547 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The 546 is a 16 channel device and the 547 is an 8 channel differential version. If input overvoltage protection is not needed, the HI-506 and HI-507 multiplexers are recommended. For further information see Application Notes 520 and 521.

The HI-546/547 are offered in both commercial and military grades. Additional Hi-Rel screening to MIL-STD-883 available, specified by the "/883" suffix. For details, see the separate "883" data sheet.

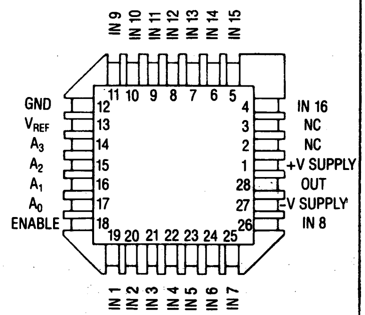
Each device is available in a 16 pin plastic or ceramic DIP, a 20 pin ceramic LCC or 20 pin plastic LCC (PLCC) package.

Pinouts



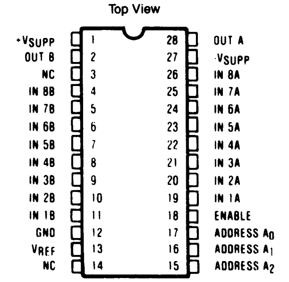
Top View
+VSUPP 1
NC 2
NC 3
IN 16 4
IN 15 5
IN 14 6
IN 13 7
IN 12 8
IN 11 9
IN 10 10
IN 9 11
GND 12
VREF 13
ADDRESS A3 14
28 OUT
27 VSUPP
26 IN 8
25 IN 7
24 IN 6
23 IN 5
22 IN 4
21 IN 3
20 IN 2
19 IN 1
18 ENABLE
17 ADDRESS A0
16 ADDRESS A1
15 ADDRESS A2

HI1-546 (ceramic)
HI3-546 (plastic)



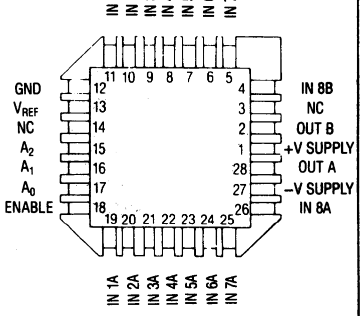
IN 9
IN 10
IN 11
IN 12
IN 13
IN 14
IN 15
11 10 9 8 7 6 5
GND 12
VREF 13
A3 14
A2 15
A1 16
A0 17
ENABLE 18
4 IN 16
3 NC
2 NC
1 +V SUPPLY
28 OUT
27 -V SUPPLY
26 IN 8
19 20 21 22 23 24 25
IN 1
IN 2
IN 3
IN 4
IN 5
IN 6
IN 7

HI4-546 (ceramic)
HI4P546 (plastic)



Top View
+VSUPP 1
OUT B 2
NC 3
IN 8B 4
IN 7B 5
IN 6B 6
IN 5B 7
IN 4B 8
IN 3B 9
IN 2B 10
IN 1B 11
GND 12
VREF 13
NC 14
28 OUT A
27 -VSUPP
26 IN 8A
25 IN 7A
24 IN 6A
23 IN 5A
22 IN 4A
21 IN 3A
20 IN 2A
19 IN 1A
18 ENABLE
17 ADDRESS A0
16 ADDRESS A1
15 ADDRESS A2

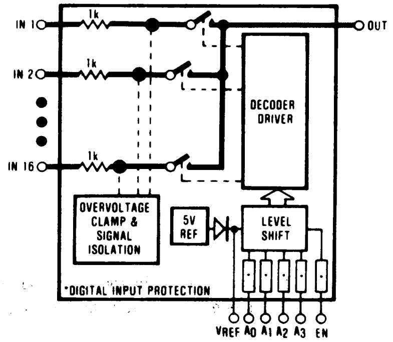
HI1-547 (ceramic)
HI3-547 (plastic)



IN 1B
IN 2B
IN 3B
IN 4B
IN 5B
IN 6B
IN 7B
11 10 9 8 7 6 5
GND 12
VREF 13
NC 14
A2 15
A1 16
A0 17
ENABLE 18
4 IN 8B
3 NC
2 OUT B
1 +V SUPPLY
28 OUT A
27 -V SUPPLY
26 IN 8A
19 20 21 22 23 24 25
IN 1A
IN 2A
IN 3A
IN 4A
IN 5A
IN 6A
IN 7A

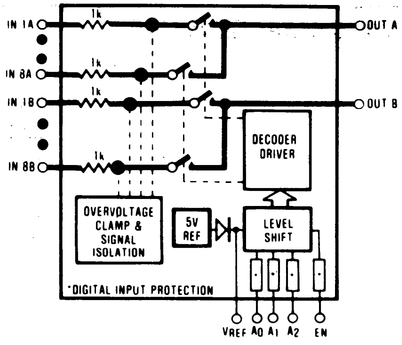
HI4-547 (ceramic)
HI4P547 (plastic)

Functional Diagrams



IN 1
IN 2
IN 16
1k
1k
1k
OUT
DECODER DRIVER
OVERVOLTAGE CLAMP & SIGNAL ISOLATION
5V REF
LEVEL SHIFT
*DIGITAL INPUT PROTECTION
VREF
A0
A1
A2
A3
EN

HI-546



IN 1A
IN 8A
IN 1B
IN 8B
1k
1k
1k
1k
OUT A
OUT B
DECODER DRIVER
OVERVOLTAGE CLAMP & SIGNAL ISOLATION
5V REF
LEVEL SHIFT
*DIGITAL INPUT PROTECTION
VREF
A0
A1
A2
EN

HI-547

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supply Pins	44 V
V_{REF} to Ground, V+ to Ground	22 V
V− to Ground	25 V
Digital Input Overvoltage:	
V_{EN}, V_A $V_{Supply}(+)$	+4 V
$V_{Supply}(-)$	−4 V
or 20 mA, whichever occurs first.	
Analog Input Overvoltage:	
V_S $V_{Supply}(+)$	+20 V
$V_{Supply}(-)$	−20 V

Continous Current, S or D:	20 mA
Peak Current, S or D (Pulsed at 1 msec, 10% duty cycle max):	40 mA
Power Dissipation* (Ceramic)	2.0 W
Operating Temperature Range:	
HI-546/547-2,	−55°C to +125°C
HI-546/547-4	−25°C to +85°C
HI-546/547-5	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

*Derate 20.0 mW/°C above $T_A = 75°C$

ELECTRICAL CHARACTERISTICS Unless Otherwise Specified:

Supplies = +15 V, −15 V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0 V; V_{AL} (Logic Level Low) = + 0.8 V. For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	HI-546/HI-547 −2			HI-546/547 −4, −5			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	−15		+15	−15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
$\triangle R_{ON}$, Any Two Channels	+25°C			7.0			7.0	%
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-546	Full			300			300	nA
HI-547	Full			200			200	nA
*I_D (OFF), with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				µA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-546	Full			300			300	nA
HI-547	Full			200			200	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-547 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold TTL Drive	Full			0.8			0.8	V
*V_{AH}, Input High Threshold (Note 8)	Full	4.0			4.0			V
V_{AL} MOS Drive (Note 9)	+25°C			0.8			0.8	V
V_{AH}	+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	µA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		0.5			0.5		µs
	Full			1.0			1.0	µs
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		µs
(0.01%)	+25°C		3.5			3.5		µs
"Off Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-546	+25°C		50			50		pF
HI-547	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current Pin 1 (Note 7)	Full		0.5	2.0		0.5	2.0	mA
*I−, Current Pin 27 (Note 7)	Full		0.02	1.0		0.02	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at −55°C.

TRUTH TABLES

HI-546

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-547

A_2	A_1	A_0	EN	ON CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

NOTES:

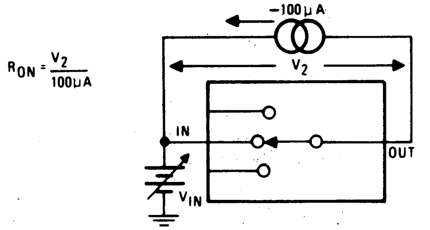
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. $V_{OUT} = \pm 10V$, $I_{OUT} = -100\ \mu A$.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33 V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1 nA at 25°C.
6. $V_{EN} = 0.8$ V, $R_L = 1$ K, $C_L = 15$ pF, $V_S = 7$ V_{RMS}, f = 100kHz Worst case isolation occurs on channel 8B due to proximity of the output pins.
7. V_{EN}, V_A = 0 V or 4.0 V.
8. To drive from DTL/TTL Circuits, 1 kΩ pull-up resistors to +5.0 V supply are recommended.
9. V_{REF} = +10 V.

Performance Characteristics and Test Circuits

Unless Otherwise Specified: T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V And V_{Ref} = Open.

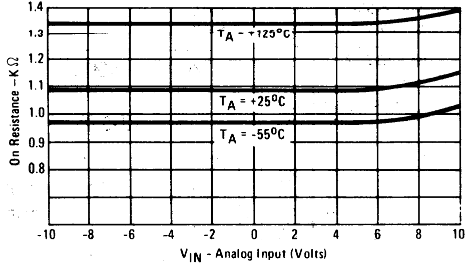
TEST CIRCUIT NO. 1

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

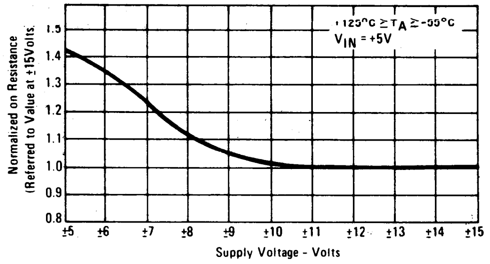


$R_{ON} = \frac{V_2}{100\mu A}$
−100 µ A
V_2
IN
OUT
V_{IN}

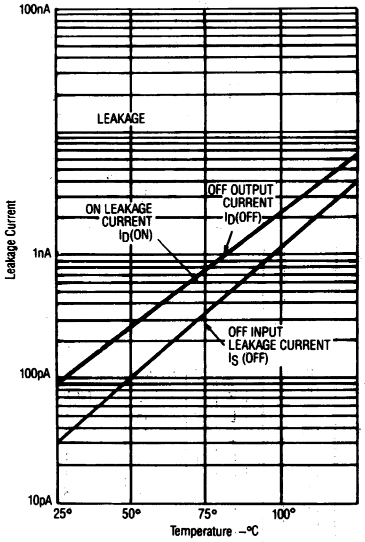
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



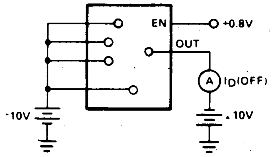
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



LEAKAGE CURRENT VS. TEMPERATURE

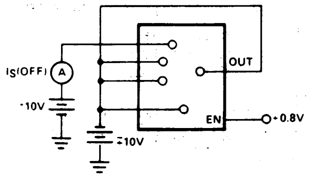


TEST CIRCUIT NO. 2*



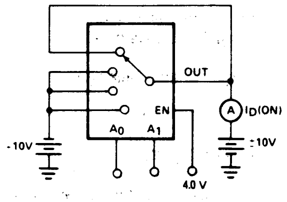
EN
+0.8V
OUT
A
I_D(OFF)
-10V
±10V

TEST CIRCUIT NO. 3*



I_S(OFF)
A
±10V
OUT
EN
+0.8V
±10V

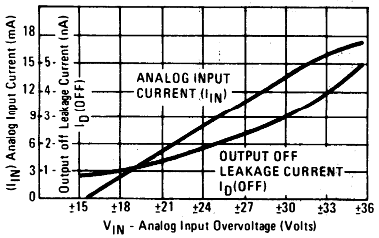
TEST CIRCUIT NO. 4*



OUT
EN
A_0
A_1
A
I_D(ON)
±10V
±10V
4.0 V

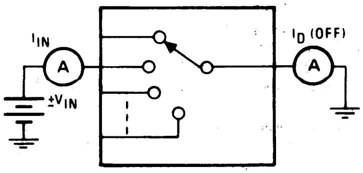
***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for I_D(OFF): +10 V/−10 V and −10 V/+10 V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



TEST CIRCUIT NO. 5

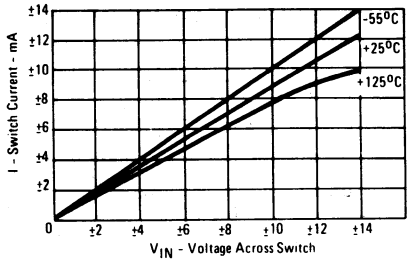
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



I_{IN}
A
±V_{IN}
I_D (OFF)
A

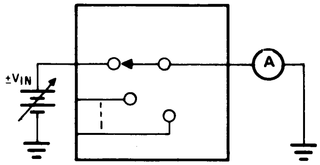
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

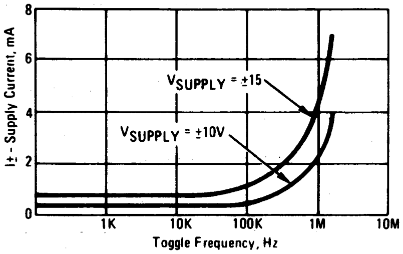


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

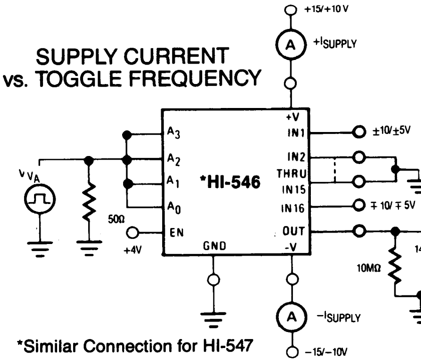


SUPPLY CURRENT vs. TOGGLE FREQUENCY



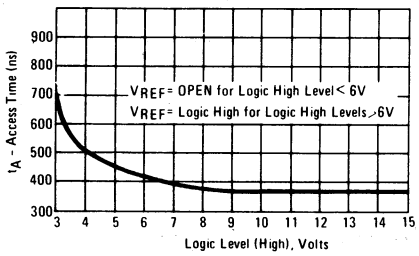
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY


+15/+10 V
A
+I_SUPPLY
+V
A3
IN1
±10/±5V
A2
IN2
A1
*HI-546
THRU
IN15
V_A
A0
IN16
∓10/∓5V
50Ω
EN
OUT
+4V
GND
-V
14 pF
10MΩ
A
-I_SUPPLY
-15/-10V

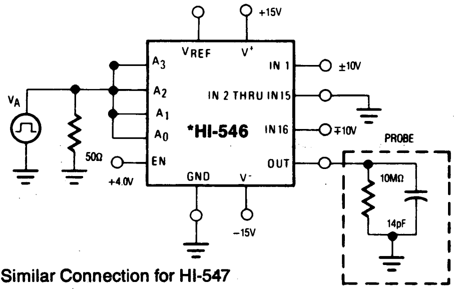
*Similar Connection for HI-547

ACCESS TIME VS. LOGIC LEVEL (HIGH)



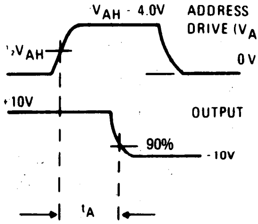
TEST CIRCUIT NO. 8

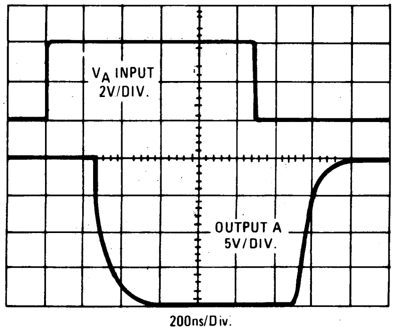
ACCESS TIME vs. LOGIC LEVEL (HIGH)


+15V
V_REF
V+
A3
IN 1
±10V
A2
IN 2 THRU IN 15
V_A
A1
A0
*HI-546
IN 16
∓10V
PROBE
50Ω
EN
OUT
+4.0V
GND
V-
10MΩ
14pF
-15V

*Similar Connection for HI-547

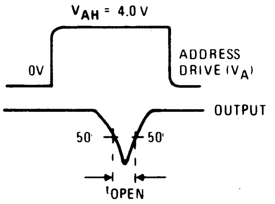
Switching Waveforms


V_AH = 4.0V
ADDRESS DRIVE (V_A)
½V_AH
0V
+10V
OUTPUT
90%
-10V
t_A

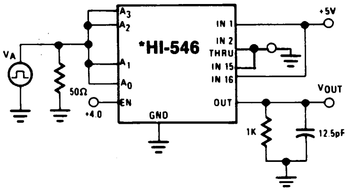


Switching Waveforms (continued)

TEST CIRCUIT NO. 9

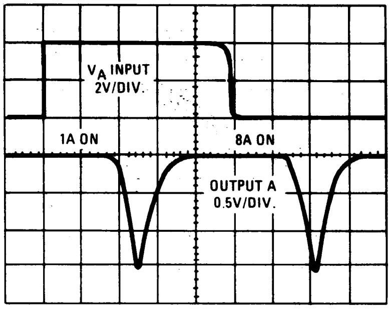

V_{AH} = 4.0 V
0V
ADDRESS DRIVE (V_A)
OUTPUT
50%
50%
t_{OPEN}

BREAK-BEFORE-MAKE DELAY (t_{OPEN})


A_3
A_2
A_1
A_0
EN
*HI-546
IN 1
IN 2 THRU IN 15
IN 16
OUT
GND
+5V
V_A
50Ω
+4.0
V_{OUT}
1K
12.5pF

*Similar Connection for HI-547

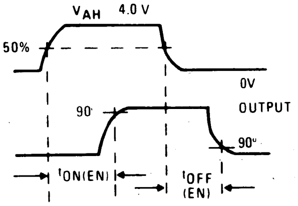
BREAK-BEFORE-MAKE DELAY(t_{OPEN})



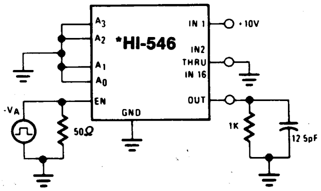
100ns/Div.

TEST CIRCUIT NO. 10

ENABLE DRIVE

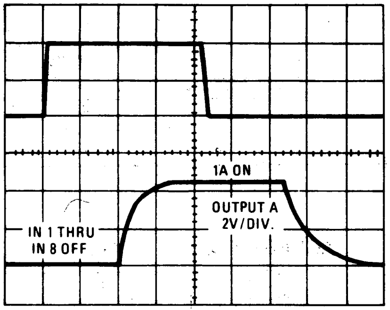

V_{AH} 4.0 V
50%
0V
90%
OUTPUT
90%
$t_{ON(EN)}$
$t_{OFF(EN)}$

ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)


A_3
A_2
A_1
A_0
EN
*HI-546
IN 1
IN2 THRU IN 16
OUT
GND
+10V
$-V_A$
50Ω
1K
12.5pF

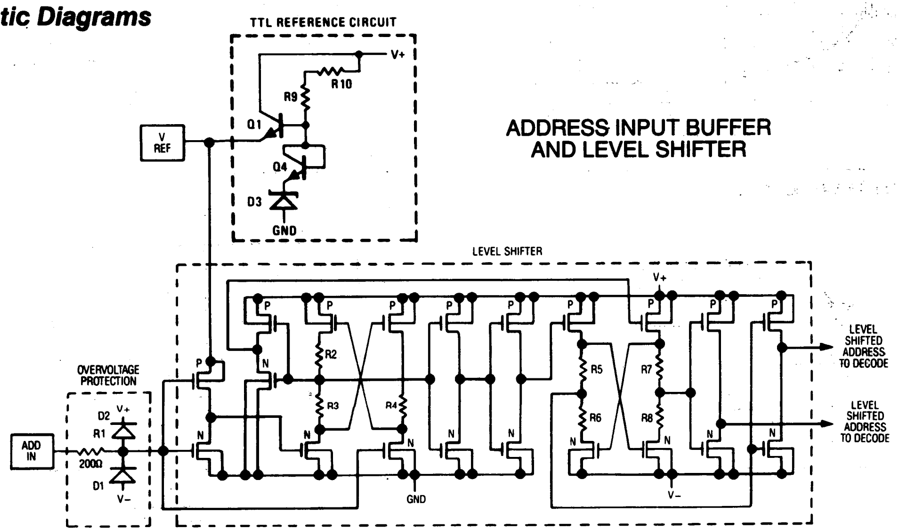
*Similar Connection for HI-547

ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)



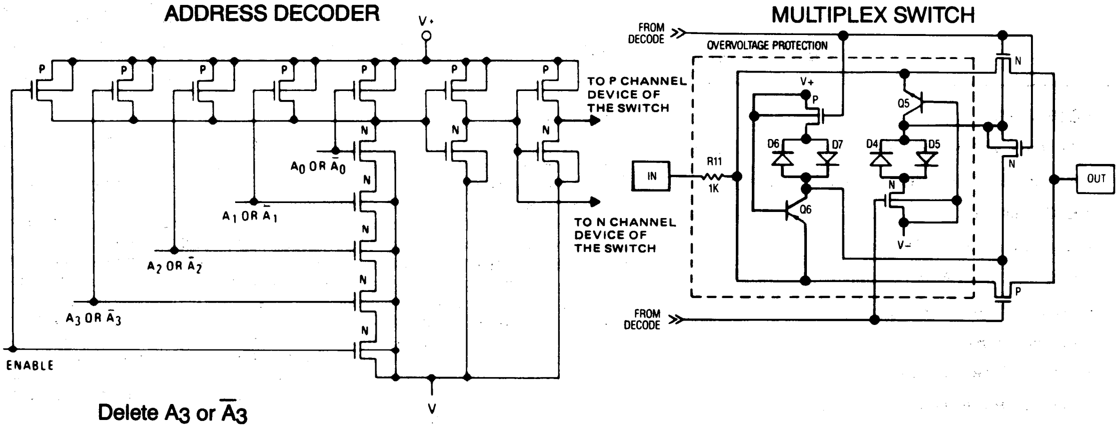
100ns/Div.

Schematic Diagrams


TTL REFERENCE CIRCUIT
V+
R10
R9
Q1
Q4
D3
GND
V REF
LEVEL SHIFTER
V+
P
N
R2
R3
R4
R5
R6
R7
R8
GND
V−
LEVEL SHIFTED ADDRESS TO DECODE
LEVEL SHIFTED ADDRESS TO DECODE
OVERVOLTAGE PROTECTION
D2
R1
200Ω
D1
V+
V−
ADD IN

ADDRESS INPUT BUFFER AND LEVEL SHIFTER

Schematic Diagrams (continued)


ADDRESS DECODER
V+
P
N
A_0 OR $\bar{A}_0$
A_1 OR $\bar{A}_1$
A_2 OR $\bar{A}_2$
A_3 OR $\bar{A}_3$
ENABLE
TO P CHANNEL DEVICE OF THE SWITCH
TO N CHANNEL DEVICE OF THE SWITCH
V
MULTIPLEX SWITCH
FROM DECODE
OVERVOLTAGE PROTECTION
V+
P
Q5
D6
D7
D4
D5
IN
R11
1K
N
Q6
V-
OUT
FROM DECODE

Delete A_3 or $\bar{A}_3$
Input for HI-547

Die Characteristics

Transistor Count		485	
Die Size		161 x 85 mils	
Thermal Constants	θja	50°C/W	For Ceramic Dip
	θjc	18°C/W	
Tie Substrate to:		−VSupply	
Process:		CMOS-DI	

HI-548/549

Single 8/Differential 4 Channel
CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- **Analog Overvoltage Protection . . . . 70 Vpp**
- **No Channel Interaction During Overvoltage**
- **ESD Resistant . . . . >4,000 Volts**
- **Guaranteed R_{ON} Matching**
- **44 V Maximum Power Supply**
- **Break-Before-Make Switching**
- **Analog Signal Range . . . . ±15 V**
- **Access Time (Typical) . . . . 500 ns**
- **Standby Power (Typical) . . . . 7.5 mW**

Applications

- **Data Acquisition**
- **Industrial Controls**
- **Telemetry**

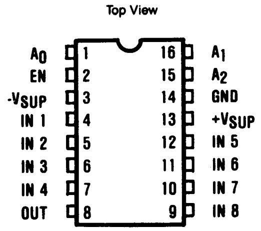
Description

The HI-548 and 549 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-548 and HI-549 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The 548 is an 8 channel device and the 549 is a 4 channel differential version. If input overvoltage protection is not needed, the HI-508 and HI-509 multiplexers are recommended. For further information see Application Notes 520 and 521.

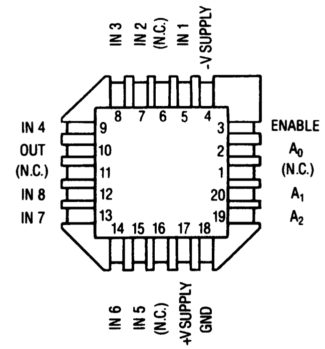
The HI-548/549 are offered in both commercial and military grades. Addition Hi-Rel screening to MIL-STD-883 available, specified by the "/883" suffix. For details, see the separate "883" data sheet.

Each device is available in a 16 pin plastic or ceramic DIP, a 20 pin ceramic LCC or 20 pin plastic LCC (PLCC) package.

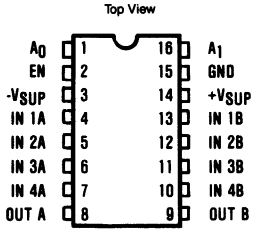
Pinouts


Top View
A0 1
EN 2
-VSUP 3
IN 1 4
IN 2 5
IN 3 6
IN 4 7
OUT 8
16 A1
15 A2
14 GND
13 +VSUP
12 IN 5
11 IN 6
10 IN 7
9 IN 8

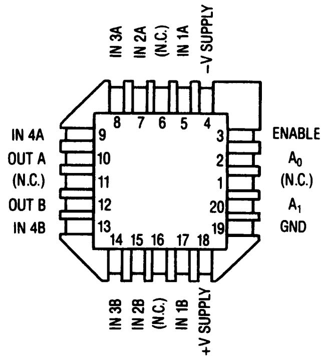
HI1-548 (ceramic)
HI3-548 (plastic)


IN 3
IN 2
(N.C.)
IN 1
-V SUPPLY
8 7 6 5 4
IN 4 9
OUT 10
(N.C.) 11
IN 8 12
IN 7 13
3 ENABLE
2 A0
1 (N.C.)
20 A1
19 A2
14 15 16 17 18
IN 6
IN 5
(N.C.)
+V SUPPLY
GND

HI4-548 (ceramic)
HI4P548 (plastic)

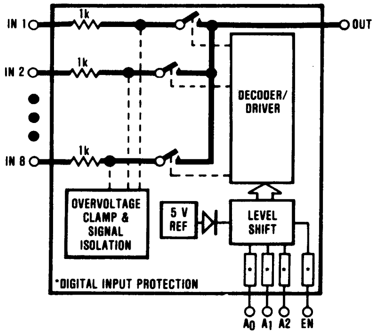

Top View
A0 1
EN 2
-VSUP 3
IN 1A 4
IN 2A 5
IN 3A 6
IN 4A 7
OUT A 8
16 A1
15 GND
14 +VSUP
13 IN 1B
12 IN 2B
11 IN 3B
10 IN 4B
9 OUT B

HI1-549 (ceramic)
HI3-549 (plastic)

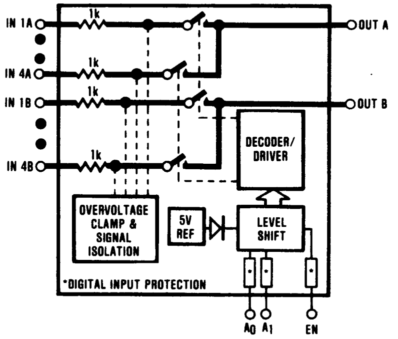

IN 3A
IN 2A
(N.C.)
IN 1A
-V SUPPLY
8 7 6 5 4
IN 4A 9
OUT A 10
(N.C.) 11
OUT B 12
IN 4B 13
3 ENABLE
2 A0
1 (N.C.)
20 A1
19 GND
14 15 16 17 18
IN 3B
IN 2B
(N.C.)
IN 1B
+V SUPPLY

HI4-549 (ceramic)
HI4P549 (plastic)

Functional Diagrams


IN 1
1k
OUT
IN 2
1k
DECODER/ DRIVER
IN 8
1k
OVERVOLTAGE CLAMP & SIGNAL ISOLATION
5 V REF
LEVEL SHIFT
*DIGITAL INPUT PROTECTION
A0 A1 A2 EN

HI-548


IN 1A
1k
OUT A
IN 4A
1k
IN 1B
1k
OUT B
DECODER/ DRIVER
IN 4B
1k
OVERVOLTAGE CLAMP & SIGNAL ISOLATION
5V REF
LEVEL SHIFT
*DIGITAL INPUT PROTECTION
A0 A1 EN

HI-549

HI-548/549 Specifications

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between Supply Pins	44 V
V+ to Ground	22 V
V− to Ground	22 V

Digital Input Overvoltage:

$V_{EN}, V_A \begin{cases} V_{Supply}(+) & +4\text{ V} \\ V_{Supply}(-) & -4\text{ V} \end{cases}$

or 20 mA, whichever occurs first.

Analog Input Overvoltage:

$V_S \begin{cases} V_{Supply}(+) & +20\text{ V} \\ V_{Supply}(-) & -20\text{ V} \end{cases}$

Continuous Current, S or D:	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max):	40 mA
Power Dissipation* (Ceramic)	1.28 W
Operating Temperature Range:	
HI-548/549-2,	−55°C to +125°C
HI-548/549-4	−25°C to +85°C
HI-548/549-5	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

*Derate 12.8 mW/°C above T_A =75°C

ELECTRICAL CHARACTERISTICS

Supplies= +15 V, −15 V; V_{AH}(Logic Level High) = +4.0 V, V_{AL}(Logic Level Low) = +0.8 V. (unless otherwise spcified).
For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-548/HI-549 -2 MIN.	TYP.	MAX.	HI-548/549 -4, -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	−15		+15	−15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
ΔR_{ON}, Any Two Channels	+25°C			7.0			7.0	%
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-548	Full			200			200	nA
HI-549	Full			100			100	nA
*$I_{D(OFF)}$ with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				µA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-548	Full			200			200	nA
HI-549	Full			100			100	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-549 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold (Note 8)	Full			0.8			0.8	V
*V_{AH},, Input High Threshold	Full	4.0			4.0			V
*I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	µA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		0.5			0.5		µs
	Full			1.0			1.0	µs
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		µs
(0.01%)	+25°C		3.5			3.5		µs
"OFF Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-548	+25°C		25			25		pF
HI-549	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current (Note 7)	Full		0.5	2.0		0.5	2.0	mA
*I−, Current (Note 7)	Full		0.02	1.0		0.02	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at −55°C.

TRUTH TABLES

HI-548

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-549

A_1	A_0	EN	ON CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2.
H	L	H	3
H	H	H	4

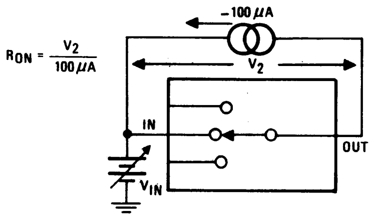
NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -100µA.
3. 10nA is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
6. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = 7V_{RMS}, f = 100kHz. Worst case isolation occurs on channel 4 due to proximity of the output pins.
7. V_{EN}, V_A = 0V or 4.0V.
8. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.

Performance Characteristics and Test Circuits

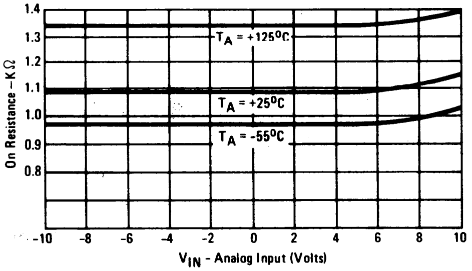
Unless Otherwise Specified T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V

TEST CIRCUIT NO. 1

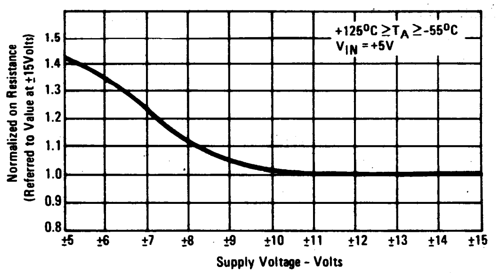
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE


-100 μA
$R_{ON} = \frac{V_2}{100\mu A}$
V_2
IN
OUT
V_{IN}

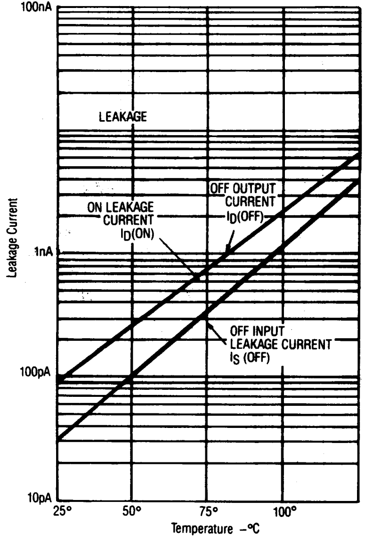
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



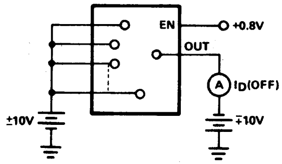
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



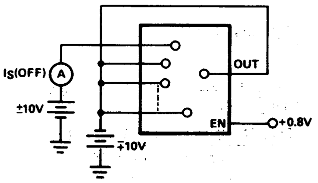
LEAKAGE CURRENT VS. TEMPERATURE



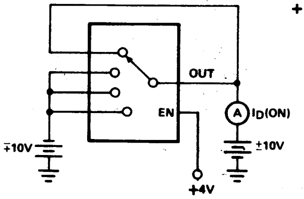
TEST CIRCUIT NO. 2*


EN
+0.8V
OUT
A
I_D(OFF)
±10V
∓10V

TEST CIRCUIT NO. 3*

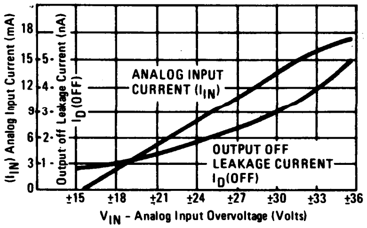

I_S(OFF)
A
±10V
OUT
EN
+0.8V
∓10V

TEST CIRCUIT NO. 4*


OUT
EN
A
I_D(ON)
∓10V
±10V
+4V

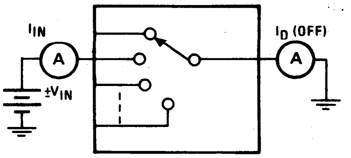
***Two measurements per channel: +10 V/–10 V and –10 V/+10 V. (Two measurements per device for I_D(OFF): +10 V/–10 V and –10 V/+10 V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



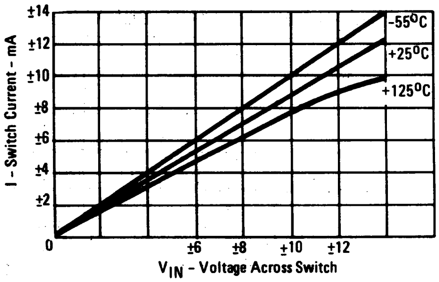
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS


I_{IN}
A
±V_{IN}
I_D (OFF)
A

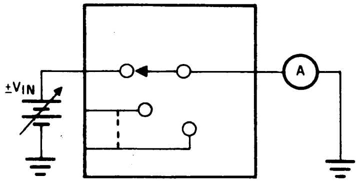
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

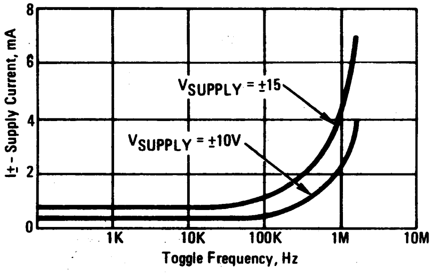


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

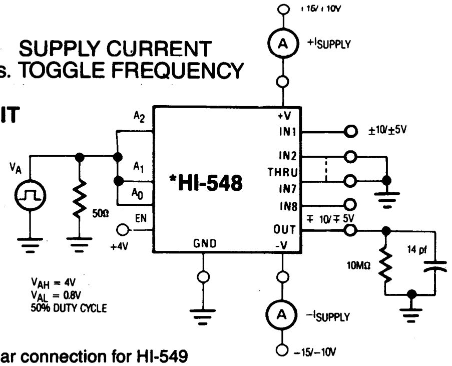


SUPPLY CURRENT vs. TOGGLE FREQUENCY



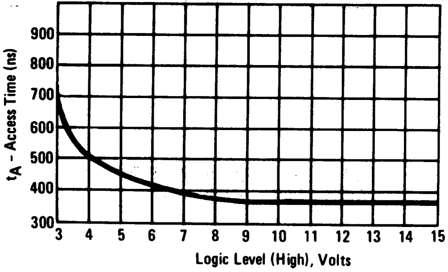
SUPPLY CURRENT vs. TOGGLE FREQUENCY

TEST CIRCUIT NO. 7


+15/+10V
A
$+I_{SUPPLY}$
A_2
A_1
A_0
V_A
50Ω
EN
+4V
*HI-548
+V
IN1
IN2
THRU
IN7
IN8
OUT
-V
GND
±10/±5V
∓ 10/∓ 5V
14 pf
10MΩ
V_{AH} = 4V
V_{AL} = 0.8V
50% DUTY CYCLE
A
$-I_{SUPPLY}$
-15/-10V

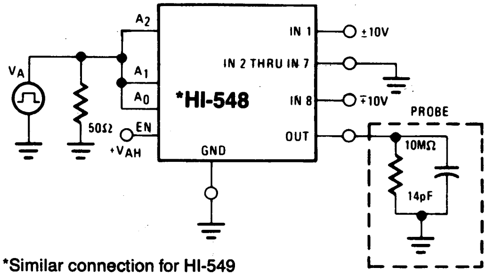
*Similar connection for HI-549

ACCESS TIME VS. LOGIC LEVEL (HIGH)



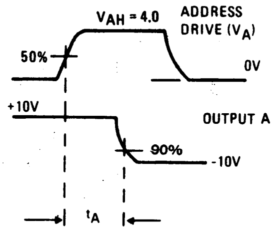
TEST CIRCUIT NO. 8

ACCESS TIME vs. LOGIC LEVEL (HIGH)

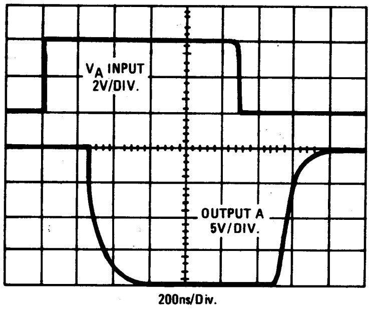

A_2
A_1
A_0
V_A
50Ω
EN
$+V_{AH}$
*HI-548
IN 1
IN 2 THRU IN 7
IN 8
OUT
GND
±10V
∓10V
PROBE
10MΩ
14pF

*Similar connection for HI-549

Switching Waveforms

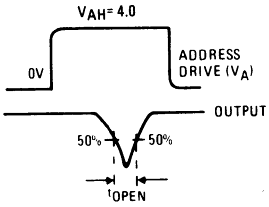

V_{AH} = 4.0
ADDRESS DRIVE (V_A)
50%
0V
+10V
OUTPUT A
90%
-10V
t_A

ACCESS TIME

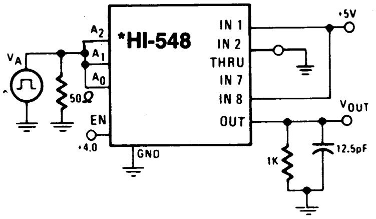


Switching Waveforms (continued)

TEST CIRCUIT NO. 9

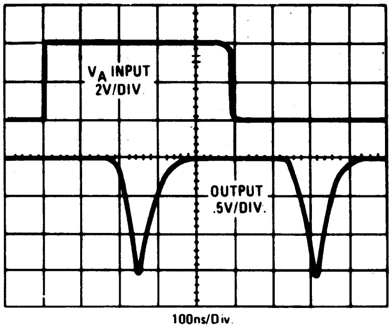

V_{AH}= 4.0
0V
ADDRESS DRIVE (V_A)
OUTPUT
50%
50%
t_{OPEN}

BREAK-BEFORE-MAKE DELAY(t_{OPEN})


*HI-548
A_2
A_1
A_0
V_A
50Ω
EN
+4.0
GND
IN 1
IN 2
THRU
IN 7
IN 8
OUT
+5V
V_{OUT}
12.5pF
1K

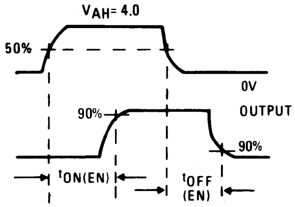
*Similar connection for HI-549

BREAK-BEFORE-MAKE DELAY (t_{OPEN})

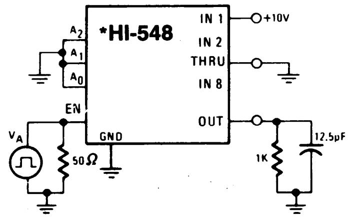


TEST CIRCUIT NO. 10

ENABLE DRIVE

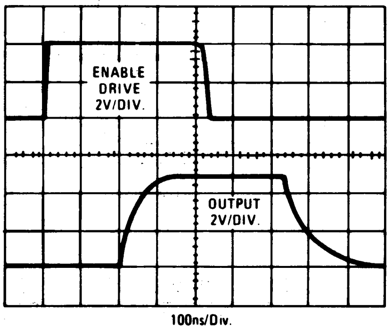

V_{AH}= 4.0
50%
0V
OUTPUT
90%
90%
$t_{ON(EN)}$
$t_{OFF(EN)}$

ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)


*HI-548
A_2
A_1
A_0
EN
V_A
50Ω
GND
IN 1
+10V
IN 2
THRU
IN 8
OUT
12.5pF
1K

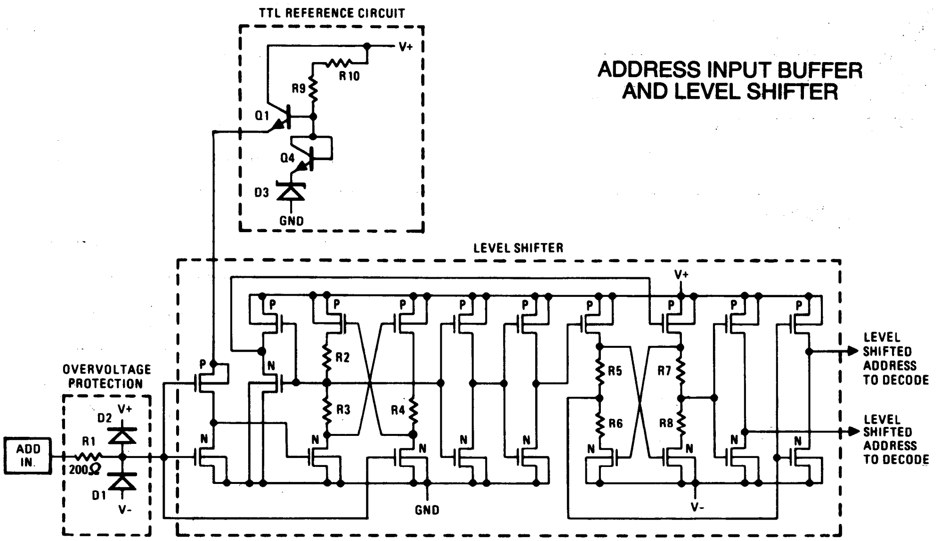
*Similar connection for HI-549

ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)

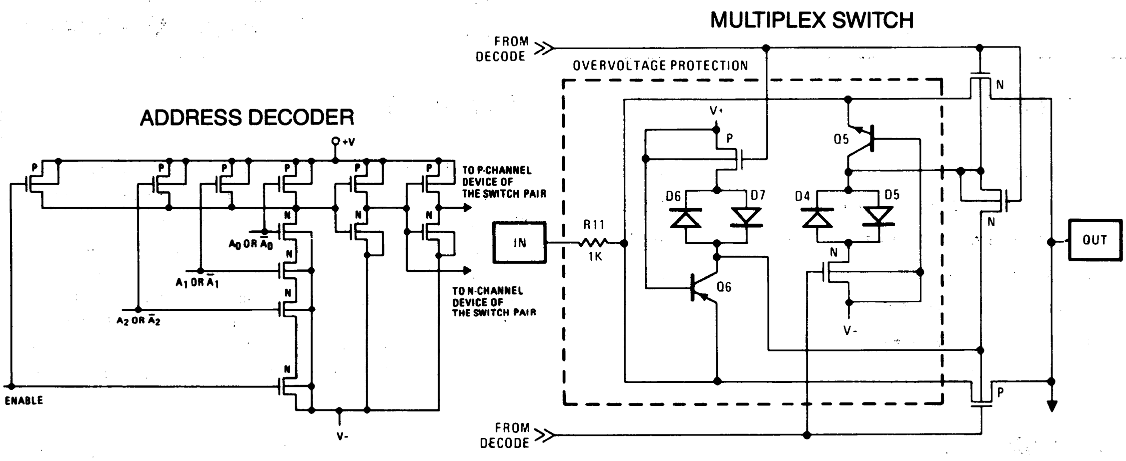


Schematic Diagrams

ADDRESS INPUT BUFFER AND LEVEL SHIFTER


TTL REFERENCE CIRCUIT
V+
R10
R9
Q1
Q4
D3
GND
LEVEL SHIFTER
V+
OVERVOLTAGE PROTECTION
ADD IN.
R1
200Ω
D2
D1
V+
V-
P
N
R2
R3
R4
R5
R6
R7
R8
GND
V-
LEVEL SHIFTED ADDRESS TO DECODE
LEVEL SHIFTED ADDRESS TO DECODE

Schematic Diagrams (continued)


ADDRESS DECODER
+V
P
P
P
P
P
P
N
N
N
N
N
N
N
TO P-CHANNEL DEVICE OF THE SWITCH PAIR
TO N-CHANNEL DEVICE OF THE SWITCH PAIR
A0 OR Ā0
A1 OR Ā1
A2 OR Ā2
ENABLE
V-
MULTIPLEX SWITCH
FROM DECODE
OVERVOLTAGE PROTECTION
V+
P
Q5
D6
D7
D4
D5
N
Q6
V-
IN
R11
1K
N
N
OUT
P
FROM DECODE

Die Characteristics

Transistor Count		253	
Die Size		116 x 79 mil	
Thermal Constants	θ_{ja}	78°C/W	For Ceramic Dip
	θ_{jc}	25°C/W	
Tie Substrate to:		$-V_{Supply}$	
Process:		CMOS - DI	

HARRIS

HI-1818A/1828A

Low Resistance Single 8/Differential 4 Channel CMOS Analog Multiplexers

FEATURES

• SIGNAL RANGE	±15V
• "ON" RESISTANCE (TYP.)	250Ω
• INPUT LEAKAGE AT +125°C (TYP.)	20nA
• ACCESS TIME (TYP.)	350ns
• POWER CONSUMPTION (TYP.)	5mW
• DTL/TTL COMPATIBLE ADDRESS	
• -55°C to +125°C OPERATION	

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

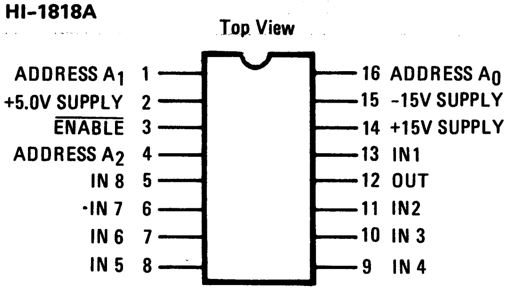
The HI-1818A/1828A are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250 Ω) assure optimum performance in low level or current mode applications.

The 1818A is a single-ended 8 channel multiplexer, while the HI-1828A is a differential 4 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

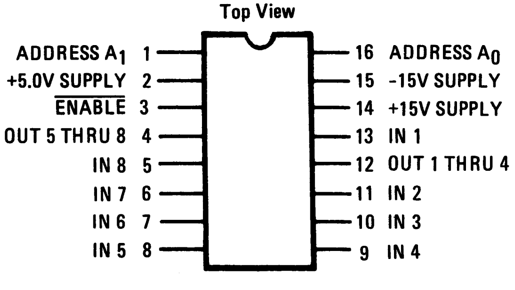
The HI-1818A/1828A is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

PINOUT

HI-1818A

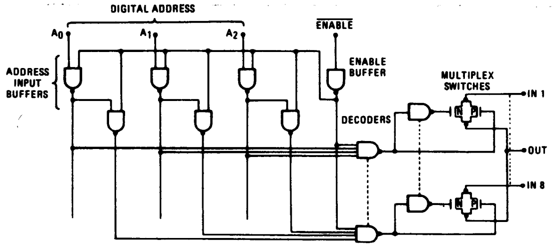

Top View
ADDRESS A1 1
+5.0V SUPPLY 2
ENABLE 3
ADDRESS A2 4
IN 8 5
IN 7 6
IN 6 7
IN 5 8
16 ADDRESS A0
15 -15V SUPPLY
14 +15V SUPPLY
13 IN1
12 OUT
11 IN2
10 IN 3
9 IN 4

HI-1828A

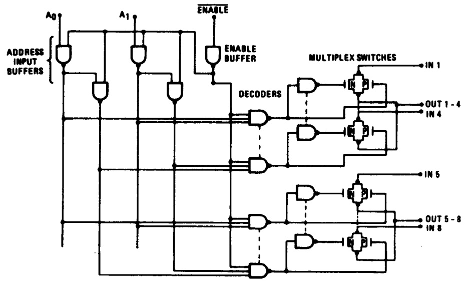

Top View
ADDRESS A1 1
+5.0V SUPPLY 2
ENABLE 3
OUT 5 THRU 8 4
IN 8 5
IN 7 6
IN 6 7
IN 5 8
16 ADDRESS A0
15 -15V SUPPLY
14 +15V SUPPLY
13 IN 1
12 OUT 1 THRU 4
11 IN 2
10 IN 3
9 IN 4

FUNCTIONAL DIAGRAM

HI-1818A


DIGITAL ADDRESS
A0
A1
A2
ENABLE
ADDRESS INPUT BUFFERS
ENABLE BUFFER
MULTIPLEX SWITCHES
DECODERS
IN 1
OUT
IN 8

HI-1828A


A0
A1
ENABLE
ADDRESS INPUT BUFFERS
ENABLE BUFFER
MULTIPLEX SWITCHES
DECODERS
IN 1
OUT 1 - 4
IN 4
IN 5
OUT 5 - 8
IN 8

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage Between Pins 14 and 15	40.0V
Logic Supply Voltage, Pin 2	30.0V
Analog Input Voltage: V^{+}_{Supply} +2V	
V^{-}_{Supply} -2V	
Digital Input Voltage	V-Supply to V+ Supply
Total Power Dissipation (Note 2)*	1.11W
Storage Temperature Range	-65°C to +150°C

*Derate 11.1mW/°C above 75°C for ceramic package.

ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V, +5V

PARAMETER	TEMP.	HI-1818A-2/1828A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-1818A-5/1828A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_{IN}, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, ON Resistance (Note 3)	+25°C		250	400		250	400	Ω
	Full		300	500		300	500	Ω
*I_S(OFF), Input Leakage Current	Full		20	50		20	50	nA
*I_D(ON), On Channel Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
I_D(OFF) Output Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.4			0.4	V
V_{AH}, Input High Threshold (Note 4)	Full	4.0			4.0			V
I_A, Input Leakage Current	Full		.01	1		.01	1	μA
SWITCHING CHARACTERISTICS								
T_S, Access Time (Note 5)	+25°C		350	500		350		ns
	Full			1000			1000	
Break-Before-Make Delay	+25°C		100			100		ns
Settling Time (0.1%)	+25°C		1.08			1.08		μs
(0.025%)	+25°C		2.8			2.8		μs
C_{IN}, Channel Input Capacitance	+25°C		4			4		pF
C_{OUT}, Channel Output Capacitance								
(HI-1818A)	+25°C		20			20		pF
(HI-1828A)	+25°C		10			10		pF
C_{DS}(OFF), Drain-To-Source Capacitance	+25°C		0.6			0.6		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
t_{ON}(EN), Enable delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OFF}(EN), Enable delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		5			5		mW
*I_+, Current Pin 14	Full		0.1	0.5		0.1	0.5	mA
*I_-, Current Pin 15	Full		0.3	1		0.3	1	mA
*I_L, Current Pin 2	Full		0.3	1		0.3	1	mA

NOTES:
1. Voltage ratings apply when voltages at all other pins are within their normal operating ranges.
2. Derate 11.1mW/°C above 75°C
3. V_{OUT} = ± 10V, I_{OUT} = -1mA.
4. To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.
5. Time measured to 90% of final output level; V_{OUT} = -5.0V to +5.0V, Digital Inputs = 0V to +4.0V.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-1818A

ADDRESS A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	NONE

HI-1828A

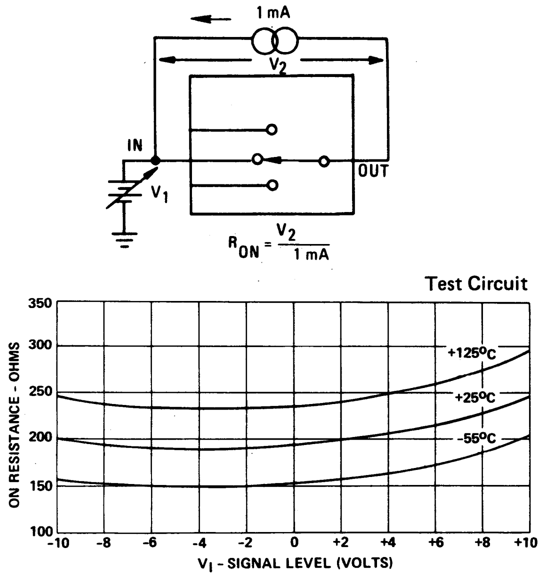
ADDRESS A_1	A_0	$\overline{EN}$	"ON" CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE

DIE CHARACTERISTICS

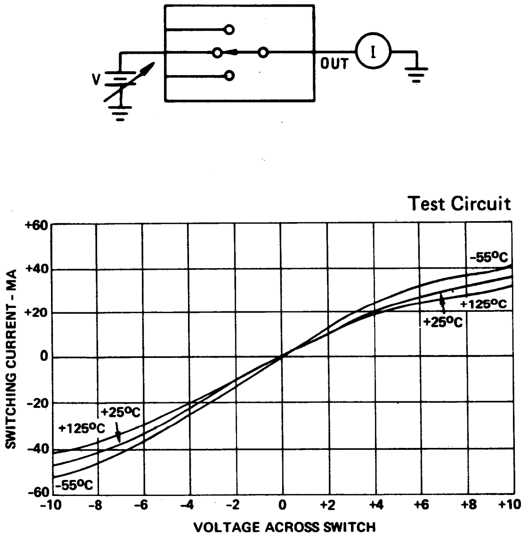
Transistor Count		210	
Die Size		68.5 x 104 mils	
Thermal Constants	θ_{ja}	90°C/W	For Ceramic DIP
	θ_{jc}	36°C/W	For Ceramic DIP
Tie Substrate to:		$-V_{Supply}$	
Process:		CMOS - DI	

PERFORMANCE CHARACTERISTICS

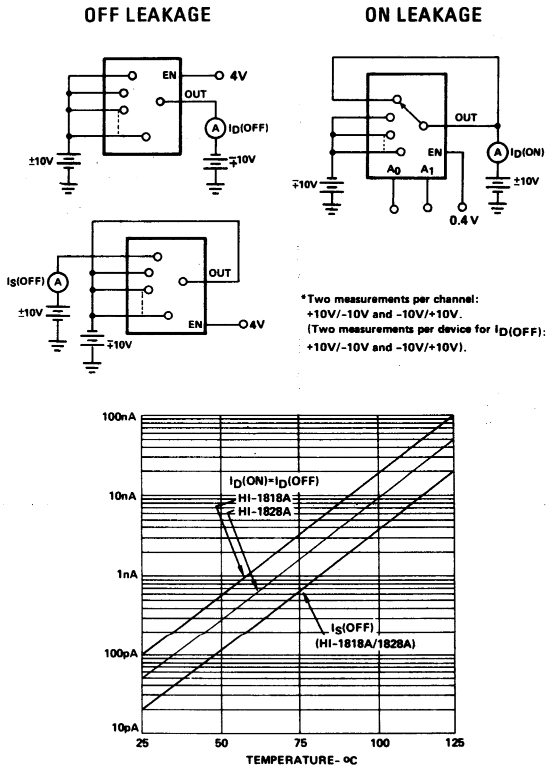
ON RESISTANCE vs. ANALOG SIGNAL LEVEL



ON CHANNEL CURRENT vs. VOLTAGE

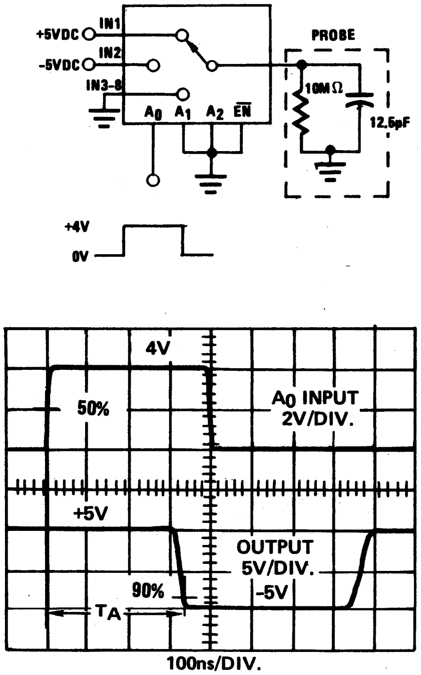


LEAKAGE CURRENTS vs. TEMPERATURE



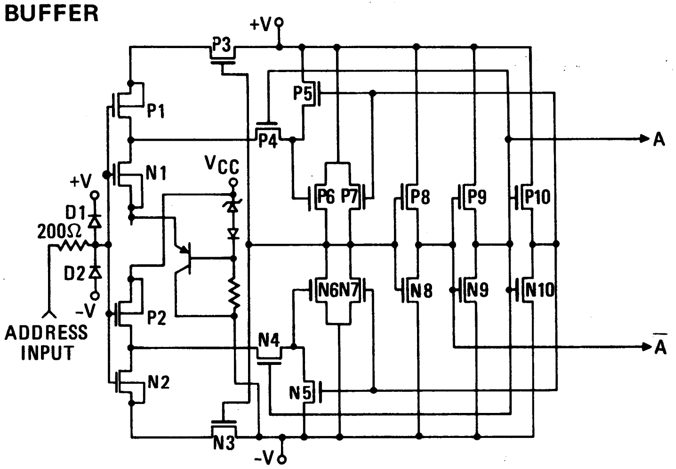
*Two measurements per channel: +10V/-10V and -10V/+10V.
(Two measurements per device for I_D(OFF): +10V/-10V and -10V/+10V).

ACCESS TIME



SCHEMATIC DIAGRAM

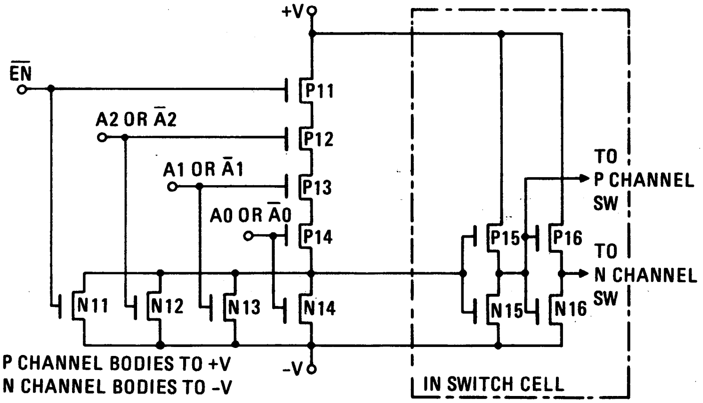
ADDRESS INPUT BUFFER


+V
P3
P1
P5
P4
A
N1
VCC
+V
D1
200Ω
D2
-V
ADDRESS INPUT
P6 P7
P8
P9
P10
N6N7
N8
N9
N10
P2
N4
Ā
N2
N5
N3
-V

ALL N-CHANNEL BODIES TO V-

ALL P-CHANNEL BODIES TO V+ UNLESS OTHERWISE INDICATED.

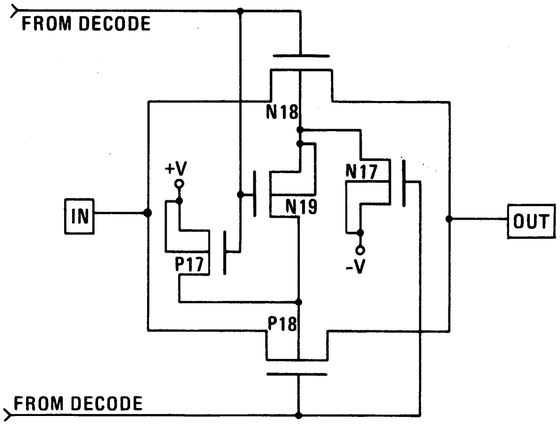
DECODER GATE


+V
EN
P11
A2 OR Ā2
P12
A1 OR Ā1
P13
A0 OR Ā0
P14
TO P CHANNEL SW
P15
P16
TO N CHANNEL SW
N11
N12
N13
N14
N15
N16
-V
IN SWITCH CELL

P CHANNEL BODIES TO +V
N CHANNEL BODIES TO -V

A2 OR Ā2 NOT USED
FOR HI-1828A

MULTIPLEX SWITCH


FROM DECODE
N18
+V
N17
N19
IN
OUT
P17
-V
P18
FROM DECODE

HARRIS

HY-9595/96

ADVANCE INFORMATION

Programmable Gain Amplifier with Multiplexed Inputs

Features

- 12 Bit Accuracy
- Digital Controlled Gain and Input Channel Selection
- Internal Latches for Channel and Gain Select Bits
- Non-Inverting Amplifier Gains ..... +1, +2, +4 and +8
- Gain Error 0.01%
- Channel-to-Channel Settling Time max 13μS
  typ 9μS
- Input Overvoltage Protection continuous ... Vsupply + 20V
  transient 2000V
- Low Power Dissipation 190mW
- Amplifier Offset Adjustment
- Compact 32 Pin DIP
- Compatible with 12 Bit A/D Converters (HI-574A, 674A, etc.) and Sampling A/D Converters (HY-9574, 9674, 9474, etc.)
- Available Temperature Ranges:
  Commercial (−5) .... 0°C to +75°C
  Industrial (−9) .... −40°C to +85°C
  Military (−2) .... −55°C to +125°C

HY-9595 Features

- 8 Differential Input Channels

HY-9596

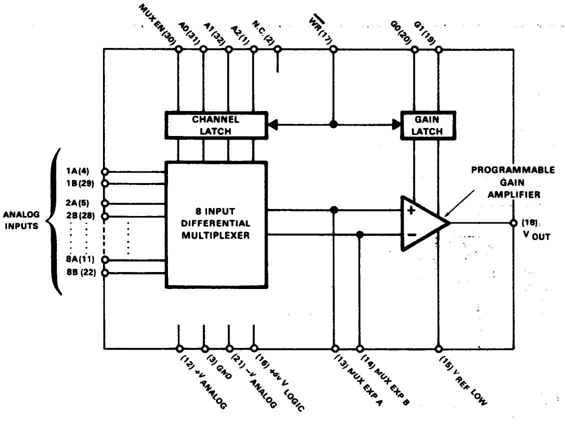
- 16 Pseudo-Differential/Single Ended Input Channels

Applications

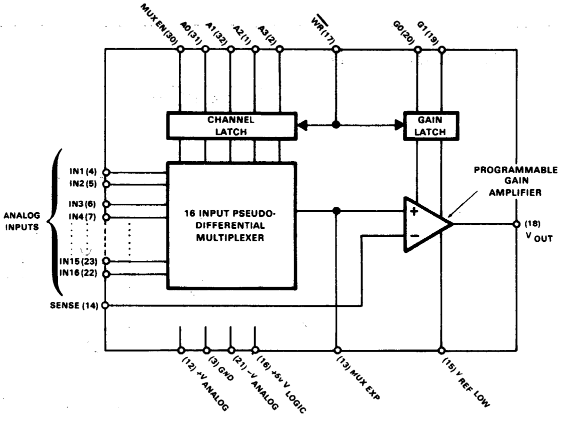
- Process Control Systems
- Status Monitoring Systems
- Multi-Channel High Reliability Data Acquisition Systems
- Industrial and Scientific Instrumentation
- Military Systems

Functional Diagram

HY-9595


MUX EN(30)
A0(31)
A1(32)
A2(1)
N.C.(2)
$\overline{WR}$(17)
G0(20)
G1(19)
CHANNEL LATCH
GAIN LATCH
ANALOG INPUTS
1A(4)
1B(29)
2A(5)
2B(28)
8A(11)
8B (22)
8 INPUT DIFFERENTIAL MULTIPLEXER
PROGRAMMABLE GAIN AMPLIFIER
+
−
(18) V OUT
(12) +V ANALOG
(3) GND
(21) −V ANALOG
(16) +5v V LOGIC
(13) MUX EXP A
(14) MUX EXP B
(15) V REF LOW

HY-9596


MUX EN(30)
A0(31)
A1(32)
A2(1)
A3(2)
$\overline{WR}$(17)
G0(20)
G1(19)
CHANNEL LATCH
GAIN LATCH
ANALOG INPUTS
IN1(4)
IN2(5)
IN3(6)
IN4(7)
IN15(23)
IN16(22)
SENSE (14)
16 INPUT PSEUDO-DIFFERENTIAL MULTIPLEXER
PROGRAMMABLE GAIN AMPLIFIER
+
−
(18) V OUT
(12) +V ANALOG
(3) GND
(21) −V ANALOG
(16) +5v V LOGIC
(13) MUX EXP
(15) V REF LOW

Description

The HY-9595/9596 is a high performance Programmable Gain Amplifier with multiplexed inputs. The amplifier gain and the input channel are selected digitally, and can be controlled through hardware or software. Internal registers latch the digital control bits, eliminating the need for external latches. This part connects multiple analog inputs to data acquisition systems.

The HY-9595 provides eight (8) pairs of multiplexed differential inputs.

The HY-9596 provides sixteen (16) single-ended (pseudo differential) multiplexed inputs.

Multiplexer Section

The analog Input Multiplexer includes active input overvoltage protection circuitry, and can withstand a continuous input up to 20 volts greater than either supply. This feature protects the multiplexer against damage when supplies are off, but input signals are present -- essential in systems where the analog inputs originate outside the equipment. Equally important, the HY-9595/9596 can withstand brief input transient spikes of over 4000 volts, which would otherwise require complex external protection.

An overvoltage condition on a deselected input does not cause distortion on the selected input channel.

The Input Multiplexer is guaranteed to break-before-make, so two channels are never shorted together.

Multiplexer Expansion ports are included so external multiplexers can be added, if required.

Programmable Gain Amplifier Section

The Programmable Gain Amplifier (PGA) provides non-inverting gains under digital control; the gains are +1, +2, +4 and +8. A different gain can be selected for each input channel. A fully differential amplifier is used in both versions, so the pseudo-differential inputs on the HY-9596 are referenced to the SENSE input, rather than to the supply ground.

The resistor network is laser trimmed to minimize gain errors.

Input Voltage Ranges

The HY-9595/9596 accepts the standard ±10V input range. Care must be taken in the system design to avoid overdriving the amplifier, which could result in output signal distortion.

Temperature Grades

The HY-9595/9596 will be available initially in Commercial (0°C to +75°C) and Industrial (−40°C to +85°C) temperature grades. A grade is also being developed for the military temperature range (−55°C to +125°C).

Power Requirements

Power requirements are +5V and ±15V, with typical dissipation of 190mW.

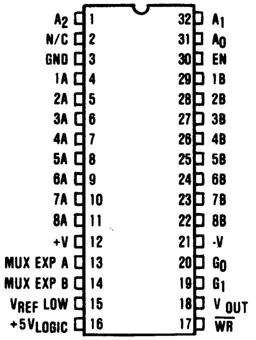
Package

All models are packaged in a 32-pin DIP with 600 mil row centers. Plastic packages are used for Commercial and Industrial grades. Ceramic hermetic packages will be used for the Military temperature grade.

Pinouts

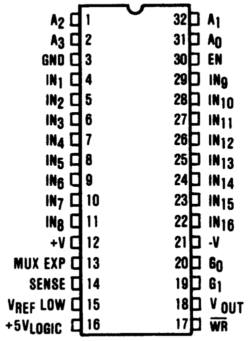
HY-9595

TOP VIEW

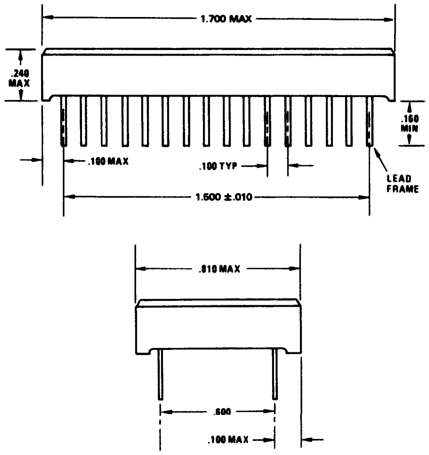

A2 1
N/C 2
GND 3
1A 4
2A 5
3A 6
4A 7
5A 8
6A 9
7A 10
8A 11
+V 12
MUX EXP A 13
MUX EXP B 14
VREF LOW 15
+5VLOGIC 16
32 A1
31 A0
30 EN
29 1B
28 2B
27 3B
26 4B
25 5B
24 6B
23 7B
22 8B
21 -V
20 G0
19 G1
18 VOUT
17 WR

HY-9596

TOP VIEW


A2 1
A3 2
GND 3
IN1 4
IN2 5
IN3 6
IN4 7
IN5 8
IN6 9
IN7 10
IN8 11
+V 12
MUX EXP 13
SENSE 14
VREF LOW 15
+5VLOGIC 16
32 A1
31 A0
30 EN
29 IN9
28 IN10
27 IN11
26 IN12
25 IN13
24 IN14
23 IN15
22 IN16
21 -V
20 G0
19 G1
18 VOUT
17 WR

Package


1.700 MAX
.240 MAX
.160 MIN
.100 MAX
.100 TYP
LEAD FRAME
1.500 ±.010
.610 MAX
.600
.100 MAX

ANALOG

Analog-to-Digital Converters

5

Product Index 5-2

Ordering Information 5-3

Standard Products Packaging Availability 5-3

Selection Guide 5-4

Product Information 5-5

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

[illegible] Fast, Complete 12-Bit A/D Converter with Microprocessor Interface .... [illegible]

HI-674A Fast, Complete 12-Bit A/D Converter with Microprocessor Interface 5-16

HI-774 Fast, Complete 12-Bit A/D Converter with Microprocessor Interface 5-27

HI-774A Fast, Complete 12-Bit A/D Converter with Microprocessor Interface 5-38

HY-9574 Sampling 12-Bit A/D Converter with 8/16-Bit Microprocessor Interface 5-51

HY-9674 Sampling 12-Bit A/D Converter with 8/16-Bit Microprocessor Interface 5-68

HY-94741/742 Low Power Sampling 12-Bit A/D Converter with 8/16-Bit Microprocessor Interface 5-84

HY-9712 Complete 12-Bit Data Acquisition Subsystem 5-86

Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H I 1 - 574A - 5

PREFIX:
H (HARRIS)

FAMILY:
A — Analog
C — Communications
D — Digital
F — Filters
I — Interface
M — Memory
V — Analog, High Voltage
Y — Analog Hybrids

PACKAGE:
1 — Dual-In-Line, Ceramic
2 — Metal Can
3 — Dual-In Line, Plastic
4 — Leadless Carriers
5 — LCC Hybrid
7 — Mini-DIP, Ceramic
0 — Chip Form

PART NUMBER

TEMPERATURE:
1 — 0°C to +200°C *
2 — -55°C to +125°C
4 — -25°C to +85°C
5 — 0°C to +75°C
6 — 100% +25°C Probe (Dice Only)
7 — Dash-7 High Reliability Commercial Product. 0°C to +75°C
8 — Dash-8 Program HA2-2520-8 (Example only)
9 — -40°C to +85°C

* Special high temperature testing available on certain product types. Consult factory for availability.

Standard Products Packaging Availability

PACKAGE		CERAMIC DIP				SURFACE MOUNT LCC
TEMPERATURE		-5	-2	-9	-8	-8
DEVICE NUMBER						
ANALOG TO DIGITAL						
	HI-574A	X	X		X	*
	HI-674A	X	X		X	*
ADVANCE	HI-774	X				
	HI-774A	X	X			
	HY-9574	X	X	X		
	HY-9674	X	X	X		

*Available as MIL-STD-883 only.

Selection Guide

A/D CONVERTERS

	Part Number	Resolution Bits	Temp. Range			Package	Non-Linearity Max. 25°C (LSB)	Differential Non-Linearity* Max. 25°C	Gain Drift ppms°C Max. Full Temp	Conversion Speed (μs) (Internal Clock)		Page
			-55°C to +125°C	0°C to +75°C	-40°C to +85°C					12-Bits	8-Bits	
	HI-574AJD	12		X		28 Pin Cerdip	±1	11-Bits	±45	20	13	5-5
	HI-574AKD			X			±1/2	12-Bits	±25			
	HI-574ALD			X			±1/2	12-Bits	±10			
	HI-574ASD		X				±1	11-Bits	±50			
	HI-574ATD		X				±1/2	12-Bits	±25			
	HI-574AUD		X				±1/2	12-Bits	±12.5			
	HI-674AJD	12		X		28 Pin Cerdip	±1	11-Bits	±45	12	8	5-16
	HI-674AKD			X			±1/2	12-Bits	±25			
	HI-674ALD			X			±1/2	12-Bits	±10			
	HI-674ASD		X				±1	11-Bits	±50			
	HI-674ATD		X				±1/2	12-Bits	±25			
	HI-674AUD		X				±1/2	12-Bits	±12.5			
	HI-774J			X		28 Pin Cerdip	±1	11-Bits	±45	8.5	6.4	5-27
	HI-774K			X			±1/2	12-Bits	±25			
	HI-774L			X			±1/2	12-Bits	±10			
	HI-774AJD	12		X		28 Pin Cerdip	±1	11-Bits	±45	7	4.5	5-38
	HI-774AKD			X			±1/2	12-Bits	±25			
	HI-774ALD			X			±1/2	12-Bits	±10			
	HI-774ASD		X				±1	11-Bits	±50			
	HI-774ATD		X				±1/2	12-Bits	±25			
	HI-774AUD		X				±1/2	12-Bits	±12.5			
ADVANCE	HY3-9574J	12		X		32 Pin Plastic	±1	11-Bits	±45	20	13	5-51
	HY3-9574K			X			±1/2	12-Bits	±25			
	HY3-9574L			X			±1/2	12-Bits	±10			
	HY3-9574A				X		±1	11-Bits	±50			
	HY3-9574B				X		±1	12-Bits	±25			
	HY3-9674J	12		X		32 Pin Plastic	±1	11-Bits	±45	12	8	5-68
	HY3-9674K			X			±1/2	12-Bits	±25			
	HY3-9674L			X			±1/2	12-Bits	±10			
	HY3-9674A				X		±1	11-Bits	±50			
	HY3-9674B				X		±1/2	12-Bits	±25			
PRELIMINARY	HY-94741 HY-94742	12	X	X	X	28 Pin Plastic or Ceramic	±1/2	12-Bits	±45	20	13	5-84
	HY-9712	12	X	X	X	N/A	±1/2	12-Bits	TBD	TBD	TBD	5-86

*Maximum resolution with no missing codes guaranteed.

HI-574A

Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

FEATURES

- COMPLETE 12 BIT A/D CONVERTER WITH REFERENCE AND CLOCK.
- FULL 8-, 12- or 16- BIT MICROPROCESSOR BUS INTERFACE.
- 150 nS BUS ACCESS TIME
- NO MISSING CODES OVER TEMPERATURE
- MINIMAL SETUP TIME FOR CONTROL SIGNALS
- 25 μS MAXIMUM CONVERSION TIME
- LOW NOISE, VIA CURRENT-MODE SIGNAL TRANSMISSION BETWEEN CHIPS
- BYTE ENABLE/SHORT CYCLE (A_0 INPUT)
    - GUARANTEES BREAK – BEFORE – MAKE ACTION, ELIMINATING BUS CONTENTION DURING READ OPERATION. LATCHED BY THE START CONVERT INPUT (TO SET THE CONVERSION LENGTH).
- IMPROVED SECOND SOURCE FOR AD574A AND HS574
- ±12V TO ±15V OPERATION

APPLICATIONS

- MILITARY AND INDUSTRIAL DATA ACQUISITION SYSTEMS
- ELECTRONIC TEST AND SCIENTIFIC INSTRUMENTATION.
- PROCESS CONTROL SYSTEMS.

DESCRIPTION

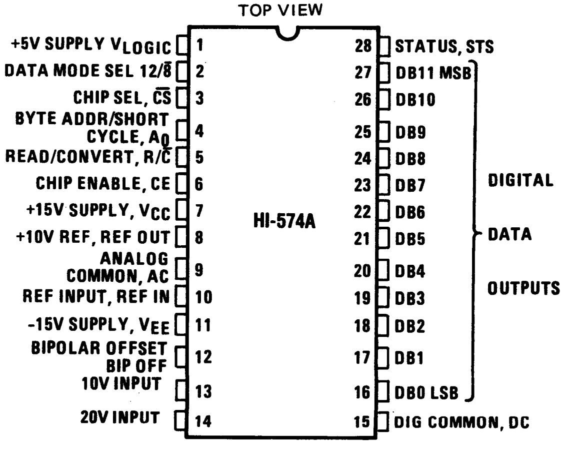
The HI-574A is a complete 12 bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

Custom design of each IC (Bipolar Analog and CMOS Digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20±1μs.

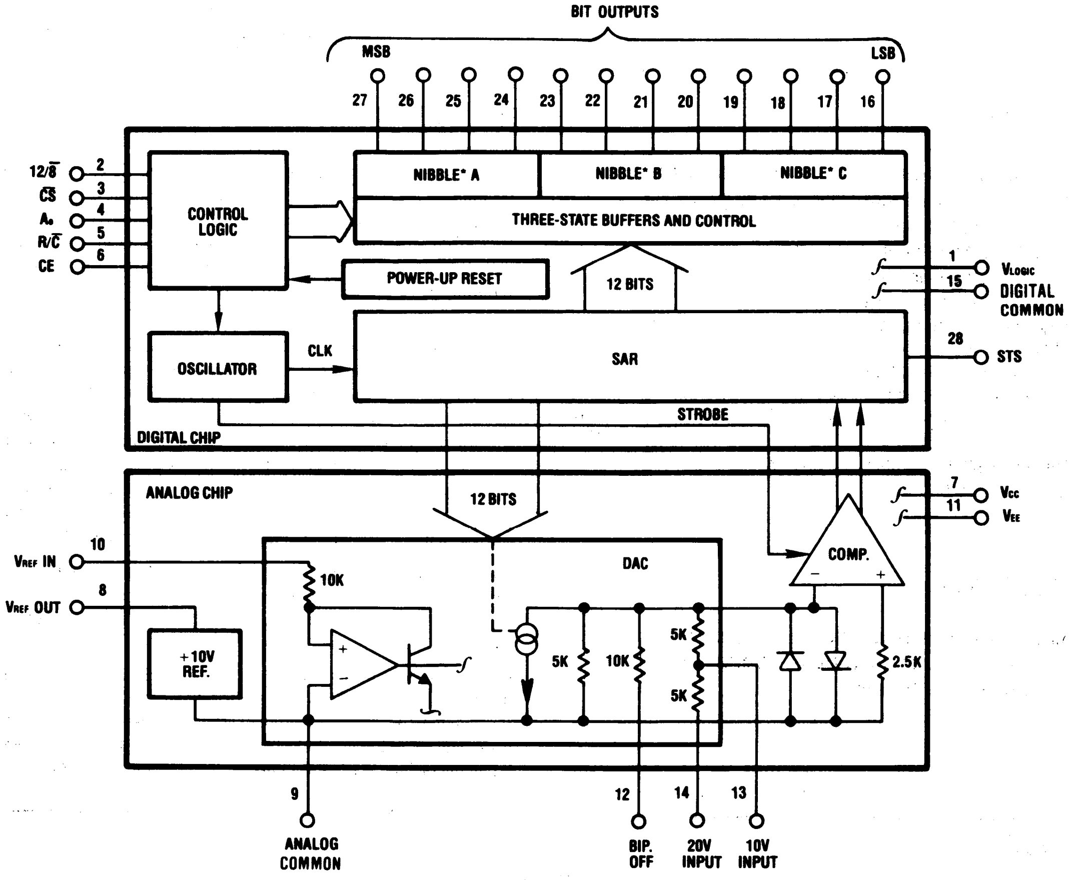
The HI-574A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW at ±12V. Three electrical grades each are offered for the commercial and military temperature ranges. All models are packaged in a 28 pin Side-Brazed DIP. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix.

PINOUT


TOP VIEW
+5V SUPPLY V_{LOGIC} 1
DATA MODE SEL 12/$\overline{8}$ 2
CHIP SEL, $\overline{CS}$ 3
BYTE ADDR/SHORT CYCLE, A_0 4
READ/CONVERT, R/$\overline{C}$ 5
CHIP ENABLE, CE 6
+15V SUPPLY, V_{CC} 7
+10V REF, REF OUT 8
ANALOG COMMON, AC 9
REF INPUT, REF IN 10
-15V SUPPLY, V_{EE} 11
BIPOLAR OFFSET BIP OFF 12
10V INPUT 13
20V INPUT 14
HI-574A
28 STATUS, STS
27 DB11 MSB
26 DB10
25 DB9
24 DB8
23 DB7
22 DB6
21 DB5
20 DB4
19 DB3
18 DB2
17 DB1
16 DB0 LSB
15 DIG COMMON, DC
DIGITAL DATA OUTPUTS

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.


BIT OUTPUTS
MSB
LSB
27
26
25
24
23
22
21
20
19
18
17
16
12/$\overline{8}$
$\overline{CS}$
A_0
R/$\overline{C}$
CE
2
3
4
5
6
CONTROL LOGIC
NIBBLE* A
NIBBLE* B
NIBBLE* C
THREE-STATE BUFFERS AND CONTROL
POWER-UP RESET
12 BITS
1
V_{LOGIC}
15
DIGITAL COMMON
OSCILLATOR
CLK
SAR
28
STS
STROBE
DIGITAL CHIP
ANALOG CHIP
12 BITS
7
V_{CC}
11
V_{EE}
10
V_{REF} IN
8
V_{REF} OUT
10K
DAC
COMP.
+10V REF.
5K
10K
5K
5K
2.5K
9
ANALOG COMMON
12
BIP. OFF
14
20V INPUT
13
10V INPUT

("NIBBLE" IS A 4 BIT DIGITAL WORD.)

SPECIFICATIONS

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	HI-574AJ	HI-574AK	HI-574AL	UNITS
Temperature Range	0 TO +75			°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	±1/2	LSB
Differential Linearity Error (Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max) (Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max) (Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.5	0.4	0.35	% of F.S.
(With adjustment to zero at +25°C)	0.22	0.12	0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2 (10)	±1 (5)	±1 (5)	LSB (ppm/°C)
Bipolar Offset	±2 (10)	±1 (5)	±1 (5)	LSB (ppm/°C)
Full Scale Calibration	±9 (45)	±5 (25)	±2 (10)	LSB (ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
$+13.5V<V_{CC}<+16.5V$ or $+11.4V<V_{CC}<+12.6V$	±2	±1	±1	LSB
$+4.5V<V_{LOGIC}<+5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V<V_{EE}<-13.5V$ or $-12.6V<V_{EE}<-11.4V$	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5 −10 to +10			Volts Volts
Unipolar	0 to +10 0 to +20			Volts Volts
Input Impedance				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} -15V Supply	21 TYP, 28 MAX			mA
Power Dissipation				
±15V, +5V	515 TYP, 720 MAX			mW
±12V, +5V	385 TYP			mW
Internal Reference Voltage	+10.00 ± 0.1 MAX			Volts
Output current,[1] available for external loads (External load should not change during conversion).	2.0 MAX			mA

[1] *When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.*

SPECIFICATIONS

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	**HI-574AS**	**HI-574AT**	**HI-574AU**	**UNITS**
Temperature Range	−55 TO +125			°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
−55°C to +125°C (max)	±1	±1	±1	LSB
Differential Linearity Error (Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max) (Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max) (Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.8	0.6	0.4	% of F.S.
(With adjustment to zero at +25°C)	0.5	0.25	0.12	% of F.S.
Temperature Coefficients Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2 (5)	±1 (2.5)	±1 (2.5)	LSB (ppm/°C)
Bipolar Offset	±4 (10)	±2 (5)	±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration	±20 (50)	±10 (25)	±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection Max change in Full Scale Calibration				
$+13.5V < V_{CC} < +16.5V$ or $+11.4V < V_{CC} < +12.6V$	±2	±1	±1	LSB
$+4.5V < V_{LOGIC} < +5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V < V_{EE} < -13.5V$ or $-12.6V < V_{EE} < -11.4V$	±2	±1	±1	LSB
Analog Inputs Input Ranges				
Bipolar	−5 to +5 −10 to +10			Volts Volts
Unipolar	0 to +10 0 to +20			Volts Volts
Input Impedance				
10 Volt Span	5K Ω, ± 25%			Ohms
20 Volt Span	10K Ω, ± 25%			Ohms
Power Supplies Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} -15V Supply	21 TYP, 28 MAX			mA
Power Dissipation				
±15V, +5V	515 TYP, 720 MAX			mW
±12V, +5V	385 TYP			mW
Internal Reference Voltage	+10.00 ± 0.1 (MAX)			Volts
Output current,[1] available for external loads (External load should not change during conversion).	2.0 MAX			mA

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[1] When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.

DIGITAL CHARACTERISTICS[1]
(ALL MODELS, OVER FULL TEMP. RANGE)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, AO, 12/$\overline{8}$)			
Logic "1"	+2.4V[2]		+5.5V
Logic "0"	−0.5V		+0.8V
Current	−5μA	±0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 ONLY)	−5μA	±0.1μA	+5μA
Capacitance		5pF	

[1] *See "HI-574A Timing Specifications" for a detailed listing of digital timing parameters.*

[2] *Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.*

ABSOLUTE MAXIMUM RATINGS

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common	0 to +16.5V
V_{EE} to Digital Common	0 to −16.5V
V_{LOGIC} to Digital Common	0 to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common	−0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, 10V_{IN}) to Analog Common	±16.5V
20V_{IN} to Analog Common	±24V
REF OUT	Indefinite short to common Momentary short to V_{CC}
Chip Temperature	175 °C
Power Dissipation *	2080mW
Lead Temperature, Soldering	300°C, 10 sec.
Storage Temperature	−65°C to +150°C
Thermal Resistance, Θ_{JA}	48°C/W

*Derate 20.8mW/°C above 75°C

HI-574A ORDERING GUIDE

MODEL	TEMP. RANGE	LINEARITY ERROR MAX (T_{MIN} to T_{MAX})	RESOLUTION (NO MISSING CODES, T_{MIN} to T_{MAX})	FULL SCALE TC (PPM/°C MAX)
HI1-574AJD-5	0 to 75°C	±1 LSB	11 Bits	45.0
HI1-574AKD-5	0 to 75°C	±1/2 LSB	12 Bits	25.0
HI1-574ALD-5	0 to 75°C	±1/2 LSB	12 Bits	10.0
HI1-574ASD-2	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-574ASD-8*	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-574ATD-2	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-574ATD-8*	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-574AUD-2	−55 to +125°C	±1 LSB	12 Bits	12.5
HI1-574AUD-8*	−55 to +125°C	±1 LSB	12 Bits	12.5

**Hi-Rel product with burn-in. For additional screening information, refer to Hi-Rel Section of current Analog catalog.*

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-574AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-574AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR
(NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-574AK, AL, AT, and AU grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-574AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the HI-574A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the HI-574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

APPLYING THE HI-574A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout –

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-574A (+15V, −15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-574A ground currents are 5.5mADC into pin 9 (Analog Common)and 7mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 1.5mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-574A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device chosen to drive the HI-574A analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 1.6μS intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 600KHz for use with the HI-574A. To check whether the output properties of a signal source are suitable, monitor the 574A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one microsecond or less. (The comparator decision is made about 1.5μS after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-574A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-574A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-574A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-574A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration –

Refer to Fig. 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem – the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one

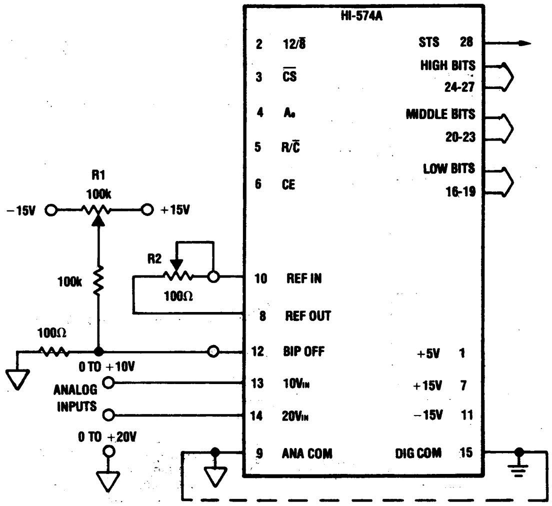

HI-574A
2 12/$\overline{8}$
3 $\overline{CS}$
4 A_0
5 R/$\overline{C}$
6 CE
10 REF IN
8 REF OUT
12 BIP OFF
13 $10V_{IN}$
14 $20V_{IN}$
9 ANA COM
STS 28
HIGH BITS 24-27
MIDDLE BITS 20-23
LOW BITS 16-19
+5V 1
+15V 7
−15V 11
DIG COM 15
R1
100k
−15V
+15V
100k
R2
100Ω
100Ω
0 TO +10V
ANALOG INPUTS
0 TO +20V

FIGURE 2. UNIPOLAR CONNECTIONS

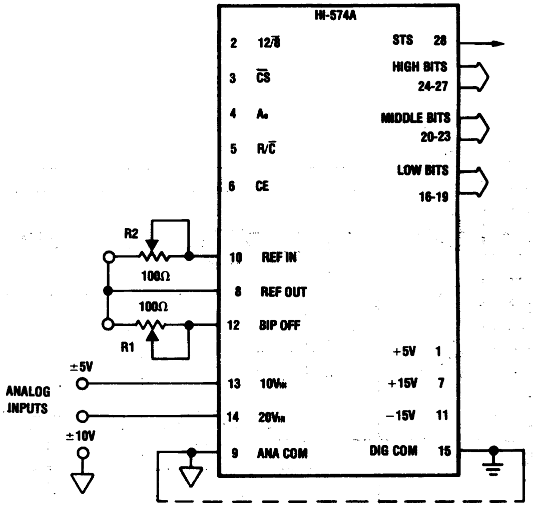

HI-574A
2 12/$\overline{8}$
3 $\overline{CS}$
4 A_0
5 R/$\overline{C}$
6 CE
10 REF IN
8 REF OUT
12 BIP OFF
13 $10V_{IN}$
14 $20V_{IN}$
9 ANA COM
STS 28
HIGH BITS 24-27
MIDDLE BITS 20-23
LOW BITS 16-19
+5V 1
+15V 7
−15V 11
DIG COM 15
R2
100Ω
100Ω
R1
±5V
ANALOG INPUTS
±10V

FIGURE 3 BIPOLAR INPUT CONNECTIONS

LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +1/2 LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1-1/2 LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration –

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage 1/2 LSB above negative full scale (i.e., −4.9988V for the ±5V range, or −9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1-1/2 LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

CONTROLLING THE HI-574A

The HI-574A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready – choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

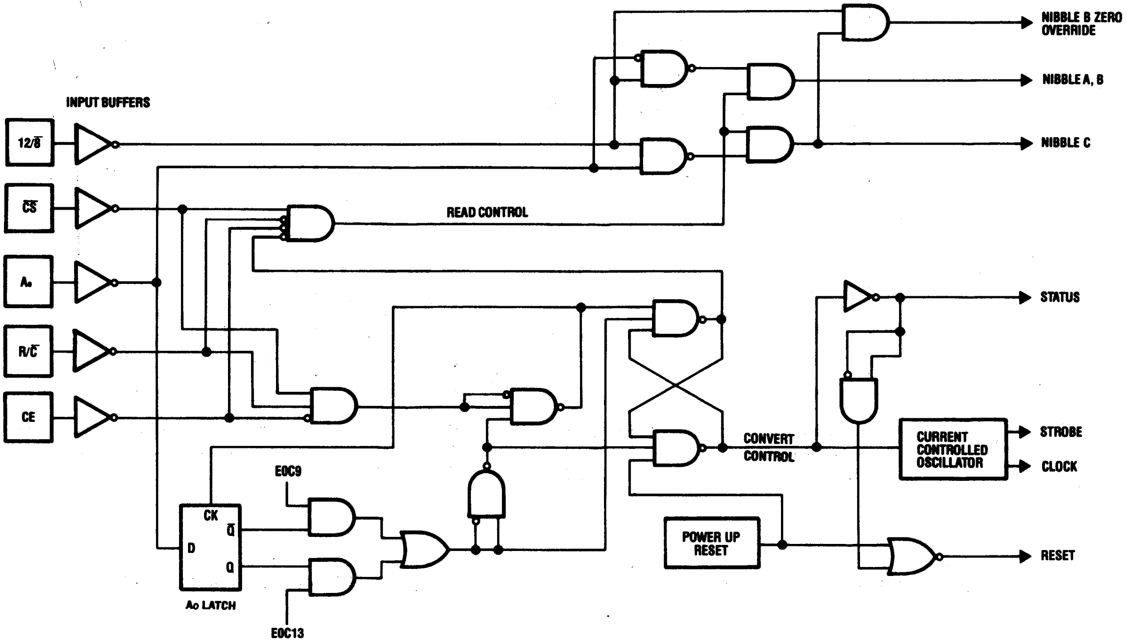


FIGURE 4. HI-574A CONTROL LOGIC

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing."

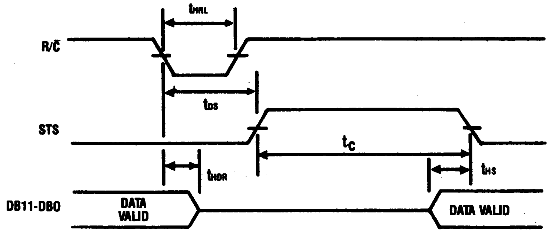

t_{HRL}
R/$\overline{C}$
t_{DS}
STS
t_C
t_{HDR}
t_{HS}
DB11-DB0
DATA VALID
DATA VALID

FIGURE 5. LOW PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED AFTER CONVERSION

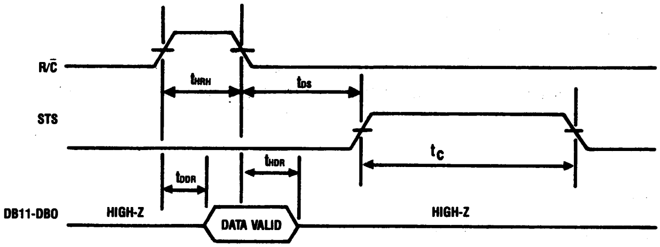

R/$\overline{C}$
t_{HRH}
t_{DS}
STS
t_C
t_{HDR}
t_{DDR}
DB11-DB0
HIGH-Z
DATA VALID
HIGH-Z

FIGURE 6. HIGH PULSE FOR R/$\overline{C}$–OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	500	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

TABLE 1

Truth Table for HI-574A Control Inputs.

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-574A Timing Specifications, Convert mode.

This variety of HI-574A control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

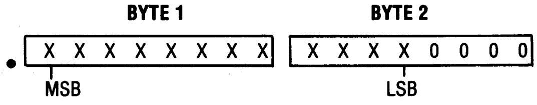
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs 12 bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 9. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-574A output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4 MSB's are disabled, bits 4 through 7 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. See Figure 8.

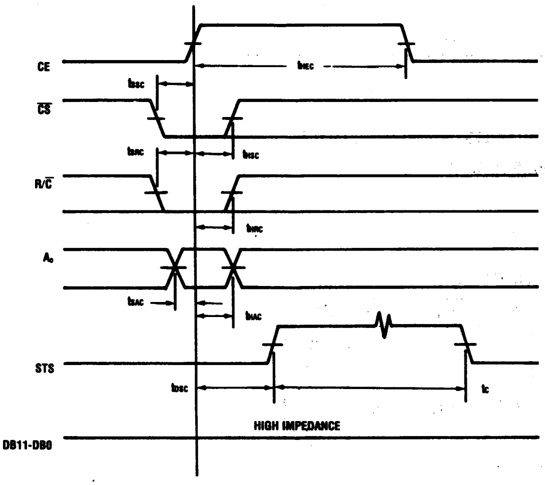


FIGURE 7. CONVERT START TIMING

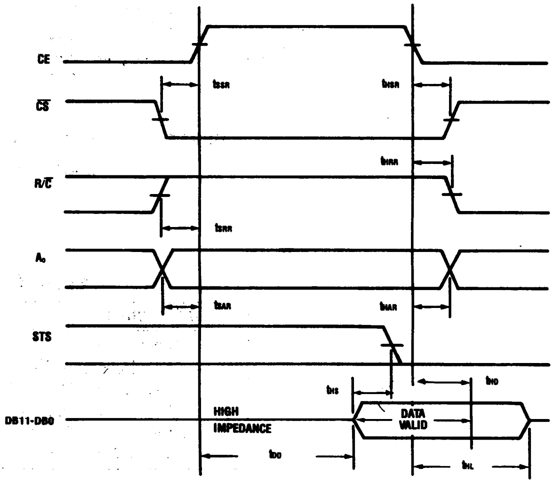


FIGURE 8. READ CYCLE TIMING

HI-574A TIMING SPECIFICATIONS

+25°C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS Delay from CE		100	200	nS
t_{HEC}	CE Pulse width	50	30		nS
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		nS
t_{HSC}	$\overline{CS}$ Low during CE High	50	20		nS
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		nS
t_{HRC}	R/$\overline{C}$ Low during CE high	50	20		nS
t_{SAC}	A_0 to CE Setup	0	0		nS
t_{HAC}	A_0 Valid during CE high	50	20		nS
t_c	Conversion time, 12 bit cycle T min to T max	15	20	25	μS
	8 bit cycle T min to T max	10	13	17	μS
Read Mode					
t_{DD}	Access time from CE		75	150	nS
t_{HD}	Data Valid after CE low	25	35		nS
t_{HL}	Output float delay		100	150	nS
t_{SSR}	$\overline{CS}$ to CE setup	50	0		nS
t_{SRR}	R/$\overline{C}$ to CE setup	0	0		nS
t_{SAR}	A_0 to CE setup	50	25		nS
t_{HSR}	$\overline{CS}$ valid after CE low	0	0		nS
t_{HRR}	R/$\overline{C}$ high after CE low	0	0		nS
t_{HAR}	A_0 valid after CE low	50	25		nS
t_{HS}	STS delay after data valid	300	500	1000	nS

Note: Time is measured from 50% level of digital transitions, tested with a 10pF and 2KΩ load.

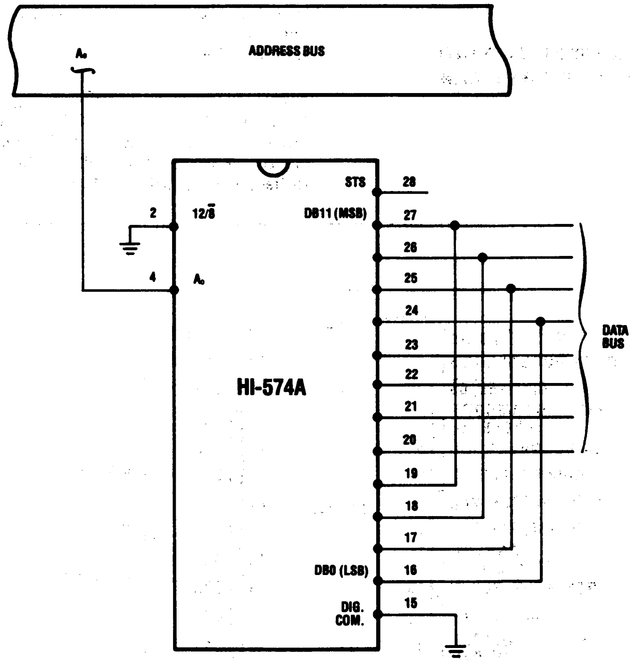


FIGURE 9 INTERFACE TO AN 8 BIT DATA BUS

DIE CHARACTERISTICS

Transistor Count		1117	Thermal Constants;	θja	48°C/W
Die Size:	Analog	204 x 104 mils		θjc	15°C/W
	Digital	158 x 84 mils	Process:		Bipolar – DI and CMOS – JI

HARRIS

HI-674A

12μs, Complete 12-Bit A/D Converter with Microprocessor Interface

FEATURES

- COMPLETE 12 BIT A/D CONVERTER WITH REFERENCE AND CLOCK.
- FULL 8-, 12- or 16- BIT MICROPROCESSOR BUS INTERFACE.
- 150 nS BUS ACCESS TIME
- NO MISSING CODES OVER TEMPERATURE
- MINIMAL SETUP TIME FOR CONTROL SIGNALS
- 15 μS MAXIMUM CONVERSION TIME
- LOW NOISE, VIA CURRENT-MODE SIGNAL TRANSMISSION BETWEEN CHIPS
- BYTE ENABLE/SHORT CYCLE (A_0 INPUT)
    - GUARANTEES BREAK-BEFORE-MAKE ACTION, ELIMINATING BUS CONTENTION DURING READ OPERATION. LATCHED BY THE START CONVERT INPUT (TO SET THE CONVERSION LENGTH).
- FASTER VERSION OF THE HI-574A.
- SAME PIN-OUTS AS HI-574A.
- ± 12V TO ± 15V OPERATION

APPLICATIONS

- MILITARY AND INDUSTRIAL DATA ACQUISITION SYSTEMS
- ELECTRONIC TEST AND SCIENTIFIC INSTRUMENTATION.
- PROCESS CONTROL SYSTEMS.

DESCRIPTION

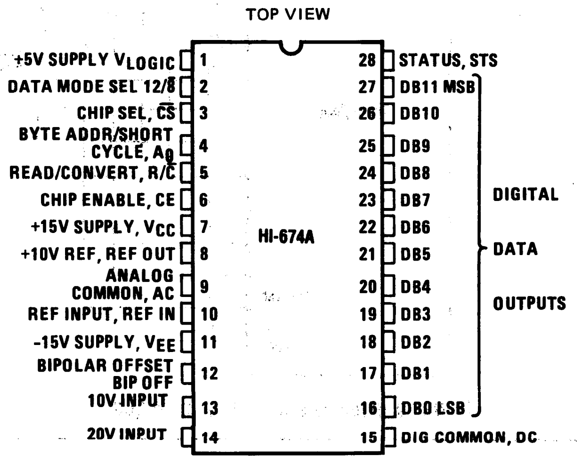
The HI-674A is a complete 12 bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28-pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2x reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 12±1 μs.

The HI-674A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

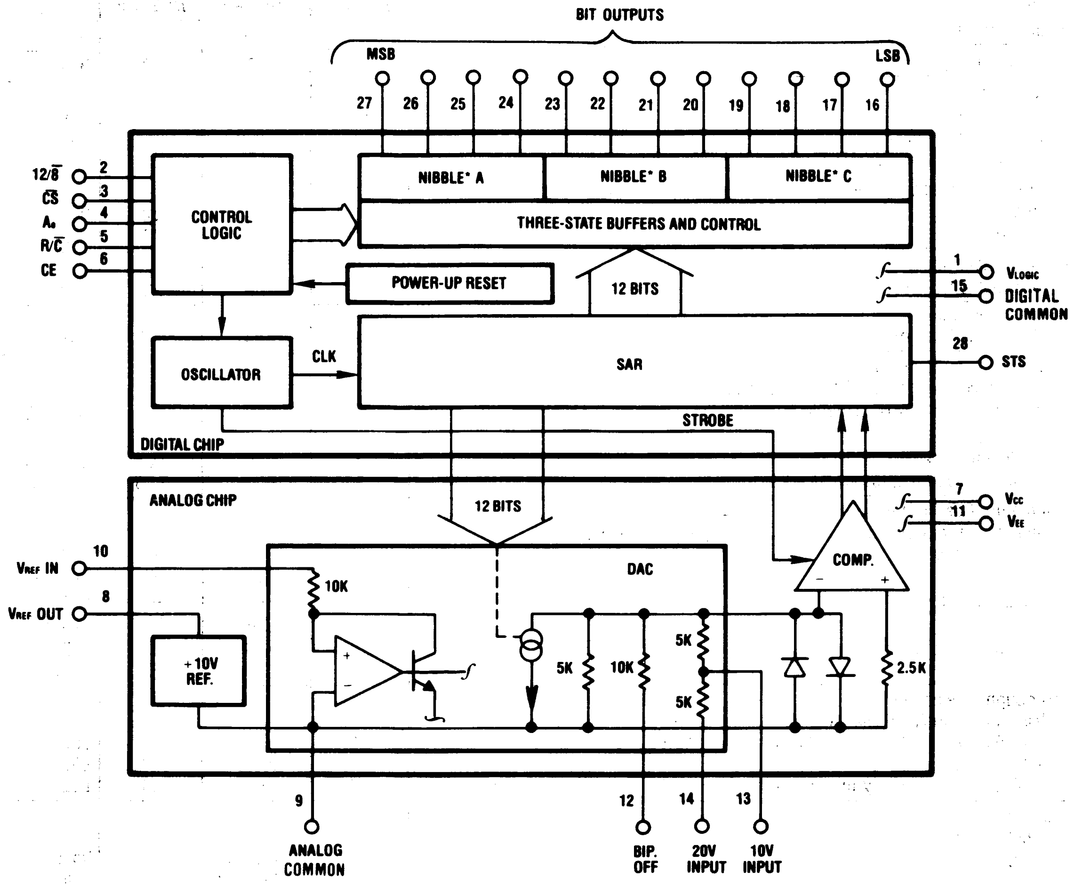
Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW at ±12V. Three electrical grades each are offered for the commercial and military temperature ranges. All models are packaged in a 28 pin Side-Brazed DIP. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix.

PINOUT


TOP VIEW
+5V SUPPLY V_{LOGIC} 1
DATA MODE SEL 12/$\overline{8}$ 2
CHIP SEL, $\overline{CS}$ 3
BYTE ADDR/SHORT CYCLE, A_0 4
READ/CONVERT, R/$\overline{C}$ 5
CHIP ENABLE, CE 6
+15V SUPPLY, V_{CC} 7
+10V REF, REF OUT 8
ANALOG COMMON, AC 9
REF INPUT, REF IN 10
-15V SUPPLY, V_{EE} 11
BIPOLAR OFFSET BIP OFF 12
10V INPUT 13
20V INPUT 14
HI-674A
28 STATUS, STS
27 DB11 MSB
26 DB10
25 DB9
24 DB8
23 DB7
22 DB6
21 DB5
20 DB4
19 DB3
18 DB2
17 DB1
16 DB0 LSB
15 DIG COMMON, DC
DIGITAL DATA OUTPUTS

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

HI-674A BLOCK DIAGRAM


BIT OUTPUTS
MSB
LSB
27
26
25
24
23
22
21
20
19
18
17
16
NIBBLE* A
NIBBLE* B
NIBBLE* C
THREE-STATE BUFFERS AND CONTROL
12/$\overline{8}$ 2
$\overline{CS}$ 3
A_0 4
R/$\overline{C}$ 5
CE 6
CONTROL LOGIC
POWER-UP RESET
12 BITS
1 V_{LOGIC}
15 DIGITAL COMMON
28 STS
OSCILLATOR
CLK
SAR
STROBE
DIGITAL CHIP
ANALOG CHIP
12 BITS
7 V_{CC}
11 V_{EE}
10 V_{REF} IN
8 V_{REF} OUT
10K
DAC
COMP.
+10V REF.
5K
10K
5K
5K
2.5K
9 ANALOG COMMON
12 BIP. OFF
14 20V INPUT
13 10V INPUT

("NIBBLE" IS A 4 BIT DIGITAL WORD.)

SPECIFICATIONS

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	HI-674AJ	HI-674AK	HI-674AL	UNITS
Temperature Range	0 TO +75			°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	±1/2	LSB
Differential Linearity Error (Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max) (Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max) (Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error 25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.5	0.4	0.35	% of F.S.
(With adjustment to zero at +25°C)	0.22	0.12	0.05	% of F.S.
Temperature Coefficients Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2 (10)	±1 (5)	±1 (5)	LSB (ppm/°C)
Bipolar Offset	±2 (10)	±1 (5)	±1 (5)	LSB (ppm/°C)
Full Scale Calibration	±9 (45)	±5 (25)	±2 (10)	LSB (ppm/°C)
Power Supply Rejection Max change in Full Scale Calibration				
$+13.5V<V_{CC}<+16.5V$ or $+11.4V<V_{CC}<+12.6V$	±2	±1	±1	LSB
$+4.5V<V_{LOGIC}<+5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V<V_{EE}<-13.5V$ or $-12.6V<V_{EE}<-11.4V$	±2	±1	±1	LSB
Analog Inputs Input Ranges				
Bipolar	−5 to +5 −10 to +10			Volts Volts
Unipolar	0 to +10 0 to +20			Volts Volts
Input Impedance				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
Power Supplies Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} -15V Supply	21 TYP, 28 MAX			mA
Power Dissipation				
±15V, +5V	515 TYP, 720 MAX			mW
±12V, +5V	385 TYP			mW
Internal Reference Voltage	+10.00 ± 0.1 MAX			Volts
Output current,[1] available for external loads (External load should not change during conversion).	2.0 MAX			mA

[1] *When supplying an external load and operating on ± 12V supplies, a buffer amplifier must be provided for the Reference Output.*

SPECIFICATIONS

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	HI-674AS	HI-674AT	HI-674AU	UNITS
Temperature Range	−55 TO +125			°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
−55°C to +125°C (max)	±1	±1	±1	LSB
Differential Linearity Error				
(Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max) (Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max) (Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.8	0.6	0.4	% of F.S.
(With adjustment to zero at +25°C)	0.5	0.25	0.12	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2 (5)	±1 (2.5)	±1 (2.5)	LSB (ppm/°C)
Bipolar Offset	±4 (10)	±2 (5)	±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration	±20 (50)	±10 (25)	±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
$+13.5V < V_{CC} < +16.5V$ or $+11.4V < V_{CC} < +12.6V$	±2	±1	±1	LSB
$+4.5V \leq V_{LOGIC} \leq +5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V < V_{EE} < -13.5V$ or $-12.6V < V_{EE} < -11.4V$	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5 −10 to +10			Volts Volts
Unipolar	0 to +10 0 to +20			Volts Volts
Input Impedance				
10 Volt Span	5K Ω, ± 25%			Ohms
20 Volt Span	10K Ω, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC} **+15V Supply**	11 TYP, 15 MAX			mA
I_{EE} **-15V Supply**	21 TYP, 28 MAX			mA
Power Dissipation				
±15V, +5V	515 TYP, 720 MAX			mW
±12V, +5V	**385 TYP**			mW
Internal Reference Voltage	+10.00 ± 0.1 (MAX)			Volts
Output current,[1] available for external loads (External load should not change during conversion).	2.0 MAX			mA

---

[1] *When supplying an external load and operating on ± 12V supplies, a buffer amplifier must be provided for the Reference Output.*

DIGITAL CHARACTERISTICS[1]
(ALL MODELS, OVER FULL TEMP. RANGE)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$)			
Logic "1"	+2.4V[2]		+5.5V
Logic "0"	−0.5V		+0.8V
Current	−5μA	±0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 ONLY)	−5μA	±0.1μA	+5μA
Capacitance		5pF	

---

[1] *See "HI-574A Timing Specifications" for a detailed listing of digital timing parameters.*

[2] *Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e.,typical input current is only 0.25% of a TTL load.*

ABSOLUTE MAXIMUM RATINGS

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common .... 0 to +16.5V
V_{EE} to Digital Common .... 0 to −16.5V
V_{LOGIC} to Digital Common .... 0 to +7V
Analog Common to Digital Common .... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common .... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common .... ±16.5V
$20V_{IN}$ to Analog Common .... ±24V
REF OUT .... Indefinite short to common
Momentary short to V_{CC}
Chip Temperature .... 175°C
Power Dissipation* 2080mW
Lead Temperature, Soldering .... 300°C, 10 sec.
Storage Temperature .... −65°C to +150°C
Thermal Resistance, Θ_{JA} .... 48°C/W

*Derate 20.8mW/°C above 75°C

HI-674A ORDERING GUIDE

MODEL	TEMP. RANGE	LINEARITY ERROR MAX (T_{MIN} to T_{MAX})	RESOLUTION (NO MISSING CODES, T_{MIN} to T_{MAX})	FULL SCALE TC (PPM/°C MAX)
HI1-674AJD-5	0 to 75°C	±1 LSB	11 Bits	45.0
HI1-674AKD-5	0 to 75°C	±1/2 LSB	12 Bits	25.0
HI1-674ALD-5	0 to 75°C	±1/2 LSB	12 Bits	10.0
HI1-674ASD-2	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-674ASD-8*	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-674ATD-2	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-674ATD-8*	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-674AUD-2	−55 to +125°C	±1 LSB	12 Bits	12.5
HI1-674AUD-8*	−55 to +125°C	±1 LSB	12 Bits	12.5

*Hi-Rel product with burn-in. For additional screening information, refer to Section 9 of the current Analog data book.

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-674AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-674AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-674AK, AL, AT, and AU grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-674AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the HI-674A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the HI-674A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

APPLYING THE HI-674A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout –

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-674A (+15V, −15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-674A ground currents are 6mADC into pin 9 (Analog Ground) and 3mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 3mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-674A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device chosen to drive the HI-674A analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 950nS intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 1MHz for use with the HI-674A. To check whether the output properties of a signal source are suitable, monitor the 674A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one half microsecond or less. (The comparator decision is made about 850 nS after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-674A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-674A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-674A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-674A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration –

Refer to Fig. 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem – the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one

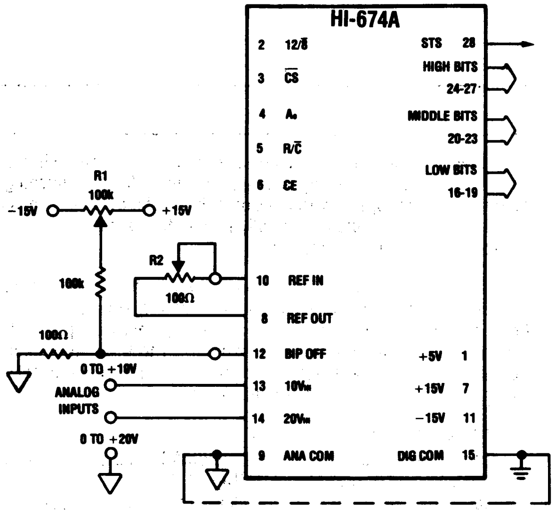

HI-674A
2 12/$\overline{8}$
3 $\overline{CS}$
4 A₀
5 R/$\overline{C}$
6 CE
STS 28
HIGH BITS 24-27
MIDDLE BITS 20-23
LOW BITS 16-19
R1
100k
−15V
+15V
100k
R2
100Ω
10 REF IN
8 REF OUT
100Ω
12 BIP OFF
0 TO +10V
ANALOG INPUTS
13 10V_IN
14 20V_IN
0 TO +20V
9 ANA COM
+5V 1
+15V 7
−15V 11
DIG COM 15

FIGURE 2. UNIPOLAR CONNECTIONS

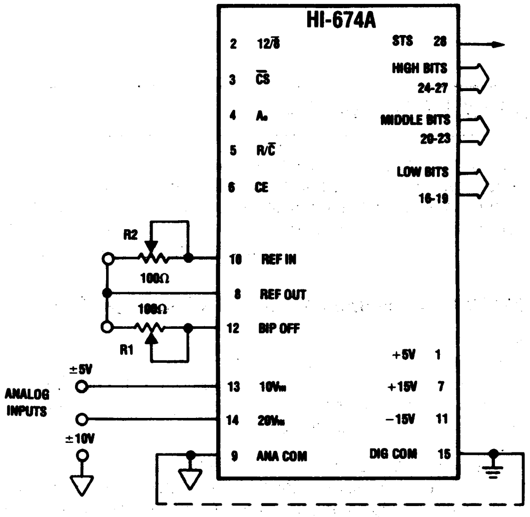

HI-674A
2 12/$\overline{8}$
3 $\overline{CS}$
4 A₀
5 R/$\overline{C}$
6 CE
STS 28
HIGH BITS 24-27
MIDDLE BITS 20-23
LOW BITS 16-19
R2
100Ω
10 REF IN
8 REF OUT
100Ω
R1
12 BIP OFF
±5V
ANALOG INPUTS
±10V
13 10V_IN
14 20V_IN
9 ANA COM
+5V 1
+15V 7
−15V 11
DIG COM 15

FIGURE 3 BIPOLAR INPUT CONNECTIONS

LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +1/2 LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1-1/2 LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration –

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage 1/2 LSB above negative full scale (i.e., −4.9988V for the ±5V range, or −9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1-1/2 LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

CONTROLLING THE HI-674A

The HI-674A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the $R/\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready – choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: ($12/\overline{8}$, $\overline{CS}$, A_0, $R/\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

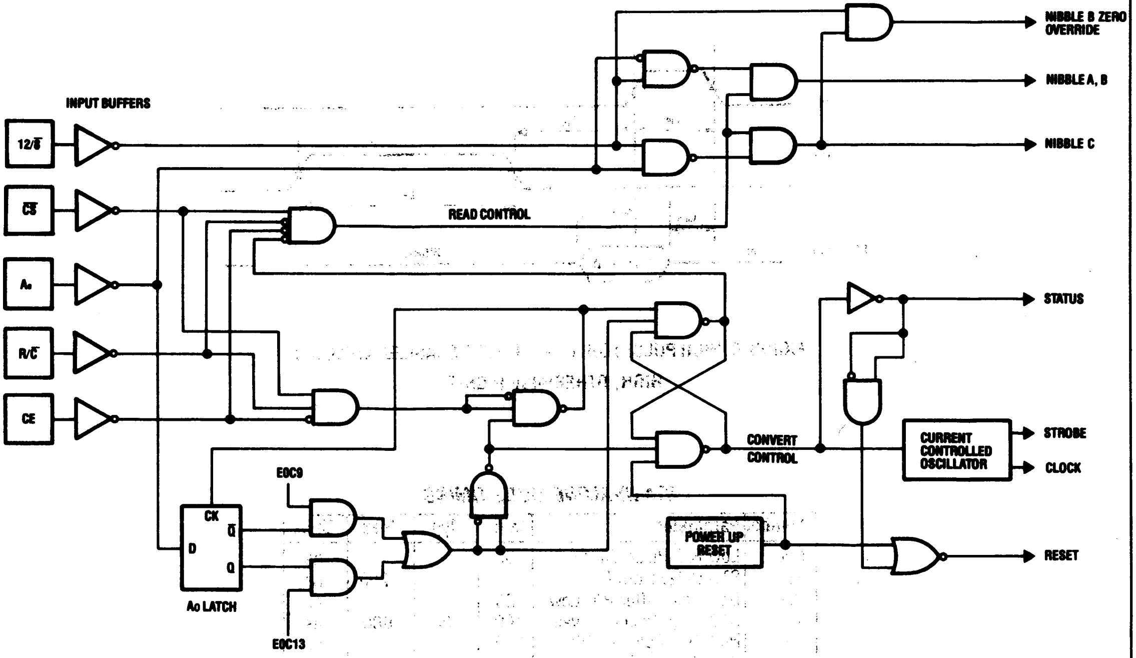
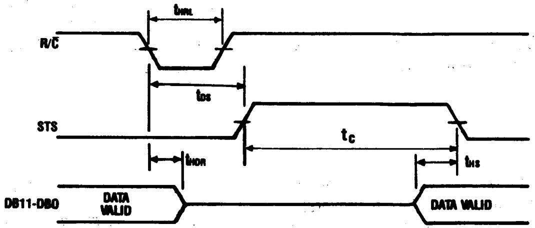


FIGURE 4. HI-674A CONTROL LOGIC

"Stand-Alone Operation"

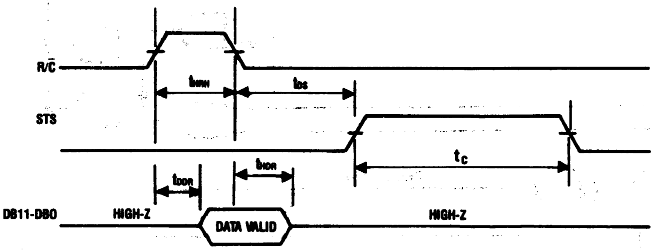
The simplest control interface calls for a single control line connected to R/C̄. Also, CE and 12/8̄ are wired high, C̄S̄ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/C̄ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/C̄ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing."



t_{HRL}
R/C̄
t_{DS}
STS
t_C
t_{HDR}
t_{HS}
DB11-DB0
DATA VALID
DATA VALID

FIGURE 5. LOW PULSE FOR R/C̄ – OUTPUTS ENABLED AFTER CONVERSION



R/C̄
t_{HRH}
t_{DS}
STS
t_C
t_{DDR}
t_{HDR}
DB11-DB0
HIGH-Z
DATA VALID
HIGH-Z

FIGURE 6. HIGH PULSE FOR R/C̄ – OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/C̄ Pulse Width	50			ns
t_{DS}	STS Delay from R/C̄			200	ns
t_{HDR}	Data Valid After R/C̄ Low	25			ns
t_{HS}	STS Delay After Data Valid	100	300	600	ns
t_{HRH}	High R/C̄ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

TABLE 1
Truth Table for HI-674A Control Inputs.

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-674A Timing Specifications, Convert mode.

This variety of HI-674A control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs 12 bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 9. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-674A output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4 MSB's are disabled, bits 4 through 7 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:

BYTE 1	BYTE 2
• X X X X X X X X	X X X X 0 0 0 0
MSB	LSB

Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. See Figure 8.

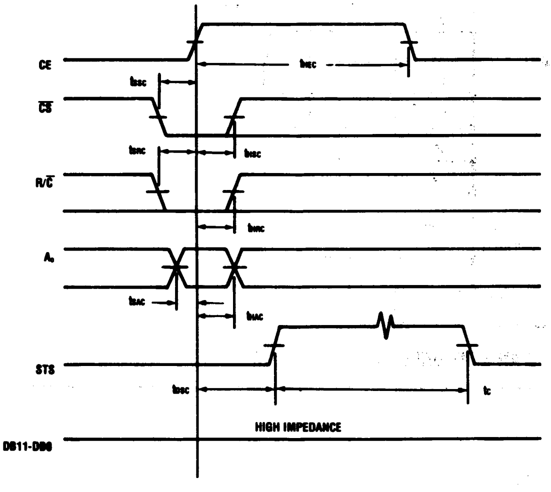


FIGURE 7. CONVERT START TIMING

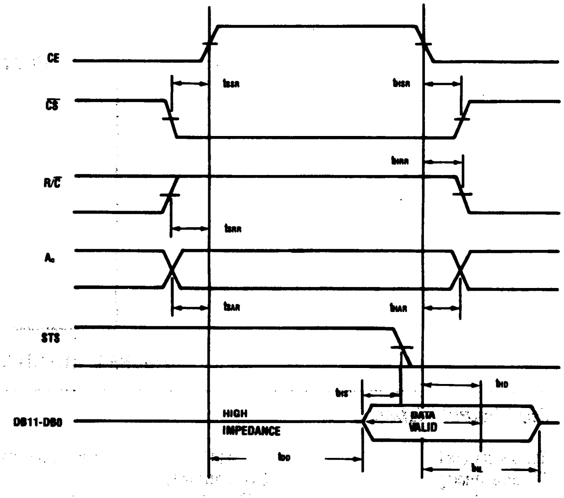


FIGURE 8. READ CYCLE TIMING

HI-674A TIMING SPECIFICATIONS

+25°C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS Delay from CE		100	200	nS
t_{HEC}	$\overline{\text{CE}}$ Pulse width	50	30		nS
t_{SSC}	$\overline{\text{CS}}$ to CE Setup	50	20		nS
t_{HSC}	$\overline{\text{CS}}$ Low during CE High	50	20		nS
t_{SRC}	R/$\overline{\text{C}}$ to CE Setup	50	0		nS
t_{HRC}	R/$\overline{\text{C}}$ Low during CE high	50	20		nS
t_{SAC}	A_0 to CE Setup	0	0		nS
t_{HAC}	A_0 Valid during CE high	50	20		nS
t_c	Conversion time, 12 bit cycle T min to T max	9	12	15	μS
	8 bit cycle T min to T max	6	8	10	μS
Read Mode					
t_{DD}	Access time from CE		75	150	nS
t_{HD}	Data Valid after CE low	25	35		nS
t_{HL}	Output float delay		100	150	nS
t_{SSR}	$\overline{\text{CS}}$ to CE setup	50	0		nS
t_{SRR}	R/$\overline{\text{C}}$ to CE setup	0	0		nS
t_{SAR}	A_0 to CE setup	50	25		nS
t_{HSR}	$\overline{\text{CS}}$ valid after CE low	0	0		nS
t_{HRR}	R/$\overline{\text{C}}$ high after CE low	0	0		nS
t_{HAR}	A_0 valid after CE low	50	25		nS
t_{HS}	STS delay after data valid	100	300	600	nS

NOTE: Time is measured from 50% level of digital transitions. Tested with a 10pF and 2KΩ load.

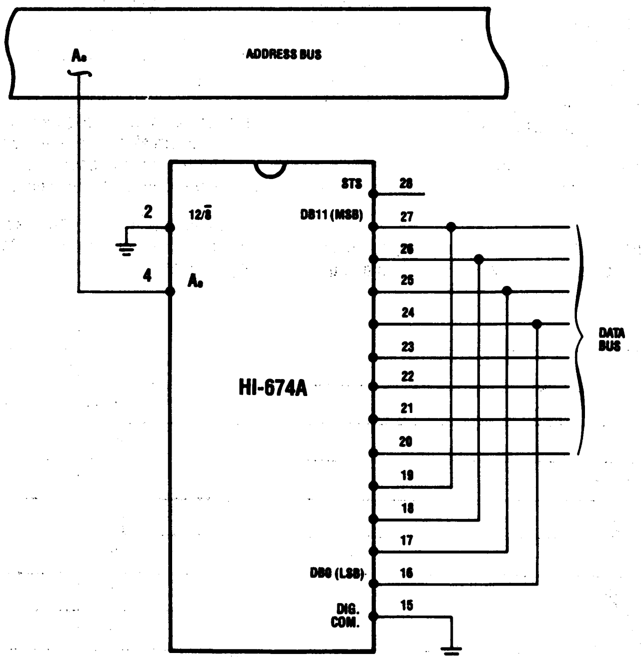


FIGURE 9. INTERFACE TO AN 8 BIT DATA BUS

Die Characteristics

Transistor Count	1117	Thermal Constants; θ_{ja}	48°C/W
Die Size; Analog	204 × 104 mils	θ_{jc}	15°C/W
Digital	158 × 84 mils	Process	Bipolar-DI CMOS-JI

HI-774

ADVANCED

8.5µs, Complete 12-Bit A/D Converter With Microprocessor Interface

Features

- **Complete 12 Bit A/D Converter With Reference and Clock**
- **Digital Error Correction**
- **Full 8-, 12-, or 16-Bit Microprocessor Bus Interface**
- **150ns Buss Access Time**
- **No Missing Codes Over Temperature**
- **Minimal Setup Time For Control Signals**
- **9µs Maximum Conversion Time Over Temperature**
- **Low Noise, Via Current-mode signal transmission between chips**
- **Byte enable/short cycle (Ao Input)**
  - ▸ **Guarantees break-before-make action, eliminating bus contention during read operation. Latched by the Start Convert Input (To Set the Conversion Length)**
- **Faster Version of the HI-574A and HI-674A**
- **Same Pin-Out as HI-574A and HI-674A**
- **±12V to ±15V Operation**

Applications

- **Industrial Data Acquisition Systems**
- **Electronics Test and Scientific Instrumentation**
- **Process Control Systems**

Description

The HI-774 is a complete 12 bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28-pin package. The bipolar analog die features the Harris Dielectric Isolation process, whch provides enhanced AC performance and freedom from latch-up. The digital die features the Smart SAR (SSAR™), which includes a digital error correction circuit.

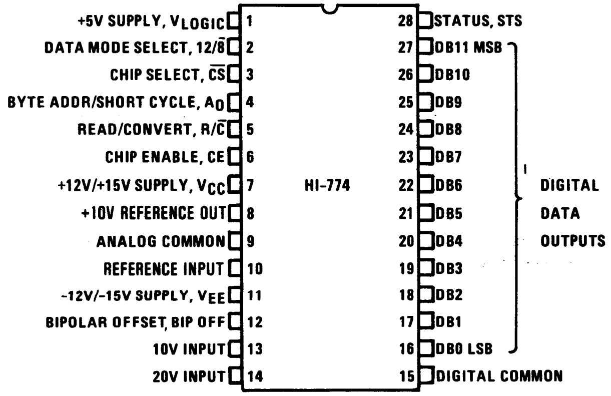
Custom design of each IC (bipolar and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current controlled for excellent stability over temperature. The oscillator is trimmed for a guaranteed conversion time of 8.5 ± 0.5µs over temperature.

The HI-774 offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The low noise buried zener reference circuit is trimmed for minimum temperature coefficient.

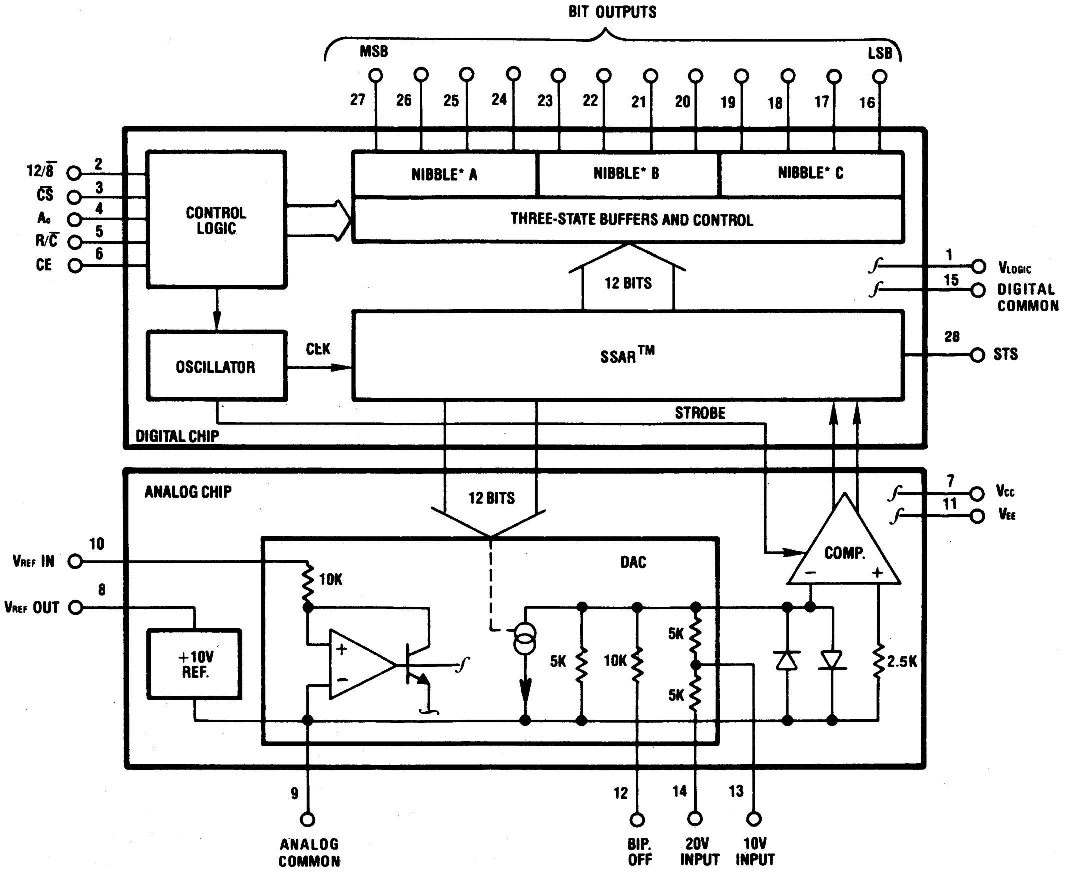
Power requirements are +5V and ±12V to ±15V, with typical dissipation of 390mW at ±12V. Three electrical grades are offered for the commercial temperature range. All models are packaged in a 28 pin side-brazed, ceramic DIP.

Pinout

TOP VIEW


+5V SUPPLY, V_{LOGIC} 1
DATA MODE SELECT, 12/$\overline{8}$ 2
CHIP SELECT, $\overline{CS}$ 3
BYTE ADDR/SHORT CYCLE, A_O 4
READ/CONVERT, R/$\overline{C}$ 5
CHIP ENABLE, CE 6
+12V/+15V SUPPLY, V_{CC} 7
+10V REFERENCE OUT 8
ANALOG COMMON 9
REFERENCE INPUT 10
-12V/-15V SUPPLY, V_{EE} 11
BIPOLAR OFFSET, BIP OFF 12
10V INPUT 13
20V INPUT 14
HI-774
28 STATUS, STS
27 DB11 MSB
26 DB10
25 DB9
24 DB8
23 DB7
22 DB6
21 DB5
20 DB4
19 DB3
18 DB2
17 DB1
16 DB0 LSB
15 DIGITAL COMMON
DIGITAL
DATA
OUTPUTS

HI-774 Block Diagram


BIT OUTPUTS
MSB
LSB
27
26
25
24
23
22
21
20
19
18
17
16
NIBBLE* A
NIBBLE* B
NIBBLE* C
THREE-STATE BUFFERS AND CONTROL
12/$\overline{8}$
$\overline{CS}$
A_0
R/$\overline{C}$
CE
2
3
4
5
6
CONTROL LOGIC
12 BITS
1
V_{LOGIC}
15
DIGITAL COMMON
OSCILLATOR
CLK
SSAR™
28
STS
STROBE
DIGITAL CHIP
ANALOG CHIP
12 BITS
7
V_{CC}
11
V_{EE}
10
V_{REF} IN
8
V_{REF} OUT
DAC
COMP.
10K
+10V REF.
5K
10K
5K
5K
2.5K
9
ANALOG COMMON
12
BIP. OFF
14
20V INPUT
13
10V INPUT

*("NIBBLE" IS A 4 BIT DIGITAL WORD.)

Die Characteristics

Analog Die	Bipolar, DI
Digital Die	CMOS, JI
Transistor Count	~2100

DC and Transfer Accuracy Specifications

(T_A = +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V unless otherwise specified)

MODEL	HI-774J	HI-774K	HI-774L	UNITS
Temperature Range	0 to +75			°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	±1/2	LSB
Differential Linearity Error				
(Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
Tmin to Tmax	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max)				
(Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
Tmin to Tmax				
(No adjustmeat at +25°C)	0.5	0.4	0.35	% of F.S.
(With adjustment to zero at +25°C)	0.22	0.12	0.05	% of F.S.
Temperature Coefficients (see definitions)				
Guaranteed max change, Tmin to Tmax (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
Bipolar Offset	±2	±1	±1	LSB
Full Scale Calibration	±9	±5	±2	LSB
Power Supply Rejection				
Max change in Full Scale Calibration				
$+13.5V<V_{CC}<+16.5V$ or $+11.4V<V_{CC}<+12.6V$	±2	±1	±1	LSB
$+4.5V<V_{LOGIC}<+5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V<V_{EE}<-13.5$ or $-12.6<V_{EE}<-11.4V$	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	-5 to +5 -10 to +10			Volts Volts
Unipolar	0 to +10 0 to +10			Volts Volts
Input Impedance				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	-11.4 to -16.5			Volts
Operating Current				
I_{LOGIC}	8 TYP, 17 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} -15V Supply	21 TYP, 28 MAX			mA
Power Dissipation ±15V, +5V Supplies	520 TYP, 730 MAX			mW
±12V, +5V Supplies	390 TYP			mW
Internal Reference Voltage	+10.00 ± 0.1 MAX			Volts
Output current, ① available for external loads (External load should not change during conversion).	2.0 MAX			mA

① When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.

Digital Characteristics (All Models, Over Full Temperature Range)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A_O, 12/$\overline{8}$)			
Logic "1"	+2.0V		+5.5V
Logic "0"	-0.5V		+0.8V
Current		0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Logic "1" (I_{SOURCE} — 10μA)	+4.5V		
Leakage (High Z State, DB11-DB0 only)		±0.1μA	±5μA
Capacitance		5pF	

HI-774 Timing Specifications (25°C unless otherwise specified.)

Into a load with $R_L = 2K\Omega$ and $C_L = 10pF$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS Delay from CE		100	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low during CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low during CE High	50	20		ns
t_{SAC}	A_O to CE Setup	0	0		ns
t_{HAC}	A_O Valid during CE High	50	30		ns
t_C	Conversion time,12 bit cycle T_{min} to T_{max}	7	8.5	9	μs
	8 bit cycle T_{min} to T_{max}	5.25	6.4	6.8	μs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data Valid after CE low	25	35		ns
t_{HL}	Output float delay		70	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0		ns
t_{SAR}	A_O to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid after CE low	0	0		ns
t_{HRR}	R/$\overline{C}$ high after CE low	0	0		ns
t_{HAR}	A_O valid after CE low	50	25		ns
t_{HS}	STS delay after data valid		90	300	ns

NOTE: Time is measured from 50% level of digital transitions, except High Z output conditions which are measured at the 10% or 90% point.

Absolute Maximum Ratings (Specifications apply to all grades, except where noted)

V_{CC} to Digital Common	0 to +16.5V
V_{EE} to Digital Common	0 to -16.5V
V_{LOGIC} to Digital Common	0 to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_O, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common	-0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common	±16.5V
$20V_{IN}$ to Analog Common	±24V

REF OUT	Indefinite short to common Momentary short to V_{CC}
Chip Temperature	+175°C
Total Power Dissipation *	2125mW
Lead Temperature, Soldering	300°C, 10 sec.
Storage Temperature	-65°C to +150°C
Thermal Resistance, θ_{JA}	47°C/W
θ_{JC}	14°C/W

* Derate 21.3mW/°C above 75°C

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-774K and L, grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-774J grade is guaranteed to ±1LSB max error. For this grade, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-774 K and L grades which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temerature ranges. The HI-774J grade guarantees no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

Temperature Coefficients

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at Tmin or Tmax.

Power Supply Rejection

The standard specifications for the HI-774 assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-Justified Data

The data format used in the HI-774 is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-774

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout—

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-774 (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-774 ground currents are 6mADC into pin 9 (Analog Common) and 3mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 3mA of DC current. (Code dependent currents flow in the VCC, VEE and VLOGIC terminals, but not through the HI-774's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device driving the HI-774 analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change as much as ±400mV with each bit decision. These input disturbances are caused by the internal DAC changing codes which causes a glitch on the summing junction. This creates abrupt changes in current at the analog input causing a "kick back" glitch from the input. Because the algorithm starts with the MSB, the first glitches will be the largest and get smaller as the conversion proceeds. These glitches can occur at 350ns intervals so an op-amp with a low output impedance and fast settling is desirable. Ultimately, the input must settle to within the window of figure 1 at the bit decision points in order to achieve 12 bit accuracy.

The HI-774 differs from the most high-speed successive approximation type ADC's in that it does not require a high performance buffer or sample and hold. With error correction the input can settle while the conversion is underway, but only during the first 4.8μs. The input must be within ±0.76% of the final value when the MSB decision is made. This occurs approximately 650ns after the conversion has been initiated. Digital error correction also loosens the bandwidth requirements of the buffer or sample and hold. As long as the input "kick back" disturbances settle within the window of figure 1 the device will remain accurate. The combined effect of settling and the "kick back' disturbances must remain in the figure 1 window.

If the design is being optimized for speed, the input device should have a closed loop bandwidth to 3MHz, and a low output impedance (calculated by dividing the open loop output resistance by the open loop gain). If the application requires a high speed sample and hold the Harris HA-5330 or HA-5320 are recommended.

In any design the input (pin 13 or 14) should be checked during a conversion to make sure that the input stays within the correctable window of figure 1.

DIGITAL ERROR CORRECTION

The HI-774 features the smart sucessive approximation register (SSAR™) which includes digital error correction. This has the advantage of allowing the initial input to vary within a +31 to -32LSB window about the final value. The input can move during the first 4.8μs, after which it must remain stable within ±½LSB. With this feature a conversion can start before the input has settled completely; however, it must be within the window as described in Figure 1.

The conversion cycle starts by making the first 8-bit decisions very quickly, allowing the internal DAC to settle only to 8-bit accuracy. Then the converter goes through two error correction cycles. At this point the input must be stable within ±½LSB. These cycles correct the 8-bit word to 12-bit accuracy for any errors made (up to +16 or -32 bits). This is up one count or down two counts at 8-bit resolution. The converter then continues to make the 4LSB decisions, settling out to 12-bit accuracy. The last four bits can adjust the code in the positive direction by up to 15 bits. This results in a total correction range of +31 to -32 bits. When an 8-bit conversion is performed, the input must settle to within ±½LSB at 8 bit resolution (which equals ±8 bits at 12-bit resolution).

With the HI-774 a conversion can be initiated before the input has completely settled, as long as it meets the constraints of the Figure 1 window. This allows the user to start conversion up to 4.8μs earlier than with a typical analog to digital converter. A typical successive approximation type ADC must have a constant input during a conversion because once a bit decision is made it is locked in and cannot change.

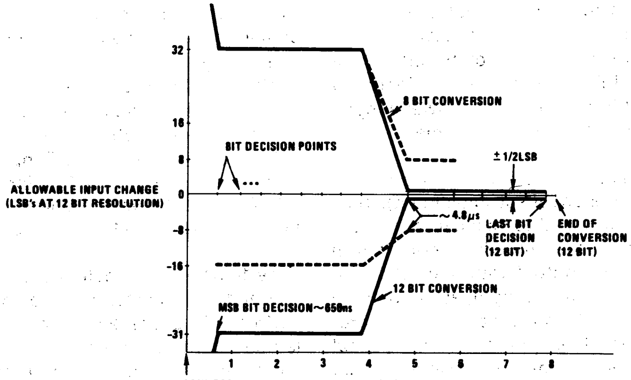


FIGURE 1. HI-774 ERROR CORRECTION WINDOW VS. TIME

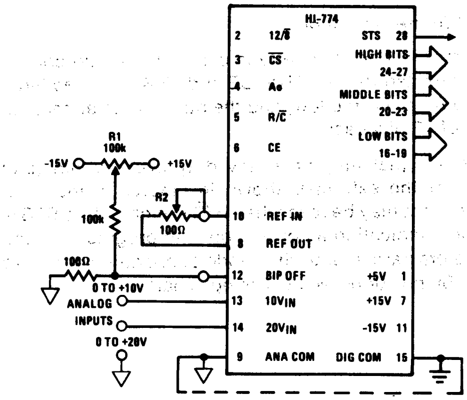

HI-774
2
12/$\overline{8}$
3
$\overline{CS}$
4
Ao
5
R/$\overline{C}$
6
CE
STS 28
HIGH BITS 24-27
MIDDLE BITS 20-23
LOW BITS 16-19
R1 100k
-15V
+15V
100k
R2
100Ω
10 REF IN
8 REF OUT
100Ω
12 BIP OFF
0 TO +10V
ANALOG INPUTS
0 TO +20V
13 10V$_{IN}$
14 20V$_{IN}$
9 ANA COM
+5V 1
+15V 7
-15V 11
DIG COM 15

FIGURE 2. UNIPOLAR CONNECTIONS

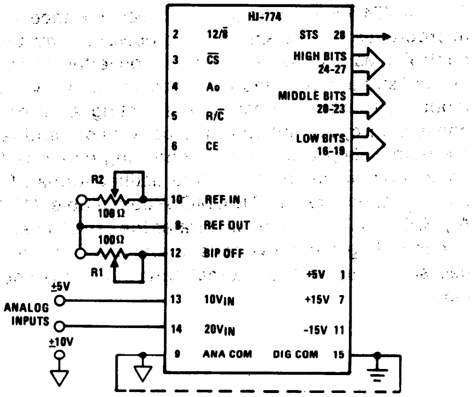

HI-774
2
12/$\overline{8}$
3
$\overline{CS}$
4
Ao
5
R/$\overline{C}$
6
CE
STS 28
HIGH BITS 24-27
MIDDLE BITS 20-23
LOW BITS 16-19
R2
100Ω
10 REF IN
8 REF OUT
100Ω
12 BIP OFF
R1
±5V
ANALOG INPUTS
±10V
13 10V$_{IN}$
14 20V$_{IN}$
9 ANA COM
+5V 1
+15V 7
-15V 11
DIG COM 15

FIGURE 3. BIPOLAR INPUT CONNECTIONS

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-774 is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-774 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration—

Refer to figure 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem—the converter operates normally.

Calibration consists in adjusting the converters's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is settling the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +½LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1½LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration—

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage ½LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1½LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

*The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48 range, add a 500Ω potentiometer in series with the pin 14.

Controlling the HI-774

The HI-774 includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/$\overline{8}$, $\overline{CS}$, A_O, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$. Also, CE and 12/8 are wired high, $\overline{CS}$ and A_O are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed in the "Stand-Alone Mode Timing" chart.

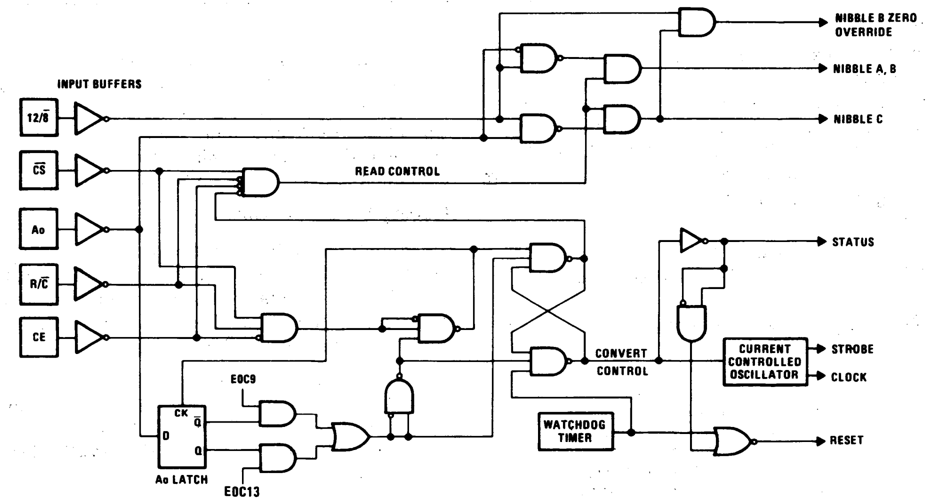

NIBBLE B ZERO OVERRIDE
NIBBLE A, B
NIBBLE C
INPUT BUFFERS
12/8̄
CS̄
A0
R/C̄
CE
READ CONTROL
STATUS
CONVERT CONTROL
CURRENT CONTROLLED OSCILLATOR
STROBE
CLOCK
EOC9
CK
Q̄
D
Q
A0 LATCH
EOC13
WATCHDOG TIMER
RESET

FIGURE 4. HI-774 CONTROL LOGIC

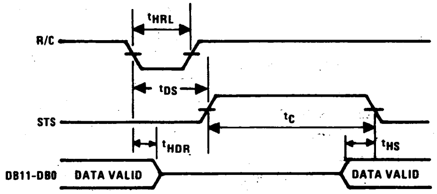

tHRL
R/C
tDS
STS
tC
tHDR
tHS
DB11-DB0
DATA VALID
DATA VALID

FIGURE 5. LOW PULSE FOR R/C—OUTPUTS ENABLED AFTER CONVERSION

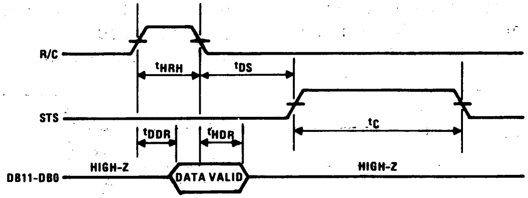

R/C
tHRH
tDS
STS
tC
tDDR
tHDR
HIGH-Z
DB11-DB0
DATA VALID
HIGH-Z

FIGURE 6. HIGH PULSE FOR R/C—OUTPUTS ENABLE WHILE R/C HIGH, OTHERWISE HIGH-Z

Stand-Alone Mode Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/C Pulse Width	50			ns
t_{DS}	STS Delay from R/C			200	ns
t_{HDR}	Data Valid After R/C Low	20			ns
t_{HS}	STS Delay After Data Valid		90	300	ns
t_{HRH}	High R/C Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_O, which determines whether the conversion continues for 12 bits (A_O low) or stops with 8 bits (A_O high). If all 12 bits are read following an 8 bit conversion, the last three LSB's will read zero and DB3 will read ONE. A_O is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

TABLE 1
TRUTH TABLE FOR HI-774 CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_o	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-774 Timing Specifications, Convert mode.

This variety of HI-774 control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high.

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_O. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_O input is ignored.

With 12/8 low, the output is organized in two 8 bit bytes, selected one at a time by A_O. This allows an 8 bit data bus to be connected as shown in figure 9. A_O is usually tied to the least significant bit of the address bus, for storing the HI-774 output in two consecutive memory locations. (With A_O low, the 8 MSB's only are enabled. With A_O high, 4 MSB's are disabled, bits 4 through 7 are forced low, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:

BYTE 1	BYTE 2
• X X X X X X X X	X X X X 0 0 0 0
MSB	LSB

Further, A_O may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

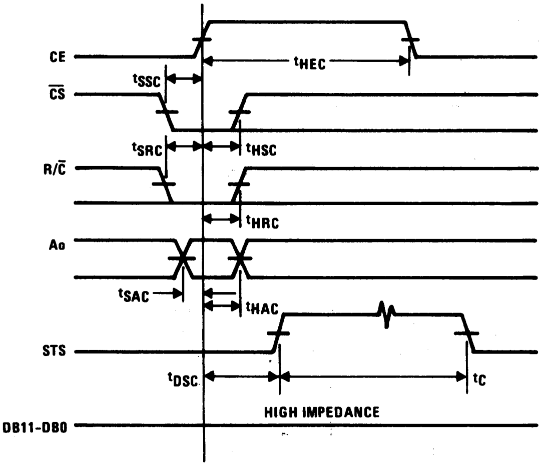


FIGURE 7. CONVERT START TIMING

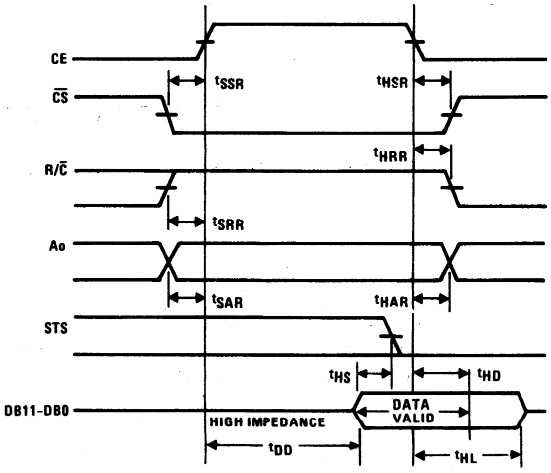


FIGURE 8. READ CYCLE TIMING

See HI-774 Timing Specifications for more information

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. See Figure 8.

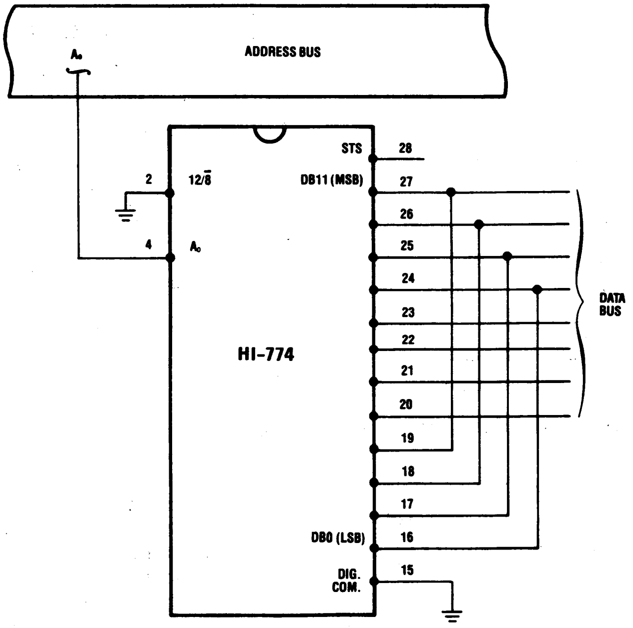

A_0
ADDRESS BUS
2
$12/\overline{8}$
4
A_0
HI-774
STS
28
DB11 (MSB)
27
26
25
24
23
22
21
20
19
18
17
DB0 (LSB)
16
DIG. COM.
15
DATA BUS

FIGURE 9. INTERFACE TO AN 8 BIT DATA BUS

HARRIS

HI-774A

ADVANCED

7µs, Complete 12-Bit A/D Converter With Microprocessor Interface

Features

- Complete 12 Bit A/D Converter With Reference and Clock
- Digital Error Correction
- Full 8-, 12-, or 16-Bit Microprocessor Bus Interface
- 150 nS Buss Access Time
- No Missing Codes Over Temperature
- Minimal Setup Time For Control Signals
- 8µs Maximum Conversion Time Over Temperature
- Low Noise, Via Current-mode signal transmission between chips
- Byte enable/short cycle (Ao Input)
  - ▶ Guarantees break-before-make action, eliminating bus contention during read operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Faster Version of the HI-574A and HI-674A
- Same Pin-Out as HI-574A and HI-674A
- ±12V to ±15V Operation

Applications

- Military and Industrial Data Acquisition Systems
- Electronics Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-774A is a complete 12 bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28-pin package. The bipolar analog die features the Harris Dielectric Isolation process, whch provides enhanced AC performance and freedom from latch-up. The digital die features the smart SAR (SSAR™), which includes a digital error correction circuit.

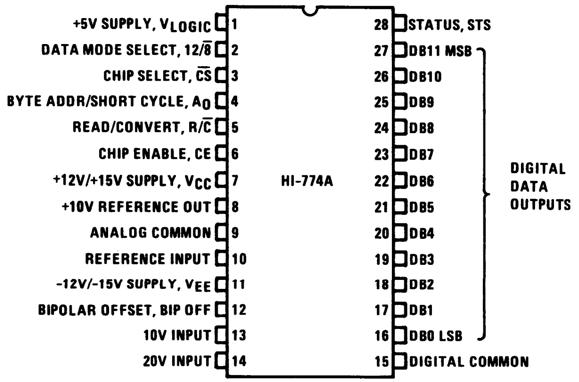
Custom design of each IC (bipolar and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current controlled for excellent stability over temperature. The oscillator is trimmed for a guaranteed conversion time of 7 ± 1µs over temperature.

The HI-774A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity gain and offset accuracy. The low noise buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 390mW at ±12V. Three electrical grades each are offered for the commercial and military temperature ranges. All models are packaged in a 28 pin side-brazed, ceramic DIP. For information on MIL-STD-883 compliant device's request the HI-774A/883 data sheet.

Pinout

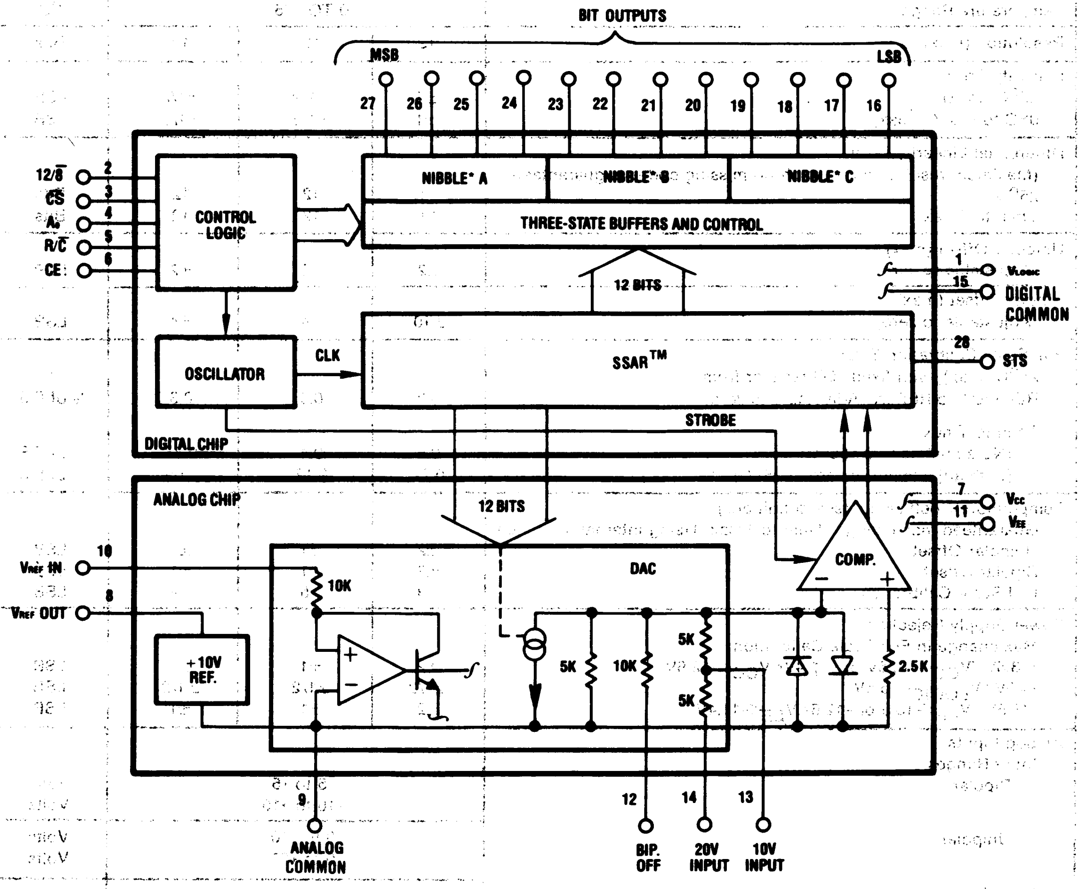
TOP VIEW



+5V SUPPLY, V_{LOGIC} 1
DATA MODE SELECT, 12/$\overline{8}$ 2
CHIP SELECT, $\overline{CS}$ 3
BYTE ADDR/SHORT CYCLE, A_0 4
READ/CONVERT, R/$\overline{C}$ 5
CHIP ENABLE, CE 6
+12V/+15V SUPPLY, V_{CC} 7
+10V REFERENCE OUT 8
ANALOG COMMON 9
REFERENCE INPUT 10
-12V/-15V SUPPLY, V_{EE} 11
BIPOLAR OFFSET, BIP OFF 12
10V INPUT 13
20V INPUT 14
HI-774A
28 STATUS, STS
27 DB11 MSB
26 DB10
25 DB9
24 DB8
23 DB7
22 DB6
21 DB5
20 DB4
19 DB3
18 DB2
17 DB1
16 DB0 LSB
15 DIGITAL COMMON
DIGITAL DATA OUTPUTS

HI-774A Block Diagram

Block Diagram


BIT OUTPUTS
MSB
LSB
27
26
25
24
23
22
21
20
19
18
17
16
12/$\overline{8}$
$\overline{CS}$
A_0
R/$\overline{C}$
CE
2
3
4
5
6
CONTROL LOGIC
NIBBLE* A
NIBBLE* B
NIBBLE* C
THREE-STATE BUFFERS AND CONTROL
12 BITS
1
V_{LOGIC}
15
DIGITAL COMMON
OSCILLATOR
CLK
SSAR™
28
STS
STROBE
DIGITAL CHIP
ANALOG CHIP
12 BITS
7
V_{CC}
11
V_{EE}
10
V_{REF} IN
8
V_{REF} OUT
10K
DAC
COMP.
+10V REF.
5K
10K
5K
5K
2.5K
9
ANALOG COMMON
12
BIP. OFF
14
20V INPUT
13
10V INPUT

*("NIBBLE" IS A 4 BIT DIGITAL WORD.)

Die Characteristics

Analog Die	Bipolar, DI
Digital Die	CMOS, JI
Transistor Count	~2100

DC and Transfer Accuracy Specifications

(T_A = +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

MODEL	HI-774AJ	HI-774AK	HI-774AL	UNITS
Temperature Range	0 TO +75			°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	±1/2	LSB
Differential Linearity Error (Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
Tmin to Tmax	11	12	12	Bits
Unipolar Offset (max) (Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max) (Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
Tmin to Tmax				
(No adjustment at +25°C)	0.5	0.4	0.35	% of F.S.
(With adjustment to zero at 25°C)	0.22	0.12	0.05	% of F.S.
Temperature Coefficients (see definitions) Guaranteed max change, Tmin to Tmax (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
Bipolar Offset	±2	±1	±1	LSB
Full Scale Calibration	±9	±5	±2	LSB
Power Supply Rejection Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5 or −12.6<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5			Volts
	−10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	8 TYP, 17 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} −15V Supply	21 TYP, 28 MAX			mA
Power Dissipation ±15V, +5V Supplies	520 TYP, 730 MAX			mW
Power Dissipation ±12V, +5V Supplies	390 TYP			mW
Internal Reference Voltage	+10.00 ± 0.1 MAX			Volts
Output current, ① available for external loads (External load should not change during conversion).	2.0 MAX			mA

① When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.

DC and Transfer Accuracy Specifications

(T_A = -25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V unless otherwise specified)

MODEL	HI-774AS	HI-774AT	HI-774AU	UNITS
Temperature Range	-55 to +125			°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1	±1	LSB
Differential Linearity Error				
(Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
Tmin to Tmax	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max)				
(Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
Tmin to Tmax				
(No adjustment at +25°C)	0.8	0.6	0.4	% of F.S.
(With adjustment to zero at 25°C)	0.5	0.25	0.12	% of F.S.
Temperature Coefficients (see definitions)				
Guaranteed max change, Tmin to Tmax (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
Bipolar Offset	±4	±2	±2	LSB
Full Scale Calibration	±20	±10	±5	LSB
Power Supply Rejection				
Max change in Full Scale Calibration				
$+13.5V < V_{CC} < +16.5V$ or $+11.4V < V_{CC} < +12.6V$	±2	±1	±1	LSB
$+4.5V < V_{LOGIC} < +5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V < V_{EE} < -13.5$ or $-12.6 < V_{EE} < -11.4V$	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	-5 to +5			Volts
	-10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	-11.4 to -16.5			Volts
Operating Current				
I_{LOGIC}	8 TYP, 17 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} -15V Supply	21 TYP, 28 MAX			mA
Power Dissipation ±15V, +5V Supplies	520 TYP, 730 MAX			mW
±12V +5V Supplies	390 TYP			mW
Internal Reference Voltage	+10.00 ± 0.1 MAX			Volts
Output current, ① available for external loads (External load should not change during conversion).	2.0 MAX			mA

① When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.

Digital Characteristics (All models, over full temp. range)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, $R/\overline{C}$, AO, 12/8)			
Logic "1"	+2.0V		+5.5V
Logic "0"	-0.5V		+0.8V
Current		0.1μA	5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Logic "1" (I_{SOURCE} — 10μA)	+4.5V		
Leakage (High Z State, DB11-DB0, Only)		±0.1μA	±5μA
Capacitance		5pF	

HI-774A Timing Specifications (25°C unless otherwise specified.)

Into a load of R_L = 2KΩ and C_L = 10pF

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Convert Mode					
t_{DSC}	STS Delay from CE		100	200	nS
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		nS
t_{HSC}	$\overline{CS}$ Low during CE High	50	20		nS
t_{SRC}	$R/\overline{C}$ to CE Setup	50	0		nS
t_{HRC}	$R/\overline{C}$ Low during CE High	50	20		nS
t_{SAC}	A_O to CE Setup	0	0		nS
t_{HAC}	A_O Valid during CE High	50	30		nS
t_c	Conversion time,12 bit cycle T_{min} to T_{max}	6	7	8	μS
	8 bit cycle T_{min} to T_{max}		4.5	6	μS
Read Mode					
t_{DD}	Access time from CE		75	150	nS
t_{HD}	Data Valid after CE low	25	35		nS
t_{HL}	Output float delay		70	150	nS
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		nS
t_{SRR}	$R/\overline{C}$ to CE Setup	0	0		nS
t_{SAR}	A_O to CE Setup	50	25		nS
t_{HSR}	$\overline{CS}$ Valid after CE low	0	0		nS
t_{HRR}	$R/\overline{C}$ high after CE low	0	0		nS
t_{HAR}	A_O valid after CE low	50	25		nS
t_{HS}	STS delay after data valid		90	300	nS

Note: Time is measured from 50% level of digital transitions, except three state conditions which are measured at the 10% or 90% point.

Absolute Maximum Ratings (Specifications apply to all grades, except where noted)

V_{CC} to Digital Common .... 0 to +16.5V
V_{EE} to Digital Common .... 0 to -16.5V
V_{LOGIC} to Digital Common .... 0 to +7V
Analog Common to Digital Common .... ±1V
Control Inputs (CE, CS, A_O, 12/8, R/C) to
Digital Common .... -0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to
Analog Common .... ±16.5V
$20V_{IN}$ to Analog Common .... ±24V

REF OUT .... Indefinite short to common
Momentary short to V_{CC}
Chip Temperature .... +175°C
Total Power Dissipation* 2125mW
Lead Temperature, Soldering .... 300°C, 10 sec.
Storage Temperature .... -65°C to +150°C
Thermal Resistance, θ_{JA} .... 47°C/W
θ_{JC} .... 14°C/W

* Derate 21.3mW/°C above 75°C

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-774AK,AL, AT, and AU, grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-774AJ, and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-774AK, AL, AT, and AU grades which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-774AJ, and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

Temperature Coefficients

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at Tmin or Tmax.

Power Supply Rejection

The standard specifications for the HI-774A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-Justified Data

The data format used in the HI-774A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-774A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout—

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-774A (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (VLOGIC supply), one from pin 7 to 9 (VCC to Analog Common) and one from pin 11 to 9 (VEE to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-774A ground currents are 6mADC into pin 9 (Analog Common) and 3mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 3mA of DC current. (Code dependent currents flow in the VCC, VEE and VLOGIC terminals, but not through the HI-774A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device driving the HI-774A analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change as much as ±400mV with each bit decision. These input disturbances are caused by the internal DAC changing codes which causes a glitch on the summing junction. This creates abrupt changes in current at the analog input causing a "kick back" glitch from the input. Because the algorithm starts with the MSB, the first glitches will be the largest and get smaller as the conversion proceeds. These glitches can occur at 350nS intervals so an op-amp with a low output impedance and fast settling is desirable. Ultimately, the input must settle to within the window of figure 1 at the bit decision points in order to achieve 12 bit accuracy.

The HI-774A differs from the most high-speed successive approximation type ADC's in that it does not require a high performance buffer or sample and hold. With error correction. The input can settle while the conversion is underway, but only during the first 4.2μS. The input must be within ±0.76% of the final value when the MSB decision is made. This occurs approximately 600nS after the conversion has been initiated. Digital error correction also loosens the bandwidth requirements of the buffer or sample and hold. As long as the input "kick back" disturbances settle within the window of figure 1 the device will remain accurate. The combined effect of settling and the "kick back' disturbances must remain in the figure 1 window.

If the design is being optimized for speed, the input device should have a closed loop bandwidth to 3MHz, and a low output impedance (calculated by dividing the open loop output resistance by the open loop gain). If the application requires a high speed sample and hold the Harris HA-5330 or HA-5320 are recommended.

In any design the input (pin 13 or 14) should be checked during a conversion to make sure that the input stays within the correctable window of figure 1.

DIGITAL ERROR CORRECTION

The HI-774A features the smart sucessive approximation register (SSAR™) which includes digital error correction. This has the advantage of allowing the initial input to vary within a +31 to -32LSB window about the final value. The input can move during the first 4.2μs, after which it must remain stable within ±½LSB. With this feature a conversion can start before the input has settled completely; however, it must be within the window as described in Figure 1.

The conversion cycle starts by making the first 8-bit decisions very quickly, allowing the internal DAC to settle only to 8-bit accuracy. Then the converter goes through two error correction cycles. At this point the input must be stable within ±½LSB. These cycles correct the 8-bit word to 12-bit accuracy for any errors made (up to +16 or -32 bits). This is up one count or down two counts at 8-bit resolution. The converter then continues to make the 4LSB decisions, settling out to 12-bit accuracy. The last four bits can adjust the code in the positive direction by up to 15 bits. This results in a total correction range of +31 to -32 bits. When an 8-bit conversion is performed, the input must settle to within ±½LSB at 8 bit resolution (which equals ±8 bits at 12-bit resolution).

With the HI-774A a conversion can be initiated before the input has completely settled, as long as it meets the constraints of the Figure 1 window. This allows the user to start conversion up to 4.2μs earlier than with a typical analog to digital converter. A typical successive approximation type ADC must have a constant input during a conversion because once a bit decision is made it is locked in and cannot change.

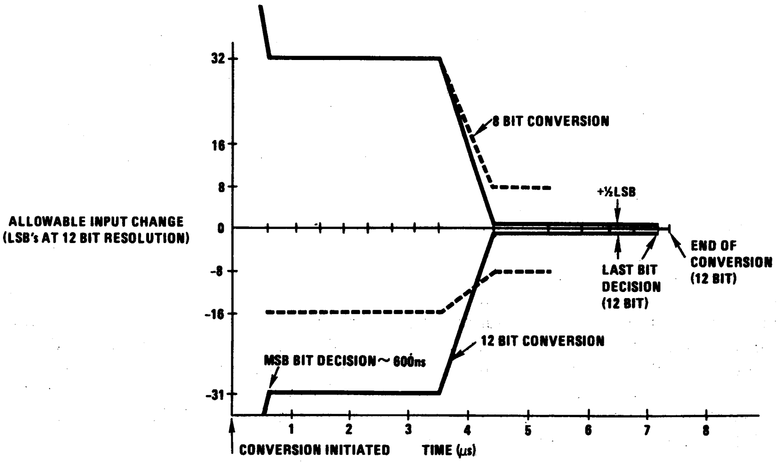


FIGURE 1. HI-774A ERROR CORRECTION WINDOW VS. TIME

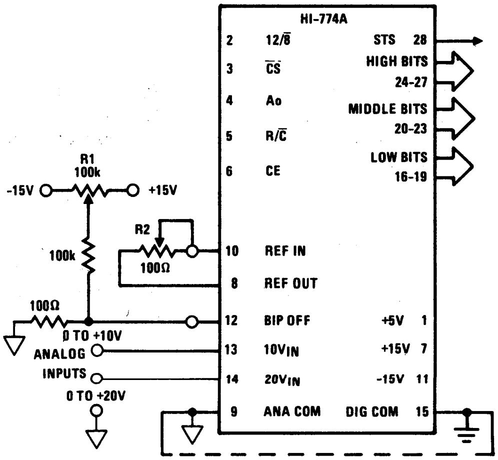

HI-774A
2 12/$\overline{8}$
3 $\overline{CS}$
4 Ao
5 R/$\overline{C}$
6 CE
10 REF IN
8 REF OUT
12 BIP OFF
13 10VIN
14 20VIN
9 ANA COM
STS 28
HIGH BITS 24-27
MIDDLE BITS 20-23
LOW BITS 16-19
+5V 1
+15V 7
-15V 11
DIG COM 15
R1 100k
-15V
+15V
R2
100Ω
100k
100Ω
0 TO +10V
ANALOG INPUTS
0 TO +20V

FIGURE 2. UNIPOLAR CONNECTIONS

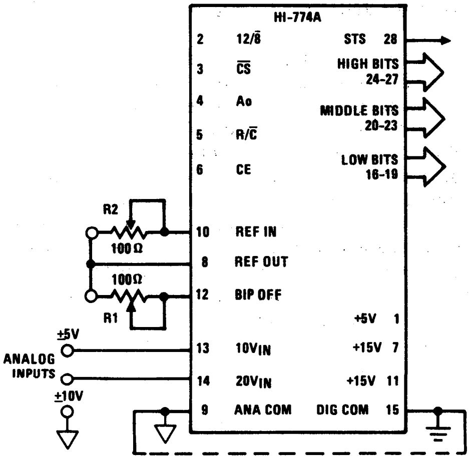

HI-774A
2 12/$\overline{8}$
3 $\overline{CS}$
4 Ao
5 R/$\overline{C}$
6 CE
10 REF IN
8 REF OUT
12 BIP OFF
13 10VIN
14 20VIN
9 ANA COM
STS 28
HIGH BITS 24-27
MIDDLE BITS 20-23
LOW BITS 16-19
+5V 1
+15V 7
+15V 11
DIG COM 15
R2
100Ω
100Ω
R1
±5V
ANALOG INPUTS
±10V

FIGURE 3. BIPOLAR INPUT CONNECTIONS

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-774A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-774A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration—

Refer to figure 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V-to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem—the converter operates normally.

Calibration consists of adjusting the converters's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is settling the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +½LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1½LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration—

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage ½LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1½LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

*The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48 range, add a 500Ω potentiometer in series with the pin 14.

Controlling the HI-774A

The HI-774A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS- compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed in the "Stand-Alone Mode Timing" chart.

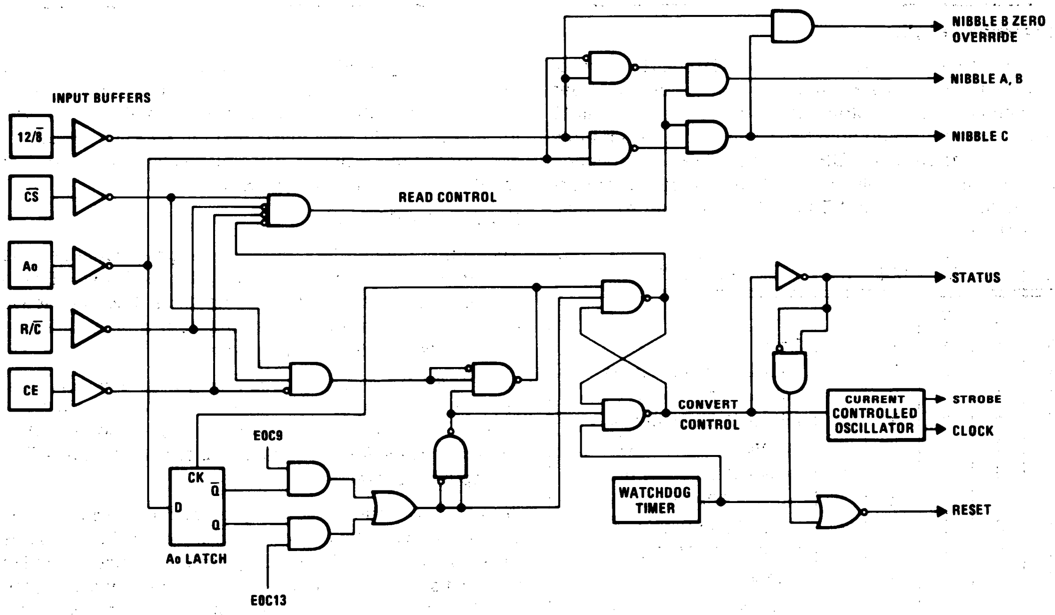

INPUT BUFFERS
12/$\overline{8}$
$\overline{CS}$
A0
R/$\overline{C}$
CE
READ CONTROL
NIBBLE B ZERO OVERRIDE
NIBBLE A, B
NIBBLE C
STATUS
CONVERT CONTROL
CURRENT CONTROLLED OSCILLATOR
STROBE
CLOCK
WATCHDOG TIMER
RESET
EOC9
CK
$\overline{Q}$
D
Q
A0 LATCH
EOC13

FIGURE 4. HI-774A CONTROL LOGIC

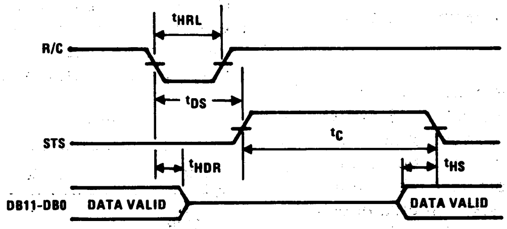

t_{HRL}
R/C
t_{DS}
STS
t_C
t_{HDR}
t_{HS}
DB11-DB0
DATA VALID
DATA VALID

FIGURE 5. LOW PULSE FOR R/$\overline{C}$—OUTPUTS ENABLED AFTER CONVERSION

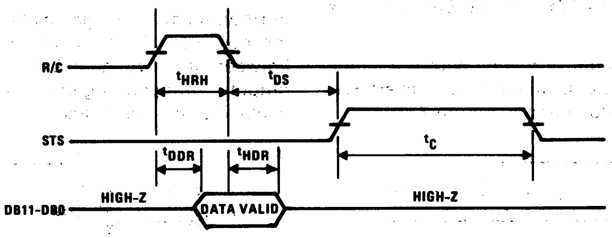

R/C
t_{HRH}
t_{DS}
STS
t_C
t_{DDR}
t_{HDR}
HIGH-Z
DB11-DB0
DATA VALID
HIGH-Z

FIGURE 6. HIGH PULSE FOR R/$\overline{C}$—OUTPUTS ENABLE WHILE R/$\overline{C}$ HIGH, OTHERWISE HIGH-Z

Stand-Alone Mode Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	20			ns
t_{HS}	STS Delay After Data Valid		90	300	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_O, which determines whether the conversion continues for 12 bits (A_O low) or stops with 8 bits (A_O high). If all 12 bits are read following an 8 bit conversion, the last three LSB's will read zero, and DB3 will read ONE. A_O is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 Bit Conversion
↑	0	0	X	1	Initiate 8 Bit Conversion
1	↑	0	X	0	Initiate 12 Bit Conversion
1	↑	0	X	1	Initiate 8 Bit Conversion
1	0	↑	X	0	Initiate 12 Bit Conversion
1	0	↑	X	1	Initiate 8 Bit Conversion
1	0	1	1	X	Enable 12 Bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

TABLE 1
TRUTH TABLE FOR HI-774A CONTROL INPUTS

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necesary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-774A Timing Specifications, Convert mode.

This variety of HI-774A control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

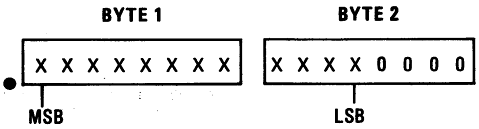
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high.

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and Ao. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The Ao input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_O. This allows an 8 bit data bus to be connected as shown in Figure 9. A_O is usually tied to the least significant bit of the address bus, for storing the HI-774A output in two consecutive memory locations. (With A_O low, the 8 MSB's only are enabled. With A_O high, 4 MSB's are disabled, bits 4 through 7 are forced low, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_O may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

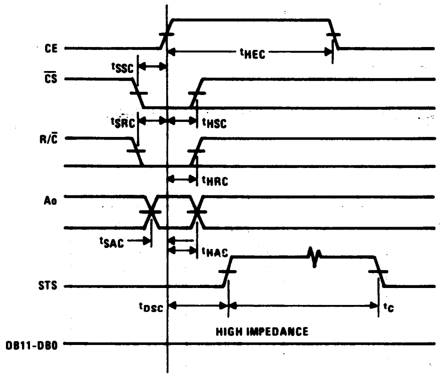


FIGURE 7. CONVERT START TIMING

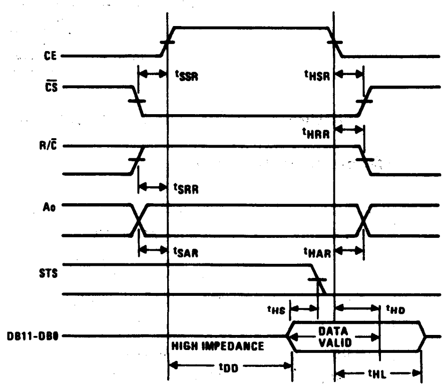
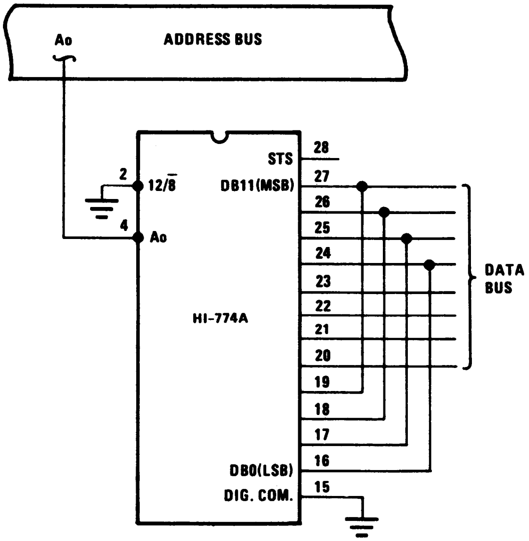


FIGURE 8. READ CYCLE TIMING

See HI-774A Timing Specifications for more information.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. See figure 8.



Ao
ADDRESS BUS
2
12/$\overline{8}$
4
Ao
HI-774A
STS
DB11(MSB)
DB0(LSB)
DIG. COM.
28
27
26
25
24
23
22
21
20
19
18
17
16
15
DATA BUS

FIGURE 9. INTERFACE TO AN 8 BIT DATA BUS

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. See figure 8.

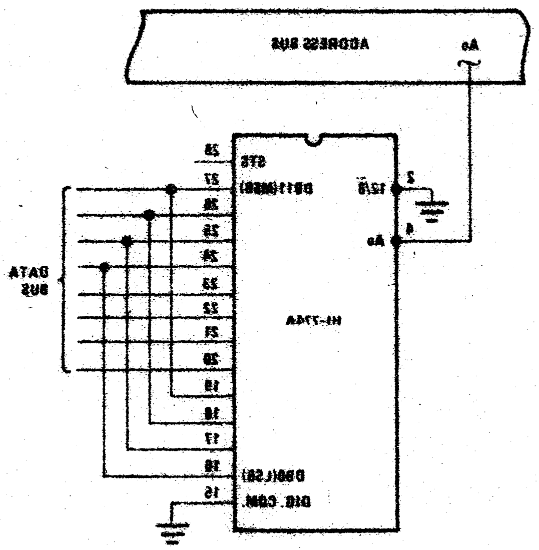

ADDRESS BUS
A0
STS
28
27
DB11(MSB)
26
25
24
23
22
21
20
19
18
17
16
DB0(LSB)
15
DIG. COM.
2
12/8
4
A0
HI-774A
DATA BUS

FIGURE 9. INTERFACE TO AN 8 BIT DATA BUS

HARRIS

HY-9574

ADVANCED

Sampling 12 Bit A/D Converter with 8/16 Bit μP Interface

Features

- Complete 12 Bit Sampling A/D Converter with Reference and Clock
- Throughput Rate (Typical) 48kHz
- 32 Pin Plastic Dual-In-Line Package

A/D Converter Features

- Full 8-, 12- or 16 Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Setup Time for Control Signals
- 25μs Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (Ao Input)

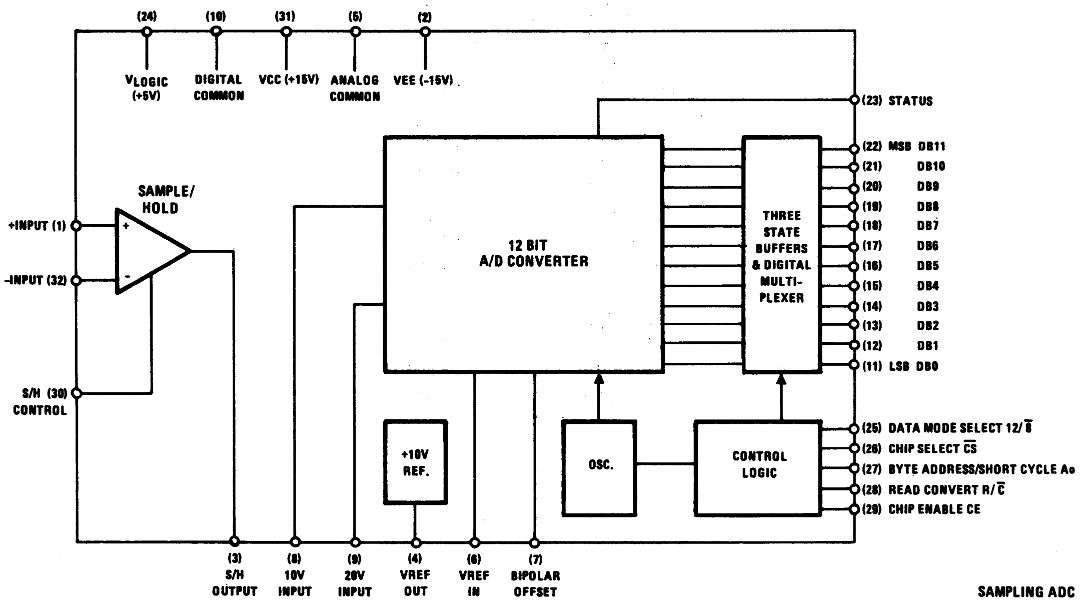
Applications

- Precision Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems
- Peak Detectors

Sample/Hold Features

- Gain DC .... 2×10^6 V/V
- Acquisition Time.................................. 1.0μs (±0.01%)
- Droop Rate .... 0.08μV/μs (25°C)
  2.4μV/μs (Full Temp.)
- Aperture Time 25ns
- Pedestal Error 1.0mV
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible

Functional Diagram


(24) VLOGIC (+5V)
(10) DIGITAL COMMON
(31) VCC (+15V)
(5) ANALOG COMMON
(2) VEE (-15V)
SAMPLE/HOLD
+INPUT (1)
-INPUT (32)
S/H (30) CONTROL
12 BIT A/D CONVERTER
THREE STATE BUFFERS & DIGITAL MULTI-PLEXER
+10V REF.
OSC.
CONTROL LOGIC
(23) STATUS
(22) MSB DB11
(21) DB10
(20) DB9
(19) DB8
(18) DB7
(17) DB6
(16) DB5
(15) DB4
(14) DB3
(13) DB2
(12) DB1
(11) LSB DB0
(25) DATA MODE SELECT 12/$\overline{8}$
(26) CHIP SELECT $\overline{CS}$
(27) BYTE ADDRESS/SHORT CYCLE Ao
(28) READ CONVERT R/$\overline{C}$
(29) CHIP ENABLE CE
(3) S/H OUTPUT
(8) 10V INPUT
(9) 20V INPUT
(4) VREF OUT
(6) VREF IN
(7) BIPOLAR OFFSET
SAMPLING ADC

Description

The HY-9574 is designed for use in precision, high speed data acquisition systems. The Harris Sample/Hold amplifier (HA-5320) and 12 bit A/D converter (HI-574A) have been combined in a single package to reduce package count and to insure component compatibility.

The Sample/Hold (HA-5320) circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The device includes a hold capacitor, so no external hold capacitor is required.

The Sample and Hold chip (HA-5320) is manufactured using the Harris Dielectric Isolation process, which minimizes stray capacitance and eliminates SCR's. This allows higher speed and latch-free operation.

The 12 bit successive approximation Analog-to-Digital section is an HA-574A chip set. It includes a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

Custom design of each IC (Bipolar Analog and CMOS Digital) has yielded improved versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20 ± 1μs.

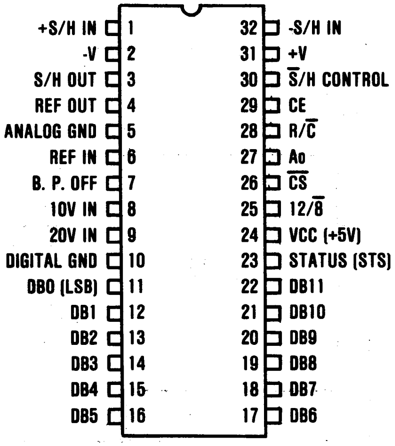
The Sample/Hold and ADC stages are not connected internally to provide maximum flexibility to the designer.

The HY-9574 offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are ±15V and +5V, with typical dissipation of 850mW. All models are packaged in a 32 pin plastic DIP with 600 mil row centers.

Pinout

TOP VIEW



HY-9574 System Specifications

Absolute Maximum Ratings

V_{CC} to Digital Common	0 to +16.5V
V_{EE} to Digital Common	0 to -16.5V
V_{Logic} to Digital Common	0 to +7V
Analog Common to Digital Common	±1V
Digital Inputs (CE, CS, A_O, 12/8, R/C, S/H) to Digital Common	-0.5V to V_{Logic} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$ +IN, -IN) to Analog Common	±16.5V
$20V_{IN}$ to Analog Common	±24V
REF OUT	Indefinite Short to Common, Momentary Short to V_{CC}
S/H Differential Input Voltage	±24V
S/H Output Current, Continuous	±20mA
Storage Temperature	-65°C to +150°C
Power Dissipation*	2560mW
Lead Temperature, Soldering	180°C
Thermal Resistance, θja	39°C/W
θjc	14°C/W

*Derate 25.6mW/°C above 75°C

		MIN	TYP	MAX	UNITS
Maximum Offset Error				±3	LSB
Maximum Sampling Rate (Note 1)				37	kHz
POWER SUPPLY REJECTION					
Maximum change in full scale calibration					
+15V ±0.5V	J and A models			±2	LSB
	All Other Models			±1	LSB
-15V ±0.5V	J and A Models			±3	LSB
	All Other Models			±2	LSB
+5V ±0.5V	All Models			±½	LSB
POWER SUPPLIES					
Operating Voltages					
V_{Logic}		4.5	5.0	5.5	Volts
V_{CC}		14.5	15.0	16.0	Volts
V_{EE}		-14.5	-15.0	-16.0	Volts
Operating Currents					
I_{Logic}			7	15	mA
I_{CC} (Note 3)			22	28	mA
I_{EE} (Note 3)			32	41	mA

(In configuration as shown in Figure 1)

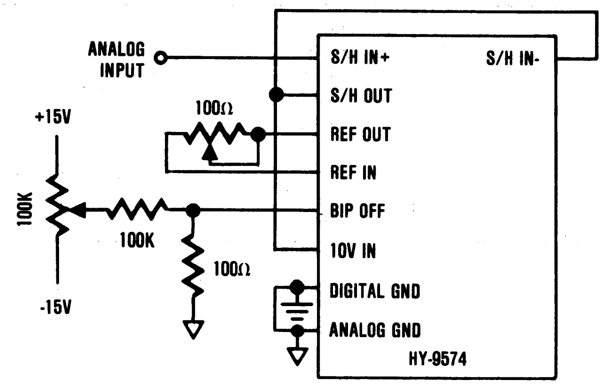


FIGURE 1. FOR CALIBRATION INSTRUCTION SEE "RANGE SELECTION AND CALIBRATION PROCEDURES" SECTION OF THIS DATA SHEET.

HY-9574 System Specifications

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Input Voltage Range	-40°C to +85°C	±10			V
Input Resistance	25°C	1	5		MΩ
D.C. & TRANSFER ACCURACY SPECIFICATIONS					
Resolution (Maximum)				12	Bits
Linearity Error	-40°C to +85°C			±1	LSB
Differential Linearity Error					
J and A Models	Full			11	Bits
All Other Models	Full			12	Bits
DIGITAL INPUT & OUTPUT CHARACTERISTICS					
Input Voltage (High), V_{IH}	Full	+2.4		+5.5	V
Input Voltage (Low), V_{IL}	Full	-0.5		+0.8	V
Input Current (V_{IL} = 0V)	Full			-5 (Note 2)	μA
Input Current (V_{IH} = +5V)	Full			+5 (Note 2)	μA
Logic "0" Output (I_{SINK} = 1.6mA)	Full			+0.4	V
Logic "1" Output (I_{SOURCE} = 500μA)	Full	+2.4			V
Leakage Current (High Z State, DB0-11 Only)	Full	-5	0.1	+5	μA
POWER SUPPLY CHARACTERISTICS					
Positive Supply Voltage		+14.5		+16.0	V
Negative Supply Voltage		-14.5		-16.0	V
Logic Supply Voltage		+4.5		+5.5	V
Positive Supply Current (Note 3)			22	28	mA
Negative Supply Current (Note 3)			32	41	mA
Logic Supply Current			7	15	mA
Power Supply Rejection V+ (Note 10)					
J & A Models	25°C			±2	LSB
All Other Models	25°C			±1	LSB
Power Supply Rejection V- (Note 10)					
J & A Models	25°C			±2	LSB
All Other Models	25°C			±1	LSB
Power Dissipation			850		mW
TIMING SPECIFICATIONS					
Conversion Time 12 Bit Cycle	+25°C	15	20	25	μs
8 Bit Cycle	+25°C	10	13	17	μs
STS Delay After Data Valid	+25°C	300	500	1000	ns
S/H Acquisition Time (0.01%)	+25°C		1.0	1.5	μs
Aperture Time	+25°C		25		ns
Aperture Uncertainty	+25°C		0.3		ns
Droop Rate	+25°C		0.08	0.5	μV/μs
	-40°C to +85°C		17	100	μV/μs
Throughput Rate (Note 1)	+25°C			37	kHz

HY-9574 Sample And Hold Amplifier Specifications

Electrical Characteristics Test Conditions (Unless otherwise specified)
V_{Supply} = ±15V; C_H - Internal; Digital Input (Pin 14), V_{AL} = +0.8V (Sample), V_{AH} = +2.0V (Hold).

OPERATING TEMP RANGE		-40°C ≤ TA ≤ 85°C			0°C ≤ TA ≤ 75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10			±10			V
Input Resistance	25°C	1	5		1	5		MΩ
Input Capacitance	25°C			3			3	pF
Offset Voltage	25°C		0.2	0.5		0.5	1.0	mV
	Full			2.0			1.5	mV
Bias Current	25°C		70	200		100	300	nA
	Full			200			300	nA
Offset Current	25°C		30	100		30	300	nA
	Full			100			300	nA
Common Mode Range	Full	±10			±10			V
CMRR (Note 4)	25°C	80	90		72	90		dB
Offset Voltage T.C.	Full		5	15		5	20	μV/°C
TRANSFER CHARACTERISTICS								
Gain, dC	25°C	10^6	2×10^6		3×10^5	2×10^6		V/V
Gain Bandwidth Product (Note 5) C_H = 100pF	25°C		2.0			2.0		MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10			±10			V
Output Current	25°C	±10			±10			mA
Full Power Bandwidth (Note 6)	25°C		600			600		kHz
Output Resistance (Hold Mode)	25°C		1.0			1.0		Ω
Total Output Noise, DC to 10MHz								
Sample	25°C		125	200		125	200	μV RMS
Hold	25°C		125	200		125	200	μV RMS
TRANSIENT RESPONSE								
Rise Time (Note 5)	25°C		100			100		ns
Overshoot (Note 5)	25°C		15			15		%
Slew Rate (Note 7)	25°C		45			45		V/μs
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{AH}	Full	2.0			2.0			V
Input Voltage (Low), V_{AL}	Full			0.8			0.8	V
Input Current (V_{AL} = 0V)	Full			4			4	μA
Input Current (V_{AH} = +5V)	Full			0.1			0.1	μA
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time (0.1%) (Note 7)	25°C		0.8	1.2		0.8	1.2	μs
Acquisition Time (0.01%) (Note 7)	25°C		1.0	1.5		1.0	1.5	μs
Aperture Time (Note 8)	25°C		25			25		ns
Effective Aperture Delay Time (See S/H Glossary)	25°C	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty	25°C		0.3			0.3		ns
Hold Capacitor, C_H			100			100		pF
Droop Rate	25°C		0.08	0.5		0.08	0.5	μV/μs
Droop Rate	Full		2.4	100		1.2	100	μV/μs
Drift Current (Note 9)	25°C		8	50		8	50	pA
Drift Current (Note 9)	Full		0.24	10		0.12	10	nA
Charge Transfer (Note 9)	25°C		0.1	0.5		0.1	0.5	pC
Hold Mode Settling Time (0.01%)	Full		165	250		165	250	ns
Hold Mode Feedthrough 10Vp-p, 100kHz	Full		2			2		mV
POWER SUPPLY CHARACTERISTICS								
Power Supply Rejection V+	Full	80			80			dB
(Note 10) V-	Full	65			65			dB

HY-9574 Analog-to-Digital Converter Specifications

DC and Transfer Accuracy Specifications

(Typical @ +25°C with V_{CC} = +15V, V_{LOGIC} = +5V, V_{EE} = -15V unless otherwise specified)

	TEMPERATURE RANGE 0°C to +75°C			
MODEL	**HY-9574J**	**HY-9574K**	**HY-9574L**	**UNITS**
Resolution (Maximum)	12	12	12	Bits
LINEARITY ERROR				
25°C (Maximum)	±1	±1/2	±1/2	LSB
0°C to +75°C (Maximum)	±1	±1/2	±1/2	LSB
DIFFERENTIAL LINEARITY ERROR				
(Max. resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{MIN} to T_{MAX}	11	12	12	Bits
Unipolar Offset (Max.) (Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (Max.) (Adjustable to zero)	±10	±4	±4	LSB
FULL SCALE CALIBRATION ERROR				
25°C (Max.), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of Full Scale
T_{MIN} to T_{MAX}				
(No adjustment at +25°C)	0.5	0.4	0.35	% of Full Scale
(With adjustment to zero at +25°C)	0.22	0.12	0.05	% of Full Scale
TEMPERATURE COEFFICIENTS				
Guaranteed max change to T_{MIN} or T_{MAX} (Using internal ref.)				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	LSB
	(45)	(25)	(10)	(ppm/°C)
POWER SUPPLY REJECTION				
Max. change in Full Scale Calibration				
$+13.5V < V_{CC} < +16.5$ or $+11.4V < V_{CC} < +12.6V$	±2	±1	±1	LSB
$+4.5V < V_{LOGIC} < +5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V < V_{EE} < -13.5V$ or $-12.6V < V_{EE} < -11.4V$	±2	±1	±1	LSB
ANALOG INPUT RANGES				
Bipolar	-5 to +5			Volts
	-10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
INPUT IMPEDANCE				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
INTERNAL REFERENCE				
Voltage	+10.0 ± 0.1 Max.			Volts
Output Current available for external loads (External load should not change during conversion.	2.0 Max.			mA

DC and Transfer Accuracy Specifications

(Typical @ +25°C with V_{CC} = +15V, V_{LOGIC} = +5V, V_{EE} = -15V unless otherwise specified)

	TEMPERATURE RANGE -40°C to +85°C		
MODEL	**HY-9574A**	**HY-9574B**	**UNITS**
Resolution (Maximum)	12	12	Bits
LINEARITY ERROR			
25°C (Maximum)	±1	±1/2	LSB
-40°C ≤ T_A ≤ 85°C (Maximum)	±1	±1	LSB
DIFFERENTIAL LINEARITY ERROR			
(Max. resolution for which no missing codes is guaranteed)			
25°C	11	12	Bits
T_{MIN} to T_{MAX}	11	12	Bits
Unipolar Offset (Max.) (Adjustable to zero)	±2	±2	LSB
Bipolar Offset (Max.) (Adjustable to zero)	±10	±4	LSB
FULL SCALE CALIBRATION ERROR			
25°C (Max.), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	% of Full Scale
T_{MIN} to T_{MAX}			
(No adjustment at +25°C)	0.8	0.6	% of Full Scale
(With adjustment to zero at +25°C)	0.5	0.25	% of Full Scale
TEMPERATURE COEFFICIENTS			
Guaranteed max change to T_{MIN} or T_{MAX} (Using internal ref.)			
Unipolar Offset	±2 (5)	±1 (2.5)	LSB (ppm/°C)
Bipolar Offset	±4 (10)	±2 (5)	LSB (ppm/°C)
Full Scale Calibration	±20 (50)	±10 (25)	LSB (ppm/°C)
POWER SUPPLY REJECTION			
Max. change in Full Scale Calibration			
+13.5V < V_{CC} < +16.5 or +11.4V < V_{CC} < +12.6V	±2	±1	LSB
+4.5V < V_{LOGIC} < +5.5V	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V	±2	±1	LSB
ANALOG INPUTS, INPUT RANGES			
Bipolar	-5 to +5 -10 to +10		Volts Volts
Unipolar	0 to +10 0 to +20		Volts Volts
INPUT IMPEDANCE			
10 Volt Span	5KΩ, ± 25%		Ohms
20 Volt Span	10KΩ, ± 25%		Ohms
INTERNAL REFERENCE			
Voltage	+10.0 ± 0.1 Max.		Volts
Output Current available for external loads (External load should not change during conversion.	2.0 Max.		mA

Digital Characteristics (Note 11)

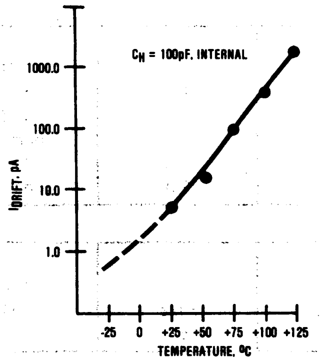
(ALL MODELS, OVER FULL TEMPERATURE RANGE)	MIN	TYP	MAX
Logic Inputs (CE, CS, R/C, A0, 12/8)			
Logic "1"	+2.4V (Note 12)		+5.5V
Logic "0"	-0.5V		+0.8V
Current	-5μA	0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 Only)	-5μA	0.1μA	+5μA
Capacitance		5pF	

NOTES:

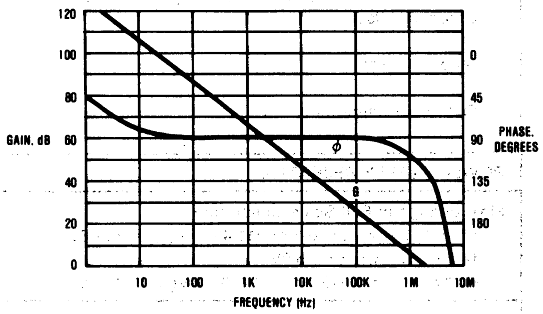
1. Maximum T.R. = $(t_{acq} + t_{conv})^{-1}$, see Harris Application Note 538.
2. Conventional current flowing into the package is designated "+", current flowing out is "—".
3. Supply current specified for a 0V differential between pins 1 and 32. Supply current will increase with differential input (as may occur in the Hold Mode) to approximately +39mA and -49mA at 20V.
4. $V_{CM} = \pm5VDC$
5. Vo = 200mVp-p; R_L = 2kΩ; C_L = 50pF.
6. Vo = 20Vp-p; R_L = 2kΩ; C_L = 50pF; Unattenuated output.
7. Vo = 10V step; R_L = 2kΩ; C_L = 50pF.
8. Derived from computer simulation only, not tested.
9. V_{IN} = 0V, V_{AH} = +3.5V, tr < 20ns (V_{IL} to V_{IH}).
10. Based on a one volt delta in each supply, i.e. 15V ± 0.5VDC.
11. See "HY-9574 ADC Timing Specifications" for a detailed listing of digital timing parameters.
12. Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.

Sample/Hold Amplifier Performance Curves $V_{SUPPLY} = \pm15VDC$

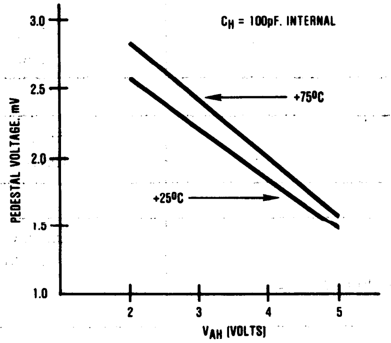
DRIFT CURRENT vs. TEMPERATURE



OPEN LOOP GAIN AND PHASE RESPONSE

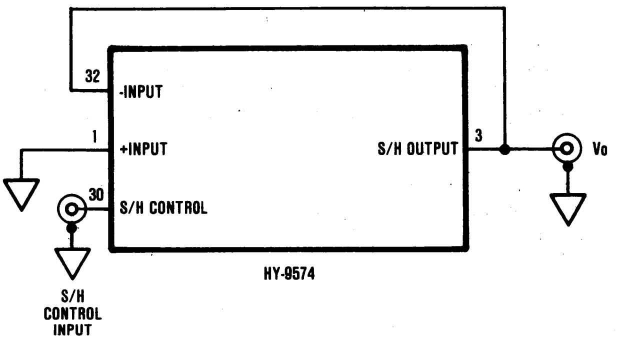


PEDESTAL vs. LOGIC (V_{AH}) VOLTAGE



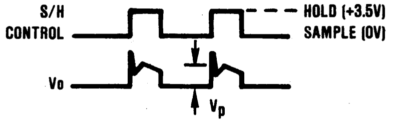
HY-9574 Sample/Hold Test Circuits

CHARGE TRANSFER AND DRIFT CURRENT


32
-INPUT
1
+INPUT
30
S/H CONTROL
S/H OUTPUT
3
Vo
HY-9574
S/H
CONTROL
INPUT

CHARGE TRANSFER TEST

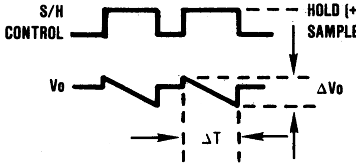
1. Observe the "pedestal" voltage V_p:


S/H
CONTROL
HOLD (+3.5V)
SAMPLE (0V)
Vo
Vp

2. Compute charge transfer: Q = VpCH

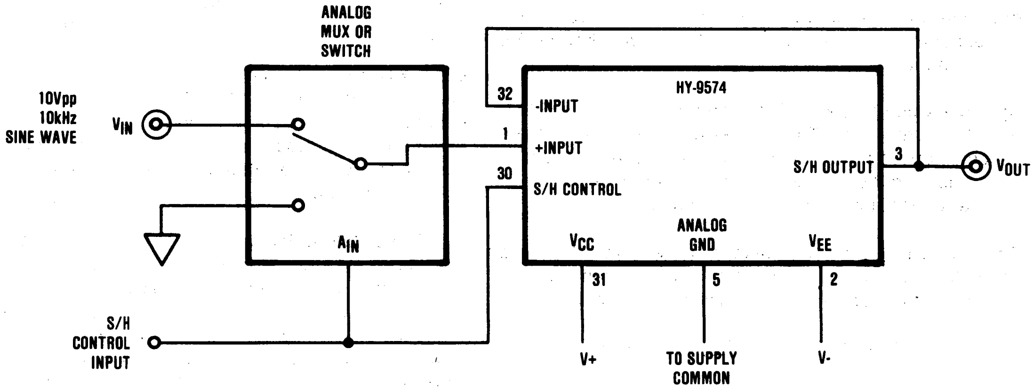
DRIFT CURRENT TEST

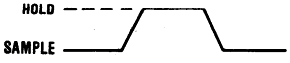
1. Observe the voltage "droop", $\Delta Vo/\Delta T$:


S/H
CONTROL
HOLD (+3.5V)
SAMPLE (0V)
Vo
ΔVo
ΔT

2. Measure the slope of the output during hold, $\Delta Vo/\Delta T$, and compute drift current: $I_D = C_H \Delta Vo/\Delta t$.

S/H HOLD MODE FEEDTHROUGH ATTENUATION


ANALOG
MUX OR
SWITCH
10Vpp
10kHz
SINE WAVE
VIN
AIN
32
-INPUT
1
+INPUT
30
S/H CONTROL
HY-9574
S/H OUTPUT
3
VOUT
VCC
ANALOG
GND
VEE
31
5
2
V+
TO SUPPLY
COMMON
V-
S/H
CONTROL
INPUT


HOLD
SAMPLE

$$\text{FEEDTHROUGH (dB)} = 20 \text{ Log } \frac{V_{OUT}}{V_{IN}}$$

WHERE V_{OUT} = VOLTS pp, Hold Mode
V_{IN} = VOLTS pp

Glossary of Terms

Sample and Hold

Acquisition Time — The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Charge Transfer — The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the Hold Mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where:

$$\text{Charge Transfer (pC)} = C_H\text{ (pF)} \times \text{Offset Error (V)}$$

Aperture Time — The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Hold Step Error — The output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{Hold Step (V)} = \frac{\text{Charge Transfer (pC)}}{100\text{pF}}$$

See Sample/Hold Amplifier Performance Curves.

Effective Aperture Delay Time (EADT) — The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty — The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Drift Current — The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D\text{ (pA)} = C_H\text{ (pF)} \times \frac{\Delta V}{\Delta T}\text{ (Volts/sec)}$$

Analog/Digital Converter

Linearity Error — Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level one and one-half (1½) LSB's beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HY-9574K, L, and B grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HY-9574J and A grades are guaranteed to ±1LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one. Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes) — A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HY-9574K, L, and B grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HY-9574J and A grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset — The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset — Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error — The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value one and one-half (1½) LSB's below the nominal full scale (9.9963 volts for 10,000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

Temperature Coefficients — The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection — The standard specifications for the HY-9574 assume use of +5.00 and ±15.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width — A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

Quantization Uncertainty — Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-Justified Data — The data format used in the HY-9574 is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HY-9574

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

Physical Mounting and Layout Considerations

Layout — Unwanted, parasitic circuit components, (L, R and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies — Supply voltages to the HY-9574 (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessasry to counter the effect of variations in supply current. Connect one pair from pin 24 to 10 (V_{LOGIC} Supply), one from pin 31 to 5 (V_{CC} to Analog Common) and one from pin 2 to 5 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections — Pin 5 (Analog Common) and pin 10 (Digital Common) should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 5 to (usually) 15V common, and from pin 10 to (usually) the +5V logic common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 5 and 10: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HY-9574's Analog Common or Digital Common.

Range Connections And Calibration Procedures

The HY-9574 is a "complete sampling" A/D converter, meaning it can be fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HY-9574 offers three standard input ranges: 0V to +10V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration — Refer to Figure 2. The resistors shown are for calibration of offset and gain. If this is not required, replace R2* with a 50Ω, 1% metal film resistor and remove the network on pin 7. Connect pin 7 to pin 5. Then connect the S/H output to pin 8 for the 0V to 10V range. Inputs to +20V (5V over the power supply) are no problem for the A/D - the converter operates normally. But the S/H cannot handle inputs over V_{CC}.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is settling the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +½LSB (+1.22mV for the 10V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is one and one-half (1½) LSB's below the nominal full scale (+9.9963V for 10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration — Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the S/H output to pin 8 for a ±5V range, or to pin 9 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage ½LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage one and one-half (1½) LSB's below positive full scale (+4.9963V for ±5V range; +9.9927 for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 8.

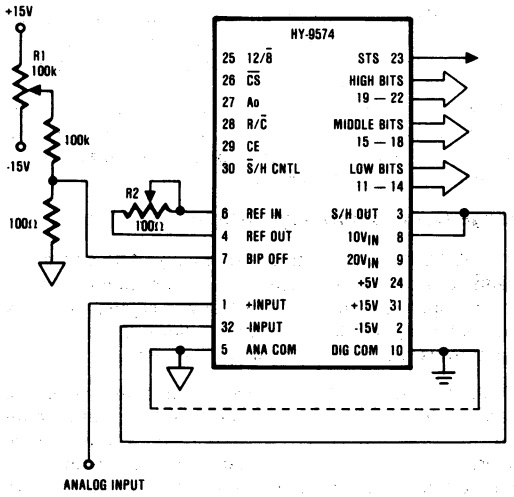

+15V
R1
100k
100k
-15V
100Ω
R2
100Ω
HY-9574
25 12/$\overline{8}$
26 $\overline{CS}$
27 A0
28 R/$\overline{C}$
29 CE
30 $\overline{S}$/H CNTL
6 REF IN
4 REF OUT
7 BIP OFF
1 +INPUT
32 -INPUT
5 ANA COM
STS 23
HIGH BITS 19 — 22
MIDDLE BITS 15 — 18
LOW BITS 11 — 14
S/H OUT 3
10V$_{IN}$ 8
20V$_{IN}$ 9
+5V 24
+15V 31
-15V 2
DIG COM 10
ANALOG INPUT

FIGURE 2. UNIPOLAR CONNECTIONS

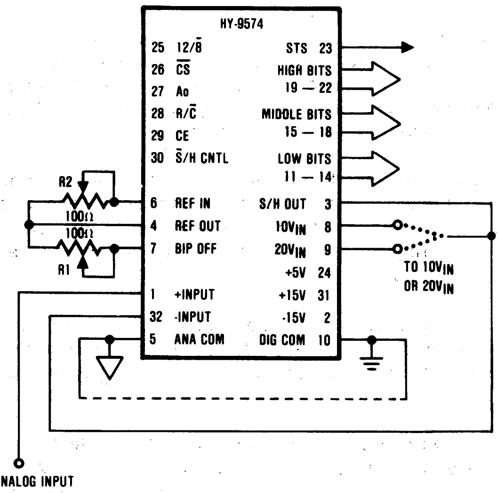

HY-9574
25 12/$\overline{8}$
26 $\overline{CS}$
27 A0
28 R/$\overline{C}$
29 CE
30 $\overline{S}$/H CNTL
6 REF IN
4 REF OUT
7 BIP OFF
1 +INPUT
32 -INPUT
5 ANA COM
STS 23
HIGH BITS 19 — 22
MIDDLE BITS 15 — 18
LOW BITS 11 — 14
S/H OUT 3
10V$_{IN}$ 8
20V$_{IN}$ 9
+5V 24
+15V 31
-15V 2
DIG COM 10
R2
100Ω
100Ω
R1
TO 10V$_{IN}$ OR 20V$_{IN}$
ANALOG INPUT

FIGURE 3. BIPOLAR INPUT CONNECTIONS

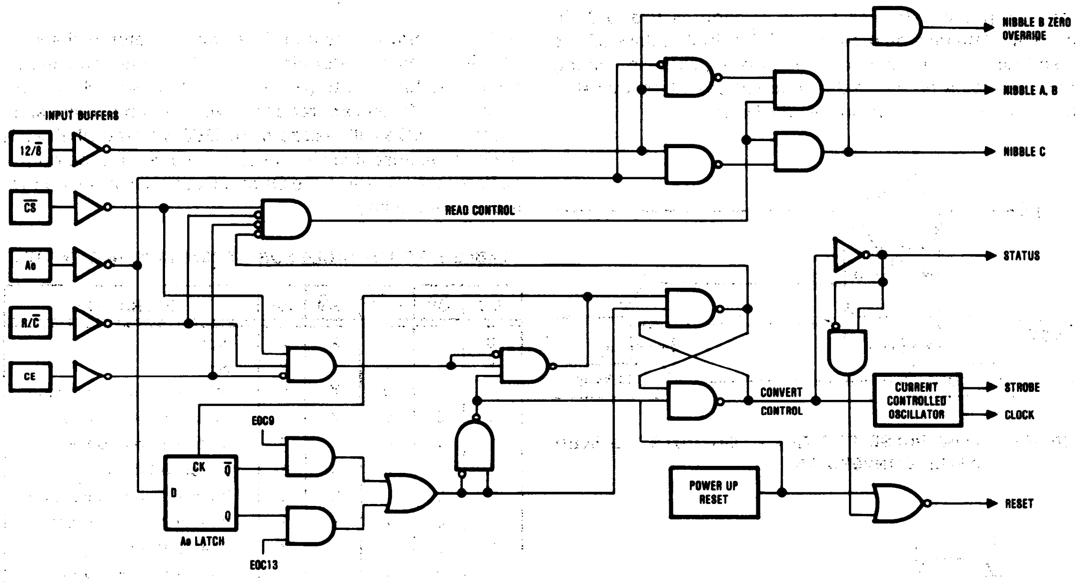

INPUT BUFFERS
12/8
CS
Ao
R/C
CE
READ CONTROL
NIBBLE B ZERO OVERRIDE
NIBBLE A, B
NIBBLE C
STATUS
CONVERT CONTROL
CURRENT CONTROLLED OSCILLATOR
STROBE
CLOCK
EOC9
CK
Q
D
Q
Ao LATCH
EOC13
POWER UP RESET
RESET

FIGURE 4. HY-9574 ADC CONTROL LOGIC

Controlling The HY-9574

The HY-9574 includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, capturing the signal with the S/H, initiating the conversion, and reading the output data when ready - choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The six control inputs are all TTL/CMOS compatible: (12/$\overline{8}$, $\overline{CS}$, Ao, $\overline{S}$/H, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic for the ADC is shown in Figure 4.

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$ as shown in Figure 5. The output data appears in words of 12 bits each.

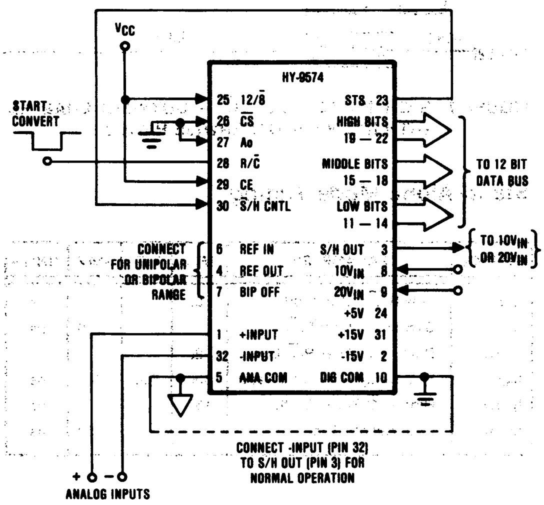

VCC
HY-9574
START CONVERT
25 12/8
26 CS
27 Ao
28 R/C
29 CE
30 S/H CNTL
STS 23
HIGH BITS 19 — 22
MIDDLE BITS 15 — 18
LOW BITS 11 — 14
TO 12 BIT DATA BUS
CONNECT FOR UNIPOLAR OR BIPOLAR RANGE
6 REF IN
4 REF OUT
7 BIP OFF
S/H OUT 3
10VIN 8
20VIN 9
TO 10VIN OR 20VIN
+5V 24
1 +INPUT
+15V 31
32 -INPUT
-15V 2
5 ANA COM
DIG COM 10
CONNECT -INPUT (PIN 32) TO S/H OUT (PIN 3) FOR NORMAL OPERATION
+ −
ANALOG INPUTS

FIGURE 5. GENERAL PURPOSE 12 BIT "STAND ALONE" CONFIGURATION

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 6 and 7. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing."

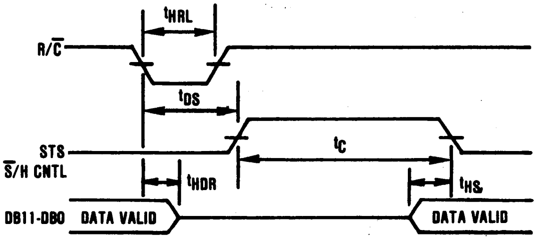


FIGURE 6. LOW PULSE FOR R/$\overline{C}$ — OUTPUTS ENABLED AFTER CONVERSION

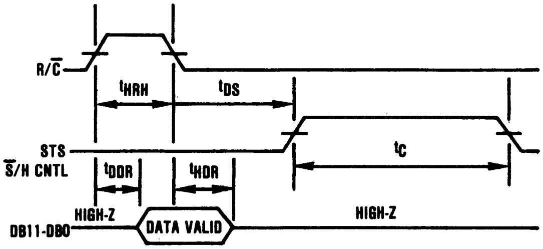


FIGURE 7. HIGH PULSE FOR R/$\overline{C}$ — OUTPUTS ENABLED WITH R/$\overline{C}$ HIGH, OTHERWISE HIGH-Z

Stand-Alone Mode Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	500	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

Conversion Length

A Convert Start transition (See Table 1) latches the state of Ao, which determines whether the conversion continues for 12 bits (Ao low) or stops with 8 bits (Ao high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB3 will read ONE. Ao is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

TABLE 1. TRUTH TABLE FOR HY-9574 CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

Once a signal is captured by the S/H, conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50ns earlier, however. See the HY-9574 Timing Specifications, Convert Mode.

This variety of HY-9574 control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 8.

The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an

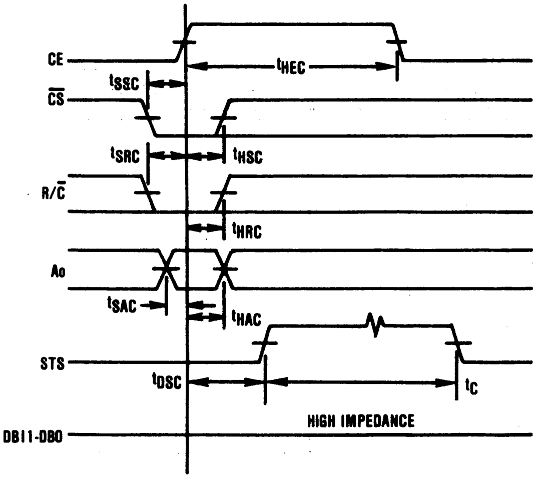


FIGURE 8. CONVERT START TIMING

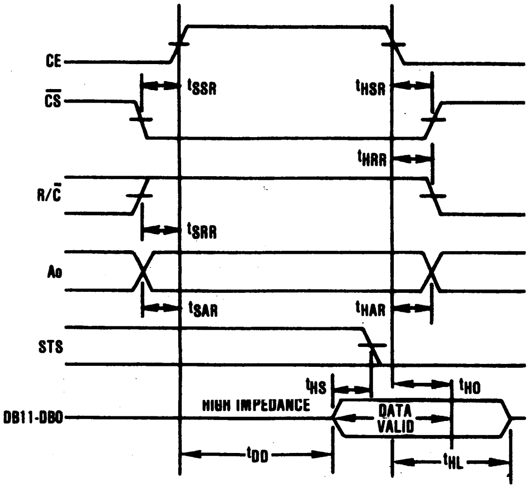


FIGURE 9. READ CYCLE TIMING

additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if Ao changes state after a conversion begins, an additional Start Convert signal will latch the new state of Ao, possibly causing a wrong cycle length (8 vs 12 bits) for that conversion).

Reading The Output Data

The output data buffers remain in a high impedance state until four conditions are met: $R/\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs $12/\overline{8}$ and Ao. Timing constraints are illustrated in Figure 9.

The $12/\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS compatible. With $12/\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The Ao input is ignored.

With $12/\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by Ao. This allows an 8 bit data bus to be connected as shown in Figure 10. Ao is usually tied to the least significant bit of the address bus, for storing the HY-9574 output in two consecutive memory locations. (With Ao low, the 8 MSB's only are enabled. With Ao high, 4 MSB's are disabled, bits 4 through 7 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:

BYTE 1	BYTE 2
X X X X X X X X	X X X X 0 0 0 0
MSB	LSB

Further, Ao may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 10 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than $(t_{DD} + t_{HS})$ before STS goes low. See Figure 9.

HY-9574 ADC Timing Specifications at +25°C *

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
t_{DSC}	STS Delay from CE		100	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low during CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low during CE High	50	20		ns
t_{SAC}	Ao to CE Setup	0	0		ns
t_{HAC}	Ao Valid during CE High	50	20		ns
t_C	Conversion Time, 12-Bit Cycle **	15	20	25	μs
	8 Bit Cycle **	10	13	17	μs
READ MODE					
t_{DD}	Access Time from CE		75	150	ns
t_{HD}	Data Valid after CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0		ns
t_{SAR}	Ao to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid after CE Low	0	0		ns
t_{HRR}	R/$\overline{C}$ High after CE Low	0	0		ns
t_{HAR}	Ao Valid after CE Low	50	25		ns
t_{HS}	STS Delay after Data Valid	300	500	1000	ns

* Time is measured from 50% level of digital transitions.

** Tmin to Tmax

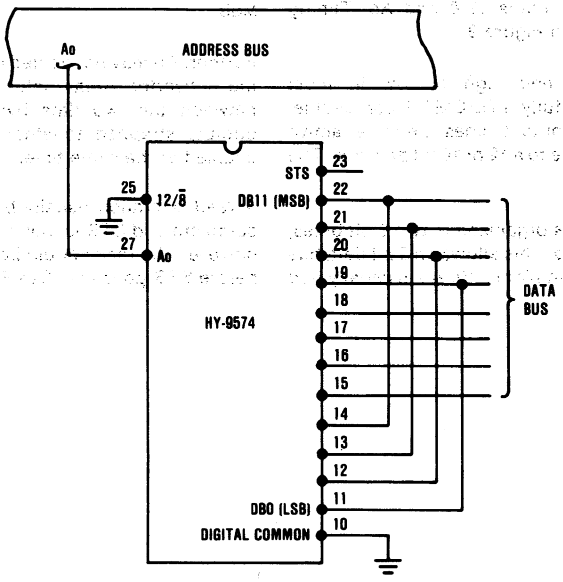
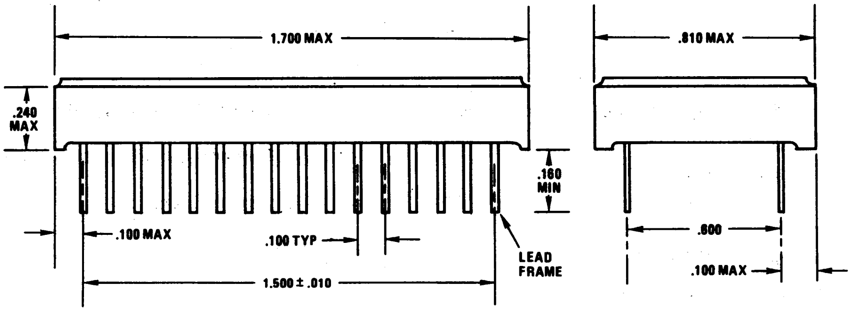

Ao
ADDRESS BUS
25
12/8̄
27
Ao
HY-9574
STS
DB11 (MSB)
DB0 (LSB)
DIGITAL COMMON
23
22
21
20
19
18
17
16
15
14
13
12
11
10
DATA BUS

FIGURE 10. INTERFACE TO AN 8-BIT DATA BUS

Package

32 PIN PLASTIC DIP


1.700 MAX
.810 MAX
.240 MAX
.160 MIN
.100 MAX
.100 TYP
LEAD FRAME
1.500 ± .010
.600
.100 MAX

Ordering Information

MODEL	TEMPERATURE	MAX LIN. ERROR	RESOLUTION NO MISS. CODE	FULL SCALE TC ppm/°C MAX
J = HY3-9574J-5	0°C to +75°C	±1 LSB	11 Bits	45.0
K = HY3-9574K-5	0°C to +75°C	±½ LSB	12 Bits	25.0
L = HY3-9574L-5	0°C to +75°C	±½ LSB	12 Bits	10.0
A = HY3-9574A-9	-40°C to +85°C	±1 LSB	11 Bits	50.0
B = HY3-9574B-9	-40°C to +85°C	±1 LSB	12 Bits	25.0

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

HARRIS

HY-9674

ADVANCED

Sampling 12 Bit A/D Converter with 8/16 Bit μP Interface

Features

- Complete 12 Bit Sampling A/D Converter with Reference and Clock
- Throughput Rate (Typical)
  - 12 Bit 77kHz
  - 8 Bit 114kHz
- Faster Version of the HY-9574
- 32 Pin Plastic Dual-In-Line Package

A/D Converter Features

- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Setup Time for Control Signals
- 15μs Maximum Conversion Time (12-Bit)
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)

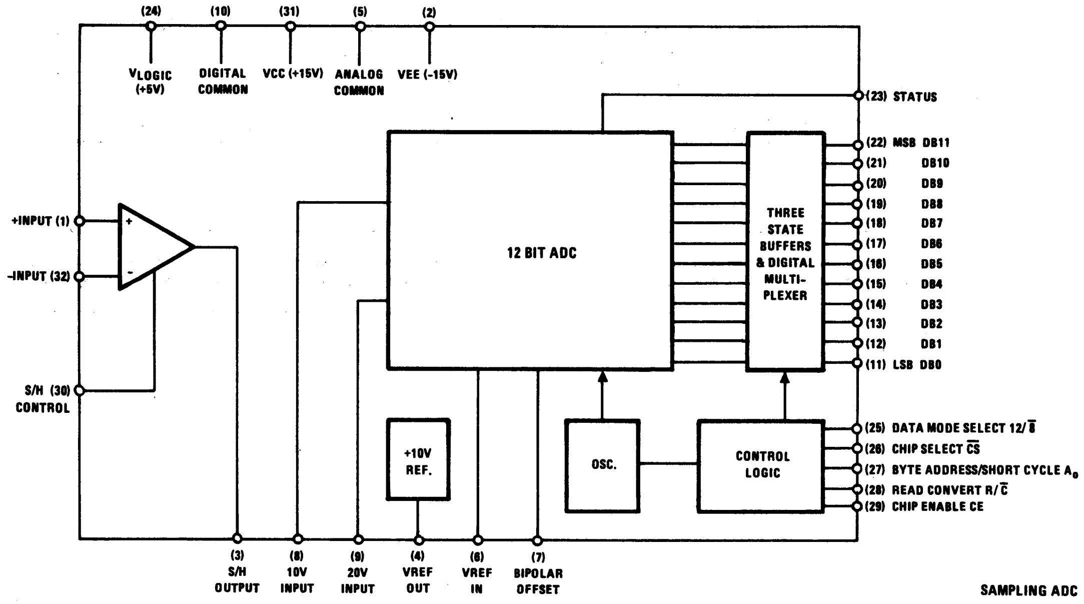
Applications

- Precision Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems
- Peak Detectors

Sample/Hold Features

- Gain DC .... 2×10^6 V/V
- Acquisition Time .... 1.0μs (±0.01%)
- Droop Rate .... 0.08μV/μs (25°C)
  2.4μV/μs (Full Temp.)
- Aperture Time 25ns
- Pedestal Error 1.0mV
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible

Functional Diagram


(24) V_{LOGIC} (+5V)
(10) DIGITAL COMMON
(31) VCC (+15V)
(5) ANALOG COMMON
(2) VEE (-15V)
(23) STATUS
(22) MSB DB11
(21) DB10
(20) DB9
(19) DB8
(18) DB7
(17) DB6
(16) DB5
(15) DB4
(14) DB3
(13) DB2
(12) DB1
(11) LSB DB0
+INPUT (1)
-INPUT (32)
S/H (30) CONTROL
12 BIT ADC
THREE STATE BUFFERS & DIGITAL MULTI-PLEXER
+10V REF.
OSC.
CONTROL LOGIC
(25) DATA MODE SELECT 12/$\overline{8}$
(26) CHIP SELECT $\overline{CS}$
(27) BYTE ADDRESS/SHORT CYCLE A_0
(28) READ CONVERT R/$\overline{C}$
(29) CHIP ENABLE CE
(3) S/H OUTPUT
(8) 10V INPUT
(9) 20V INPUT
(4) VREF OUT
(6) VREF IN
(7) BIPOLAR OFFSET
SAMPLING ADC

Description

The HY-9674 is designed for use in precision, high speed data acquisition systems. The Harris Sample/Hold amplifier (HA-5320) and 12 bit A/D converter (HI-674A) have been combined in a single package to reduce package count and to insure component compatibility.

The Sample/Hold (HA-5320) circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The device includes a hold capacitor, so no external hold capacitor is required.

The Sample and Hold chip (HA-5320) is manufactured using the Harris Dielectric Isolation process, which minimizes stray capacitance and eliminates SCR's. This allows higher speed and latch-free operation.

The 12 bit successive approximation Analog-to-Digital section is an HA-674A chip set. It includes a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

Custom design of each IC (Bipolar Analog and CMOS Digital) has yielded improved versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 12 ± 1μs.

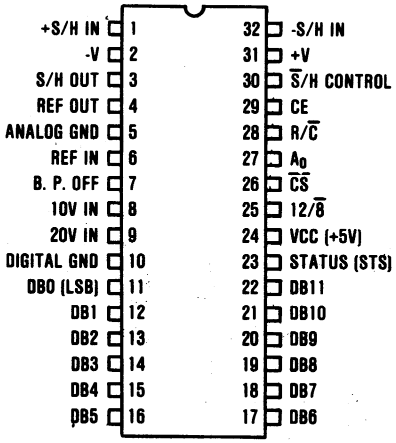
The Sample/Hold and ADC stages are not connected internally to provide maximum flexibility to the designer.

The HY-9674 offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are ±15V and +5V, with typical dissipation of 850mW. All models are packaged in a 32 pin plastic DIP with 600 mil row centers.

Pinout

TOP VIEW


+S/H IN 1
-V 2
S/H OUT 3
REF OUT 4
ANALOG GND 5
REF IN 6
B. P. OFF 7
10V IN 8
20V IN 9
DIGITAL GND 10
DB0 (LSB) 11
DB1 12
DB2 13
DB3 14
DB4 15
DB5 16
32 -S/H IN
31 +V
30 $\overline{S}$/H CONTROL
29 CE
28 R/$\overline{C}$
27 A_0
26 $\overline{CS}$
25 12/$\overline{8}$
24 VCC (+5V)
23 STATUS (STS)
22 DB11
21 DB10
20 DB9
19 DB8
18 DB7
17 DB6

HY-9674 System Specifications

Absolute Maximum Ratings

V_{CC} to Digital Common....................................0 to +16.5V
V_{EE} to Digital Common ....0 to -16.5V
V_{Logic} to Digital Common....................................0 to +7V
Analog Common to Digital Common......................... ±1V
Digital Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$, $\overline{S}$/H)
to Digital Common........................-0.5V to V_{Logic} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$ +IN, -IN)
to Analog Common... ±16.5V
$20V_{IN}$ to Analog Common .... ±24V

REF OUT .... Indefinite Short to Common, Momentary Short to V_{CC}
S/H Differential Input Voltage .... ±24V
S/H Output Current, Continuous ....±20mA
Storage Temperature ....-65°C to +150°C
Power Dissipation *... 2560mW
Lead Temperature, Soldering ....180°C
Thermal Resistance, θja ....39°C/W
θjc ....14°C/W

* Derate 25.6mW°C above 75°C

	MIN	TYP	MAX	UNITS
Maximum Offset Error			±3	LSB
12-Bit Throughput Rate (Note 1) 25°C	60	77	100	kHz
POWER SUPPLY REJECTION				
Maximum change in full scale calibration				
+15V ±0.5V J and A models			±2	LSB
All Other Models			±1	LSB
-15V ±0.5V J and A Models			±3	LSB
All Other Models			±2	LSB
+5V ±0.5V All Models			±½	LSB
POWER SUPPLIES				
Operating Voltages				
V_{Logic}	4.5	5.0	5.5	Volts
V_{CC}	14.5	15.0	16.0	Volts
V_{EE}	-14.5	-15.0	-16.0	Volts
Operating Currents				
I_{Logic}		7	15	mA
I_{CC} (Note 3)		22	28	mA
I_{EE} (Note 3)		32	41	mA

(In configuration as shown in Figure 1)

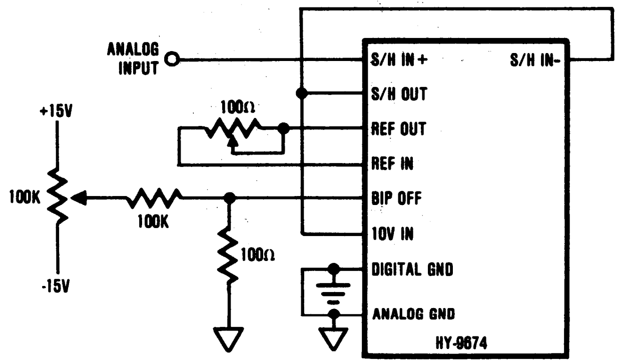


FIGURE 1. FOR CALIBRATION INSTRUCTION SEE "RANGE SELECTION AND CALIBRATION PROCEDURES" SECTION OF THIS DATA SHEET.

HY-9674 System Specifications

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Input Voltage Range	-40°C to +85°C	±10			V
Input Resistance	25°C	1	5		MΩ
D.C. & TRANSFER ACCURACY SPECIFICATIONS					
Resolution (Maximum)				12	Bits
Linearity Error	-40°C to +85°C			±1	LSB
Differential Linearity Error					
J and A Models	Full			11	Bits
All Other Models	Full			12	Bits
DIGITAL INPUT & OUTPUT CHARACTERISTICS					
Input Voltage (High), V_{IH}	Full	+2.4		+5.5	V
Input Voltage (Low), V_{IL}	Full	-0.5		+0.8	V
Input Current (V_{IL} = 0V)	Full			-5 (Note 2)	μA
Input Current (V_{IH} = +5V)	Full			+5 (Note 2)	μA
Logic "0" Output (I_{SINK} = 1.6mA)	Full			+0.4	V
Logic "1" Output (I_{SOURCE} = 500μA)	Full	+2.4			V
Leakage Current (High Z State, DB0-11 Only)	Full	-5	0.1	+5	μA
POWER SUPPLY CHARACTERISTICS					
Positive Supply Voltage		+14.5		+16.0	V
Negative Supply Voltage		-14.5		-16.0	V
Logic Supply Voltage		+4.5		+5.5	V
Positive Supply Current (Note 3)			22	28	mA
Negative Supply Current (Note 3)			32	41	mA
Logic Supply Current			7	15	mA
Power Supply Rejection V+ (Note 10)					
J & A Models	25°C			±2	LSB
All Other Models	25°C			±1	LSB
Power Supply Rejection V- (Note 10)					
J & A Models	25°C			±2	LSB
All Other Models	25°C			±1	LSB
Power Dissipation			850		mW
TIMING SPECIFICATIONS					
Conversion Time 12 Bit Cycle	+25°C	9	12	15	μs
8 Bit Cycle	+25°C	6	8	10	μs
STS Delay After Data Valid	+25°C	100	300	600	ns
S/H Acquisition Time (0.01%)	+25°C		1.0	1.5	μs
Aperture Time	+25°C		25		ns
Aperture Uncertainty	+25°C		0.3		ns
Droop Rate	+25°C		0.08	0.5	μV/μs
	-40°C to +85°C		17	100	μV/μs
Throughput Rate (Note 1) 12 Bit	+25°C	60	77	100	kHz
8 Bit	+25°C	87	110	140	kHz

HY-9674 Sample And Hold Amplifier Specifications

Electrical Characteristics Test Conditions (Unless otherwise specified)
V_{Supply} = ±15V; C_H - Internal; Digital Input (Pin 14), V_{AL} = +0.8V (Sample), V_{AH} = +2.0V (Hold).

OPERATING TEMP RANGE		-40°C ≤ TA ≤ 85°C			0°C ≤ TA ≤ 75°C			
PARAMETER	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10			±10			V
Input Resistance	25°C	1	5		1	5		MΩ
Input Capacitance	25°C			3			3	pF
Offset Voltage	25°C		0.2	0.5		0.5	1.0	mV
	Full			2.0			1.5	mV
Bias Current	25°C		70	200		100	300	nA
	Full			200			300	nA
Offset Current	25°C		30	100		30	300	nA
	Full			100			300	nA
Common Mode Range	Full	±10			±10			V
CMRR (Note 4)	25°C	80	90		72	90		dB
Offset Voltage T.C.	Full		5	15		5	20	µV/°C
TRANSFER CHARACTERISTICS								
Gain, dC	25°C	10^6	2 x 10^6		3 x 10^5	2 x 10^6		V/V
Gain Bandwidth Product (Note 5) C_H = 100pF	25°C		2.0			2.0		MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10			±10			V
Output Current	25°C	±10			±10			mA
Full Power Bandwidth (Note 6)	25°C		600			600		kHz
Output Resistance (Hold Mode)	25°C		1.0			1.0		Ω
Total Output Noise, DC to 10MHz								
Sample	25°C		125	200		125	200	µV RMS
Hold	25°C		125	200		125	200	µV RMS
TRANSIENT RESPONSE								
Rise Time (Note 5)	25°C		100			100		ns
Overshoot (Note 5)	25°C		15			15		%
Slew Rate (Note 7)	25°C		45			45		V/µs
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{AH}	Full	2.0			2.0			V
Input Voltage (Low), V_{AL}	Full			0.8			0.8	V
Input Current (V_{AL} = 0V)	Full			4			4	µA
Input Current (V_{AH} = +5V)	Full			0.1			0.1	µA
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time (0.1%) (Note 7)	25°C		0.8	1.2		0.8	1.2	µs
Acquisition Time (0.01%) (Note 7)	25°C		1.0	1.5		1.0	1.5	µs
Aperture Time (Note 8)	25°C		25			25		ns
Effective Aperture Delay Time (See S/H Glossary)	25°C	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty	25°C		0.3			0.3		ns
Hold Capacitor, C_H			100			100		pF
Droop Rate	25°C		0.08	0.5		0.08	0.5	µV/µs
Droop Rate	Full		2.4	100		1.2	100	µV/µs
Drift Current (Note 9)	25°C		8	50		8	50	pA
Drift Current (Note 9)	Full		0.24	10		0.12	10	nA
Charge Transfer (Note 9)	25°C		0.1	0.5		0.1	0.5	pC
Hold Mode Settling Time (0.01%)	Full		165	250		165	250	ns
Hold Mode Feedthrough 10Vp-p, 100kHz	Full		2			2		mV
POWER SUPPLY CHARACTERISTICS								
Power Supply Rejection V+	Full	80			80			dB
(Note 10) V-	Full	65			65			dB

HY-9674 Analog-to-Digital Converter Specifications

DC and Transfer Accuracy Specifications

(Typical @ +25°C with V_{CC} = +15V, V_{LOGIC} = +5V, V_{EE} = -15V unless otherwise specified)

MODEL	TEMPERATURE RANGE 0°C to +75°C			UNITS
	HY-9674J	HY-9674K	HY-9674L	
Resolution (Maximum)	12	12	12	Bits
LINEARITY ERROR				
25°C (Maximum)	±1	±1/2	±1/2	LSB
0°C to +75°C (Maximum)	±1	±1/2	±1/2	LSB
DIFFERENTIAL LINEARITY ERROR				
(Max. resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{MIN} to T_{MAX}	11	12	12	Bits
Unipolar Offset (Max.) (Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (Max.) (Adjustable to zero)	±10	±4	±4	LSB
FULL SCALE CALIBRATION ERROR				
25°C (Max.), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of Full Scale
T_{MIN} to T_{MAX}				
(No adjustment at +25°C)	0.5	0.4	0.35	% of Full Scale
(With adjustment to zero at +25°C)	0.22	0.12	0.05	% of Full Scale
TEMPERATURE COEFFICIENTS				
Guaranteed max change to T_{MIN} or T_{MAX} (Using internal ref.)				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	LSB
	(45)	(25)	(10)	(ppm/°C)
POWER SUPPLY REJECTION				
Max. change in Full Scale Calibration				
$+13.5V < V_{CC} < +16.5$ or $+11.4V < V_{CC} < +12.6V$	±2	±1	±1	LSB
$+4.5V < V_{LOGIC} < +5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V < V_{EE} < -13.5V$ or $-12.6V < V_{EE} < -11.4V$	±2	±1	±1	LSB
ANALOG INPUT RANGES				
Bipolar	-5 to +5 -10 to +10			Volts Volts
Unipolar	0 to +10 0 to +20			Volts Volts
INPUT IMPEDANCE				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
INTERNAL REFERENCE				
Voltage	+10.0 ± 0.1 Max			Volts
Output Current available for external loads (External load should not change during conversion.	2.0 Max.			mA

DC and Transfer Accuracy Specifications

(Typical @ +25°C with V_{CC} = +15V, V_{LOGIC} = +5V, V_{EE} = -15V unless otherwise specified)

	TEMPERATURE RANGE -40°C to +85°C		
MODEL	**HY-9674A**	**HY-9674B**	**UNITS**
Resolution (Maximum)	12	12	Bits
LINEARITY ERROR			
25°C (Maximum)	±1	±1/2	LSB
-40°C ≤ T_A ≤ 85°C (Maximum)	±1	±1	LSB
DIFFERENTIAL LINEARITY ERROR			
(Max. resolution for which no missing codes is guaranteed)			
25°C	11	12	Bits
T_{MIN} to T_{MAX}	11	12	Bits
Unipolar Offset (Max.) (Adjustable to zero)	±2	±2	LSB
Bipolar Offset (Max.) (Adjustable to zero)	±10	±4	LSB
FULL SCALE CALIBRATION ERROR			
25°C (Max.), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	% of Full Scale
T_{MIN} to T_{MAX}			
(No adjustment at +25°C)	0.8	0.6	% of Full Scale
(With adjustment to zero at +25°C)	0.5	0.25	% of Full Scale
TEMPERATURE COEFFICIENTS			
Guaranteed max change to T_{MIN} or T_{MAX} (Using internal ref.)			
Unipolar Offset	±2	±1	LSB
	(5)	(2.5)	(ppm/°C)
Bipolar Offset	±4	±2	LSB
	(10)	(5)	(ppm/°C)
Full Scale Calibration	±20	±10	LSB
	(50)	(25)	(ppm/°C)
POWER SUPPLY REJECTION			
Max. change in Full Scale Calibration			
$+13.5V < V_{CC} < +16.5$ or $+11.4V < V_{CC} < +12.6V$	±2	±1	LSB
$+4.5V < V_{LOGIC} < +5.5V$	±1/2	±1/2	LSB
$-16.5V < V_{EE} < -13.5V$ or $-12.6V < V_{EE} < -11.4V$	±2	±1	LSB
ANALOG INPUTS, INPUT RANGES			
Bipolar	-5 to +5		Volts
	-10 to +10		Volts
Unipolar	0 to +10		Volts
	0 to +20		Volts
INPUT IMPEDANCE			
10 Volt Span	5KΩ, ± 25%		Ohms
20 Volt Span	10KΩ, ± 25%		Ohms
INTERNAL REFERENCE			
Voltage	+10.0 ± 0.1 Max.		Volts
Output Current available for external loads (External load should not change during conversion.	2.0 Max.		mA

Digital Characteristics (Note 11)

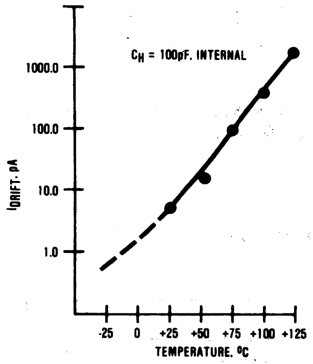
(ALL MODELS, OVER FULL TEMPERATURE RANGE)	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A_O, 12/$\overline{8}$)			
Logic "1"	+2.4V (Note 12)		+5.5V
Logic "0"	-0.5V		+0.8V
Current	-5μA	0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 Only)	-5μA	0.1μA	+5μA
Capacitance		5pF	

NOTES:

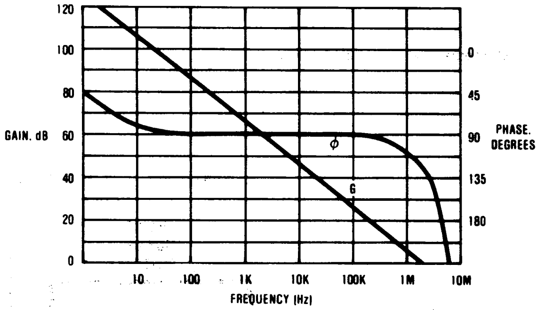
1. Maximum T.R. = $(t_{acq} + t_{conv})^{-1}$, see Harris Application Note 538.
2. Conventional current flowing into the package is designated "+", current flowing out is "—".
3. Supply current specified for a 0V differential between pins 1 and 32. Supply current will increase with differential input (as may occur in the Hold Mode) to approximately +39mA and -49mA at 20V.
4. V_{CM} = ±5VDC
5. Vo = 200mVp-p; R_L = 2kΩ; C_L = 50pF.
6. Vo = 20Vp-p; R_L = 2kΩ; C_L = 50pF; Unattenuated output.
7. Vo = 10V step; R_L = 2kΩ; C_L = 50pF.
8. Derived from computer simulation only, not tested.
9. V_{IN} = 0V, V_{AH} = +3.5V, tr < 20ns (V_{IL} to V_{IH}).
10. Based on a one volt delta in each supply, i.e. 15V ± 0.5VDC.
11. See "HY-9674 ADC Timing Specifications" for a detailed listing of digital timing parameters.
12. Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.

Sample/Hold Amplifier Performance Curves V_{SUPPLY} = ±15VDC

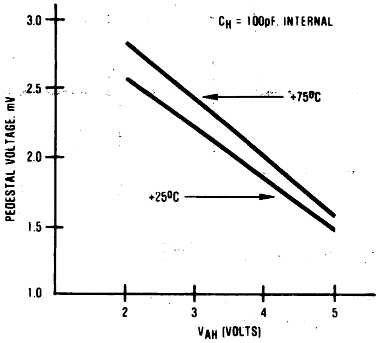
DRIFT CURRENT vs. TEMPERATURE



OPEN LOOP GAIN AND PHASE RESPONSE

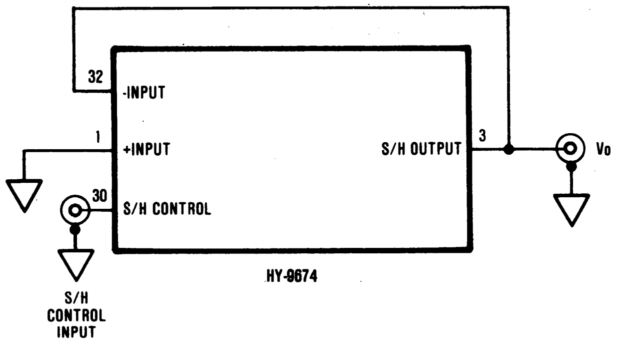


PEDESTAL vs. LOGIC (V_{AH}) VOLTAGE



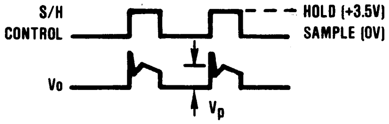
HY-9674 Sample/Hold Test Circuits

CHARGE TRANSFER AND DRIFT CURRENT


32
-INPUT
1
+INPUT
30
S/H CONTROL
S/H OUTPUT
3
Vo
S/H CONTROL INPUT
HY-9674

CHARGE TRANSFER TEST

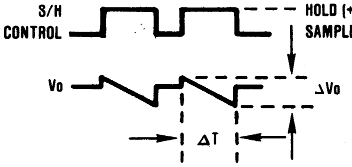
1. Observe the "pedestal" voltage V_p:


S/H CONTROL
HOLD (+3.5V)
SAMPLE (0V)
Vo
Vp

2. Compute charge transfer: $Q = V_p C_H$

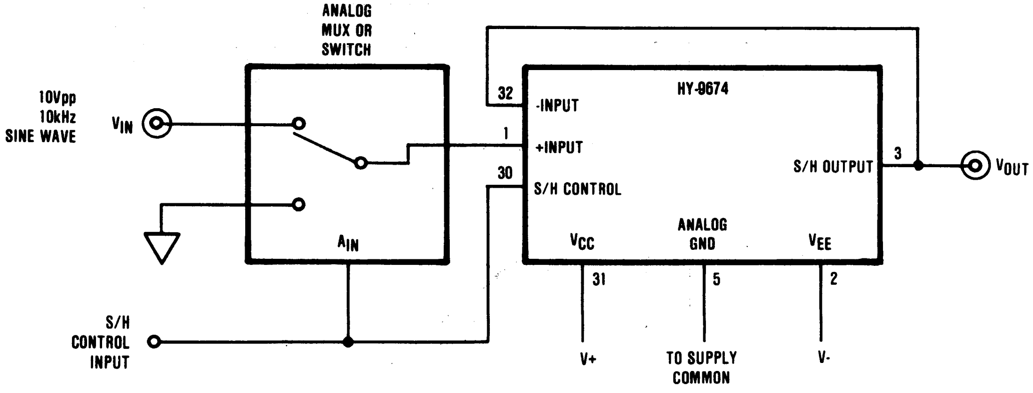
DRIFT CURRENT TEST

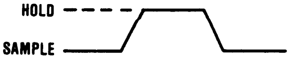
1. Observe the voltage "droop", $\Delta V_O/\Delta T$:


S/H CONTROL
HOLD (+3.5V)
SAMPLE (0V)
Vo
ΔVo
ΔT

2. Measure the slope of the output during hold, $\Delta V_O/\Delta T$, and compute drift current: $I_D = C_H \, \Delta V_O/\Delta t$.

S/H HOLD MODE FEEDTHROUGH ATTENUATION


ANALOG MUX OR SWITCH
10Vpp
10kHz
SINE WAVE
VIN
AIN
S/H CONTROL INPUT
HY-9674
32
-INPUT
1
+INPUT
30
S/H CONTROL
S/H OUTPUT
3
VOUT
VCC
ANALOG GND
VEE
31
5
2
V+
TO SUPPLY COMMON
V-


HOLD
SAMPLE

$$\text{FEEDTHROUGH (dB)} = 20 \text{ Log } \frac{V_{OUT}}{V_{IN}}$$

WHERE V_{OUT} = VOLTS pp, Hold Mode
V_{IN} = VOLTS pp

Glossary of Terms

Sample and Hold

Acquisition Time — The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Charge Transfer — The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the Hold Mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where:

$$\text{Charge Transfer (pC)} = C_H \text{ (pF)} \times \text{Offset Error (V)}$$

Aperture Time — The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Hold Step Error — The output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{Hold Step (V)} = \frac{\text{Charge Transfer (pC)}}{100\text{pF}}$$

See Sample/Hold Amplifier Performance Curves.

Effective Aperture Delay Time (EADT) — The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty — The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Drift Current — The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D \text{ (pA)} = C_H \text{ (pF)} \times \frac{\Delta V}{\Delta T} \text{ (Volts/sec)}$$

Analog/Digital Converter

Linearity Error — Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level one and one-half (1½) LSB's beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HY-9674K, L, and B grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HY-9674J and A grades are guaranteed to ±1LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one. Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes) — A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HY-9674K, L, and B grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HY-9674J and A grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset — The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset — Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error — The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value one and one-half (1½) LSB's below the nominal full scale (9.9963 volts for 10,000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

Temperature Coefficients — The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection — The standard specifications for the HY-9674 assume use of +5.00 and ±15.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width — A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

Quantization Uncertainty — Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-Justified Data — The data format used in the HY-9674 is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HY-9674

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

Physical Mounting and Layout Considerations

Layout — Unwanted, parasitic circuit components, (L, R and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies — Supply voltages to the HY-9674 (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessasry to counter the effect of variations in supply current. Connect one pair from pin 24 to 10 (V_{LOGIC} Supply), one from pin 31 to 5 (V_{CC} to Analog Common) and one from pin 2 to 5 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections — Pin 5 (Analog Common) and pin 10 (Digital Common) should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 5 to (usually) 15V common, and from pin 10 to (usually) the +5V logic common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 5 and 10: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HY-9674's Analog Common or Digital Common.

Range Connections And Calibration Procedures

The HY-9674 is a "complete sampling" A/D converter, meaning it can be fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HY-9674 offers three standard input ranges: 0V to +10V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration — Refer to Figure 2. The resistors shown are for calibration of offset and gain. If this is not required, replace R2* with a 50Ω, 1% metal film resistor and remove the network on pin 7. Connect pin 7 to pin 5. Then connect the S/H output to pin 8 for the 0V to 10V range. Inputs to +20V (5V over the power supply) are no problem for the A/D - the converter operates normally. But the $\overline{S}$/H cannot handle inputs over V_{CC}.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is settling the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +½LSB (+1.22mV for the 10V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is one and one-half (1½) LSB's below the nominal full scale (+9.9963V for 10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration — Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the $\overline{S}$/H output to pin 8 for a ±5V range, or to pin 9 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage ½LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage one and one-half (1½) LSB's below positive full scale (+4.9963V for ±5V range; +9.9927 for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 8.

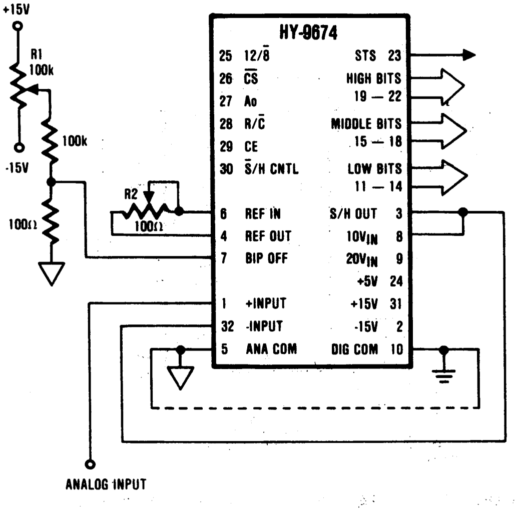

+15V
R1
100k
100k
-15V
R2
100Ω
100Ω
HY-9674
25 12/$\overline{8}$
26 $\overline{CS}$
27 A0
28 R/$\overline{C}$
29 CE
30 $\overline{S}$/H CNTL
6 REF IN
4 REF OUT
7 BIP OFF
1 +INPUT
32 -INPUT
5 ANA COM
STS 23
HIGH BITS 19 — 22
MIDDLE BITS 15 — 18
LOW BITS 11 — 14
S/H OUT 3
10V$_{IN}$ 8
20V$_{IN}$ 9
+5V 24
+15V 31
-15V 2
DIG COM 10
ANALOG INPUT

FIGURE 2. UNIPOLAR CONNECTIONS

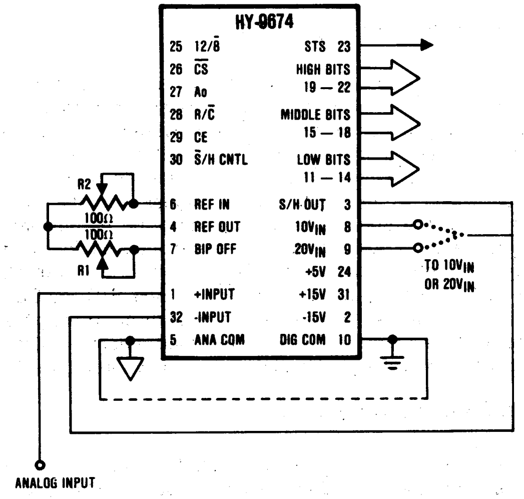

HY-9674
R2
100Ω
100Ω
R1
25 12/$\overline{8}$
26 $\overline{CS}$
27 A0
28 R/$\overline{C}$
29 CE
30 $\overline{S}$/H CNTL
6 REF IN
4 REF OUT
7 BIP OFF
1 +INPUT
32 -INPUT
5 ANA COM
STS 23
HIGH BITS 19 — 22
MIDDLE BITS 15 — 18
LOW BITS 11 — 14
S/H OUT 3
10V$_{IN}$ 8
20V$_{IN}$ 9
+5V 24
+15V 31
-15V 2
DIG COM 10
TO 10V$_{IN}$ OR 20V$_{IN}$
ANALOG INPUT

FIGURE 3. BIPOLAR INPUT CONNECTIONS

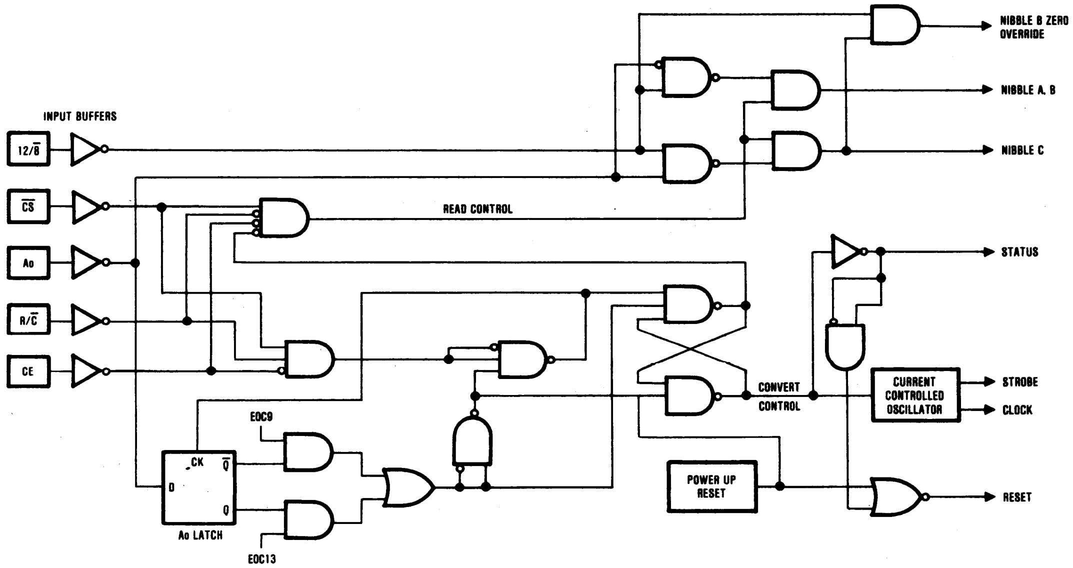

NIBBLE B ZERO OVERRIDE
NIBBLE A, B
NIBBLE C
INPUT BUFFERS
$12/\overline{8}$
$\overline{CS}$
A_0
$R/\overline{C}$
CE
READ CONTROL
STATUS
CONVERT CONTROL
CURRENT CONTROLLED OSCILLATOR
STROBE
CLOCK
EOC9
CK
$\overline{Q}$
D
Q
A_0 LATCH
EOC13
POWER UP RESET
RESET

FIGURE 4. HY-9674 ADC CONTROL LOGIC

Controlling The HY-9674

The HY-9674 includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the $R/\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, capturing the signal with the $\overline{S}/H$, initiating the conversion, and reading the output data when ready - choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The six control inputs are all TTL/CMOS compatible: ($12/\overline{8}$, $\overline{CS}$, A_O, $\overline{S}/H$, $R/\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic for the ADC is shown in Figure 4.

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to $R/\overline{C}$ as shown in Figure 5. The output data appears in words of 12 bits each.

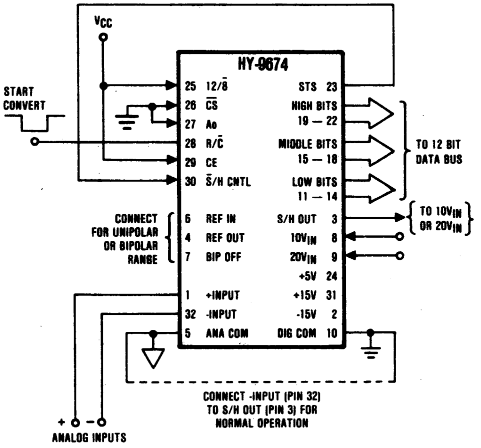

V_{CC}
HY-9674
START CONVERT
25 $12/\overline{8}$
26 $\overline{CS}$
27 A_0
28 $R/\overline{C}$
29 CE
30 $\overline{S}/H$ CNTL
STS 23
HIGH BITS 19 — 22
MIDDLE BITS 15 — 18
LOW BITS 11 — 14
TO 12 BIT DATA BUS
CONNECT FOR UNIPOLAR OR BIPOLAR RANGE
6 REF IN
4 REF OUT
7 BIP OFF
S/H OUT 3
$10V_{IN}$ 8
$20V_{IN}$ 9
+5V 24
1 +INPUT
+15V 31
32 -INPUT
-15V 2
5 ANA COM
DIG COM 10
TO $10V_{IN}$ OR $20V_{IN}$
CONNECT -INPUT (PIN 32) TO S/H OUT (PIN 3) FOR NORMAL OPERATION
+
-
ANALOG INPUTS

FIGURE 5. GENERAL PURPOSE 12 BIT "STAND ALONE" CONFIGURATION

The $R/\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 6 and 7. In general, data may be read when $R/\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing."

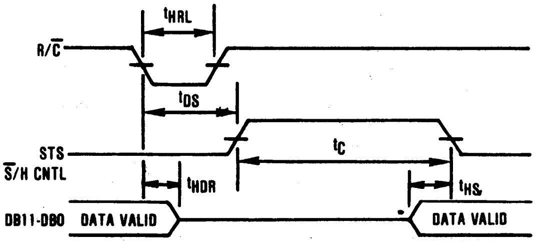


FIGURE 6. LOW PULSE FOR $R/\overline{C}$ — OUTPUTS ENABLED AFTER CONVERSION

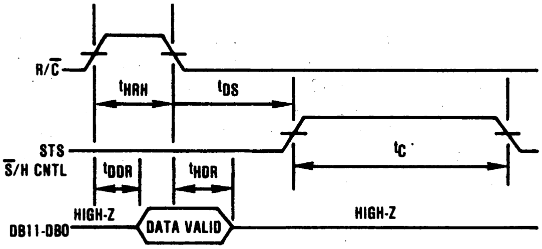


FIGURE 7. HIGH PULSE FOR $R/\overline{C}$ — OUTPUTS ENABLED WITH $R/\overline{C}$ HIGH, OTHERWISE HIGH-Z

Stand-Alone Mode Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low $R/\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from $R/\overline{C}$			200	ns
t_{HDR}	Data Valid After $R/\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	100	300	600	ns
t_{HRH}	High $R/\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

Conversion Length

A Convert Start transition (See Table 1) latches the state of A_O, which determines whether the conversion continues for 12 bits (A_O low) or stops with 8 bits (A_O high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB3 will read ONE. A_O is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

TABLE 1. TRUTH TABLE FOR HY-9674 CONTROL INPUTS

CE	$\overline{CS}$	$R/\overline{C}$	$12/\overline{8}$	A_O	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

Once a signal is captured by the $\overline{S}$/H, conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or $R/\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50ns earlier, however. See the HY-9674 Timing Specifications, Convert Mode.

This variety of HY-9674 control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 8.

The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an

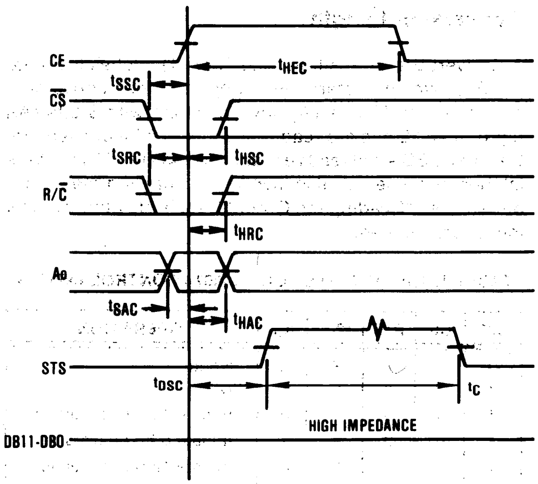


FIGURE 8. CONVERT START TIMING

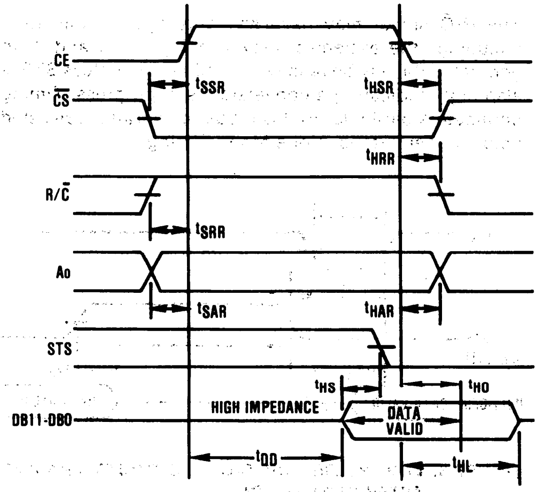


FIGURE 9. READ CYCLE TIMING

additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_O changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_O, possibly causing a wrong cycle length (8 vs 12 bits) for that conversion).

Reading The Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_O. Timing constraints are illustrated in Figure 9.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_O input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_O. This allows an 8 bit data bus to be connected as shown in Figure 10. A_O is usually tied to the least significant bit of the address bus, for storing the HY-9674 output in two consecutive memory locations. (With A_O low, the 8 MSB's only are enabled. With A_O high, 4 MSB's are disabled, bits 4 through 7 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:

BYTE 1								BYTE 2							
X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0
MSB											LSB				

Further, A_O may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 10 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. See Figure 9.

HY-9674 ADC Timing Specifications at +25°C *

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
t_{DSC}	STS Delay from CE		100	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low during CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low during CE High	50	20		ns
t_{SAC}	A_0 to CE Setup	0	0		ns
t_{HAC}	A_0 Valid during CE High	50	20		ns
t_C	Conversion Time, 12-Bit Cycle**	9	12	15	µs
	8-Bit Cycle**	6	8	10	µs
READ MODE					
t_{DD}	Access Time from CE		75	150	ns
t_{HD}	Data Valid after CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0		ns
t_{SAR}	A_0 to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid after CE Low	0	0		ns
t_{HRR}	R/$\overline{C}$ High after CE Low	0	0		ns
t_{HAR}	A_0 Valid after CE Low	50	25		ns
t_{HS}	STS Delay after Data Valid	100	300	600	ns

* Time is measured from 50% level of digital transitions.

** Tmin to Tmax

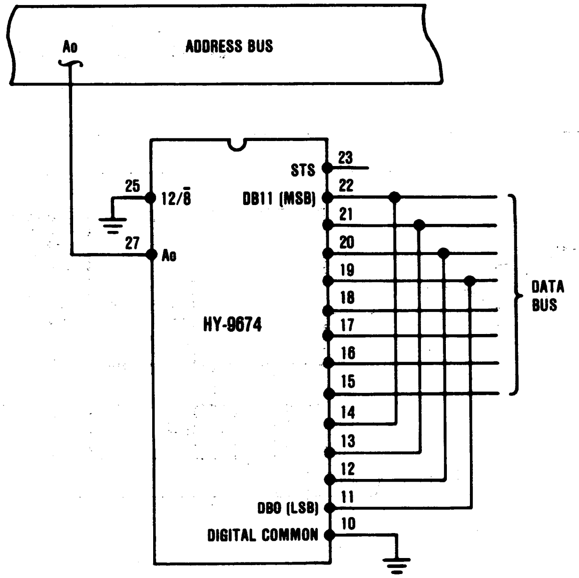

A0
ADDRESS BUS
25
12/8̄
27
A0
HY-9674
STS
DB11 (MSB)
DB0 (LSB)
DIGITAL COMMON
23
22
21
20
19
18
17
16
15
14
13
12
11
10
DATA BUS

FIGURE 10. INTERFACE TO AN 8-BIT DATA BUS

HARRIS HY-94741/742

PRELIMINARY

Low Power Sampling 12 Bit A/D Converter With 8/16 Bit µP Interface

Features

- Pin for Pin Replacement for the Industry Standard 574 A/D Converter
- Sample-and-Hold Circuit Added for Improved Performance
- Sample-and-Hold Controlled Internally - Operation is Transparent to the User
- 12- or 8-Bit Resolution Modes, Software Selectable
  - ▶ Permits Faster Measurements when Inputs are Changing Quickly and Resolution is not as Important — Full 12-bit Resolution Available when Inputs Settle
- Throughput Rate 12-bit .... 43kHz (23.2 µs)
  (Typical) 8-bit .... 65kHz (15.3 µs)
- Successive Approximation A/D Converter
- Full 8-, 12-, or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- Plastic 28-Pin Dual-In-Line Package (DIP) for Commercial and Industrial Temperature Ranges; Hermetic Ceramic Package for Military Range

HY-94741

- 10V Input Range (Bipolar & Unipolar)

HY-94742

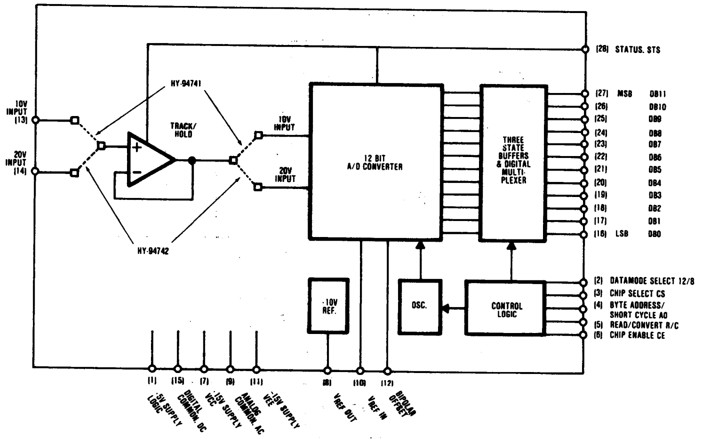
- 20V Bipolar Input Range

Applications

- Process Control Systems
- Precision Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation

Functional Diagram

HY-94741/94742
SAMPLING A/D CONVERTER


10V INPUT (13)
20V INPUT (14)
HY-94741
TRACK/ HOLD
HY-94742
10V INPUT
20V INPUT
12 BIT A/D CONVERTER
THREE STATE BUFFERS & DIGITAL MULTI-PLEXER
(28) STATUS, STS
(27) MSB DB11
(26) DB10
(25) DB9
(24) DB8
(23) DB7
(22) DB6
(21) DB5
(20) DB4
(19) DB3
(18) DB2
(17) DB1
(16) LSB DB0
-10V REF.
OSC.
CONTROL LOGIC
(2) DATAMODE SELECT 12/8
(3) CHIP SELECT CS
(4) BYTE ADDRESS/ SHORT CYCLE A0
(5) READ/CONVERT R/C
(6) CHIP ENABLE CE
(1) +5V SUPPLY LOGIC
(15) DIGITAL COMMON, DC
(7) +15V SUPPLY VCC
(9) ANALOG COMMON, AC
(11) -15V SUPPLY VEE
(8) VREF OUT
(10) VREF IN
(12) BIPOLAR OFFSET

Description

The HY-9474x is a complete 12-bit Sampling Analog-to-Digital Converter, pin- and functionally-compatible with the popular 574 A/D Converter. A high performance Track-and-Hold Amplifier has been integrated into the 28-pin 574 package to provide accuracy and repeatability when sampling rapidly changing signals. Analog input circuits can now enjoy the benefits of a Track-and-Hold without the need for redesign, because the HY-9474x is a direct replacement for the 574 A/D.

The Track-and-Hold feature is transparent to the user, and requires no special considerations. The HY-9474x is operated exactly like a plain 574 A/D, with the T/H function being controlled internally.

A/D Section

The Analog-to-Digital (A/D) section uses the proven HI-574A, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice (bipolar analog and CMOS digital) housed in the 28-pin package.

T/H Section

The Track-and-Hold (T/H or S/H) section uses the Harris HA-2420 chip, consisting of a high performance operational amplifier, an ultra-low leakage analog switch and a MOSFET-input amplifier to drive the A/D. A hold capacitor is included inside the package, and none is required externally. The T/H is configured for non-inverting unity gain.

Process

The T/H and the A/D bipolar chip feature the Harris Dielectric Isolation process which minimizes stray capacitance for enhanced AC performance. Also, parasitic SCRs are eliminated, providing latch-free operation. The CMOS digital chip of the A/D uses the Harris Self-Aligned Junction Isolation (SAJI) process.

Input Ranges

The HY-9474x offers the most popular unipolar and bipolar input ranges, as shown below:

HY-9474x INPUT VOTAGE RANGES

MODEL NUMBER	BIPOLAR RANGE	UNIPOLAR RANGE
HY-94741	-5 to +5V	0 to +10V
HY-94742	-10 to +10V	0 to 10V (11 Bits)

NOTE:

The T/H curcuit used in the HY-9474x cannot tolerate input voltages which exceed the power supply, so the 0 to +20V input range available on the 574 A/D is not supported by the HY-9474x.

Temperature Grades

The HY-9474x will be available initially in Commercial (0 to +75°C) and Industrial (-40 to +85°C) temperature grades. A grade is also being developed for the military temperature range (-55 to +125°C).

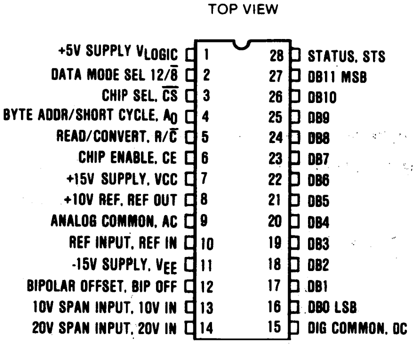
Power Requirements

Power requirements are +5V and ±15V with typical dissipation of 700mW.

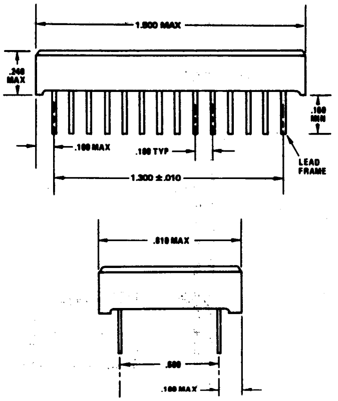
Package

All models are packaged in a 28-pin DIP with 600 mil row centers. Plastic packages are used for commercial and industrial grades. Ceramic hermetic packages will be used for the military temperature grade.

Pinout


TOP VIEW
+5V SUPPLY V_{LOGIC} 1
DATA MODE SEL 12/$\overline{8}$ 2
CHIP SEL. $\overline{CS}$ 3
BYTE ADDR/SHORT CYCLE. A_0 4
READ/CONVERT. R/$\overline{C}$ 5
CHIP ENABLE. CE 6
+15V SUPPLY. VCC 7
+10V REF. REF OUT 8
ANALOG COMMON. AC 9
REF INPUT. REF IN 10
-15V SUPPLY. V_{EE} 11
BIPOLAR OFFSET. BIP OFF 12
10V SPAN INPUT. 10V IN 13
20V SPAN INPUT. 20V IN 14
28 STATUS. STS
27 DB11 MSB
26 DB10
25 DB9
24 DB8
23 DB7
22 DB6
21 DB5
20 DB4
19 DB3
18 DB2
17 DB1
16 DB0 LSB
15 DIG COMMON. DC

Package


1.500 MAX
.240 MAX
.100 MIN
.100 MAX
.100 TYP
LEAD FRAME
1.300 ± .010
.610 MAX
.600
.100 MAX

HARRIS

HY-9712

PRELIMINARY

Complete 12-Bit Data Acquisition Subsystem

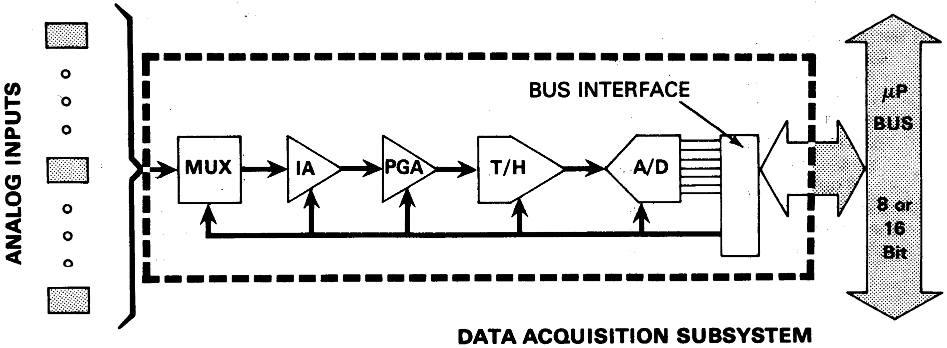
Features

- Complete Multi-Channel Data Acquisition System in a Single Module
- Companion to the HY-98C86 Microprocessor Module
- Input Multiplexer
  - 16 channels pseudo differential or 8 channels differential
  - input overvoltage protection
  - multiplexer expansion pins provided
  - channel select word latched in internal control register
- Precision Instrumentation Amplifier (IA)
  - resistor programmable gains from 1 to 1000
- Programmable Gain Amplifier (PGA)
  - software controllable gains: 1, 2, 4, 8, 128, 256, 512, 1024
  - uncommitted output - filtering or waveshaping can be inserted
  - gain select word latched in internal control register
- Track-and-Hold (T/H)
  - self contained - no external capacitor required
  - low droop rate
  - low apperture uncertainty
  - uncommitted output
- Analog-to-Digital Converter (A/D)
  - 12 bit resolution
  - 8 bit mode for high speed measurements
  - 10V and 20V input ranges
  - bipolar and unipolar conversion modes
  - no missing codes over temperature
  - bus interface for 8MHz systems (8 or 16 bit)
- Precision 10V Reference with 10mA Drive Capability
- Bi-directional 8 Bit Data Bus Interface
  - input control register for channel and gain selection
  - two 8 bit data registers for high and low byte of A/D output
- Interrupt Output Line to Tell Microprocessor When Data is Available
- "Lost Data" Flag Tells When Data Has Not Been Read Before Next Conversion is Completed
- Temperature Grades Offered
  - Military (−55 to +125°C)
  - Industrial (−40 to +85°C)
  - Commercial (0 to +75°C)

Applications

- Avionics
- Portable Data Acquisition Systems
- Process Control
- Robotics

Functional Diagram



DATA ACQUISITION SUBSYSTEM

ANALOG Digital-to-Analog Converters 6

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ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

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HI-565A
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Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H I 1 - 562A - 5

PREFIX:
H (HARRIS)

FAMILY:
A — Analog
C — Communications
D — Digital
F — Filters
I — Interface
M — Memory
V — Analog, High Voltage
Y — Analog Hybrids

PACKAGE:
1 — Dual-In-Line, Ceramic
2 — Metal Can
3 — Dual-In Line, Plastic
4 — Leadless Carriers (LCC)
5 — LCC Hybrid
7 — Mini-DIP, Ceramic
0 — Chip Form

PART NUMBER

TEMPERATURE:
1 — 0°C to +200°C *
2 — -55°C to +125°C
4 — -25°C to +85°C
5 — 0°C to +75°C
6 — 100% +25°C Probe (Dice Only)
7 — Dash-7 High Reliability Commercial Product. 0°C to +75°C
8 — Dash-8 Program HA2-2520-8 (Example only)
9 — -40°C to +85°C

* Special high temperature testing available on certain product types. Consult factory for availability.

Standard Products Packaging Availability

PACKAGE	PLASTIC DIP	CERAMIC DIP				SURFACE MOUNT LCC
TEMPERATURE	-5	-2	-4	-5	-8	-8
DEVICE NUMBER						
DIGITAL TO ANALOG						
HI-562A		X		X	X	X
HI-565A		X		X	X	
HI-5610		X		X	X	
HI-5618A		X		X	X	
HI-5618B		X		X	X	
HI-5660		X		X	X	
HI-5660A		X		X	X	
HI-5680I				X		
HI-5680V				X		
HI-5685AI			X			
HI-5685AV			X			
HI-5685I			X			
HI-5685V			X			
HI-5687I		X			X	
HI-5687V		X			X	*
HI-5690V				X		
HI-5695V			X			
HI-5697V		X			X	*
HI-5811	X	X	X	X		
HI-7541		X	X	X	X	
HI-DAC16B/16C				X		

*Available as MIL-STD-883 Only.

Selection Guide

D/A CONVERTERS

Part Number	Features	Resolution (Bits)	Maximum Output Range	Settling Time to ±1/2 LSB (Typ.)	Gain Error (% FSR)	Differential Non-Linearity (Max. @ 25°C) (LSB)	Intergral Non-Linearity (Max. @ 25°C) (LSB)	Reference Requirements VIN/RIN (V/Ω)	Supply Voltage Power Dissipation † (V/mW, Typ.)	DIP Package Pin Count	Page
						-5/-2	-5/-2				
HI-562A	Industry Standard	12	-2mA	300ns	±0.024	±1/2 to ±1/4	±1/2 to ±1/4	+10/20K	+5, -15/280	24*	6-5
HI-565A	+10V Reference On-Chip	12	-2mA	350ns	±0.1	±1/2 to ±3/4	±1/4 to ±1/2	+10/20K (Internal)	±15/320	24	6-10
HI-5610	High Speed	10	-5mA	85ns	±0.05	±1/2	±1/2	+10/8K	+5, -15/420	24	6-17
HI-5618A	High Speed	8	-5mA	65ns	±0.78	±1/4	±1/4	+10/8K	+5, -15/330	18	6-23
HI-5618B	High Speed	8	-5mA	65ns	±0.78	±1/2	±1/2	+10/8K	+5, -15/330	18	6-23
HI-5660	Low Glitch	12	-2mA	250ns	±0.1	±3/4	±1/2	+10/20K	±15/230	24	6-30
HI-5660A	Low Glitch	12	-2mA	250ns	±0.1	±1/2	±1/4	+10/20K	±15/230	24	6-30
HI-5680V/I	Voltage Current DAC 80, 0°C to +75°C	12	±10V -2mA	1.5µs/ 300ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	+5, ±12/320	24	6-39
HI-5685V/I	Voltage/Current DAC 80, -25°C to +85°C	12	±10V -2mA	1.5µs/ 300ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	+5, ±12/320	24	6-45
HI-5685AV/I	Voltage/Current Low Drift -25°C to +85°C	12	±10V -2mA	1.5µs/ 300ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	+5, ±12/320	24	6-45
HI-5687V/I	Voltage/Current DAC 80, -55°C to +125°C	12	±10V -2mA	1.5µs/ 300ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	+5, ±12/320	24*	6-48
HI-5690V	Fast Settling V_O; DAC 80 0°C to +75°C	12	±10V	750ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	±12/555	24	6-51
HI-5695V	Fast Settling V_O; DAC 80 -25°C to +85°C	12	±10V	750ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	±12/555	24	6-51
HI-5697V	Fast Settling V_O; DAC 80 -55°C to +125°C	12	±10V	750ns	±0.1	±3/4	±1/2	+6.3/12.6K (Internal)	±12/555	24*	6-51
HI-5811	Voltage Out Latched	12	±10V	3µs	±0.1	±1/2	±1/4	+6.3/5.36K (Internal)	±15/625	28	6-57
HI-7541	Multiplying; Low Power; CMOS	12	1mA	1.0µs Max.	±0.305	±0.5 to ±1.0	±0.5 to ±1.0	±10/9K	+15/30 Max.	18	6-66
HI-DAC16B	16 Bit Monolithic	16	-2mA	1.0µs (14 Bits)	±0.1	±1 Typ.	±1.5 Typ.	+10/10K	±15/465	40	6-73
HI-DAC16C	16 Bit Monolithic	16	-2mA	1.0µs (14 Bits)	±0.1	±2 Typ.	±3 Typ.	+10/10K	±15/465	40	6-73

*Surface Mount Package Available

† Most supplies can be varied from ±12 volts to ±15 volts, please see data sheets for specific information.

HARRIS

HI-562A

12 Bit High Speed Monolithic Digital-to-Analog Converter

Features

- **Output Current .... 2mA, F.S.**
- **Monolithic Construction**
- **Extremely Fast Settling .... 300ns To 0.01% (Typ)**
- **Low Gain Drift .... ±10ppm/°C (Max)**
- **Linearity Guaranteed Over Temperature...... ±1/2 LSB (Max)**
- **Designed for Minimum Glitches**
- **Monotonic Over Temperature**

Applications

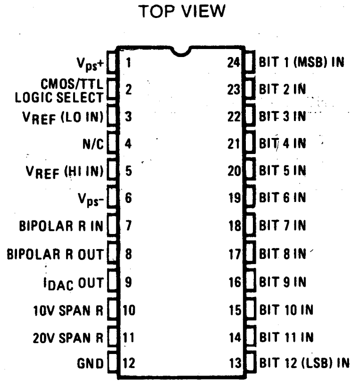
- **CRT Display Generation**
- **High Speed A/D Converters**
- **Video Signal Reconstruction**
- **Waveform Synthesizers**
- **High Speed Data Acquisition**
- **High-Rel Applications**
- **Precision Instruments**

Description

The Harris HI-562A is the first monolithic digital-to-analog converter to combine both high speed performance and 12-bit accuracy on the same chip. The HI-562A's fast output current settling of 300ns to 0.01% is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562A by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562A with guaranteed 12-bit linearity to within ±1/2 LSB maximum at +25°C for -4 and -5 parts and to within ±1/4 LSB maximum at +25°C for -2 and -8 parts. The HI-562A is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 3.3 MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562A is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

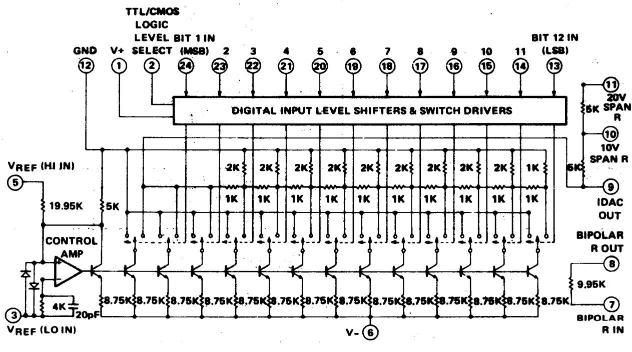
The HI-562A is offered in commercial, industrial and military grades. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix. All are available in a hermetically sealed 24-lead dual-in-line package.

Pinout


TOP VIEW
Vps+ 1
CMOS/TTL LOGIC SELECT 2
VREF (LO IN) 3
N/C 4
VREF (HI IN) 5
Vps- 6
BIPOLAR R IN 7
BIPOLAR R OUT 8
IDAC OUT 9
10V SPAN R 10
20V SPAN R 11
GND 12
24 BIT 1 (MSB) IN
23 BIT 2 IN
22 BIT 3 IN
21 BIT 4 IN
20 BIT 5 IN
19 BIT 6 IN
18 BIT 7 IN
17 BIT 8 IN
16 BIT 9 IN
15 BIT 10 IN
14 BIT 11 IN
13 BIT 12 (LSB) IN

For LCC Pinout see page 6.

Schematic


TTL/CMOS LOGIC LEVEL SELECT
GND ⑫
V+ ①
②
BIT 1 IN (MSB) ㉔
2 ㉓
3 ㉒
4 ㉑
5 ⑳
6 ⑲
7 ⑱
8 ⑰
9 ⑯
10 ⑮
11 ⑭
BIT 12 IN (LSB) ⑬
DIGITAL INPUT LEVEL SHIFTERS & SWITCH DRIVERS
⑪ 20V SPAN R
5K
⑩ 10V SPAN R
5K
⑨ IDAC OUT
BIPOLAR R OUT ⑧
9.95K
⑦ BIPOLAR R IN
VREF (HI IN) ⑤
19.95K
5K
2K
1K
CONTROL AMP
4K
20pF
8.75K
③ VREF (LO IN)
V- ⑥

Absolute Maximum Ratings (Referred to Ground)[1]

Power Supply Inputs	
$V_{ps}+$	+20V
$V_{ps}-$	-20V
Reference Inputs	
V_{REF} (High)	±16.5V
Digital Inputs	
Bits 1-12 (TTL)	-1V, +7.5V
Bits 1-12 (CMOS)	-1V, $V_{ps}+$
CMOS/TTL Logic Select	-1V, +16.5V
Outputs	
Pins 7, 8, 10, 11	$\pm V_{ps}$
Pin 9	$+V_{ps}$, -5V
Power Dissipation	
Pd, Package (Ceramic DIP)	2000mW*

Operating Temperature Range	
HI-562A-2	-55°C to +125°C
HI-562A-4	-25°C to +85°C
HI-562A-5	0°C to +75°C
HI-562A-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

*Derate 20mW/°C above 75°C

Electrical Characteristics (@ +25°C, $V_{ps}+$ = +5V, $V_{ps}-$ = −15V, V_{REF} = +10V, pin 2 tied to pin 12 unless otherwise noted)

PARAMETER	CONDITIONS	HI-562A-2/HI-562A-8			HI-562A-4/HI-562A-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Digital Inputs (3)	Bit ON "Logic 1" Bit OFF "Logic 0"							
TTL/CMOS Input Voltage (2)	($V_{ps}+$ <9.5V) Pin 2 tied to Pin 12 Over full temp. range							
Logic "1"		2.0			2.0			V
Logic "0"				0.8			0.8	V
Input Current (2)								
Logic "1"			20	±500		20	±500	nA
Logic "0"			-50	-100		-50	-100	μA
CMOS Input Voltage	Pin 2 tied to Pin 1 ($V_{ps}+ \geq +9.5V$) over full temp. range							
Logic "1"		$0.7V_{ps}+$			$0.7V_{ps}+$			V
Logic "0"				$0.3V_{ps}+$			$0.3V_{ps}+$	V
Input Current								
Logic "I"			20	±500		20	±500	nA
Logic "0"			-50	-100		50	-100	μA
Reference Input								
Input Resistance	(± 20%)		19.95K			19.95K		Ω
Input Voltage			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Over full temp. range			12			12	Bits
Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range		±1/2	±1			±1	
Differential Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range		MONOTONICITY GUARANTEED					
Relative Accuracy (6)	With 50Ω (1%) Resistors							
Gain Error	All Bits ON		±.024	±0.25		±.024	±0.25	%FSR (4)
Bipolar Offset Error	All Bits OFF		±.024	±0.25		±.024	±0.25	
Unipolar Offset Error			±.012	±0.05		±.012	±0.05	
Adjustment Range	See Operating Instructions							
Gain	With 100Ω Trim		±0.3			±0.3		%FSR
Bipolar Offset	Potentiometers		±0.6			±0.6		
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (3)	Over full temp. range		±6	±10			±10	ppm of FSR/°C
Offset Drift (3)								
Unipolar Offset	All Bits OFF			±2			±2	
Bipolar Offset				±4			±4	
Differential Nonlinearity	Over full temp. range		±1	±2		±1	±2	
Settling Time (3) to ±1/2 LSB	All Bits ON-to-OFF or OFF-to-ON		300	400		300	400	ns

Specifications HI-562A (continued)

PARAMETER	CONDITIONS	HI-562A-2/HI-562A-8			HI-562A-4/HI-562A-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Major Carry Transient								
Peak Amplitude	From 011...1 to 100...0		0.7			0.7		mA
Settling Time to 90% Complete	or 100...0 to 011...1		35			35		ns
Power Supply Sensitivity (3)								
Unipolar Offset	All Bits OFF							ppm of FSR/%V_{ps}
$V_{ps}+$ @ +5V or +15V			±0.5			±0.5		
$V_{ps}-$ @ −15V			±0.5			±0.5		
Bipolar Offset								
$V_{ps}+$ @ 5V or +15V	All Bits OFF, Bipolar mode		±1.5			±1.5		
$V_{ps}-$ @ −15V			±1.5			±1.5		
Gain								
$V_{ps}+$ @ +5V or +15V	All Bits ON			±3.5			±3.5	
V_{ps-} @ −15V				±7.5			±7.5	
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar		-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar		±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	
Resistance			2K			2K		ohms
Capacitance			20			20		pF
Output Voltage Ranges								
Unipolar	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections		0 to +5 0 to +10			0 to +5 0 to +10		V
Bipolar			±2.5 ±5 ±10			±2.5 ±5 ±10		
Compliance Limit (3)		-3		+10	-3		+10	V
Compliance Voltage (3)	Over full temp. range		±1.0			±1.0		V
Output Noise	0.1 to 10 Hz (All Bits ON)		30			30		μV (p-p)
	0.1 to 5 MHz (All Bits ON)		100			100		
POWER REQUIREMENTS								
$V_{ps}+$ (7)	Over full temp. range	4.5	5	16.5	4.75	5	16.5	V
$V_{ps}-$		-13.5	-15	-16.5	-13.5	-15	-16.5	
$I_{ps}+$ (5)	All Bits ON or OFF in either TTL or CMOS mode (25°C)		8	15		8	15	mA
I_{ps-} (5)			16	23		16	23	
$I_{ps}+$ (5)	Same as above except over full temp. range		11	20		11	20	mA
$I_{ps}-$ 5			20	30		20	30	
Power Dissipation	$V_{ps}+ = +5V$ (25°C) $V_{ps}- = -15V$		280	420		280	420	mW

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these condiitons is not necessarily implied.
2. $V_{ps}+$ tolerance is ±10% for HI-562A-2, -8, and ±5% for HI-562A-4, -5.
3. See Definitions.
4. FSR is "full scale range" and is 20V for ±10V ranges, 10V for ±5V ranges, etc., or 2mA (±20%) for current output.
5. After 30 seconds warm-up.
6. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R1 and R2. Errors are adjustable to zero using R1 and R2 potentiometers. (See Operating Instructions Figure 2.)
7. The HI-562A is designed for $V_{ps}+ = 5V$, but $+4.5V \leq V_{ps}+ \leq 16.5V$ may be connected if convenient. (For $V_{ps}+$ above +5V, there is an increase in power dissipation but little change in performance.

Die Characteristics

Transistor Count 150
Die Size .... 103 x 209 mils
Thermal Impedance
θja ....50°C/W
θjc ....15°C/W
Tie Substrate to ....V_{REF} Lo (Analog Ground)
Process ....Bipolar-DI

Definitions of Specifications

Digital Inputs

The HI-562A accepts digital input codes in binary format and may be user connected for any one of three binary codes: Straight Binary, Two's Complement, or Offset Binary (see Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	1/2 FS	Zero	-FS
111...111	+FS - 1 LSB	+ FS - 1 LSB	1/2 FS - 1 LSB
011...111	1/2 FS - 1 LSB	Zero - 1 LSB	+FS - 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

Accuracy

INTEGRAL NONLINEARITY—The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY—The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY—The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

Drift

GAIN DRIFT—The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT—The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

Compliance

Compliance voltage is the maximum output range for which specified accuracy limits are guaranteed. Compliance limit implies functional operation only and makes no claims to accuracy.

Glitch

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Operating Instructions

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-562A (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

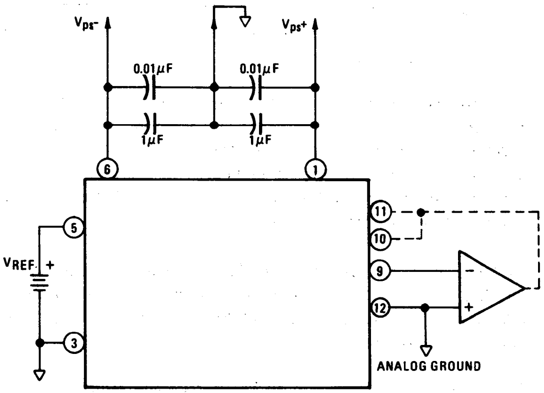
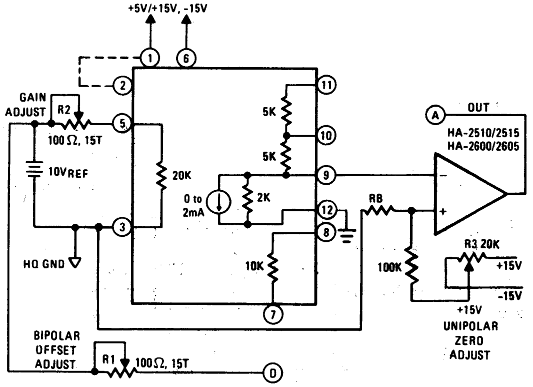


FIGURE 1.

Unipolar and Bipolar Voltage Output Connections

CONNECTIONS—Using an external resistive load, the output compliance should not exceed ±1V to maintain specified accuracy. For higher output voltages, accuracy can be maintained by using an external op amp and the internal span resistors as shown in Figure 2 and defined in Table 1 for unipolar and bipolar modes.



* For TTL and DTL compatibility, connect +5V to pin 1 and tie pin 2 to pin 12. For CMOS compatibility, connect digital power supply (9.5V ≤ VDD ≤ +12V) to pin 1 and short pin 2 to pin 1.

** Bias resistor, RB, should be chosen to equalize op amp offset voltage due to bias current. Its value is calculated from the parallel combination of the current source output resistance (2K) and the op amp feedback resistor. See Table 1 for values of RB.

FIGURE 2.

Table 1

	OUTPUT RANGE	CONNECTIONS				BIAS (R_B) RESISTOR
		Pin 7 to	Pin 8 to	Pin 10 to	Pin 11 to	
Unipolar Mode	0 to +10V	N.C.	N.C.	A	N.C.	1.43K
	0 to +5V	N.C.	N.C.	A	9	1.11K
Bipolar Mode	±10V	D	9	N.C.	A	760Ω
	±5V	D	9	A	N.C.	840Ω
	±2.5V	D	9	A	9	766Ω

External Gain and Zero Calibration (See Figure 2)

The input reference resistor (20K nominal) and bipolar offset resistors shown in Figure 2 are both intentionally set low by 50Ω to allow the user to externally trim-out initial errors to a very high degree of precision. The adjustments are made in the voltage output mode using an external op amp as current-to-voltage converter and the HI-562A internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. For best accuracy over temperature, select an op amp that has good front-end temperature coefficients such as the HA-2600/2605 with offset voltage and offset current tempco's of 5 μV/°C in 1nA/°C, respectively. For high speed voltage mode applications where fast settling is required, the HA-2510/2515 is recommended for better than 1.5μs settling to 0.01%. Using either one, potentiometer R_3 conveniently nulls unipolar offset plus op amp offset in one operation (for HA-2510/2515 and HA-2600/2605 use R_3 = 20K and 100K, respectively). For bipolar mode operation, R_3 should be used to null op amp offset to optimize its tempco (i.e., short 9 to A and adjust R_3 for zero before calibrating in bipolar mode). The gain and bipolar offset adjustment range using 100Ω potentiometers is ±12 LSB and ±25 LSB respectively. If desired, the potentiometers can be replaced with fixed 50Ω (1%) resistors resulting in an initial gain and bipolar offset accuracy of typically ±1/2 LSB.

UNIPOLAR CALIBRATION

Step 1: Unipolar Offset
- Turn all bits OFF
- Adjust R3 for zero volts output

Step 2: Gain
- Turn all bits ON
- Adjust R2 for an output of FS - 1 LSB
  That is, adjust for:
  9.9976V for 0V to +10V range
  4.9988V for 0V to +5V range

BIPOLAR CALIBRATION

Step 1: Bipolar Offset
- Turn all bits OFF
- Adjust R1 for an output of:
  -10V for ±10V range
  -5V for ±5V range
  -2.5V for ±2.5V range

Step 2: Gain
- Turn bit 1 (MSB) ON; all other bits OFF
- Adjust R2 for zero volts output

HARRIS

HI-565A

High Speed Monolithic Digital-to-Analog Converter with Reference

FEATURES

- DAC AND REFERENCE ON A SINGLE CHIP
- PIN COMPATIBLE WITH AD565A
- VERY HIGH SPEED: SETTLES TO 1/2 LSB IN 250ns, MAX.
  FULL SCALE SWITCHING TIME 30ns, TYP.
- GUARANTEED FOR OPERATION WITH ±12V SUPPLIES
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- 1/2 LSB MAX NONLINEARITY GUARANTEED OVER TEMPERATURE
- LOW GAIN DRIFT (MAX, DAC PLUS REFERENCE) 25ppm/°C
- LOW POWER DISSIPATION 250mW

APPLICATIONS

- CRT DISPLAYS
- HIGH SPEED A/D CONVERTERS
- SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIS

DESCRIPTION

The HI-565A is a fast, 12 bit current output, digital to analog converter. The monolithic chip includes a precision voltage reference, thin-film R-2R ladder, reference control amplifier and twelve high-speed bipolar current switches.

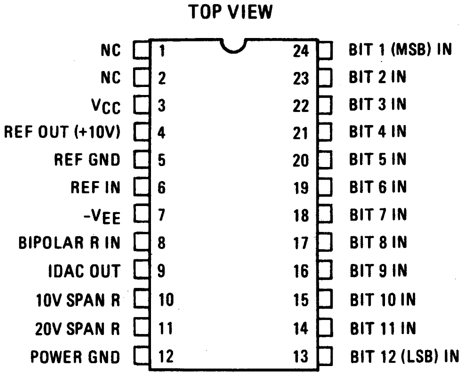
The Harris Semiconductor dielectric isolation process provides latch-free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code-dependent ground currents.

HI-565A dice are laser trimmed for a maximum integral nonlinearity error of ±1/4 LSB at +25°C. In addition, the low noise buried zener reference is trimmed both for absolute value and minimum temperature coefficient.

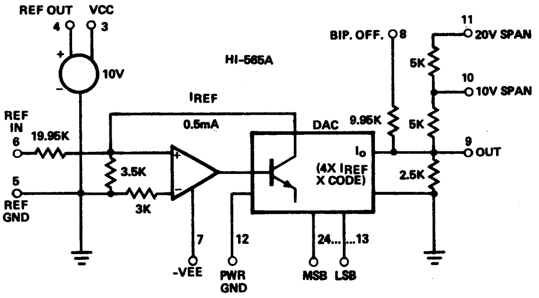
The HI-565A is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. See Ordering Information.

Package is a 24 pin side-brazed ceramic DIP. Power dissipation is typically 250mW, with ±15V supplies.

PINOUT


TOP VIEW
NC 1
NC 2
VCC 3
REF OUT (+10V) 4
REF GND 5
REF IN 6
-VEE 7
BIPOLAR R IN 8
IDAC OUT 9
10V SPAN R 10
20V SPAN R 11
POWER GND 12
24 BIT 1 (MSB) IN
23 BIT 2 IN
22 BIT 3 IN
21 BIT 4 IN
20 BIT 5 IN
19 BIT 6 IN
18 BIT 7 IN
17 BIT 8 IN
16 BIT 9 IN
15 BIT 10 IN
14 BIT 11 IN
13 BIT 12 (LSB) IN

FUNCTIONAL DIAGRAM


REF OUT
VCC
4
3
+
10V
-
HI-565A
BIP. OFF. 8
11
20V SPAN
5K
10
10V SPAN
IREF
0.5mA
DAC
9.95K
5K
REF IN 6
19.95K
3.5K
Io
(4X IREF X CODE)
9
OUT
2.5K
5
REF GND
3K
7
-VEE
12
PWR GND
24... ...13
MSB
LSB

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Power Ground	0V to +18V	10V Span R to Reference Ground	±12V
V_{EE} to Power Ground	0V to -18V	20V Span R to Reference Ground	±24V
Voltage on DAC Output (Pin 9)	-3V to +12V	Ref Out	Indefinite Short to Power Ground Momentary Short to V_{CC}
Digital Inputs (Pins 13-24) to Power Ground	-1V to +7.0V		
Ref In to Reference Ground	±12V	Package Power Dissipation Ceramic (D)*	1960mW
Bipolar Offset to Reference Ground	±12V		

* Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired.

** Derate 19.6mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, Unless Otherwise Specified)

MODEL	HI-565AJ, HI-565AS			HI-565AK, HI-565AT			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX}) Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		.01	+1.0		.01	+1.0	μA
Bit OFF Logic "0"		-2.0	-20		-2.0	-20	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	1.8k	2.5k	3.2k	1.8k	2.5k	3.2k	Ω
Offset Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 2, R_3 = 50Ω Fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		20			20		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-1.5		+10	-1.5		+10	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of F.S.
T_{MIN} to T_{MAX}		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % OF F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED						
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	40		10	25	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB							
With High Z External Load (Note 2)		350	500		350	500	ns
With 75Ω External Load		150	250		150	250	ns

SPECIFICATIONS (Continued)

MODEL	HI-565AJ, HI-565AS MIN	TYP	MAX	HI-565AK, HI-565AT MIN	TYP	MAX	UNITS
FULL SCALE TRANSITION (From 50% of Logic Input to 90% of Analog Output)							
Rise Time		15	30		15	30	ns
Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating (HI-565AJ/K)	0		+75	0		+75	°C
(HI-565AS/T)	-55		+125	-55		+125	°C
Storage							
D Package (All)	-65		+150	-65		+150	°C
N Package (J, K)	-25		+150	-25		+150	°C
POWER REQUIREMENTS							
I_{CC}, +11.4 to +16.5V DC		9.0	11.8		9.0	11.8	mA
I_{EE}, -11.4 to -16.5V DC		-9.5	-14.5		-9.5	-14.5	mA
POWER SUPPLY GAIN SENSITIVITY (Note 3)							
V_{CC} = +11.4 to +16.5 VDC		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5 VDC		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (See Table 1)	0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15K	20K	25K	15K	20K	25K	
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (Available for External Loads)	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		250	375		250	375	mW

NOTES:

1. Guaranteed but not tested over the operating temperature range.
2. See settling time discussion and Figure 3.
3. The Power Supply Gain Sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V.

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-565A accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement*, or Offset Binary, (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB...LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	Zero – 1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition, settling to within 1/2 LSB of final value.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in –15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

APPLYING THE HI-565A

OP AMP SELECTION

The HI-565A's current output may be converted to voltage using the standard connections shown in Figures 1 and 2. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy.

For highest precision, use an HA-5130. This amplifier contributes negligible error, but requires about 11μs to settle within ±0.1% following a 10V step.

The Harris Semiconductor HA-2600 is the best all-around choice for this application, and it settles in 1.5μs (also to ±0.1% following a 10V step). Remember, settling time for the DAC-amplifier combination is $\sqrt{t_D^2 + t_A^2}$, where t_D, t_A are settling times for the DAC and amplifier.

NO-TRIM OPERATION

The HI-565A will perform as specified without calibration adjustments. To operate without calibration, substitute 50 Ω resistors for the 100 Ω trimming potentiometers: In Figure 1 replace R2 with 50Ω ; also remove the network on pin 8 and connect 50Ω to ground. For bipolar operation in Figure 2, replace R3 and R4 with 50Ω resistors.

Table 1 — Operating Modes and Calibration

	CIRCUIT CONNECTIONS:				CALIBRATION:		
MODE	OUTPUT RANGE	PIN10 TO	PIN 11 TO	RESISTOR (R)	APPLY INPUT CODE	ADJUST	TO SET V_O
Unipolar (See Fig. 1)	0 to +10V	V_O	Pin 10	1.43K	All 0's All 1's	R1 R2	0V +9.99756V
	0 to +5V	V_O	Pin 9	1.1K	All 0's All 1's	R1 R2	0V +4.99878V
Bipolar (See Fig. 2)	±10V	NC	V_O	1.69K	All 0's All 1's	R3 R4	-10V +9.99512V
	±5V	V_O	Pin 10	1.43K	All 0's All 1's	R3 R4	-5V +4.99756V
	±2.5V	V_O	Pin 9	1.1K	All 0's All 1's	R3 R4	-2.5V +2.49878V

With these changes, performance is guaranteed as shown under Specifications, "External Adjustments". Typical unipolar zero will be ±1/2 LSB plus the op amp offset.

The feedback capacitor C must be selected to minimize settling time.

CALIBRATION

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero. For the HI-565A, these adjustments are similar whether the current output is used, or whether an external op amp is added to convert this current to a voltage. Refer to Table 1 for the voltage output case, along with Figure 1 or 2.

Calibration is a two step process for each of the five output ranges shown in Table 1. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum value is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

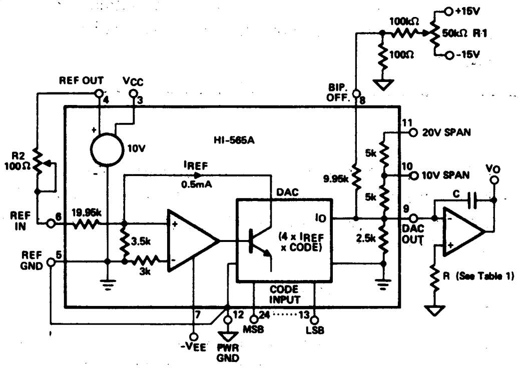

+15V
100kΩ
50kΩ R1
100Ω
-15V
REF OUT
VCC
4
3
BIP. OFF.
8
HI-565A
R2 100Ω
+
10V
-
IREF
0.5mA
11
20V SPAN
5k
10
10V SPAN
9.95k
VO
5k
C
DAC
REF IN
6
19.95k
IO
9
+
-
3.5k
(4 x IREF x CODE)
2.5k
DAC OUT
REF GND
5
3k
R (See Table 1)
CODE INPUT
7
12
24
13
MSB
LSB
-VEE
PWR GND

Figure 1 — Unipolar Voltage Output

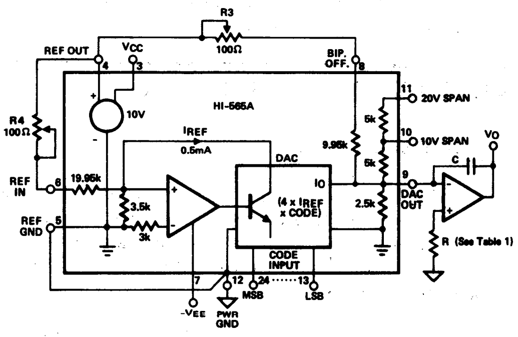

R3
100Ω
REF OUT
VCC
4
3
BIP. OFF.
8
HI-565A
R4 100Ω
+
10V
-
IREF
0.5mA
11
20V SPAN
5k
10
10V SPAN
9.95k
VO
5k
C
DAC
REF IN
6
19.95k
IO
9
+
-
3.5k
(4 x IREF x CODE)
2.5k
DAC OUT
REF GND
5
3k
R (See Table 1)
CODE INPUT
7
12
24
13
MSB
LSB
-VEE
PWR GND

Figure 2 — Bipolar Voltage Output

SETTLING TIME

This is a challenging measurement, in which the result depends on the method chosen, the precision and quality of test equipment and the operating configuration of the DAC (test conditions). As a result, the different techniques in use by converter manufacturers can lead to consistently different results. An engineer should understand the advantage and limitations of a given test method before using the specified settling time as a basis for design.

The approach used for several years at Harris Analog Products Division calls for a strobed comparator to sense final perturbations of the DAC output waveform. This gives the LSB a reasonable magnitude (814μV for the HI-565A), which provides the comparator with enough overdrive to establish an accurate ±1/2 LSB window about the final settled value. Also, the required test conditions simulate the DAC's environment for a common application – use in a successive approximation A/D converter. Considerable experience has shown this to be a reliable and repeatable way to measure settling time.

The usual specification is based on a 10V step, produced by simultaneously switching all bits from off-to-on (t_{ON}) or on-to-off (t_{OFF}). The slower of the two cases is specified, as measured from 50% of the digital input transition to the final entry within a window of ±1/2 LSB about the settled value. Four measurements characterize a given type of DAC:

(a) t_{ON}, to final value +1/2 LSB
(b) t_{ON}, to final value -1/2 LSB
(c) t_{OFF}, to final value +1/2 LSB
(d) t_{OFF}, to final value -1/2 LSB

(Cases (b) and (c) may be eliminated unless the overshoot exceeds 1/2 LSB). For example, refer to Figure 3 for the measurement of case (d).

PROCEDURE

As shown in Figure 3B, settling time equals t_X plus the comparator delay (t_D = 15ns). To measure t_X,

- Adjust the delay on generator # 2 for a t_X of several microseconds. This assures that the DAC output has settled to its final value.
- Switch on the LSB (+5V).
- Adjust the V_{LSB} supply for 50 percent triggering at COMPARATOR OUT. This is indicated by traces of equal brightness on the oscilloscope display as shown in Figure 3B. Note DVM reading.
- Switch the LSB to Pulse (P).
- Readjust the V_{LSB} supply for 50% triggering as before, and note DVM reading. One LSB equals one tenth the difference in the DVM readings noted above.
- Adjust the V_{LSB} supply to reduce the DVM reading by 5 LSB's (DVM reads 10X, so this sets the comparator to sense the final settled value minus 1/2 LSB). Comparator output disappears.
- Reduce generator # 2 delay until comparator output reappears, and adjust for "equal brightness".
- Measure t_X from scope as shown in Figure 3B. Settling time equals t_X + t_D, i.e. t_X +15ns.

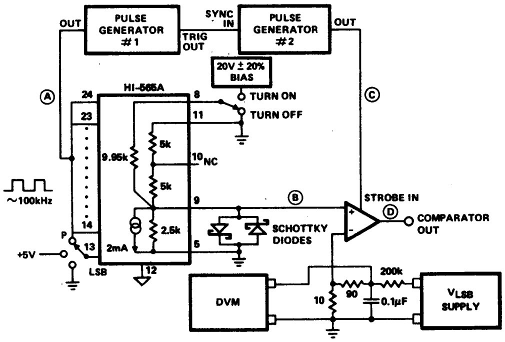

OUT
PULSE GENERATOR #1
SYNC IN
TRIG OUT
PULSE GENERATOR #2
OUT
20V ± 20% BIAS
TURN ON
TURN OFF
Ⓐ
Ⓒ
HI-565A
24
23
14
13
8
11
10 NC
9
5
12
9.95k
5k
5k
2.5k
2mA
~100kHz
P
+5V
LSB
Ⓑ
SCHOTTKY DIODES
STROBE IN
Ⓓ
COMPARATOR OUT
DVM
10
90
200k
0.1µF
VLSB SUPPLY

Figure 3A

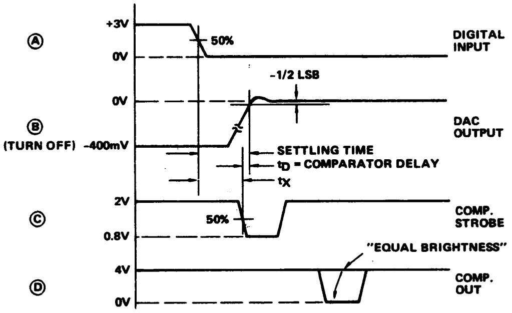

Ⓐ
+3V
0V
50%
DIGITAL INPUT
-1/2 LSB
0V
Ⓑ
(TURN OFF) -400mV
DAC OUTPUT
SETTLING TIME
tD = COMPARATOR DELAY
tX
Ⓒ
2V
0.8V
50%
COMP. STROBE
"EQUAL BRIGHTNESS"
Ⓓ
4V
0V
COMP. OUT

Figure 3B

OTHER CONSIDERATIONS

GROUNDS

The HI-565A has two ground terminals, pin 5 (REF GND) and pin 12 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 5 and 12).

The current through pin 5 is near-zero DC*; but pin 12 carries up to 1.75mA of code – dependent current from bits 1, 2, and 3. The general rule is to connect pin 5 directly to the system "quiet" point, usually called signal or analog ground. Connect pin 12 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

LAYOUT

Connections to pin 9 (I_{OUT}) on the HI-565A are most critical for high speed performance. Output capacitance of the DAC is only 20pF, so a small change or additional capacitance may alter the op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should be short on the side connecting to pin 9 (as for feedback capacitor C). See the Settling Time section.

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI-565A also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 12 is sufficient, since supply current variations are small.

*Current cancellation is a two-step process within the HI-565A in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First an auxiliary 9 bit R-2R ladder is driven by the complement of the DAC's input code. Together, the main and auxiliary ladders draw a continuous 2.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 5).

DIE CHARACTERISTICS

Transistor Count	200
Die Size	179 x 107 mils
Thermal Constants; θ_{ja}	51°C/W
θ_{jc}	16°C/W
Tie Substrate to:	Rer. Ground
Process:	Bipolar - DI

HARRIS

HI-5610

10-Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING . . . . 85ns TO ½LSB TYP.
- LOW GAIN DRIFT . . . . ±5ppm/°C TYP.
- EXCELLENT LINEARITY OVER TEMPERATURE . . . . ± ½LSB MAX.
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH RELIABILITY APPLICATIONS
- PRECISION INSTRUMENTS

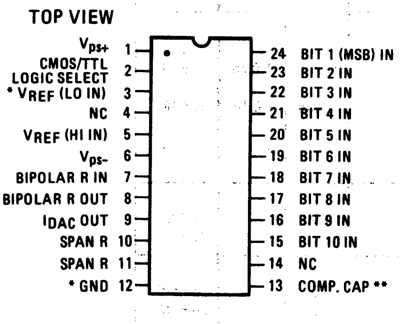
DESCRIPTION

The HI-5610 is an ultra-high speed 10 bit monolithic current output digital-to-analog converter. The fast output current settling of 85ns to ½LSB of its final value is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-5610 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-on and turn-off switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also eliminates thermal transients during switching. High stability thin film resistor processing, together with laser trimming provide the HI-5610 with true 10 bit linearity to within ± ½LSB maximum over operating temperature range. The HI-5610's low offset and gain drift over the operating temperature range assures that its absolute accuracy when referred to a fixed 10V reference will not deviate more than ± 1LSB for both unipolar and bipolar operation.

The HI-5610 is recommended as a replacement for high cost hybrid and modular units for increased reliability and accuracy in applications such as CRT Displays, precision instruments and data acquisition system requiring through-put rates as high as 12MHz for full range transitions. Its small size makes it an ideal choice as the essential part of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-5610 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-5610 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. All are available in a hermetically sealed 24 lead dual-in-line package.

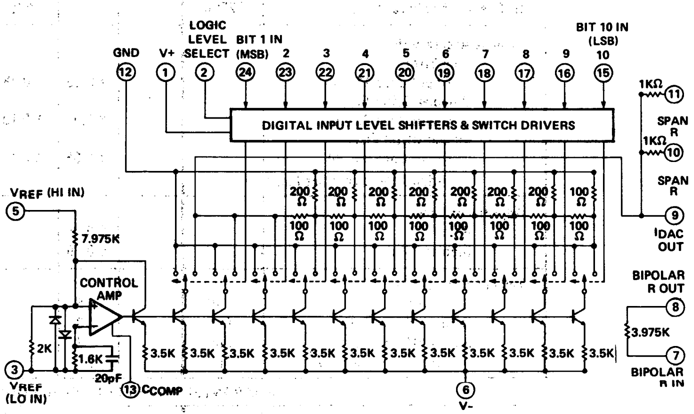
PINOUT


TOP VIEW
V_{ps+} 1
CMOS/TTL LOGIC SELECT 2
* V_{REF} (LO IN) 3
NC 4
V_{REF} (HI IN) 5
V_{ps-} 6
BIPOLAR R IN 7
BIPOLAR R OUT 8
I_{DAC} OUT 9
SPAN R 10
SPAN R 11
* GND 12
24 BIT 1 (MSB) IN
23 BIT 2 IN
22 BIT 3 IN
21 BIT 4 IN
20 BIT 5 IN
19 BIT 6 IN
18 BIT 7 IN
17 BIT 8 IN
16 BIT 9 IN
15 BIT 10 IN
14 NC
13 COMP. CAP **

* Pin 3 connected to bottom case for high frequency shielding.

** For high speed operation, connect 0.01µF between Pin 13 and GND. Otherwise, leave Pin 13 open.

FUNCTIONAL DIAGRAM


GND
V+
LOGIC LEVEL SELECT
BIT 1 IN (MSB)
2
3
4
5
6
7
8
9
BIT 10 IN (LSB) 10
12
1
2
24
23
22
21
20
19
18
17
16
15
DIGITAL INPUT LEVEL SHIFTERS & SWITCH DRIVERS
1KΩ
11
SPAN R
1KΩ
10
SPAN R
9
I_{DAC} OUT
BIPOLAR R OUT
8
3.975K
7
BIPOLAR R IN
200 Ω
100 Ω
VREF (HI IN)
5
7.975K
CONTROL AMP
2K
1.8K
20pF
3
VREF (LO IN)
13 CCOMP
3.5K
6
V-

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	Vps+	+20V
	Vps-	20V
Reference Inputs	VREF (Hi)	+16.5V
	VREF (Lo)	0V
Digital Inputs	Bits 1 -12 (TTL)	-1V, +7.5V
	Bits 1-12 (CMOS)	-1V, Vps+
	CMOS/TTL Logic Sel	-1V, +16.5V
Outputs	Pins 7, 8, 10, 11	+Vps
	Pin 9	+Vps, -5V

Power Dissipation* 2000mW

Operating Temperature Range
HI-5610-2 . . . . -55°C to +125°C
HI-5610-5 . . . . 0°C to +75°C
HI-5610-8 . . . . -55°C to +125°C

Storage Temperature Range . . . . -65°C to +150°C

* Derate 20mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{ps}+$, = +5V, $V_{ps}-$ = -15V, V_{REF} = +10V, pin 2 ground unless otherwise noted)

PARAMETER	TEMP	HI-5610-2 HI-5610-8 MIN	TYP	MAX	HI-5610-5 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (2)								
TTL Logic Input Voltage (3)								
Logic "1"	Full	2.0			2.0			V
Logic "0"	Full			0.8			0.8	V
Input Current								
Logic "1"	Full		20	500		20	500	nA
Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)								
Logic "1"	Full	$0.7V_{ps}+$			$0.7V_{ps}+$			V_{ps+}
Logic "0"	Full			$0.3V_{ps}+$			$0.3V_{ps}+$	V_{ps+}
Input Current								
Logic "1"	Full		20	500		20	500	nA
Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input								Ω
Input Resistance			8K			8K		
Input Voltage (I_{OUT} = 5mA + 20%)			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Full			10			10	Bits
Integral Nonlinearity (5)	25°C			±½			±½	LSB
Differential Nonlinearity (5)	25°C			±½			±½	LSB
Relative Accuracy (6)								
Gain Error								(9)
(Input Code 11....1)			±0.05	±0.25		±0.05	±0.25	% FSR
Unipolar Offset Error								
(Input Code 00....0)			±0.05	±0.10		±0.05	±0.10	% FSR
Bipolar Offset Error								
(Input Code 00....0)			±0.05	±0.15		±0.05	±0.15	% FSR
(Adjustable to zero, see Fig. 4, 5)								
Adjustment Range								
Gain			±0.25			±0.25		% FSR
Bipolar Offset			±0.25			±0.25		% FSR
Temperature Stability								
Gain Drift	Full		±5			±5		ppm/°C
Unipolar Offset Drift	Full		±3			±3		ppm/°C
Bipolar Offset Drift	Full		±3			±3		ppm/°C
Differential Nonlinearity	Full		±2			±2		ppm/°C
MONOTONICITY - GUARANTEED OVER FULL OPERATING TEMPERATURE RANGE								
Settling Time to ½LSB (5)								
From all 0's to all 1's			85			85		ns
From all 1's to all 0's			85			85		ns
Major Carry Switching to 90% Complete			40			40		ns

SPECIFICATIONS (continued)

PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Power Supply Sensitivity (5)								ppm of FSR/%V_{ps}
$V_{ps}+$ = +5V, $V_{ps}-$ = -13.5V to -16.5V								
Gain (Input Code 11....1)				±3.5			±3.5	
Unipolar Offset (Input Code 00....0)			±0.5			±0.5		
Bipolar Offset (Input Code 00....0)			±1.5			±1.5		
$V_{ps}-$ = -15V, $V_{ps}+$ = 4.5V to 5.5V								
Gain (Input Code 11....1)				±7.5			±7.5	
Unipolar Offset (Input Code 00....0)			±0.5			±0.5		
Bipolar Offset (Input Code 00....0)			±1.5			±1.5		
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar		-4.0	-5.0	-6.0	-4.0	-5.0	-6.0	mA
Bipolar		±2.0	±2.5	±3.0	±2.0	±2.5	±3.0	mA
Output Resistance			200			200		Ω
Output Capacitance			20			20		pF
Output Voltage Range (7)								
Unipolar			+5 +2.5			+5 +2.5		V V
Bipolar			±2.5 ±1.25			±2.5 ±1.25		V V
Output Compliance Limit (5)		-3		+10	-3		+10	V
Output Compliance Voltage (5)	Full		±1.5			±1.5		V
Output Noise Voltage (8)								
0.1Hz to 100Hz			10			10		µVp-p
0.1Hz to 1MHz			100			100		µVp-p
POWER REQUIREMENTS								
$V_{ps}+$ (4)	Full	4.5	5	16.5	4.75	5	16.5	V
$V_{ps}-$	Full	-13.5	-15	-16.5	-13.5	-15	-16.5	V
$I_{ps}+$ (All 1's or all 0's in (10) either TTL or CMOS Mode)	25°C Full		9 15	15 20		9 15	15 20	mA mA
$I_{ps}-$ (Same as above) (10)	25°C Full		25 30	30 35		25 30	30 35	mA mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5610 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions).
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The $V_{ps}+$ tolerance is ±10% for HI-5610-2,-8. And ±5% for HI-5610-5.
4. For CMOS compatibility based on $V_{ps}+ \geq 9.5V$, (switching thresholds equal $V_{ps}+/2$), connect pins 1 and 2. For CMOS levels below 9.5V, connect pin 2 to ground only (this provides a threshold of approximately +1.4V).
5. See definitions.
6. Using an external op amp with internal span resistors and 24.9Ω ±1% external trim resistors in place of potentiometers R1 and R2. These errors are adjustable to zero using R1 and R2. (See operating instructions.)
7. Using an external op amp and internal span resistors. (See operating instructions for connections.)
8. Specified for digital input in all '1's or all '0's.
9. FSR is "Full Scale Range" and is 5V for ±2.5V range, 2.5V for ±1.25V range, etc., or 5mA (±20%) for current output.
10. After 30 seconds warm-up.

DEFINITIONS OF SPECIFICATIONS

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00. . .0 and 11. . .1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

Settling time is the time required for the output to settle within the specified error band for any input code transition. It is usually specified for a full scale transition (11. . .1 to 00. . .0 or vice versa).

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (TL) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011. . .1 to 100. . .0 or vice versa. For example, if turn ON is greater than turn OFF for 011. . .1 to 100. . .0, an intermediate state of 000. . .0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

OPERATING INSTRUCTIONS

DECOUPLING AND GROUNDING

For best accuracy and high speed performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5610 (preferably to the device pin) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

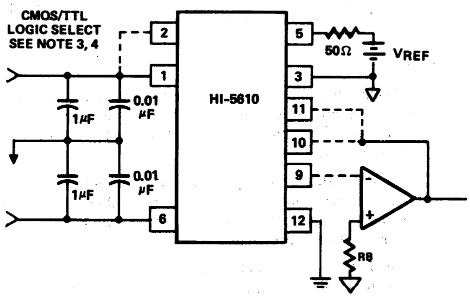


FIGURE 1

HIGH PRECISION PERFORMANCE

The output accuracy of the HI-5610 depends mainly on the accuracy of voltage applied to the V_{REF} input, since full scale output current is approximately $4V_{REF}/8K\Omega$. For precision performance a +10V voltage reference with reasonably low temperature coefficient such as HA-1608 is recommended. For voltage output operation use an external op amp as current-to-voltage converter and the HI-5610 internal scaling resistors as feedback elements. The selected op amp should have a good front-end temperature coefficient such as HA-2600/2605 with offset voltage and offset current tempco's of $5\mu V/^{o}C$ and $1nA/^{o}C$, respectively. The input reference resistor ($7.975K\Omega$) and bipolar offset resistor ($3.975K\Omega$) are both intentionally set low by 25Ω to allow the user to externally trim-out initial errors to a very high degree of precision. For high speed voltage output applications where fast settling is required, the HA-2510/2515 is recommended for better than $1\mu s$ settling to 1/2 LSB.

UNIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for unipolar +5V and +2.5V voltage output using an external op amp and the internal span resistors are shown in Figure 2 and Figure 3, respectively.

CALIBRATION - UNIPOLAR

Step 1 Offset
- Turn all bits off (all 0's)
- Adjust R3 for zero volts output

Step 2 Gain
- Turn all bits on (all 1's)
- Adjust R1 for an output of FS–1LSB
  That is, adjust for:
  4.99512V for 0V to +5V range
  2.49756V for 0V to +2.5V range

UNIPOLAR - STRAIGHT BINARY
0V TO +5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT
11 1	FS - 1LSB = 4.99512V
10 0	½FS = 2.50000V
01 1	½FS -1LSB = 2.49512V
00 0	Zero = 0.00000V

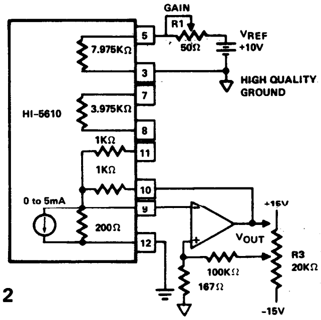


FIGURE 2

UNIPOLAR - STRAIGHT BINARY
0V TO +2.5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT
11 1	FS - 1LSB = 2.49756V
10 0	½FS = 1.25000V
01 1	½FS -1LSB = 1.24756V
00 0	Zero = 0.00000V

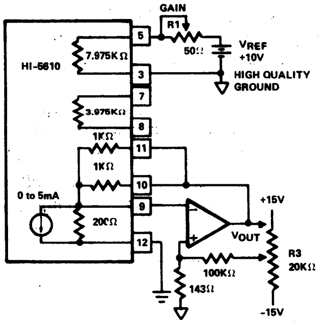


FIGURE 3

BIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for Bipolar ± 2.5V and ± 1.25V voltage output using an external op amp and the internal span resistors are shown in Figure 4 and Figure 5, respectively.

CALIBRATION - BIPOLAR

Step 1, Offset:
- Turn all bits off (all 0's)
- Adjust R2 for output voltage as follows:
  -2.5V, ±2.5V range
  -1.25V, ±1.25V range

Step 2, Gain:
- Turn all bits on (all 1's)
- Adjust R1 for an output voltage of (+FS -1LSB).
  That is:
  +2.49512V, ±2.5V range
  +1.24756V, ±1.25V range

OPERATING INSTRUCTIONS (continued)

BIPOLAR - OFFSET BINARY
± 2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS - 1 LSB	= +2.49512V
10 0	ZERO	= +0.00000V
01 1	Zero - 1 LSB	= -0.00488V
00 0	-FS	= -2.50000V

BIPOLAR TWO'S COMPLEMENT **
± 2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1LSB	= +2.49512V
00 0	Zero	= +0.00000V
11 1	Zero - 1LSB	= -0.00488V
10 0	-FS	= -2.50000V

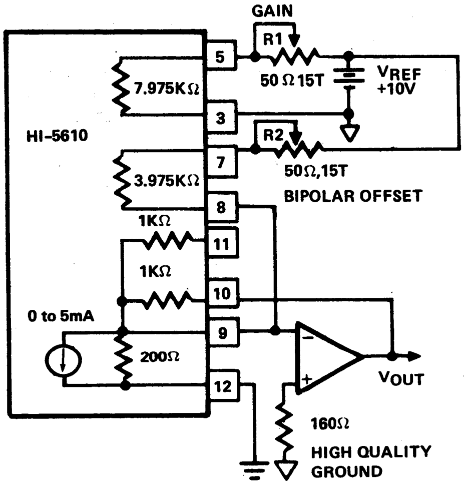

GAIN
R1
5
7.975KΩ
50 Ω 15T
VREF +10V
3
HI-5610
R2
7
3.975KΩ
50Ω,15T
BIPOLAR OFFSET
8
1KΩ
11
1KΩ
10
0 to 5mA
9
200Ω
12
VOUT
160Ω
HIGH QUALITY GROUND

FIGURE 4

BIPOLAR - OFFSET BINARY
± 1.25V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS - 1LSB	= +1.24756V
10 0	Zero	= +0.00000V
01 1	Zero - 1LSB	= -0.00244V
00 0	-FS	= -1.25000V

BIPOLAR - TWO'S COMPLEMENT **
± 1.25V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1LSB	= +1.24756V
00 0	Zero	= +0.00000V
11 1	Zero - 1LSB	= -0.00244V
10	-FS	= -1.25000V

** Invert MSB with external inverter
to obtain two's complement coding.

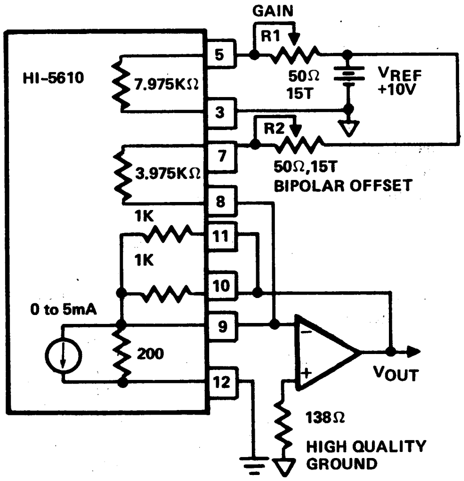

GAIN
R1
5
HI-5610
7.975KΩ
50Ω 15T
VREF +10V
3
R2
7
3.975KΩ
50Ω,15T
BIPOLAR OFFSET
8
1K
11
1K
10
0 to 5mA
9
200
12
VOUT
138Ω
HIGH QUALITY GROUND

FIGURE 5

DIE CHARACTERISTICS

Transistor Count		138
Die Size:		103 x 209 mils
Thermal Constants;	θ_{ja}	50°C/W
	θ_{jc}	15°C/W
Tie Substrate to:		Ground (V_{REF} Lo)
Process:		Bipolar - DI

HARRIS

HI-5618A/5618B

8-Bit High Speed Digital-to-Analog Converters

FEATURES

- VERY FAST SETTLING CURRENT OUTPUT 65ns
- MINIMUM NONLINEARITY ERROR
  - HI-5618A ±1/4 LSB MAX
  - HI-5618B ±1/2 LSB MAX
- LOW POWER OPERATION 340mW TYP
- ON-CHIP RESISTORS FOR GAIN AND BIPOLAR OFFSET
- GUARANTEED MONOTONIC OVER TEMPERATURE
- CMOS, TTL, OR DTL COMPATIBLE

APPLICATIONS

- HIGH SPEED PROCESS CONTROL
- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERSION
- WAVEFORM SYNTHESIS
- HIGH RELIABILITY APPLICATIONS
- VIDEO SIGNAL RECONSTRUCTION

DESCRIPTION

The HI-5618A/B are very high speed 8 bit current output D/A converters. These monolithic devices are fabricated with dielectrically isolated bipolar processing, which reduces internal parasitic capacitance to allow fast rise and fall times. This achieves a typical full scale settling time of 65ns to ±1/2 LSB. Output glitches are minimized by incorporation of equally weighted current sources, switched to either an R-2R ladder network or ground for symmetrical turn ON and turn OFF times. High stability thin film resistors provide excellent accuracy without trimming. For example, the HI-5618A has ±1/4 LSB maximum nonlinearity error at +25°C, with ±3/8 LSB guaranteed over the full operating temperature range.

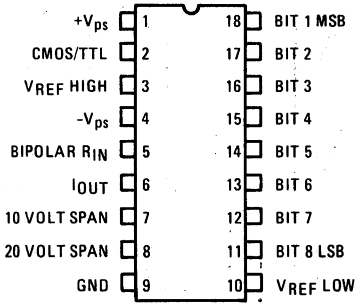
The HI-5618A/B are recommended for any application requiring high speed and accurate conversions. They can be used in CRT displays and systems requiring throughput rates as high as 20MHz for full scale transitions. Other applications include high speed process control, defense systems, avionics, and space instrumentation.

The HI-5618A-5 and HI-5618B-5 are specified for operation from 0°C to +75°C. The "-2" versions are specified from -55°C to +125°C. The HI-5618A/B is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

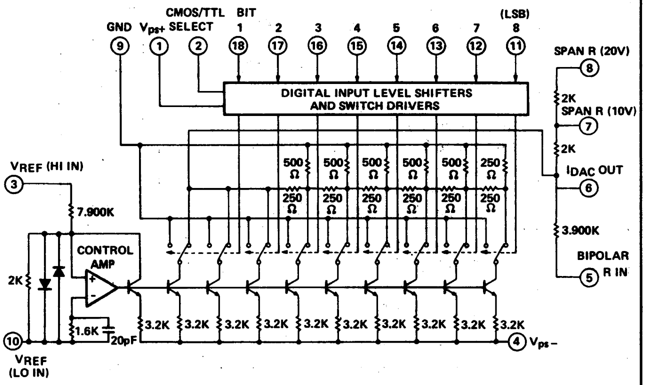
Power requirements are +5V and -15V. Package is an 18 pin ceramic DIP.

PINOUT

TOP VIEW


$+V_{ps}$ 1
CMOS/TTL 2
V_{REF} HIGH 3
$-V_{ps}$ 4
BIPOLAR R_{IN} 5
I_{OUT} 6
10 VOLT SPAN 7
20 VOLT SPAN 8
GND 9
18 BIT 1 MSB
17 BIT 2
16 BIT 3
15 BIT 4
14 BIT 5
13 BIT 6
12 BIT 7
11 BIT 8 LSB
10 V_{REF} LOW

FUNCTIONAL DIAGRAM


GND
V_{ps+}
CMOS/TTL SELECT
BIT 1 2 3 4 5 6 7 8
(LSB)
9 1 2 18 17 16 15 14 13 12 11
DIGITAL INPUT LEVEL SHIFTERS AND SWITCH DRIVERS
SPAN R (20V) 8
2K
SPAN R (10V) 7
2K
I_{DAC} OUT 6
3.900K
BIPOLAR R IN 5
500 Ω
250 Ω
V_{REF} (HI IN) 3
7.900K
CONTROL AMP
2K
1.6K
20pF
3.2K
4 V_{ps-}
10 V_{REF} (LO IN)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground) (1)

Power Supply Inputs Vps+ . . . . +20V
Vps- 20V
Reference Inputs VREF (Hi). . . . . +16.5V
VREF (Lo) 0V
Digital Inputs Bits 1 -12 (TTL) . . . -1V, +7.5V
Bits 1-12 (CMOS). . . -1V, Vps+
CMOS/TTL Logic Sel -1V, +16.5V
Outputs Pins 5, 7, 8. . . . . +Vps
Pin 6 . . . . +Vps, -2.5V

*Derate 13.3mW/°C above 75°C.

Power Dissipation* 1330mW

Operating Temperature Range
HI-5618A/B-2. . . . . -55°C to +125°C
HI-5618A/B-5. . . . . 0°C to +75°C
HI-5618A/B-8 . . . . -55°C to +125°C

Storage Temperature Range . . . . -65°C to +150°C

ELECTRICAL CHARACTERISTICS ($V_{ps}+ = +5V$; $V_{ps}- = -15V$; $V_{REF} = +10V$; Pin 2 to GND, unless otherwise noted)

		HI-5618A/B-2 HI-5618A/B-8			HI-5618A/B-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (2) TTL logic Input Voltage (3) Logic "1"	Full	2.0			2.0			V
Logic "0"	Full			0.8			0.8	V
TTL Logic Input Current Logic "1"	Full		20	500		20	500	nA
Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4) Logic "1"	Full	$0.7V_{ps}+$			$0.7V_{ps}+$			V
Logic "0"	Full			$0.3V_{ps}+$			$0.3V_{ps}+$	V
CMOS Logic Input Current Logic "1"	Full		20	500		20	500	nA
Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input Input Resistance	+25°C		8k			8k		Ω
Input Voltage (I_{OUT} = 5mA ± 20%)	+25°C		+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Full		8			8		Bits
Nonlinearity, Integral and Differential HI-5618A	25°C			±1/4			±1/4	LSB
	Full			±3/8			±3/8	LSB
HI-5618B	25°C			±1/2			±1/2	LSB
	Full			±5/8			±5/8	LSB
Initial Accuracy (6) (Relative to External +10V Reference) Gain	25°C			±2			±2	LSB
Unipolar Zero	25°C			±1/8			±1/8	LSB
Bipolar Offset (Neg. Full Scale)	25°C			±2			±2	LSB
Temperature Stability Gain Drift	Full			±1/4			±1/4	LSB
Unipolar Zero Drift	Full			±1/16			±1/16	LSB
Bipolar Zero Drift	Full			±1/4			±1/4	LSB
Settling Time (5) to 1/2 LSB High Impedance (11) (from all 0's to all 1's) or (from all 1's to all 0's)	+25°C		65	75		65	75	ns

SPECIFICATIONS (Continued)

PARAMETER	TEMP	HI-5618A/B-2 HI-5618A/B-8			HI-5618A/B-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSFER CHARACTERISTICS (Continued)								
Glitch (5) - Major Carry Transition								
Duration	+25°C		20			20		ns
Amplitude (See Fig. 4)	+25°C		350			350		mV
Area	+25°C		3500			3500		mV–ns
Power Supply Sensitivity (5)								
$V_{ps}+ = +5V$, $V_{ps}- = -13V$ to $-16.5V$								
Gain (Input Code 11 . . . 1)	+25°C			±5			±5	ppm of FSR/% Vps (9)
Unipolar Zero (Input Code 00 . . . 0)	+25°C		±0.5			±0.5		
Bipolar Offset (Input Code 00 . . . 0)	+25°C		±1.5			±1.5		
$V_{ps}- = -15V$, $V_{ps}+ = 4.5V$ to $5.5V$								
Gain (Input Code 11 . . . 1)	+25°C			±5			±5	
Unipolar Zero (Input Code 00 . . . 0)	+25°C		±0.5			±0.5		
Bipolar Offset (Input Code 00 . . . 0)	+25°C		±1.5			±1.5		
OUTPUT CHARACTERISTICS								
Output Current Unipolar	+25°C	-4	-5	-6	-4	-5	-6	mA
Bipolar	+25°C	±2.0	±2.5	±3.0	±2.0	±2.5	±3.0	mA
Output Resistance	+25°C		500			500		Ω
Output Capacitance	+25°C		20			20		pF
Output Voltage Range (7) Unipolar	+25°C		+10			+10		V
	+25°C		+5			+5		V
Bipolar	+25°C		±10			±10		V
	+25°C		±5			±5		V
	+25°C		±2.5			±2.5		V
Output Compliance Voltage (5)	+25°C		±1.5			±1.5		V
Output Noise Voltage (8) 0.1Hz to 100Hz	+25°C		30			30		μVp-p
0.1Hz to 1Mhz	+25°C		100			100		μVp-p
POWER REQUIREMENTS (4)								
$V_{ps}+$	Full	4.5	5	16.5	4.5	5	16.5	V
$V_{ps}-$	Full	−13.5	−15	−16.5	−13.5	−15	−16.5	V
$I_{ps}+$ (10) (All 1's or all 0's in either	+25°C		9			9		mA
TTL or CMOS mode) (3, 4)	Full			12			12	mA
$I_{ps}-$ (10) (All 1's or all 0's in either	+25°C		19			19		mA
TTL or CMOS mode) (3, 4)	Full			26			26	mA

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

2. The HI-5618 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions)

3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The $V_{ps}+$ tolerance is ± 10% for HI-5618A/B -2, -8; and ±5% for HI-5618A/B-5.

4. For CMOS compatibility based on $V_{ps}+ \geqslant 9.5V$, (switching thresholds equal $V_{ps}+/2$), connect pins 1 and 2. For CMOS levels below 9.5V, connect pin 2 to ground only (this provides a threshold of approximately +1.4V).

5. See definitions.

6. These errors may be adjusted to zero using external potentiometers R_1, R_2, R_3. R_1 and R_2 each provide more than ± 3 LSB's adjustment. (See Operating Instructions). The specifications listed under initial accuracy are based on use of an external op amp, internal span and offset resistors, and 100 Ω ± 1% resistors, in place of R_1 and R_2.

7. Using an external op amp with the internal span and offset resistors. See Operating Instructions.

8. Specified for all "1's" or all "0's" digital input.

9. FSR is "Full Scale Range", i.e., 20V for ± 10V range; 10V for ± 5V range, etc. Nominal full scale output current is 5mA.

10. After 30 seconds warm-up.

11. See Test Circuit, Figure 3.

12. See Test Circuit , Figure 4.

DEFINITIONS OF SPECIFICATIONS

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00. . .0 and 11. . .1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in fractional LSB's, or parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

ZERO DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Zero error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Zero Drift is calculated for high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two representing worst case drift.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale transition. D/A settling time may vary depending upon the impedance level being driven. A comparator presents a high impedance, while an op amp connected for current to voltage conversion presents a low impedance. Figure 3a shows the test circuit used for testing the HI-5618A/B for T_S (OFF) into a high impedance.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011. . .1 to 100. . .0 or vice versa. For example, if turn ON is greater than turn OFF for 100. . .1 to 100. . .0, an intermediate state of 000. . .0 exists, such that, the output momentarily glitches toward zero output. In general, when a D/A is driven by a set of external logic gates, the unmatched turn on – turn off times at the gates will add to the glitch problem. See Figure 4.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in the +5V or -15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE VOLTAGE

When the D/A converter is used without an op amp, it may be configured for various ranges of voltage at its output. However, Compliance Voltage is the maximum full scale voltage for which the converter will comply with its specifications.

OPERATING INSTRUCTIONS

DECOUPLING AND GROUNDING

For best accuracy and high speed performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5618A/B; preferably to the device pin. A solid tantalum or electrolytic capacitor in parallel with a smaller ceramic type is recommended.

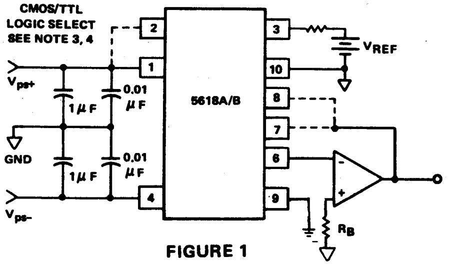


FIGURE 1

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

Make connections as shown in the table and Figure 2, for five standard output ranges:

	OUTPUT RANGE	CONNECTIONS			BIAS RESISTOR R_B
		PIN 5 TO	PIN 7 TO	PIN 8 TO	
Unipolar Mode	0 to +10V	NC	A	NC	400Ω
	0 to +5V	NC	A	6	330Ω
Bipolar Mode	± 10V	D	NC	A	400Ω
	± 5V	D	A	NC	360Ω
	± 2.5V	D	A	6	310Ω

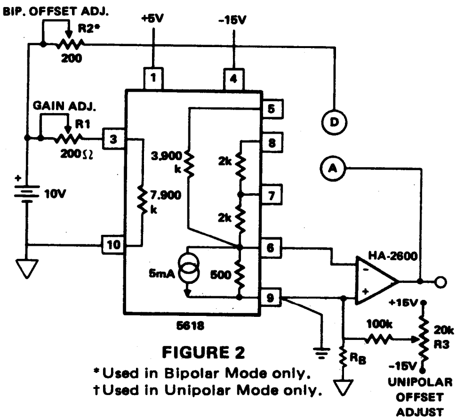


FIGURE 2

*Used in Bipolar Mode only.
†Used in Unipolar Mode only.

OPERATING INSTRUCTIONS (continued)

The HI-5618A/B accepts an 8 bit digital word in Straight Binary code. In the bipolar mode this code becomes Offset Binary. Also in bipolar mode, the MSB may be complemented using an external inverter to obtain 2's complement code. Here are the correct outputs for some key input codes:

UNIPOLAR - STRAIGHT BINARY
0V TO +10V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1 LSB	= 9.96094V
10 0	½FS	= 5.00000V
01 1	½FS - 1 LSB	= 4.96094V
00 0	Zero	= 0.00000V

UNIPOLAR - STRAIGHT BINARY
0V TO +5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1 LSB	= 4.98047V
10 0	½FS	= 2.50000V
01 1	½FS - 1 LSB	= 2.48047V
00 0	Zero	= 0.00000V

BIPOLAR - OFFSET BINARY
± 10V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS -1 LSB	= +9.92188V
10 0	Zero	= +0.00000V
01 1	Zero -1 LSB	= -0.07813V
00 0	-FS	= -10.0000V

BIPOLAR - TWO'S COMPLEMENT **
± 10V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1 LSB	= +9.92188V
00 0	Zero	= +0.00000V
11 1	Zero - 1 LSB	= -0.07813V
10 0	-FS	= -10.0000V

** Invert MSB with external inverter to obtain two's complement coding.

Output Accuracy of the HI-5618A/B is affected directly by the reference voltage, since $I_O(F/S) \simeq 4\,(V_{REF}/8k\Omega)$. For precision performance, a stable +10V reference with low temperature coefficient is recommended.

The output current may be converted to voltage using an external op amp with the internal span and offset resistors, as shown above in the table. The op amp should have good front end temperature coefficients. For example, the HA-2600/2605 is well suited to this application, with offset voltage and offset current tempco's of 5 μV/°C and 1nA/°C, respectively. The input reference resistor (7.9kΩ) and bipolar offset resistor (3.9kΩ) are both intentionally set low by 100Ω to allow the user to externally trim out initial errors to a high degree of precision.

For high speed voltage output applications where fast settling is required, the HA-2510/25 is recommended for settling times better than 250ns to 1/2 LSB. The HA-5190/95 is recommended for applications requiring settling times less than 150ns. (See Applications).

CALIBRATION (See Figure 2)

UNIPOLAR MODE -

1. Apply zero (all 0's) input, and adjust R_3 for 0V output.
2. Apply full scale (all 1's) input, and adjust R_1 for:
   +9.96094 Volts, +10 Volt range
   +4.98047 Volts, +5 Volt range

BIPOLAR MODE -

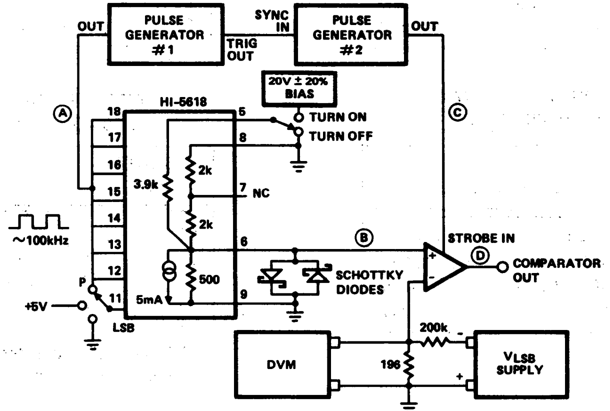
1. Apply negative full scale (also called bipolar offset): All 0's for offset binary; 1000 . . . . for 2's complement. Adjust R_2 for output voltages as follows:
   -10 Volts, ±10 Volt Range
   -5 Volts, ± 5 Volt Range
   -2.5 Volts, ±2.5 Volt Range
2. Apply positive full scale (all 1's for offset Binary; 0111. . . . for 2's complement) Adjust R_1 for output voltages as follows:
   +9.92188 Volts, ± 10 Volt Range
   +4.96094 Volts, ±5 Volt Range
   +2.48047 Volts, ±2.5 Volt Range
3. Apply zero input (1000. . . . for offset Binary; 0000. . . . for 2's complement). Output should be zero volts. Any error is due to nonlinearity in the DAC, and cannot be nulled without disrupting the calibration in steps 2 and 3.

SETTLING TIME

Turn-off settling time ($T_{S(OFF)}$) is somewhat longer than $T_{S(ON)}$ for the HI-5618. Typical $T_{S(OFF)}$ performance is shown in Figure 3C, using the circuit of Figure 3A.

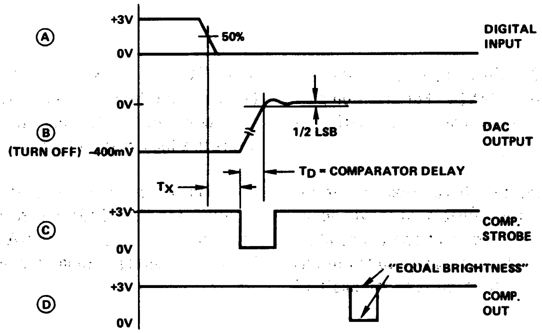
Refer to Figure 3B; Settling time following turn-off equals T_X plus T_D. The comparator delay T_D may be measured at 1mV/cm, using a Tektronix 7A13 differential comparator or equivalent. Then, T_X is easily measured in a short procedure:

- Adjust delay on generator #2 for T_X approximately 1μs
- Switch the LSB to +5V (ON).
- Adjust the V_{LSB} supply for 50 percent triggering at COMP. OUT (equal brightness).
- DVM reads -1 LSB. Adjust V_{LSB} supply so DVM reads -1/2 LSB.
- Switch the LSB to P (pulse); COMP. OUT pulse disappears.
- Reduce generator #2 delay until COMP. OUT pulse reappears; adjust delay for "equal brightness".
- Measure T_X from scope. (Any overshoot will be less than 1/2 LSB, so it is not necessary to examine the other side of the envelope, i.e. final value plus 1/2 LSB.)



OUT
PULSE GENERATOR #1
SYNC IN
TRIG OUT
PULSE GENERATOR #2
OUT
20V ± 20% BIAS
HI-5618
Ⓐ
Ⓒ
18
17
16
15
14
13
12
11
5
8
7 NC
6
9
TURN ON
TURN OFF
3.9k
2k
2k
500
5mA
~100kHz
P
+5V
LSB
Ⓑ
STROBE IN
Ⓓ
COMPARATOR OUT
SCHOTTKY DIODES
200k
196
DVM
VLSB SUPPLY

Figure 3A



Ⓐ
+3V
0V
50%
DIGITAL INPUT
0V
Ⓑ
(TURN OFF) -400mV
1/2 LSB
DAC OUTPUT
TX
TD = COMPARATOR DELAY
Ⓒ
+3V
0V
COMP. STROBE
"EQUAL BRIGHTNESS"
Ⓓ
+3V
0V
COMP. OUT

Figure 3B

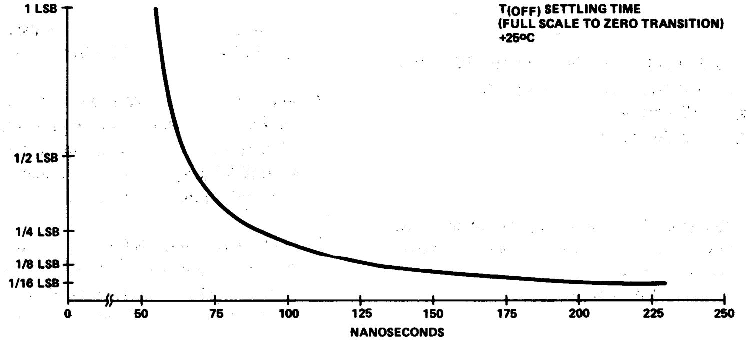
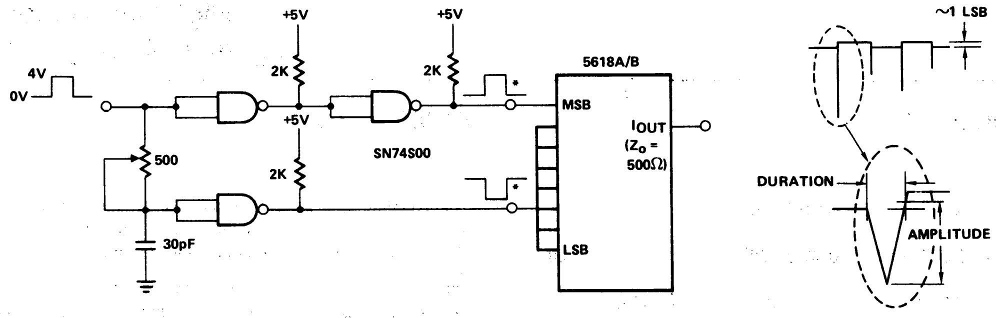


Figure 3C

TEST CIRCUIT (Continued)

OUTPUT GLITCH MEASUREMENT

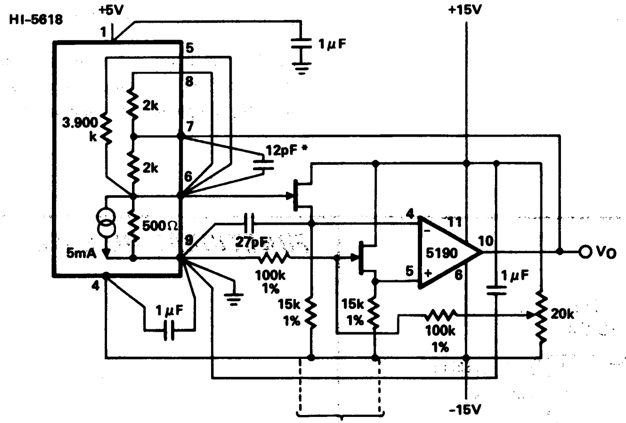

+5V
+5V
+5V
+5V
2K
2K
2K
4V
0V
500
30pF
SN74S00
5618A/B
MSB
LSB
IOUT
(Zo = 500Ω)
*
*
~1 LSB
DURATION
AMPLITUDE

* ADJUST 500Ω TRIMMER SO THAT INPUT SIGNALS CROSS THEIR RESPECTIVE SWITCHING THRESHOLDS AT THE SAME TIME.

Figure 4

APPLICATIONS

HIGH SPEED VOLTAGE OUTPUT


HI-5618
+5V
1
1µF
5
8
2k
3.900 k
7
12pF *
2k
6
500Ω
5mA
9
27pF
100k 1%
4
1µF
15k 1%
15k 1%
+15V
4
11
5190
10
5
6
1µF
100k 1%
20k
Vo
-15V

MATCHED DUAL N-FET, MICRO POWER SYSTEMS MP-835 OR EQUIVALENT

* NOMINAL VALUE, SELECTED FOR OPTIMUM STEP RESPONSE.

DIE CHARACTERISTICS

Transistor Count		122
Die Size:		103 x 209 mils
Thermal Constants;	θ_{ja}	75°C/W
	θ_{jc}	17°C/W
Tie Substrate to:		Ground (V_{REF} Lo)
Process:		Bipolar - DI

HARRIS

HI-5660/5660A

High Speed Monolithic Digital-to-Analog Converter

FEATURES

- MONOLITHIC CONSTRUCTION
- FAST SETTLING (TO ±1/2 LSB) 350ns
- ±1/2 LSB MAX. NONLINEARITY GUARANTEED OVER TEMPERATURE
- INTERNAL CANCELLATION OF GROUND CURRENT
- EXCELLENT POWER SUPPLY REJECTION 1ppm/%PS
- LOW COST

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- CRT DISPLAYS
- WAVEFORM SYNTHESIS

DESCRIPTION

The HI-5660 is a current output, 12 bit monolithic digital-to-analog converter. It offers high speed plus enhanced accuracy, through internal cancellation of ground currents.

Fabrication of the HI-5660 features the Harris bipolar dielectric isolation process, which eliminates latchup and minimizes parasitic capacitance and leakage currents. The chip includes nichrome thin-film resistors, laser trimmed at the wafer level to a maximum linearity error of ±1/4 LSB at +25°C.

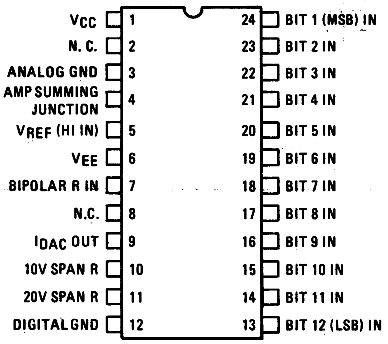
Near zero current in the Analog Ground terminal simplifies use of the HI-5660 by minimizing noise and offsets between the package and the system analog ground. This is accomplished by adding a complement current to the internal ground from an auxiliary R-2R ladder, and then supplying the resultant DC current from the positive power supply.

Electrical performance is similar to that of the AD566A. Pinouts are identical except for pin 1, which requires a +5V supply (versus no connection on the AD566A).

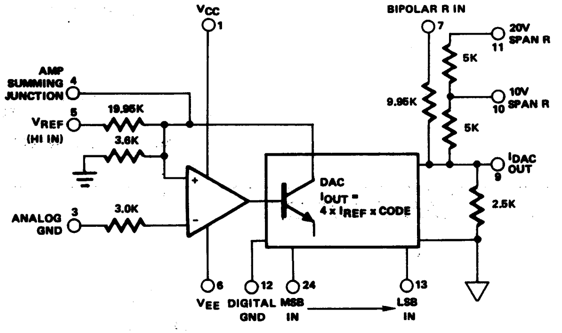
The HI-5660 is offered in two accuracy grades each for the commercial and military temperature ranges. Package is a 24 pin ceramic DIP, and power requirements are ± 12V to +15V.

PINOUT

TOP VIEW
24 LEAD DIP


VCC 1
N. C. 2
ANALOG GND 3
AMP SUMMING JUNCTION 4
VREF (HI IN) 5
VEE 6
BIPOLAR R IN 7
N.C. 8
IDAC OUT 9
10V SPAN R 10
20V SPAN R 11
DIGITAL GND 12
24 BIT 1 (MSB) IN
23 BIT 2 IN
22 BIT 3 IN
21 BIT 4 IN
20 BIT 5 IN
19 BIT 6 IN
18 BIT 7 IN
17 BIT 8 IN
16 BIT 9 IN
15 BIT 10 IN
14 BIT 11 IN
13 BIT 12 (LSB) IN

FUNCTIONAL DIAGRAM


VCC
1
BIPOLAR R IN
7
20V SPAN R
11
5K
AMP SUMMING JUNCTION
4
10V SPAN R
10
9.95K
5
VREF (HI IN)
19.95K
3.6K
5K
IDAC OUT
9
DAC
IOUT = 4 x IREF x CODE
2.5K
ANALOG GND
3
3.0K
6
VEE
12
DIGITAL GND
24
MSB IN
13
LSB IN

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS †

V_{CC} to Power Ground	0V to +18V	10V Span R to Reference Ground	±12V
V_{EE} to Power Ground	0V to -18V	20V Span R to Reference Ground	±24V
Voltage on DAC Output (Pin 9)	-3V to +12V	Package Power Dissipation	
Digital Inputs (Pins 13-24) to Power Ground	-1V to +7.0V	Ceramic *	1920mW
Ref In to Reference Ground	±12V		
Bipolar Offset to Reference Ground	±12V		

† Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired.

* Derate 19.2mW°C above 75°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, V_{REF} = 10V, Unless Otherwise Specified)

	HI-5660-5			HI-5660A-5			
MODEL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX})							
Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0"	0.0		0.8	0.0		0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		2	10		2	10	μA
Bit OFF Logic "0"		-10	-50		-10	-50	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	2.0K	2.5K	3.0K	2.0K	2.5K	3.0K	Ω
Offset Unipolar		.01	.05		.01	.05	% of FS
Bipolar (Figure 2, R_3 = 50Ω Fixed)		.05	.15		.05	0.10	% of FS
Capacitance		25			25		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-3		+12	-3		+12	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of FS
T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of FS
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED (±1 LSB MAX)						
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		7	10	ppm/°C
Differential Nonlinearity		2	6		2	2	ppm/°C
SETTLING TIME TO 1/2 LSB							
With High Z External Load (Note 2)		500			500		ns
With 75Ω External Load		250			250		ns

SPECIFICATIONS (continued)

MODEL	HI-5660-5			HI-5660A-5			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE							
Operating	0		+75	0		+75	°C
Storage	-25		+150	-25		+150	°C
POWER REQUIREMENTS							
V_{CC}, +4.5V to +16.5V_{DC}		7	12		7	12	mA
V_{EE}, -11.4 to -16.5V_{DC}		-13	-17		-13	-17	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +4.5 to +16.5V_{DC}; V_{EE} = -15V		1	10		1	10	ppm of FS/%
V_{EE} = -11.4 to -16.5V_{DC}; V_{CC} = +15V		1	10		1	10	ppm of FS/%
PROGRAMMABLE OUTPUT RANGES (See Table 1)	0 to +5			0 to +5			V
	-2.5 to +2.5			-2.5 to +2.5			V
	0 to +10			0 to +10			V
	-5 to +5			-5 to +5			V
	-10 to +10			-10 to +10			V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R_2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of FS
Bipolar Offset Error with Fixed 50Ω Resistor for R_3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of FS
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of FS
Bipolar Offset Adjustment Range (Fig. 2)	±0.15			±0.15			% of FS
REFERENCE INPUT							
Input Impedance	16K	20K	24K	16K	20K	24K	Ω
POWER DISSIPATION		230	330		230	330	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants	Two (2): Bipolar Operation at Digital Input Only.						
Reference Voltage	Unipolar: +10V Max, +2V Min.						
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 2V_{DC} Reference Voltage.						
Reference Feedthrough (Unipolar Mode, All Bits OFF, and +2V to +10V (p-p), Sinewave Frequency for 1/2 LSB (p-p) Feedthrough)	22kHz Typical						
Output Slew Rate 10%-90%	1.3mA/μs						
Output Slew Rate 90%-10%	1.3mA/μs						
Output Settling Time (All Bits ON and a +2V to +10V Step Change in Reference Voltage)	1.5μs to 0.01% F.S.						
CONTROL AMPLIFIER							
Full Power Bandwidth (+10V to +3V)		200			200		kHz
Small Signal Closed-Loop Bandwidth		2.4			2.4		MHz

NOTES:

1. The Digital Input Levels are Guaranteed but not Tested Over the Temperature Range.
2. See Settling Time Section.

SPECIFICATIONS (continued)

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, Unless Otherwise Specified)

MODEL	HI-5660-2, HI-5660-8 MIN	TYP	MAX	HI-5660A-2, HI-5660A-8 MIN	TYP	MAX	UNITS
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX}) Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0"	0.0		0.8	0.0		0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		2	10		2	10	µA
Bit OFF Logic "0"		-10	-50		-10	-50	µA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	2.0K	2.5K	3.0K	2.0K	2.5K	3.0K	Ω
Offset Unipolar		.01	.05		.01	.05	% of FS
Bipolar (Figure 2, R_3 = 50Ω Fixed)		.05	.15		.05	.10	% of FS
Capacitance		25			25		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-3		+12	-3		+12	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of FS
T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of FS
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED (±1 LSB MAX)						
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		7	10	ppm/°C
Differential Nonlinearity		2	6		2	2	ppm/°C
SETTLING TIME TO 1/2 LSB							
With High Z External Load (Note 2)		500			500		ns
With 75Ω External Load		250			250		ns

SPECIFICATIONS (continued)

	HI-5660-2, HI-5660-8			HI-5660A-2, HI-5660A-8			
MODEL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +4.5V to +16.5V_{DC}		7	12		7	12	mA
V_{EE}, -11.4 to -16.5V_{DC}		-13	-17		-13	-17	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +4.5 to +16.5V_{DC}; V_{EE} = -15V		1	10		1	10	ppm of FS/%
V_{EE} = -11.4 to -16.5V_{DC}; V_{CC} = +15V		1	10		1	10	ppm of FS/%
PROGRAMMABLE OUTPUT RANGES (See Table 1)	0 to +5			0 to +5			V
	-2.5 to +2.5			-2.5 to +2.5			V
	0 to +10			0 to +10			V
	-5 to +5			-5 to +5			V
	-10 to +10			-10 to +10			V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R_2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of FS
Bipolar Offset Error with Fixed 50Ω Resistor for R_3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of FS
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of FS
Bipolar Offset Adjustment Range (Fig. 2)	±0.15			±0.15			% of FS
REFERENCE INPUT							
Input Impedance	16K	20K	24K	16K	20K	24K	Ω
POWER DISSIPATION		230	330		230	330	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants	Two (2): Bipolar Operation at Digital Input Only.						
Reference Voltage	Unipolar: +10V Max, +2V Min.						
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 2V_{DC} Reference Voltage.						
Reference Feedthrough (Unipolar Mode, All Bits OFF, and +2V to +10V (p-p), Sinewave Frequency for 1/2 LSB (p-p) Feedthrough)	22kHz Typical						
Output Slew Rate 10%-90%	1.3mA/μs						
90%-10%	1.3mA/μs						
Output Settling Time (All Bits ON and a +2V to +10V Step Change in Reference Voltage)	1.5μs to 0.01% F.S.						
CONTROL AMPLIFIER							
Full Power Bandwidth (+10V to +3V)		200			200		kHz
Small Signal Closed-Loop Bandwidth		2.4			2.4		MHz

NOTES:

1. The Digital Input Levels are Guaranteed but not Tested Over the Temperature Range.
2. See Settling Time Section.

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-5660 accepts digital input codes in binary format and may be user connected for any one of three binary codes: Straight Binary, Two's Complement*, or Offset Binary (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB...LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	Zero – 1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i. e. the line is drawn between the end-points of the actual transfer characteristic (codes 00. . .0 and 11. . .1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in –15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

APPLYING THE HI-5660

OP AMP SELECTION

The HI-5660's current output may be converted to voltage using the standard connections shown in Figures 1 and 2. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy.

For highest precision, use an HA-5130. This amplifier contributes negligible error, but requires about 11μs to settle within ±0.1% following a 10V step.

The Harris Semiconductor HA-2600 is the best all-around choice for this application, and it settles in 1.5μs (also to ±0.1% following a 10V step). Remember, settling time for the DAC-amplifier combination is $\sqrt{t_D^2 + t_A^2}$, where t_D, t_A are settling times for the DAC and amplifier.

Table 1 — Operating Modes and Calibration

	CIRCUIT CONNECTIONS:				CALIBRATION:		
MODE	OUTPUT RANGE	PIN10 TO	PIN 11 TO	RESISTOR (R)*	APPLY INPUT CODE	ADJUST	TO SET V_O
Unipolar (See Fig. 1)	0 to +10V	V_O	Pin 10	1.43K	All 0's All 1's	R1 R2	0V +9.99756V
	0 to +5V	V_O	Pin 9	1.1K	All 0's All 1's	R1 R2	0V +4.99878V
Bipolar (See Fig. 2)	±10V	NC	V_O	1.69K	All 0's All 1's	R3 R4	-10V +9.99512V
	±5V	V_O	Pin 10	1.43K	All 0's All 1's	R3 R4	-5V +4.99756V
	±2.5V	V_O	Pin 9	1.1K	All 0's All 1's	R3 R4	-2.5V +2.49878V

*Many op amps do not require this resistor, since a bias current of 60nA produces a worst case output error of only 100µV. For a low bias current amplifier, connect its non-inverting input directly to ground.

NO-TRIM OPERATION

The HI-5660 will perform as specified without calibration adjustments. To operate without calibration, substitute 50 Ω resistors for the 100 Ω trimming potentiometers: In Figure 1 replace R2 with 50 Ω ; also remove the network on pin 7 and connect 50 Ω to ground. For bipolar operation in Figure 2, replace R3 and R4 with 50Ω resistors.

With these changes, performance is guaranteed as shown under Specifications, "External Adjustments". Typical unipolar zero will be ±1/2 LSB plus the op amp offset.

When using wide bandwidth op amps, the feedback capacitor C may be selected to minimize settling time.

CALIBRATION

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero. For the HI-5660, these adjustments are similar whether the current output is used, or whether an external op amp is added to convert this current to a voltage. Refer to Table 1 for the voltage output case, along with Figure 1 or 2.

Calibration is a two step process for each of the five output ranges shown in Table 1. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum value is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

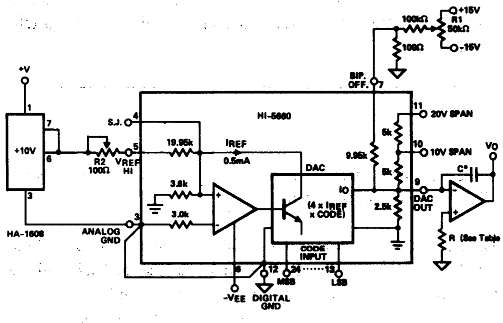

100kΩ
R1
50kΩ
+15V
-15V
100Ω
+V
BIP. OFF.
7
HI-5660
1
7
6
3
+10V
HA-1608
S.J.
4
5
R2
100Ω
VREF HI
19.95k
IREF
0.5mA
3.6k
3.0k
3
ANALOG GND
DAC
IO
(4 x IREF x CODE)
CODE INPUT
9.95k
5k
5k
2.5k
11
20V SPAN
10
10V SPAN
9
DAC OUT
C*
VO
R (See Table 1)
6
12
24
13
MSB
LSB
-VEE
DIGITAL GND

Figure 1 — Unipolar Voltage Output

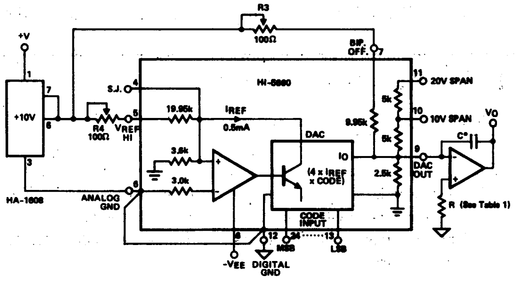

R3
100Ω
+V
BIP. OFF.
7
HI-5660
1
7
6
3
+10V
HA-1608
S.J.
4
5
R4
100Ω
VREF HI
19.95k
IREF
0.5mA
3.6k
3.0k
6
ANALOG GND
DAC
IO
(4 x IREF x CODE)
CODE INPUT
9.95k
5k
5k
2.5k
11
20V SPAN
10
10V SPAN
9
DAC OUT
C*
VO
R (See Table 1)
6
12
24
13
MSB
LSB
-VEE
DIGITAL GND

Figure 2 — Bipolar Voltage Output

SETTLING TIME

This is a challenging measurement, in which the result depends on the method chosen, the precision and quality of test equipment and the operating configuration of the DAC (test conditions). As a result, the different techniques in use by converter manufacturers can lead to consistently different results. An engineer should understand the advantage and limitations of a given test method before using the specified settling time as a basis for design.

The approach used for several years at Harris Analog Products Division calls for a strobed comparator to sense final perturbations of the DAC output waveform. This gives the LSB a reasonable magnitude (814μV for the HI-5660), which provides the comparator with enough overdrive to establish an accurate ±1/2 LSB window about the final settled value. Also, the required test conditions simulate the DAC's environment for a common application – use in a successive approximation A/D converter. Considerable experience has shown this to be a reliable and repeatable way to measure settling time.

The usual specification is based on a 10V step, produced by simultaneously switching all bits from off-to-on (t_{ON}) or on-to-off (t_{OFF}). The slower of the two cases is specified, as measured from 50% of the digital input transition to the final entry within a window of ±1/2 LSB about the settled value. Four measurements characterize a given type of DAC:

(a) t_{ON}, to final value +1/2 LSB
(b) t_{ON}, to final value -1/2 LSB
(c) t_{OFF}, to final value +1/2 LSB
(d) t_{OFF}, to final value -1/2 LSB

(Cases (b) and (c) may be eliminated unless the overshoot exceeds 1/2 LSB). For example, refer to Figure 3 for the measurement of case (d).

PROCEDURE

As shown in Figure 3B, settling time equals t_X plus the comparator delay (t_D = 15ns). To measure t_X,

- Adjust the delay on generator # 2 for a t_X of several microseconds. This assures that the DAC output has settled to its final value.
- Switch on the LSB (+5V).
- Adjust the V_{LSB} supply for 50 percent triggering at COMPARATOR OUT. This is indicated by traces of equal brightness on the oscilloscope display as shown in Figure 3B. Note DVM reading.
- Switch the LSB to Pulse (P).
- Readjust the V_{LSB} supply for 50% triggering as before, and note DVM reading. One LSB equals one tenth the difference in the DVM readings noted above.
- Adjust the V_{LSB} supply to reduce the DVM reading by, 5 LSB's (DVM reads 10X, so this sets the comparator to sense the final settled value minus 1/2 LSB). Comparator output disappears.
- Reduce generator # 2 delay until comparator output reappears, and adjust for "equal brightness".
- Measure t_X from scope as shown in Figure 3B. Settling time equals $t_X + t_D$, i.e. t_X +15ns.

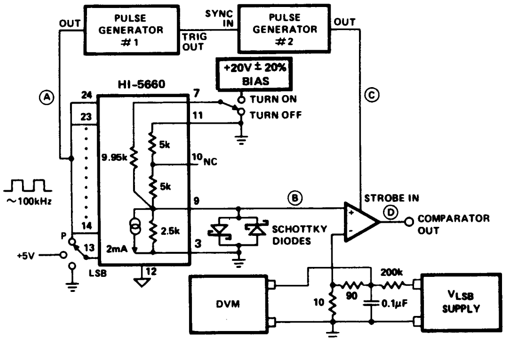

PULSE GENERATOR #1
OUT
TRIG OUT
SYNC IN
PULSE GENERATOR #2
OUT
+20V ± 20% BIAS
TURN ON
TURN OFF
HI-5660
Ⓐ
Ⓑ
Ⓒ
Ⓓ
24
23
14
13
7
11
10 NC
9
3
12
9.95k
5k
5k
2.5k
2mA
~100kHz
P
+5V
LSB
SCHOTTKY DIODES
STROBE IN
COMPARATOR OUT
DVM
10
90
200k
0.1µF
V_LSB SUPPLY

Figure 3A

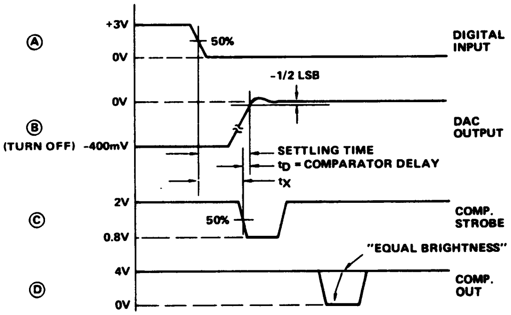

Ⓐ
+3V
0V
50%
DIGITAL INPUT
Ⓑ
(TURN OFF)
0V
-400mV
-1/2 LSB
DAC OUTPUT
SETTLING TIME
tD = COMPARATOR DELAY
tX
Ⓒ
2V
0.8V
50%
COMP. STROBE
"EQUAL BRIGHTNESS"
Ⓓ
4V
0V
COMP. OUT

Figure 3B

OTHER CONSIDERATIONS

GROUNDS

The HI-5660 has two ground terminals, pin 3 (ANALOG GND) and pin 12 (DIGITAL GND). The current through pin 3 is near-zero DC, but pin 12 carries up to 1.75mA of code-dependent current from bits 1, 2 and 3. The general rule is to connect pin 3 to the system analog ground and pin 12 to the power or digital ground. If the system has a single ground point, provide separate paths to pins 3 and 12.

Current cancellation in pin 3 is accomplished as follows: An auxiliary 9 bit R-2R ladder is driven by the complement of the HI-5660 input code. Together, the main and auxiliary ladders draw a constant 2.25mA from the internal analog ground, regardless of input code. This current is then sourced from the positive supply via a current mirror, yielding near-zero current through pin 3.

LAYOUT

Connections to pin 9 (I_{OUT}) on the HI-5660 are very critical for high speed performance. Output capacitance of the DAC is only 25pF, so a small change or additional capacitance may alter the output op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should be short on the side connecting to pin 9 (as for feedback capacitor C).

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI-5660 also. If no op amp is used, a 0.01µF ceramic capacitor from each supply terminal to pin 12 is sufficient.

DIE CHARACTERISTICS

Transistor Count		158
Die Size:		104 x 172 mils
Thermal Constants;	θ_{ja}	52°C/W
	θ_{jc}	17°C/W
Tie Substrate to:		Analog Ground
Process:		Bipolar - DI

HARRIS

HI-5680

12-Bit Low Cost Monolithic Digital-to-Analog Converter

FEATURES

- DAC 80 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED MONOTONIC 0°C to 75°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

DESCRIPTION

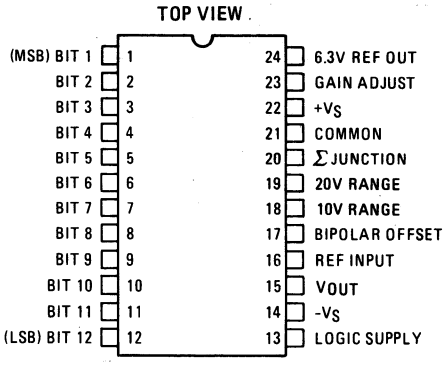
The HI-5680 is a monolithic, direct replacement for the popular DAC80-CBI, DAC80Z-CBI, and DAC85C-CBI, incorporating the best features of each. Single chip construction, along with several design innovations, make the HI-5680 the optimum choice for low cost, high reliability applications.

Harris' unique Dielectric Isolation(DI) processing reduces internal parasitics, resulting in fast switching times and minimum glitch. On-board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5680V), or with a user supplied external amplifier (HI-5680I).

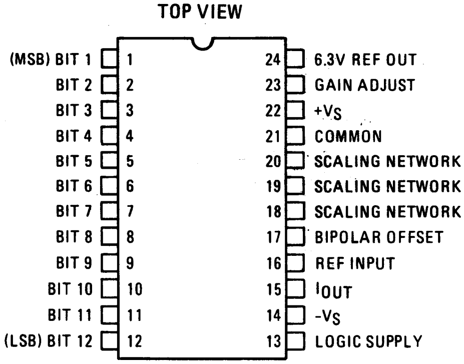
Internally, the HI-5680 eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5680 is available in both current and voltage output models which are guaranteed over the 0°C to +75°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ±(11.4V to 16.5V).

PINOUTS

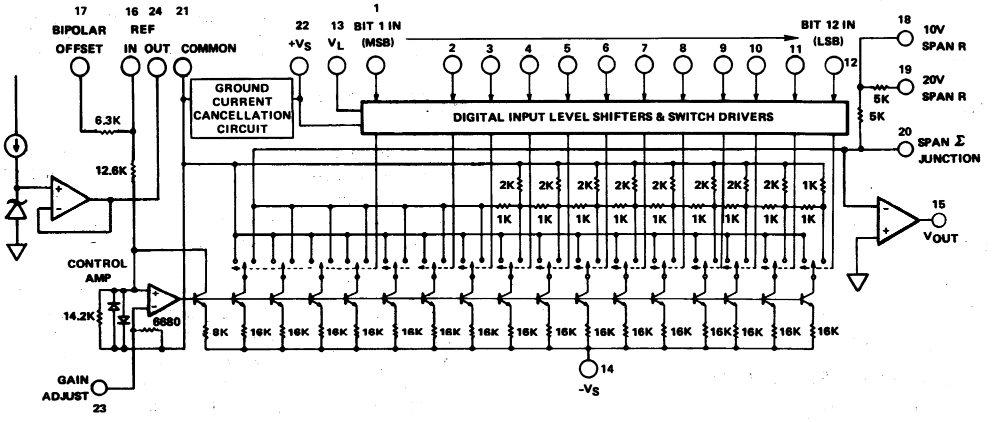

TOP VIEW
(MSB) BIT 1 1
BIT 2 2
BIT 3 3
BIT 4 4
BIT 5 5
BIT 6 6
BIT 7 7
BIT 8 8
BIT 9 9
BIT 10 10
BIT 11 11
(LSB) BIT 12 12
24 6.3V REF OUT
23 GAIN ADJUST
22 +VS
21 COMMON
20 Σ JUNCTION
19 20V RANGE
18 10V RANGE
17 BIPOLAR OFFSET
16 REF INPUT
15 VOUT
14 -VS
13 LOGIC SUPPLY

HI-5680V
VOLTAGE OUTPUT


TOP VIEW
(MSB) BIT 1 1
BIT 2 2
BIT 3 3
BIT 4 4
BIT 5 5
BIT 6 6
BIT 7 7
BIT 8 8
BIT 9 9
BIT 10 10
BIT 11 11
(LSB) BIT 12 12
24 6.3V REF OUT
23 GAIN ADJUST
22 +VS
21 COMMON
20 SCALING NETWORK
19 SCALING NETWORK
18 SCALING NETWORK
17 BIPOLAR OFFSET
16 REF INPUT
15 IOUT
14 -VS
13 LOGIC SUPPLY

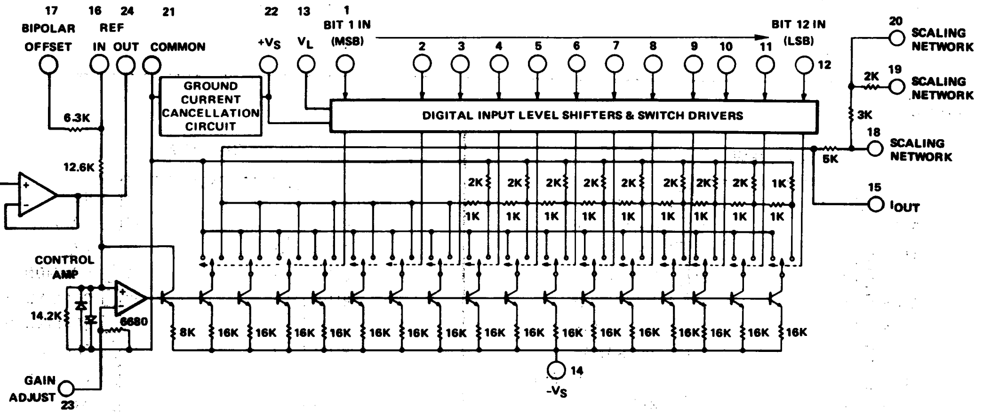
HI-5680I
CURRENT OUTPUT

FUNCTIONAL DIAGRAM VOLTAGE OUTPUT


17
BIPOLAR OFFSET
16 24
REF
IN OUT
21
COMMON
22
+V_S
13
V_L
1
BIT 1 IN
(MSB)
2
3
4
5
6
7
8
9
10
11
BIT 12 IN
(LSB)
12
18
10V SPAN R
19
20V SPAN R
5K
5K
20
SPAN Σ JUNCTION
GROUND CURRENT CANCELLATION CIRCUIT
DIGITAL INPUT LEVEL SHIFTERS & SWITCH DRIVERS
6.3K
12.6K
2K
1K
15
V_{OUT}
CONTROL AMP
14.2K
6680
8K
16K
14
-V_S
GAIN ADJUST
23

HI-5680 V
HI-5685 V
HI-5687 V

FUNCTIONAL DIAGRAM CURRENT OUTPUT


17
BIPOLAR OFFSET
16 24
REF
IN OUT
21
COMMON
22
+V_S
13
V_L
1
BIT 1 IN
(MSB)
2
3
4
5
6
7
8
9
10
11
BIT 12 IN
(LSB)
12
20
SCALING NETWORK
2K
19
SCALING NETWORK
3K
18
SCALING NETWORK
5K
15
I_{OUT}
GROUND CURRENT CANCELLATION CIRCUIT
DIGITAL INPUT LEVEL SHIFTERS & SWITCH DRIVERS
6.3K
12.6K
2K
1K
CONTROL AMP
14.2K
6680
8K
16K
14
-V_S
GAIN ADJUST
23

HI-5680 I
HI-5685 I
HI-5687 I

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Inputs	$+V_S$	+20V
	$-V_S$	−20V
	$+V_{LOGIC}$	+20V
Reference	Input (pin 16)	$+V_S$
	Output drain	2.5mA
Digital Inputs	Bits 1 to 12	−1V to +12V

Power Dissipation *		2040mW
Operating Temperature Range	HI-5680I/V-5	0°C to +75°C
Storage Temperature Range		−65°C to +150°C

* Derate 20.4mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_s = ±15V, V_{LOGIC} = +5V, PIN 16 CONNECTED TO PIN 24 UNLESS OTHERWISE SPECIFIED.)

PARAMETER	CONDITIONS	HI-5680 MIN	HI-5680 TYP	HI-5680 MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1 µA	+2		+5.5	Volts
Logic "0"	at -100µA	0		+0.8	Volts
ACCURACY (3)					
Linearity Error	0°C to +75°C		±¼	±½	LSB
Differential Lin. Error	0°C to +75°C		±½	±¾	LSB
Gain Error (2)			±0.1	±0.3	%FSR
Offset Error (2)			±.05	±0.15	%FSR
Monotonicity	0°C to +75°C		Guaranteed		
DRIFT (3)	0°C to +75°C				
Total Bipolar Drift (Includes gain, offset and linearity drifts.)				±20	ppm/°C
Total Error	0°C to +75°C				
Unipolar (Note 6)			± 0.08	±0.15	%FSR
Bipolar (Note 6)			± 0.06	±.1	%FSR
Gain	Including internal reference		±15	±30	ppm/°C
	Exclusive of internal reference		±5	±7	ppm/°C
Unipolar Offset			±1	±3	ppm/°C
Bipolar Offset			±5	±10	ppm/°C
CONVERSION SPEED (3)					
Voltage Models					
Settling time (3)	to ±0.01% of FSR for FSR Change				
With 10KΩ Feedback			3		µs
With 5KΩ Feedback			1.5		µs
For 1 LSB change			1.5		µs
Slew Rate		10	15		V/µs
Current Models					
Settling time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1KΩ load			1000		ns
ANALOG OUTPUT					
Voltage Models					
Output current		±5			mA
Output Resistance			.05		Ω
Short Circuit Duration	to common		continuous		

SPECIFICATIONS (continued)

PARAMETER	CONDITIONS	HI-5680X			UNITS
		MIN	TYP	MAX	
ANALOG OUTPUT					
Current Models					
Output Current					
Unipolar		-1.6	–2	-2.4	mA
Bipolar		±0.8	±1	±1.2	mA
Output Resistance					
Unipolar			2.0		KΩ
Bipolar			2.0		KΩ
Compliance (3)		-2.5		+10	V
INTERNAL REFERENCE					
Output Voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			20		ppm/°C
POWER SUPPLY SENSITIVITY (3)					
+15V supply				.002	$\frac{\%FSR}{\Delta V_s}$
–15V supply				.002	
+5V supply				.002	
POWER SUPPLY REQUIREMENTS (5)					
Range					
+15V		+11.4	+15	+16.5	V
–15V		-11.4	-15	-16.5	V
+5V		+ 4.5	+ 5	+16.5	V
Current					
+15V			8	11	mA
- 15V			-12	-20	mA
+5V			4.5	8	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See definitions.
4. FSR is "Full Scale Range" and is 20V for ± 10V range, 10V for ± 5V range, etc., or 2mA (± 20%) for current output.
5. The HI-5680 will operate with supply voltages as low as ± 11.4V. It is recommended that output voltage range -10V to +10V not be used if the supply voltages are less than ± 12V.
6. With gain and offset errors adjusted to zero at 25°C.

DIE CHARACTERISTICS

Transistor Count		259
Die Size:		210 x 125 mils
Thermal Constants;	θ_{ja}	49°C/W
	θ_{jc}	12°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-5680 accepts digital input codes in complementary, binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	Complementary Binary	Complementary Offset Binary	Complementary Two's Complement *
MSB LSB			
000...000	+ Full Scale	+ Full Scale	-LSB
100...000	Mid Scale -1 LSB	-1 LSB	+ Full Scale
111...111	Zero	- Full Scale	Zero
011...111	+½ Full Scale	Zero	- Full Scale

* Invert MSB with external inverter to obtain CTC Coding

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V or bipolar full scale step, to be measured from 50% of the input digital transition, and a window of ±½ LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H −25°C) and low ranges (+25°C−T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H −25°C) and low (+25°C −T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

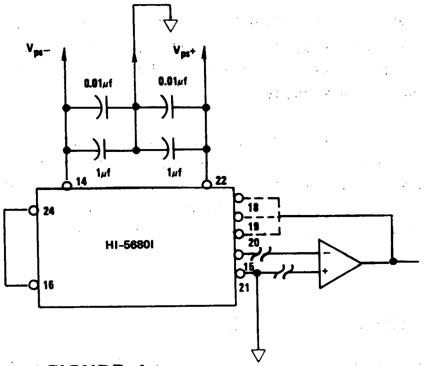
GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from inequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

OPERATING INSTRUCTIONS

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5680 (preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.



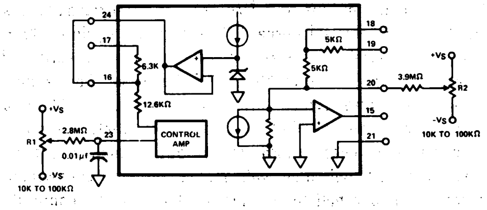
$V_{ps}-$
$V_{ps}+$
0.01µf
0.01µf
1µf
1µf
14
22
24
16
HI-5680I
18
19
20
15
21
ANALOG GROUND

FIGURE 1

REFERENCE SUPPLY

An internal 6.3Volt reference is provided on board all HI-5680 models. This voltage (pin 24) is accurate to ±2% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-5680. All gain adjustments should be made under constant load conditions.

VOLTAGE OUTPUT HI-5680V/85V/87V



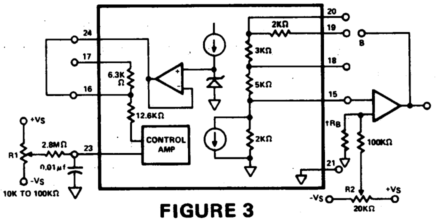
24
17
16
6.3K
12.6KΩ
5KΩ
5KΩ
18
19
20
15
21
3.9MΩ
+Vs
R2
-Vs
10K TO 100KΩ
+Vs
2.8MΩ
23
R1
0.01µf
-Vs
10K TO 100KΩ
CONTROL AMP

FIGURE 2

RANGE CONNECTIONS

		CONNECT		
	RANGE	PIN 15	PIN 17	PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to + 10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±5V	18	20	N.C.
	±10V	19	20	15

CURRENT OUTPUT HI-5680I/85I/87I



24
17
16
6.3K Ω
12.6KΩ
2KΩ
3KΩ
5KΩ
2KΩ
20
19
18
15
B
†RB
100KΩ
21
+Vs
2.8MΩ
23
R1
0.01µf
-Vs
10K TO 100KΩ
CONTROL AMP
R2
-Vs
+Vs
20KΩ

FIGURE 3

†R_B should equal the DAC's output resistance, which is 2KΩ // $R_{FEEDBACK}$.

EXTERNAL AMPLIFIER CONNECTIONS

To use the HI-5680I with an external amplifier, connect as follows:

RANGE	PIN 17 to	PIN 18 to	PIN 19 to	PIN 20 to
0 to +10V	N.C.	B	18*	19*
0 to +5V	N.C.	B	15	N.C.
±10V	15	N.C.	B	N.C.
±5V	15	B	18*	19*
±2.5V	15	B	15	N.C.

*these connections help reduce stray capacitance in the feedback loop.

GAIN AND OFFSET CALIBRATION

(Applies to Figure 2 and 3.)

UNIPOLAR CALIBRATION

Step 1: Offset

Turn all bits OFF (11...1)
Adjust R_2 for zero volts out

Step 2: Gain

Turn all bits ON (00...0)
Adjust R_1 for FS-1LSB
That Is:
4.9988 for 0 to +5V range
9.9976 for 0 to +10V range

BIPOLAR CALIBRATION

Step 1: Offset

Turn all bits OFF (11...1)
Adjust R_2 for Negative FS
That Is:
−10V for ±10V range
−5V for ±5V range
−2.5V for ±2.5 range

Step 2: Gain

Turn all bits ON (00...0)
Adjust R_1 for positive FS-1LSB
That Is:
+9.9951V for ±10V range
+4.9976V for ±5V range
+2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

HI-5685/5685A

High Performance Monolithic 12-Bit Digital-to-Analog Converter

FEATURES

- DAC 85 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED MONOTONIC −25°C TO +85°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

DESCRIPTION

The HI-5685 is a monolithic direct replacement for the popular DAC85-CBI and the ACCA85LD-CBI. Single chip construction along with several design innovations make the HI-5685 the optimum choice for low cost, high reliability applications.

Harris unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5685V), or with a user supplied external amplifier (HI-5685).

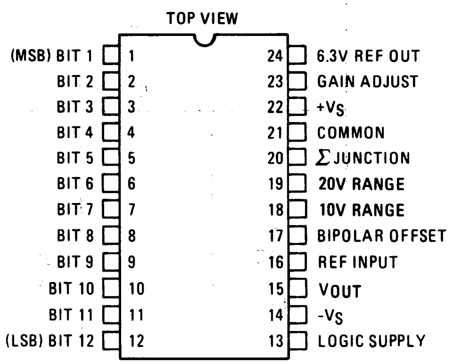
Internally, the HI-5685 eliminates code dependent ground currents by routing current form the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5685 and HI-5685A are available in both current and voltage output models which are guaranteed over the -25°C to +85°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include and on-board output amplifier. Both versions operate with a +5V logic supply and a ±V_S in the range of ±(11.4V to 16.5V).

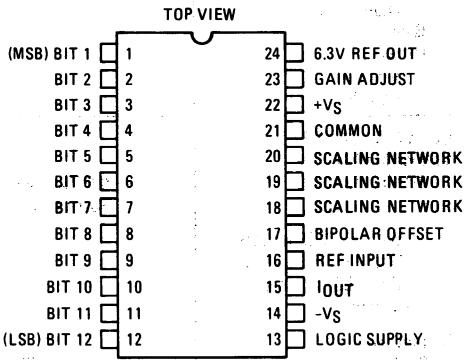
Reference HI-5680 for Functional Diagrams, (see pg. 5-40), Definitions of Specifications, (see pg. 5-43), and Operating Instructions (see pg. 5-44).

The HI-5685A offers exceptionally low drift over temperature. Gain drift is a maximum +10ppm/°C, over -25°C to +85°C.

PINOUTS


TOP VIEW
(MSB) BIT 1
1
BIT 2
2
BIT 3
3
BIT 4
4
BIT 5
5
BIT 6
6
BIT 7
7
BIT 8
8
BIT 9
9
BIT 10
10
BIT 11
11
(LSB) BIT 12
12
24
6.3V REF OUT
23
GAIN ADJUST
22
+VS
21
COMMON
20
Σ JUNCTION
19
20V RANGE
18
10V RANGE
17
BIPOLAR OFFSET
16
REF INPUT
15
VOUT
14
-VS
13
LOGIC SUPPLY

HI-5685V
VOLTAGE OUTPUT


TOP VIEW
(MSB) BIT 1
1
BIT 2
2
BIT 3
3
BIT 4
4
BIT 5
5
BIT 6
6
BIT 7
7
BIT 8
8
BIT 9
9
BIT 10
10
BIT 11
11
(LSB) BIT 12
12
24
6.3V REF OUT
23
GAIN ADJUST
22
+VS
21
COMMON
20
SCALING NETWORK
19
SCALING NETWORK
18
SCALING NETWORK
17
BIPOLAR OFFSET
16
REF INPUT
15
IOUT
14
-VS
13
LOGIC SUPPLY

HI-5685I
CURRENT OUTPUT

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Inputs	$+V_S$	+20V
	$-V_S$	−20V
	$+V_{LOGIC}$	+20V
Reference	Input (pin 16)	$\pm V_S$
	Output drain	2.5mA
Digital Inputs	Bits 1 to 12	−IV to +12V

Power Dissipation *		2040mW
*Derate 20.4mW/°C above 75°C		
Operating Temperature Range		
	HI-5685I/V–4	−25°C to +85°C
	HI-5685AI/V–4	−25°C to +85°C
Storage Temperature Range		−65° to +150°C

For functional diagram, definition of specifications and operating instructions, see the HI-5680.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_S = ±15V, V_{LOGIC} = 5V, PIN 16 CONNECTED TO PIN 24 UNLESS OTHERWISE SPECIFIED)

PARAMETER	CONDITIONS	HI-5685			UNITS
		MIN	TYP	MAX	
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1 µA	+2		+5.5	V
Logic "0"	at −100 µA	0		+0.8	V
Accuracy (3)					
Linearity Error	at +25°C			±½	LSB
	−25°C to +85°C			±½	LSB
Differential Lin. Error				±½	LSB
Gain Error (2)			±0.1	±0.15	%FSR (4)
Offset Error (2)			±0.05	±0.1	%FSR
Monotonicity	-25°C to +85°C		GUARANTEED		
DRIFT (3) HI-5685	−25°C to +85°C				
Gain				±20	
Offset					
Unipolar			±1	±3	PPM/°C
Bipolar			±5	±10	
DRIFT (3) HI-5685A (Low Drift)	−25°C to +85°C				
Gain				±10	
Offset					PPM/°C
Unipolar			±1		
Bipolar				±5	
CONVERSION SPEED					
Voltage Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
With 10KΩ Feedback			3		µs
With 5KΩ Feedback			1.5		µs
For 1 LSB Change			1.5		µs
Slew Rate			15		V/µs
Current Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1KΩ load			1.0		µs

SPECIFICATIONS (continued)

PARAMETER	CONDITIONS	HI-5685			UNITS
		MIN	TYP	MAX	
ANALOG OUTPUT					
Voltage Models					
Output Current		±5			mA
Output Impedance (DC)			0.05		Ω
Current Models					
Output Current	Full Scale				
Unipolar		-1.6	−2	-2.4	mA
Bipolar		±0.8	±1	±1.2	mA
Output Resistance					
Unipolar			2.0		KΩ
Bipolar			2.0		KΩ
Compliance (3)		−2.5		+10	V
INTERNAL REFERENCE					
Output voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			±10	±20	PPM/°C
POWER SUPPLY SENSITIVITY (3)					
+15V				.002	$\frac{\%FSR}{\Delta V_s}$
−15V				.002	
+5V				.002	
POWER SUPPLY REQUIREMENTS(5)					
Range					
+15V		+11.4	+15	+16.5	V
−15V		−11.4	−15	−16.5	V
+5V		+4.5	+5	+16.5	V
Current					
+15V			8	11	mA
−15V			-12	-20	mA
+5V			4.5	8	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See Definitions on HI-5680.
4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
5. The HI-5685 will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range −10V to +10V not be used if the supply voltages are less than ±12.5V.

DIE CHARACTERISTICS

Transistor Count		259
Die Size:		210 x 125 mils
Thermal Constants;	θ ja	49°C/W
	θ jc	12°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

HARRIS

HI-5687

Wide Temperature Range Monolithic 12-Bit Digital-to-Analog Converter

FEATURES

- DAC 87 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED SPECIFICATIONS -55°C to 125°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION
- MIL STD 883 PROCESSING AVAILABLE

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

DESCRIPTION

The HI-5687 is a monolithic direct replacement for the popular DAC87-CBI wide temperature range d-to-a converter. Single chip construction, along with several design innovations make the HI-5687 the optimum choice for low cost, high reliablility applications.

Harris unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. ON board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5687V), or with a user supplied external amplifier (HI-5687I).

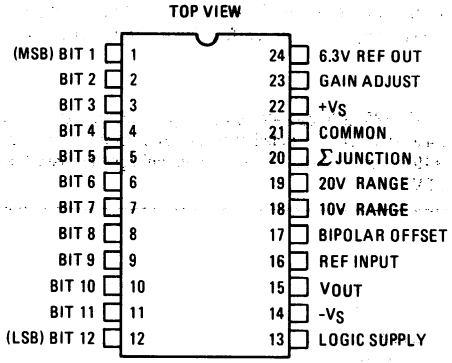
Internally, the HI-5687 eliminates code dependent ground currents by routing current from the positive supply to the internal ground mode, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5687 is available in both current and voltage output models which are 100% tested over the -55°C to +125°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ± (11.4V to 16.5V).

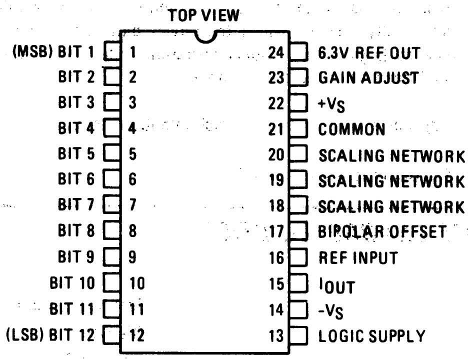
Reference HI-5680 for Functional Diagrams, (see pg. 5-40), Definitions of Specifications, (see pg. 5-43), and Operating Instructions, (see pg. 5-44).

For additional Hi-Rel screening including a 160 hour burn-in, specify the "-8" suffix.

PINOUT


TOP VIEW
(MSB) BIT 1 1
BIT 2 2
BIT 3 3
BIT 4 4
BIT 5 5
BIT 6 6
BIT 7 7
BIT 8 8
BIT 9 9
BIT 10 10
BIT 11 11
(LSB) BIT 12 12
24 6.3V REF OUT
23 GAIN ADJUST
22 +VS
21 COMMON
20 Σ JUNCTION
19 20V RANGE
18 10V RANGE
17 BIPOLAR OFFSET
16 REF INPUT
15 VOUT
14 -VS
13 LOGIC SUPPLY

HI-5687V
VOLTAGE OUTPUT


TOP VIEW
(MSB) BIT 1 1
BIT 2 2
BIT 3 3
BIT 4 4
BIT 5 5
BIT 6 6
BIT 7 7
BIT 8 8
BIT 9 9
BIT 10 10
BIT 11 11
(LSB) BIT 12 12
24 6.3V REF OUT
23 GAIN ADJUST
22 +VS
21 COMMON
20 SCALING NETWORK
19 SCALING NETWORK
18 SCALING NETWORK
17 BIPOLAR OFFSET
16 REF INPUT
15 IOUT
14 -VS
13 LOGIC SUPPLY

HI-5687I
CURRENT OUTPUT

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Inputs	$+V_S$	+20V
	$-V_S$	−20V
	$+V_{LOGIC}$	+20V
Reference	Input (pin 16)	$\pm V_S$
	Output drain	2.5mA
Digital Inputs	Bits 1 to 12	−1V to +12V

Power Dissipation *	2040mW
* Derate 20.4mW/°C abpve 75°C	
Operating Temperature Range	
HI-5687I/V-2	−55°C to +125°C
HI-5687I/V-8	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

For functional diagram, definition of specifications and operating instructions, see the HI-5680.

ELECTRICAL CHARACTERISTICS

(T_A=+25°C, V_s=±15V, V_{LOGIC} = +5V, PIN 16 CONNECTED TO PIN 24 UNLESS OTHERWISE SPECIFIED.)

PARAMETER	CONDITIONS	HI-5687			
		MIN	TYP	MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1μA	+2		+5.5	V
Logic "0"	at −100μA	0		+0.8	V
ACCURACY (3)					
Linearity Error	At +25°C		±¼	±½	LSB
	−55°C to +125°C			+¾	LSB
Differential Lin. Error	at +25°C			±¾	LSB
	−55°C to +125°C		±½	±1	LSB (4)
Gain Error (2)			±0.1	±0.2	%FSR
Offset Error (2)			±0.05	±0.1	%FSR
Monotonicity	-55°C to +125°C		GUARANTEED		
DRIFT (3)	−55°C to +125°C				
Total Bipolar Drift (includes gain, offset and linearity drifts)			±15	±30	ppm/°C
Total Error (NOTE 6)					
Unipolar			±0.13	±0.3	%FSR
Bipolar			±0.12	±0.24	%FSR
Gain					
including internal reference			±10	±25	ppm/°C
excluding internal reference			±5	±10	ppm/°C
Unipolar Offset			±1	±3	ppm/°C
Bipolar Offset			±5	±10	ppm/°C
CONVERSION SPEED					
Voltage Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
With 10KΩ Feedback			3		μs
With 5KΩ Feedback			1.5		μs
For 1 LSB Change			1.5		μs
Slew Rate			15		V/μs
Current Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1KΩ load			1.0		μs

SPECIFICATIONS (continued)

PARAMETER	CONDITIONS	HI-5687			
		MIN	TYP	MAX	UNITS
ANALOG OUTPUT					
Voltage Models					
Output Current		+5			mA
Output Impedance (DC)			0.05		Ω
Current Models					
Output Current	Full Scale				
Unipolar		-1.6	−2	-2.4	mA
Bipolar		±0.8	±1	±1.2	mA
Output Resistance					
Unipolar			2.0		KΩ
Bipolar			2.0		KΩ
Compliance (3)		-2.5		+10	V
INTERNAL REFERENCE					
Output Voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			±5	±10	ppm/°C
POWER SUPPLY SENSITIVITY (3)					
+15V				±.002	$\frac{\%FSR}{\Delta V_s}$
−15V				±.002	
+5V				±.002	
POWER SUPPLY REQUIREMENTS (5)					
Range					
+15V		+11.4	+15	+16.5	V
−15V		−11.4	−15	−16.5	V
+5V		+4.5	+5	+16.5	V
Current					
+15V			8	11	mA
−15V			-12	-20	mA
+5V			4.5	8	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See Definitions.
4. FSR is a "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
5. The HI-5687 will operate with supply voltages as low as ±11.4V. It is recommended that output voltage ranges -10V to +10V and not be used if the supply voltages are less than ±12.5V.
6. With gain and offset errors adjusted to zero at 25°C.

DIE CHARACTERISTICS

Transistor Count		259
Die Size:		210 x 125 mils
Thermal Constants;	θ ja	49°C/W
	θ jc	12°C/W
Tie Substrate to:		Ground
Process:		Bipolar - DI

HARRIS HI-5690V/95V/97V

ADVANCED

High Speed, 12 Bit Low Cost Monolithic Digital-to-Analog Converter

Features

- **Voltage Output with Fast Settling 750ns**
  High Slew Rate 50V/μs
- **Industry Standard Pinout - AD-DAC 80 & HI-5680 compatible**
- **Two-Supply Operation .... 11.4V to 16.5V**
  -11.4V to -16.5V
- **Low Noise Voltage Reference**
  1/F (0.1Hz to 10Hz) 15μVp-p
- **Guaranteed Monotonic Over Full Temperature Range**
- **Application Resistors On-Chip**
- **Monolithic Construction (Single Chip)**
- **Dielectric Isolation (DI) Processing**
- **Complete Family of Temperature Grades**

Applications

- **High Speed A/D Converters**
- **Precision Instrumentation**
- **CRT Display Generation**

Description

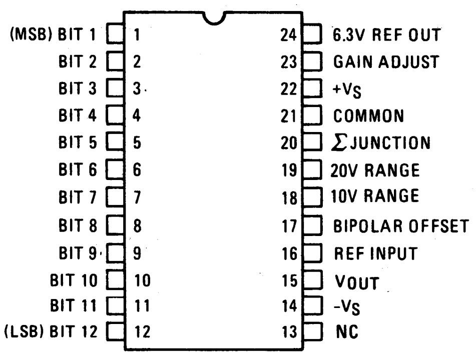
The HI-5690V series of complete 12 bit digital to analog converters includes a low noise, low temperature coefficient buried zener reference and a fast settling output amplifier. The series consists of the HI-5690V, -5695V and -5697V, for the commercial, industrial and military temperature ranges. Monolithic (single chip) construction along with several design innovations make these converters an optimum choice for high speed, high reliability applications.

The Harris unique Dielectric Isolation (DI) processing reduces internal parasitics, resulting in fast switching times and minimum glitch. Wafer-level laser trimming of span resistors and bit current cells ensures high accuracy and exceptional tracking over temperature.

Internally, the HI-5690V series eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents, allowing virtually zero variation in current through the package common, thus minimizing analog ground noise seen by the converter.

The HI-5690V series operates from two supplies ±Vs in the range of ±11.4 Volts to ±16.5 volts. It is pin compatible with the AD-DAC 80 series and HI-5680 series, and since Pin 13 is not internally connected (Logic supply on standard 5680's) this device is compatible in applications with or without +5 Volts applied to Pin 13. The converter performance is guaranteed over the full power supply operating range, but not all output ranges are available with low supply voltages. Hi-Rel screening including a 160 hour burn-in, may be specified by adding the suffix -8. The package is a 24 pin side-brazed, ceramic DIP.

Pinout



MODEL	INPUT CODE	OUTPUT MODE	TEMPERATURE RANGE
HI1-5690V-5	Complementary Binary	Voltage	0°C to 75°C
HI1-5695V-4	Complementary Binary	Voltage	-25°C to +85°C
HI1-5697V-2	Complementary Binary	Voltage	-55°C to +125°C
HI1-5697V-8*	Complementary Binary	Voltage	-55°C to +125°C

*The suffix "-8" signifies military high reliability product with burn-in (160 hours).

Absolute Maximum Ratings (Note 1)

Power Supply Inputs+Vs .... +20V
-Vs .... -20V
Reference
Input (pin 16) +Vs
Analog output can be shorted to common or either supply. (Note2)
Digital Inputs
Bits 1 to 12 .... -1V to +12V
Power Dissipation* 2040mW

Operating Temperature Range

HI-5690V-5 .... 0°C to +75°C
HI-5695V-4 .... -25°C to +85°C
HI-5697V-2 .... -55°C to +125°C
HI-5697V-8 .... -55°C to +125°C
Storage Temperature Range .... -65°C to +150°C

*Derate 20.4mW/°C above 75°C

Electrical Characteristics

(Guaranteed over the specified ranges for both temperature and supply voltage unless otherwise noted. Pin 16 connected to Pin 24, unless otherwise noted. R_L = 2KΩ)

	HI-5690V, HI-5695V, and HI-5697V				
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT (Note 3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic '1'	+1μA	+2		+5.5	Volts
Logic '0'	-100μA	0		+0.8	Volts
Input Currents					
I_{IH}	+2V			+1	μA
I_{IL}	+0.8V			-100	μA
ACCURACY (Note 3)					
Linearity Error All grades	+25°C		±3/16	±1/2	LSB
HI-5690V, HI-5695V			±1/5	±1/2	LSB
HI-5697V			±1/4	±3/4	LSB
Differential Lin.Error					
HI-5690V			±1/5	±3/4	LSB
HI-5695V			±1/5	±3/4	LSB
HI-5697V			±1/4	±1	LSB
Monotonicity			Guaranteed		
Gain Error (Note 4)					
HI-5690	+25°C		±0.05	±0.30	%FSR (5)
HI-5695V	+25°C		±0.05	±0.20	%FSR
HI-5697V	+25°C		±0.05	±0.20	%FSR
Offset Error (Note 4)					
HI-5690V	+25°C		±0.02	±0.15	%FSR
HI-5695V, HI-5697V	+25°C		±0.02	±0.10	%FSR
THERMAL DRIFT (Note 3)					
Total Bipolar Drift (Includes gain, offset & linearity drifts.)					
HI-5690V			±15	±25	ppm/°C
HI-5695V			±10	±20	ppm/°C
HI-5697V			±15	±30	ppm/°C
Gain					
HI-5690V			±10	±30	ppm/°C
HI-5695V			±8	±20	ppm/°C
HI-5697V			±8	±20	ppm/°C

PARAMETER	HI-5690V, HI-5695V, and HI-5697V				UNITS
	CONDITIONS	MIN	TYP	MAX	
Unipolar Offset			±1.5	±4	ppm/°C
Bipolar Offset			±5	±15	ppm/°C
Total Error (Note 6)					
Unipolar					
HI-5690V			±0.08	±0.17	%FSR (4)
HI-5695V			±0.10	±0.20	%FSR
HI-5697V			±0.13	±0.30	%FSR
Bipolar					
HI-5690V			±0.06	±0.12	%FSR
HI-5695V			±0.09	±0.12	%FSR
HI-5697V			±0.12	±0.30	%FSR
CONVERSION SPEED (Note 3)					
Settling Time (Note 3)	to ±0.01% of FSR for FSR Change				
With 10K Feedback	FSR = 20V; ±15V Supplies		0.9	1.5	μs
With 5K Feedback	FSR = 10V				
HI-5690V, HI-5695V			0.75	1.2	μs
HI-5697V			0.75	1.2	μs
For 1 LSB change	Major Carry		0.50		μs
Slew Rate			50		V/μs
ANALOG OUTPUT					
Output current		±5			mA
Output Resistance	DC		0.05		Ω
INTERNAL REFERENCE					
Output Voltage		+6.250	+6.3	+6.350	V
Output Resistance	DC		1.5		Ω
External Current				+2.5	mA
Reference Drift					
HI-5690V			±5	±20	ppm/°C
HI-5695V			±5	±20	ppm/°C
HI-5697V			±5		ppm/°C
Output Noise at +25°C					
Wideband	10Hz to 10kHz		12.5		μVrms
Low Frequency	0.1Hz to 10Hz		15		μVp-p
POWER SUPPLY SENSITIVITY (Note 3)					
+Vs (Pin 22)			0.0008	0.002	%FSR/%Vs
-Vs (Pin 14)			0.001	0.002	%FSR/%Vs
POWER SUPPLY REQUIREMENT (Note 7)					
Range					
+Vs (Pin 22)		+11.4	+15	+16.5	V
-Vs (Pin 14)		-11.4	-15	-16.5	V
Current					
+Vs (Pin 22)	≤ +15V		18.5	22	mA
-Vs (Pin 14)	≥ -15V		-20.5	-26	mA
Pin 13 (No Connection)			0		mA

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The output is designed to withstand a temporary short to common or either supply for a mimimum of one minute.
3. See definitions.
4. Adjustable to zero using external potentiometers.
5. FSR is "Full Scale Range" and is equal to the full scale output voltage minus the zero scale output voltage (i.e. 20V for ±10V range, 10V for ±5V range, etc.)
6. With gain and offset errors adjusted to zero at 25°C.
7. The HI-569XV series will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range -10V to +10V not be used if the supply voltages are less than ±13V.

Digital Inputs

The HI-5690V series accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	COMPLEMENTARY BINARY	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO's COMPLEMENT*
MSB LSB			
000....000	+Full Scale	+Full Scale	-LSB
100....000	Mid Scale -1 LSB	-1 LSB	+Full Scale
111....111	Zero	-Full Scale	Zero
011....111	+1/2 Full Scale	Zero	-Full Scale

*Invert MSB with external inverter to obtain CTC Coding

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low. In a 12 bit system ±1/2 LSB = ±0.012% of FSR.

Thermal Drift

Thermal drift is based on measurements at +25°C, at high (T_H) and low (T_L) temperatures. Drift calculations are made for the high (T_H-25°C) and low (+25°C-T_L) ranges, and the larger of the two values is given as a specification representing worstcase drift.

Gain Drift, Offset Drift, Reference Drift and Total Bipolar Drift are calculated in parts per million per °C as follows:

$$\text{Gain Drift} = \frac{\Delta\,\text{FSR}/\Delta^{o}\text{C}}{\text{FSR}} \times 10^6$$

$$\text{Offset Drift} = \frac{\Delta\,\text{Offset}/\Delta^{o}\text{C}}{\text{FSR}} \times 10^6$$

$$\text{Reference Drift} = \frac{\Delta\,V_{REF}/\Delta^{o}\text{C}}{V_{REF}} \times 10^6$$

$$\text{Total Bipolar Drift} = \frac{\Delta V_O/\Delta^{o}\text{C}}{\text{FSR}} \times 10^6$$

NOTE: FSR = Full Scale Output Voltage
- Zero Scale Output Voltage

Δ FSR = FSR (T_H) - FSR (+25°C)
or FSR (+25°C) - FSR (T_L)
V_O = Steady-state response to any input code.

Total Bipolar Drift is the variation of output voltage with temperature, in the bipolar mode of operation. It represents the net effect of drift in Gain, Offset, Linearity and Reference Voltage. Total Bipolar Drift values are calculated, based on measurements as explained above. Gain and Offset need not be calibrated to zero at +25°C. The specified limits for TBD apply for any input code and for any power supply setting within the specified operating range.

Accuracy

LINEARITY ERROR (Short for "Integral Linearity Error." Also, sometimes called "Integral Nonlinearity"and "Nonlinearity".)- The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to end-point linearity for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL LINEARITY ERROR - The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY - The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

TOTAL ERROR-The net output error resulting from all internal effects (primarily non-ideal Gain, Offset, Linearity and Reference Voltage). Supply voltages may be set to any values within the specified operating range. Gain and offset errors must be calibrated to zero at +25°C. Then the specified limits for Total Error apply for any input code and for any temperature within the specified operating range.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -Vs, or +Vs supplies. It is specified under DC conditions and expressed as full scale range percent of change divided by power supply percent change.

$$\text{P.S.S.} = \frac{\dfrac{\Delta \text{ Full Scale Range x 100}}{\text{Full Scale Range (Nominal)}}}{\dfrac{\Delta \text{ Vs x 100}}{\text{Vs (Nominal)}}}$$

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale, i.e. the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-569XV (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

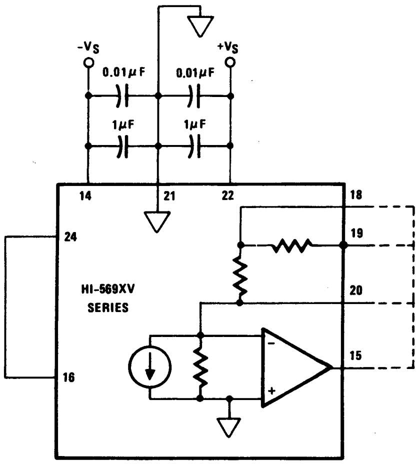


Figure 1.

Reference Supply

An internal 6.3 Volt reference is provided on board all HI-569XV models. This voltage (pin 24) is accurate to ±0.8% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-569XV. All gain adjustments should be made under constant load conditions.

Output Voltage Ranges

HI-569XV

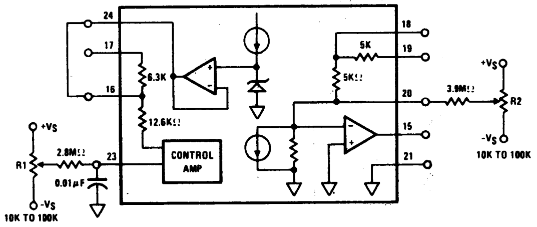


Figure 2.

RANGE CONNECTIONS

	RANGE	CONNECT PIN 15	CONNECT PIN 17	CONNECT PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to +10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±2.5V	18	20	N.C.
	±10V	19	20	15

Gain and Offset Calibration

UNIPOLAR CALIBRATION

Step 1: Offset
Turn all bits OFF (11...1)
Adjust R_2 for zero volts out

Step 2: Gain
Turn all bits ON (00...0)
Adjust R_1 for FS-1LSB
That is:
4.9988 for 0 to +5V range
9.9976 for 0 to +10V range

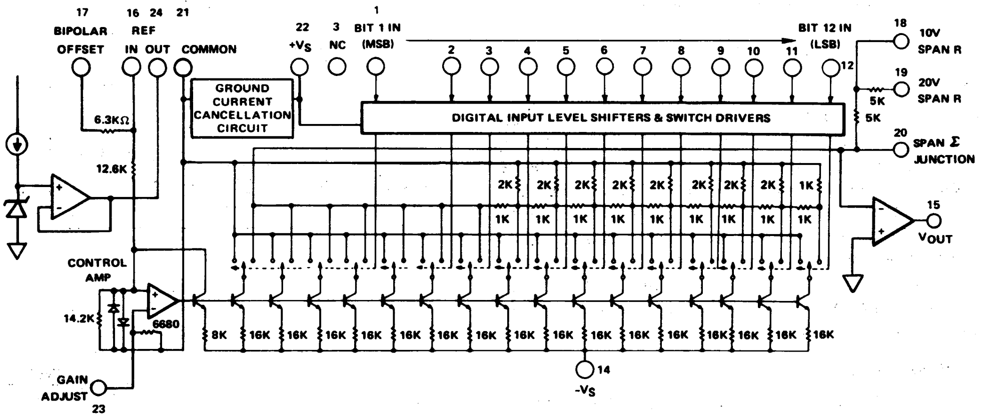
BIPOLAR CALIBRATION

Step 1: Offset
Turn all bits OFF (11...1)
Adjust R2 for Negative FS
That Is:
-10V for ±10V range
-5V for ±5V range
-2.5V for ±2.5 range

Step 2: Gain
Turn all bits ON (00...0)
Adjust R1 for positive FS-1LSB
That is:
+9.9951V for ±10V range
+4.9976V for ±5V range
+2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

Functional Block Diagram


17
BIPOLAR OFFSET
16 24
REF
IN OUT
21
COMMON
22
+VS
3
NC
1
BIT 1 IN (MSB)
BIT 12 IN (LSB)
2
3
4
5
6
7
8
9
10
11
12
18
10V SPAN R
19
20V SPAN R
5K
5K
20
SPAN Σ JUNCTION
15
VOUT
GROUND CURRENT CANCELLATION CIRCUIT
DIGITAL INPUT LEVEL SHIFTERS & SWITCH DRIVERS
6.3KΩ
12.6K
2K
1K
CONTROL AMP
14.2K
6680
8K
16K
14
-VS
GAIN ADJUST
23

Die & Package Characteristics

Transistor Count	280
Die Size	219 x 123 mils
Thermal Impedance;	
θja	49°C/W
θjc	12°C/W
Tie Substrate to:	Ground
Process	Bipolar-DI

ADVANCED

HI-5811

Complete, Monolithic 12-Bit Latched Digital-to-Analog Converter

Features

- **Microcomputer Interface with Double-Buffered Latches**
- **Single Chip Construction**
- **Alternate Source for the DAC811**
- **6.3V Reference On-Chip**
- **Voltage Output: ±10V, ±5V, +10V**
- **Monotonicity Guaranteed Over Temperature**
- **Linearity guaranteed over temperature: 1/2 LSB Max**
- **Guaranteed for Operation with ±12V and ±15V Supplies**
- **TTL/5V CMOS-Compatible Logic Inputs**

Applications

- **Microprocessor Controlled Data Acquisition Systems**
- **Precision Instrumentation**
- **Waveform Synthesizers**
- **Industrial Process Control**

Description

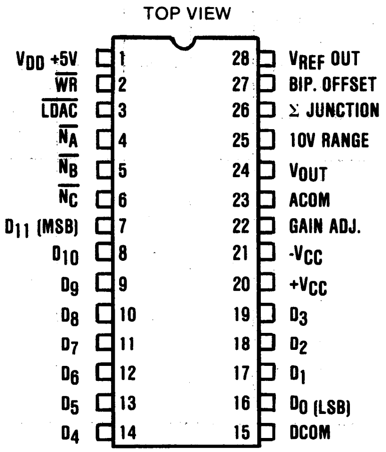
The HI-5811 is a complete, monolithic 12 bit digital-to-analog converter. It includes a precision voltage reference, microcomputer interface logic, double-buffered latch and a voltage output amplifier. The DAC features high speed current switches and a laser-trimmed thin film resistor network for fast, accurate operation.

The input latch is separated into three independently controlled 4-bit groups (nibbles), which allows the twelve input data lines to connect directly to a 4, 8, 12 or 16 bit bus. Data may be either left or right justified. An additional 12 bit latch buffers the internal DAC and blocks conversion of the partial and temporary words which appear while assembling 12 bits from a narrower data bus. Thus, the converter output can receive full 12 bit updates from a 4 bit or 8 bit data bus. To save computer instructions, the same command may load (strobe) both the D/A latch and the final input nibble(s).

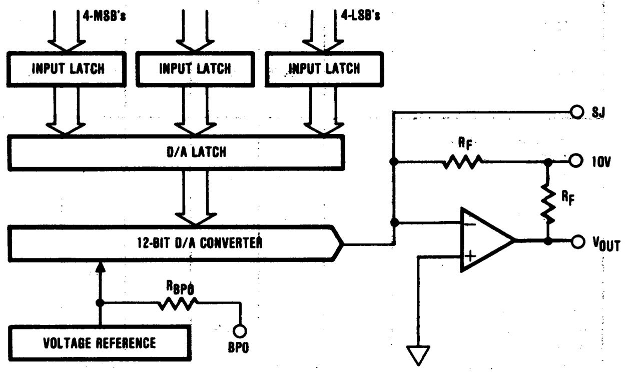
The HI-5811 is offered in two electrical grades for each of three operating temperature ranges: J-K, A-B, and R-S grades for the commercial, industrial, and military ranges. Each grade is laser-trimmed at the wafer level and guaranteed monotonic over its operating range. The maximum linearity error at +25°C is ±1/4LSB (K, B and S grade) and ±1/2 LSB (J, A and R grades).

Settling Time to ±0.01% of full scale is 4μs maximum. The HI-5811 is specified for operation with supplies form ±12V to ±15V, with a maximum power dissipation of 800mW. Package is 28 pin plastic DIP (J and K grades) or a 28 pin ceramic side-brazed DIP (A, B, R, and S grades).

Pinout


TOP VIEW
VDD +5V 1
WR 2
LDAC 3
NA 4
NB 5
NC 6
D11 (MSB) 7
D10 8
D9 9
D8 10
D7 11
D6 12
D5 13
D4 14
28 VREF OUT
27 BIP. OFFSET
26 Σ JUNCTION
25 10V RANGE
24 VOUT
23 ACOM
22 GAIN ADJ.
21 -VCC
20 +VCC
19 D3
18 D2
17 D1
16 D0 (LSB)
15 DCOM

Functional Diagram


4-MSB's
4-LSB's
INPUT LATCH
INPUT LATCH
INPUT LATCH
D/A LATCH
12-BIT D/A CONVERTER
SJ
RF
10V
RF
VOUT
RBPO
VOLTAGE REFERENCE
BPO

Absolute Maximum Ratings

+V_{CC} to ACOM .... 0 to +18V
-V_{CC} to ACOM .... 0 to -18V
V_{DD} to DCOM .... 0 to +7V
V_{DD} to ACOM .... ±7V
ACOM to DCOM .... ±7V
Digital Inputs (pins 2-14, 16-19)
to DCOM .... -0.4V to +18V
External Voltage Applied to 10V Range Resistor.... ±12V
REF OUT .... Indefinite short to ACOM
External Voltage Applied to DAC Output ....-5V to +5V
Power Dissipation(A, B, R, S)* 2000mW
(J, K) (75°C) 1600mW

Operating Temperature

J, K .... 0°C to +75°C
A, B .... -25°C to +85°C
R, S .... -55°C to +125°C
Storage Temperature (A, B, R, S) .... -65°C to +150°C
(J, K) .... -60°C to +100°C

*Derate 20mW/°C above 75°C

NOTE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability. Metal lids of ceramic packages are connected to -V_{CC}.

Electrical Characteristics

T_A = +25°C, ±VCC = 12V or 15V unless otherwise noted.

MODEL	HI-5811A,J			HI-5811B,K			HI-5811R			HI-5811S			UNITS
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT													
DIGITAL INPUT													
Resolution			12			12						12	Bits
Codes ①		USB, BOB			USB, BOB			USB, BOB			USB, BOB		
Digital Input Over Operating Temp. Range ②													
V_{IH}	+2.0		+15	+2.0		+15	+2.0		+15	+2.0		+15	VDC
V_{IL}	0.0		+0.8	0.0		+0.8	0.0		+0.8	0.0		+0.8	VDC
I_{IH}, V_1 = +2.7V			+10			+10			+10			+10	μA
I_{IL}, V_1 = +0.4V			±20			±20			±20			±20	μA
Digital Interface Timing Over Temp. Range													
t_{WP}, $\overline{WR}$ pulse width	50			50			50			50			nsec
t_{AW}①, $\overline{N_X}$ and $\overline{LDAC}$ valid to end of $\overline{WR}$	50			50			50			50			nsec
t_{DW}, data valid to end of $\overline{WR}$	80			80			80			80			nsec
t_{DH}, data valid hold time	0			0			+10			+10			nsec
TRANSFER CHARACTERISTICS													
ACCURACY													
Linearity Error		±1/4	±1/2		±1/8	±1/4		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4		±1/4	±1/2	LSB
Gain Error ③		±0.1	±0.2		±0.1	±0.2		±0.1	±0.2		±0.1	±0.2	% of FSR
Offset Error ③ ④		±0.05	±0.15		±0.05	±0.15		±0.05	±0.15		±0.05	±0.15	% of FSR ⑤
Monotonicity		Guaranteed			Guaranteed			Guaranteed			Guaranteed		
Power Supply Sensitivity,													
+V_{CC}		±0.001	±0.003		±0.001	±0.003		±0.001	±0.003		±0.001	±0.003	% of FSR/%V_{CC}
-V_{CC}		±0.002	±0.006		±0.002	±0.006		±0.002	±0.006		±0.002	±0.006	% of FSR/%V_{CC}
V_{DD}		±0.0005	±0.0015		±0.0005	±0.0015		±0.0005	±0.0015		±0.0005	±0.0015	% of FSR/%V_{DD}
DRIFT (over operating temperature range)													
Gain		±10	±30		±10	±20		±15	±30		±15	±30	ppm of FSR/°C
Unipolar Offset		±5	±10		±5	±7		±5	±10		±5	±7	ppm of FSR/°C
Bipolar Zero		±5	±10		±5	±7		±5	±10		±5	±7	ppm of FSR/°C
Lin. Error Over Temp. Range		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4		±1/4	±1/2	LSB
Monotonicity Over Temperature Range		Guaranteed			Guaranteed			Guaranteed			Guaranteed		

Specifications HI-5811

MODEL PARAMETER	HI-5811A,J			HI-5811B,K			HI-5811R			HI-5811S			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CONVERSION SPEED													
SETTLING TIME⑥ (to within ±0.01% of FSR of final value; 2kΩ load) For Full Scale Range Change,													
20V Range		3	4		3	4		3	4		3	4	μsec
10V Range		3	4		3	4		3	4		3	4	μsec
For 1LSB Chg. at Major carry ⑦		1			1			1			1		μsec
Slew Rate ⑥	8	12		8	12		8	12		8	12		V/μsec
OUTPUT													
ANALOG OUTPUT Voltage Range (±VCC = 15V) ⑧													
Unipolar		0 to +10			0 to +10			0 to +10			0 to +10		V
Bipolar		±5, ±10			±5, ±10			±5, ±10			±5, ±10		V
Output Current	±5			±5			±5			±5			mA
Output Impedance (at DC)		0.2			0.2			0.2			0.2		Ω
Short Circuit to Common Duration		Indefinite			Indefinite			Indefinite			Indefinite		
REFERENCE VOLTAGE													
Voltage	+6.2	+6.3	+6.4	+6.2	+6.3	+6.4	+6.2	+6.3	+6.4	+6.2	+6.3	+6.4	V
Source Current Available for external loads	+2.0			+2.0			+2.0			+2.0			mA
Temperature Coefficient		±10	±30		±10	±20		±10	±30		±10	±20	ppm/°C
Short Circuit to Common Duration		Indefinite			Indefinite			Indefinite			Indefinite		
POWER SUPPLY REQUIREMENTS													
Voltage,													
$+V_{CC}$	+11.4	+15	+16.5	+11.4	+15	+16.5	+11.4	+15	+16.5	+11.4	+15	+16.5	VDC
$-V_{CC}$	-11.4	-15	-16.5	-11.4	-15	-16.5	-11.4	-15	-16.5	-11.4	-15	-16.5	VDC
V_{DD}	+4.5	+5	+5.5	+4.5	+5	+5.5	+4.5	+5	+5.5	+4.5	+5	+5.5	VDC
Current (no load),													
$+V_{CC}$		+16	+25		+16	+25		+16	+25		+16	+25	mA
$-V_{CC}$		-23	-35		-23	-35		-23	-35		-23	-35	mA
V_{DD}		+8	+15		+8	+15		+8	+15		+8	+15	mA
Potential at DCOM with Respect to ACOM ⑨			±0.5			±0.5			±0.5			±0.5	V
Power Dissipation		625	800		625	800		625	800		625	800	mW

Notes:

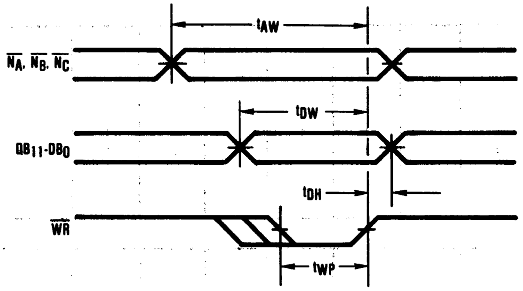
1. USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary.
2. Refer to Logic Input Compatiblity Section.
3. Adjustable to zero with external trim potentiometer.
4. Error at input code 000$_{16}$ for both unipolar and bipolar ranges.
5. FSR means Full Scale Range and is 20V for the ±10V Range.
6. Maximum or minimum represent the 3σ limit. Not 100% tested for this parameter.
7. At the major carry, 7FF$_{16}$ to 800$_{16}$ and 800$_{16}$ to 7FF$_{16}$.
8. Minimum supply voltage required for ±10V outut swing is ±13.5V. Output swing for ±11.4 supplies is at least -8V to +8V.
9. The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

Ordering Information

	Linearity Error (Max @ 25°C in LSBs)	Differential Linearity Error (Max @ 25°C in LSBs)	Temperature Range
HI3-5811J-5	1/2	3/4	0°C to +75°C
HI3-5811K-5	1/4	1/2	0°C to +75°C
HI1-5811A-4	1/2	3/4	-25°C to +85°C
HI1-5811B-4	1/4	1/2	-25°C to +85°C
HI1-5811R-2	1/2	3/4	-55°C to +125°C
HI1-5811S-2	1/4	1/2	-55°C to +125°C

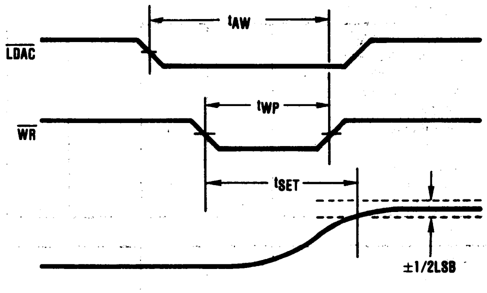
Timing Diagrams

(LOAD FIRST RANGE FROM DATA BUS: $\overline{LDAC}$ = 1)



WRITE CYCLE #1

(LOAD SECOND RANK FROM FIRST RANK: $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ = 1)



WRITE CYCLE #2

Pin Nomenclature

PIN	NAME	FUNCTION
1	V_{DD}	Logic Supply, +5V
2	$\overline{WR}$	WRITE, command signal to load latches. Logic low loads latches.
3	$\overline{LDAC}$	LOAD D/A CONVERTER, enables $\overline{WR}$ to load the D/A latch. Logic low enables.
4	$\overline{N_A}$	NIBBLE A, enables $\overline{WR}$ to load input latch A. (the most significant nibble. Logic low enables.
5	$\overline{N_B}$	NIBBLE B, enables $\overline{WR}$ to load input latch B. Logic low enables.
6	$\overline{N_C}$	NIBBLE C, enables $\overline{WR}$ to load input latch C (the least significant nybble). Logic low enables.
7	D_{11}	DATA, Bit 12, MSB; positive true.
8	D_{10}	DATA, Bit 11
9	D_9	DATA, Bit 10
10	D_8	DATA, Bit 9
11	D_7	DATA, Bit 8

PIN	NAME	FUNCTION
12	D_6	DATA, Bit 7
13	D_5	DATA, Bit 6
14	D_4	DATA, Bit 5
15	DCOM	DIGITAL COMMON, V_{DD} supply return
16	D_0	DATA, Bit 1, LSB
17	D_1	DATA, Bit 2
18	D_2	DATA, Bit 3
19	D_3	DATA, Bit 4
20	$+V_{CC}$	Analog Supply Input, +15V or +12V
21	$-V_{CC}$	Analog Supply Input, -15V or -12V
22	GAIN ADJ.	To externally adjust gain
23	ACOM	Analog Common, $\pm V_{CC}$ supply return
24	V_{OUT}	D/A converter voltage output
25	10V Range	Connect to pin 24 for 10V Range
26	SJ	SUMMING JUNCTION of output amplifier
27	BPO	BIPOLAR OFFSET. Connect to pin 26 for Bipolar Operation
28	Ref Out	6.3V reference output

Discussion of Specifications

INPUT CODES

The HI-5811 accepts positive true binary input codes. HI-5811 may be connected by the user for any one of the following codes: USB (unipolar straight binary), BOB (bipolar offset binary) or, using an external inverter on the MSB line, BTC (binary two's complement). See Table 1.

TABLE 1. DIGITAL INPUT CODES.

DIGITAL INPUT	ANALOG OUTPUT		
MSB ↓ LSB ↓	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
111111111111	+ Full Scale	+ Full Scale	-1 LSB
100000000000	+ 1/2 Full Scale	Zero	-Full Scale
011111111111	1/2 Full Scale -1 LSB	-1 LSB	+ Full Scale
000000000000	Zero	-Full Scale	Zero

* Invert the MSB of the BOB code with external inverter to obtain BTC code.

ACCURACY

INTEGRAL NONLINEARITY—The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i. e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY - The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY - The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C - T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT- The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%). See Figure 1.

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

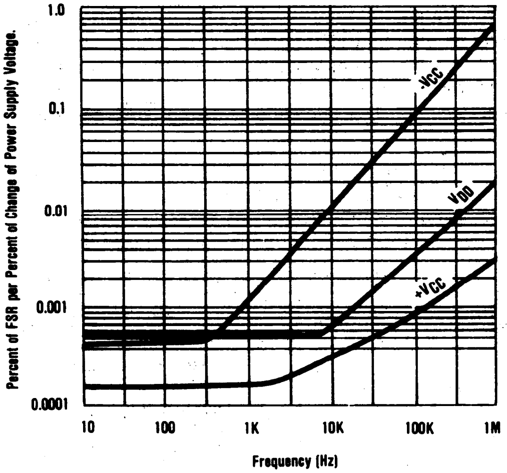


FIGURE 1. POWER SUPPLY REJECTION VERSUS POWER SUPPLY RIPPLE FREQUENCY.

Operation

HI-5811 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 2.

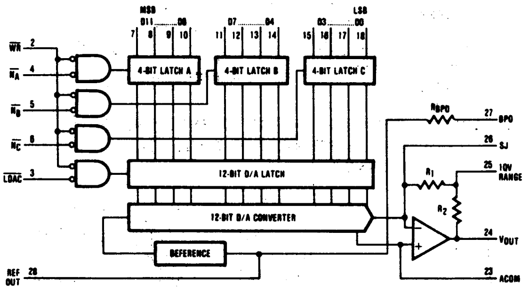


FIGURE 2. HI-5811 BLOCK DIAGRAM.

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{WR}$. $\overline{N_A}$, $\overline{N_B}$, and $\overline{N_C}$ are internally NORed with $\overline{WR}$ so that the input latches transmit data when both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ are at logic "0". When either $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) or $\overline{WR}$ go to logic "1", the input data is latched into the input registers and held until both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ go to logic "0".

The D/A latch is controlled by $\overline{LDAC}$ and $\overline{WR}$. $\overline{LDAC}$ and $\overline{WR}$ are internally NORed so that the latches transmit data to the D/A switches when both $\overline{LDAC}$ and $\overline{WR}$ are at logic "0". When either $\overline{LDAC}$ or $\overline{WR}$ are at logic "1", the data is latched in the D/A latch and held until $\overline{LDAC}$ and $\overline{WR}$ go to logic "0".

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for all latches is given in Table 2.

TABLE 2. HI-5811 INTERFACE LOGIC TRUTH TABLE.

$\overline{WR}$	$\overline{N_A}$	$\overline{N_B}$	$\overline{N_C}$	$\overline{LDAC}$	OPERATION
1	X	X	X	X	No Operation
0	0	1	1	1	Enables Input Latch 4 MSB's
0	1	0	1	1	Enables Input Latch 4 Middle Bits
0	1	1	0	1	Enables Input Latch 4 LSB's
0	1	1	1	0	Loads D/A Latch From Input Latches
0	0	0	0	0	All Latches Transparent

"X" = Don't Care.

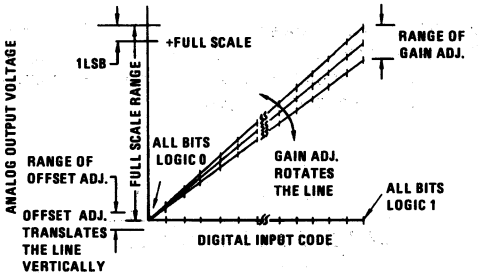

ANALOG OUTPUT VOLTAGE
+FULL SCALE
1LSB
FULL SCALE RANGE
RANGE OF GAIN ADJ.
ALL BITS LOGIC 0
GAIN ADJ. ROTATES THE LINE
RANGE OF OFFSET ADJ.
ALL BITS LOGIC 1
OFFSET ADJ. TRANSLATES THE LINE VERTICALLY
DIGITAL INPUT CODE

FIGURE 3. RELATIONSHIP OF OFFSET AND GAIN ADJUSTMENTS FOR A UNIPOLAR D/A CONVERTER

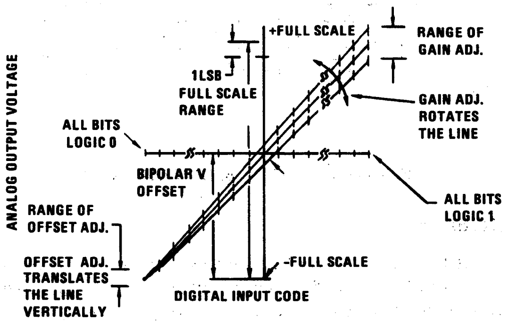

ANALOG OUTPUT VOLTAGE
+FULL SCALE
RANGE OF GAIN ADJ.
1LSB
FULL SCALE RANGE
GAIN ADJ. ROTATES THE LINE
ALL BITS LOGIC 0
BIPOLAR V OFFSET
ALL BITS LOGIC 1
RANGE OF OFFSET ADJ.
OFFSET ADJ. TRANSLATES THE LINE VERTICALLY
-FULL SCALE
DIGITAL INPUT CODE

FIGURE 4. RELATIONSHIP OF OFFSET AND GAIN ADJUSTMENTS FOR A BIPOLAR D/A CONVERTER

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the Offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is — 10V. See Table 3 for corresponding codes.

TABLE 3. DIGITAL INPUT/ANALOG OUTPUT VOLTAGE

	ANALOG OUTPUT VOLTAGE		
DIGITAL INPUT	0 to +10V	±5V	±10V
12-Bit Resolution MSB LSB			
111111111111	+9.9976V	+4.9976V	+9.9951V
100000000000	+5.0000V	0.0000V	0.00000V
011111111111	+4.9976V	-0.0024V	-0.0049
000000000000	0.0000V	-5.0000V	-10.0000V
1LSB	2.44mV	2.44mV	4.88mV

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum postive voltage output. Adjust the Gain potentiometer for this postive full scale voltage. See Table 3 for positive full scale voltages.

±12V OPERATION

The HI-5811 is fully specified for operation on ±12V power supplies. However, in order for the output to swing to ±10V, the power supplies must be ±13.5V or greater. When operating with ±12V supplies, the output swing should be restricted to ±8V in order to meet specifications.

LOGIC INPUT COMPATIBILITY

The HI-5811 digital inputs are TTL, LSTTL, and 54/74HC CMOS-compatible over the operating range of V_{DD}. The input switching threshold remains at the TTL threshold over the supply range.

The logic input current over temperature is low enough to permit driving the HI-5811 directly from the outputs of 4000B and 54/74C CMOS devices.

Installation

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram, Figure 5.

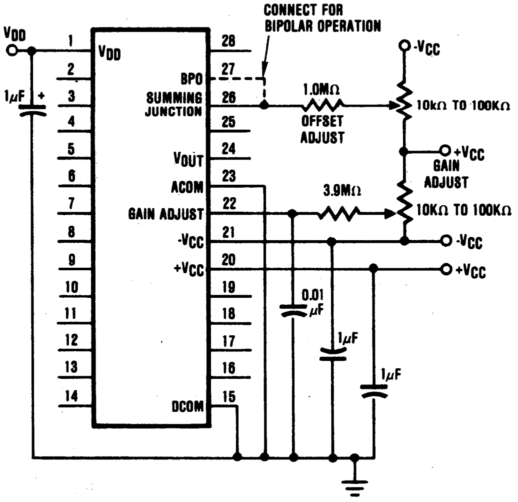

CONNECT FOR
BIPOLAR OPERATION
VDD
1μF
VDD
BPO
SUMMING JUNCTION
VOUT
ACOM
GAIN ADJUST
-VCC
+VCC
DCOM
1.0MΩ
OFFSET ADJUST
10kΩ TO 100KΩ
-VCC
+VCC
GAIN ADJUST
3.9MΩ
10KΩ TO 100KΩ
-VCC
+VCC
0.01 μF
1μF
1μF

FIGURE 5. POWER SUPPLY, GAIN, AND OFFSET POTENTIOMETER CONNECTIONS.

These capacitors (1μF tantalum recommended) should be located close to the HI-5811.

The HI-5811 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The Analog Common (pin 23) and Digital Common (pin 15) should be connected together at one point. Separate returns minimize current flow in low level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output, therefore, some caution is required in applying these common connections.

The Analog Common is the high quality return for the D/A converter and should be connected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 5. TCR of the potentiometers should be 100 ppm/°C or less. The 1.0MΩ and 3.9MΩ resistors (20% carbon or better) should be located close to the HI-5811 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 6, may be substituted in each case. The Gain Adjust (pin 22) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Analog Common to reduce noise pickup in all applications, including those not employing external gain adjustment.

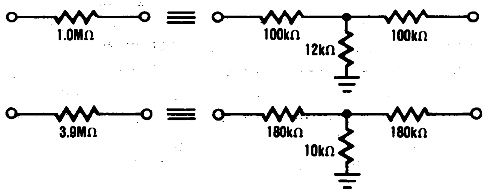

1.0MΩ
100kΩ
12kΩ
100kΩ
3.9MΩ
180kΩ
10kΩ
180kΩ

FIGURE 6. EQUIVALENT RESISTANCES.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the HI-5811 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 7. Connections for the output ranges are listed in Table IV.

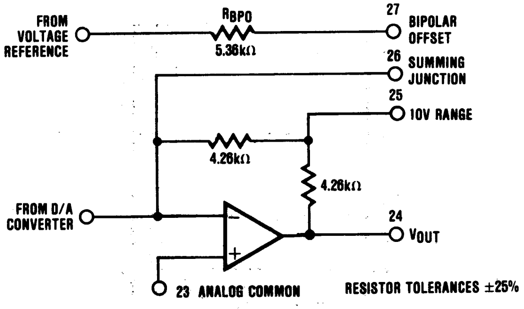

FROM VOLTAGE REFERENCE
RBPO
5.36kΩ
27
BIPOLAR OFFSET
26
SUMMING JUNCTION
25
10V RANGE
4.26kΩ
4.26kΩ
FROM D/A CONVERTER
24
VOUT
23 ANALOG COMMON
RESISTOR TOLERANCES ±25%

FIGURE 7. OUTPUT AMPLIFIER VOLTAGE RANGE SCALING CIRCUIT.

TABLE 4. OUTPUT RANGE CONNECTIONS.

Output Range	Digital Input Codes	Connect Pin 25 to	Connect Pin 27 to
0 to +10V	USB	24	23
±5V	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

Applications

MICROCOMPUTER BUS INTERFACING

The HI-5811 interface logic allows easy interface microcomputer bus structures. The control signal $\overline{WR}$ is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable line $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{LDAC}$ determine which of the latches are enabled. It is permissible to enable two or more latches simultaneously as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several HI-5811's and later strobed into the D/A latch of all D/A's simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are unused, the base address decoder can be simplified or eliminated altogether. For instance if half the memory space is unused, address line A_{15} of the microcomputer can be used as the chip select control.

4-BIT INTERFACE

An interface to a 4-bit microcomputer is shown in Figure 8. Each HI-5811 occupies four address locations. A 74LS139 provides the two to four decoder and selects these with the base address. Memory Write ($\overline{WR}$) of the microcomputer is connected directly to the $\overline{WR}$ pin of the HI-5811. A 8205 decoder is an alternative device to use instead of the 74LS139.

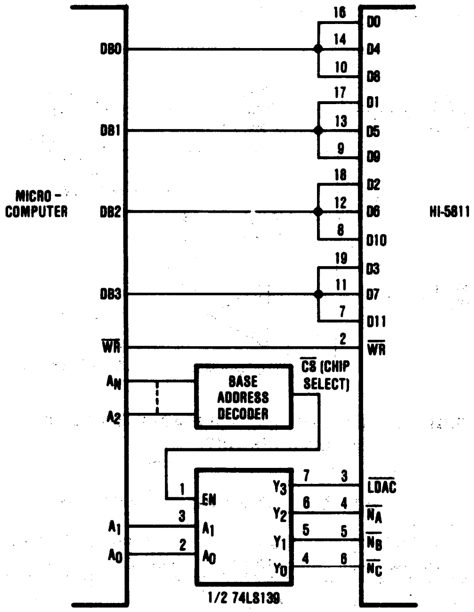

MICRO-
COMPUTER
DB0
DB1
DB2
DB3
WR
AN
A2
A1
A0
BASE ADDRESS DECODER
CS (CHIP SELECT)
1
3
2
EN
A1
A0
Y3
Y2
Y1
Y0
7
6
5
4
3
4
5
6
1/2 74LS139
16
14
10
17
13
9
18
12
8
19
11
7
2
D0
D4
D8
D1
D5
D9
D2
D6
D10
D3
D7
D11
WR
LDAC
NA
NB
NC
HI-5811

FIGURE 8. ADDRESSING AND CONTROL FOR 4-BIT MICROCOMPUTER INTERFACE.

8-BIT INTERFACE

The control logic of HI-5811 permits interfacing to right- or left-justified data formats illustrated in Figure 9. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figures 10 and 11 show an addressing scheme for right-justified and left justified data respectively. The base address is decoded from the high-order address bits. A_0 and A_1 address the appropriate latches. Note that adjacent addresses are used. For the right justified case X...X10 loads the 8 LSB's and X...X01 loads the 4 MSB's and simultaneously transfers input latch data to the D/A latch. Addresses X...X00 and X...X11 are not used.

Left-justified data is handled in a similar manner, shown in Figure 11. The HI-5811still occupies two adjacent locations in the microcomputer's memory map.

X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

.a. Right-Justified

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

b. Left-Justified

FIGURE 9. 12-BIT DATA FORMATS FOR 8-BIT SYSTEMS.

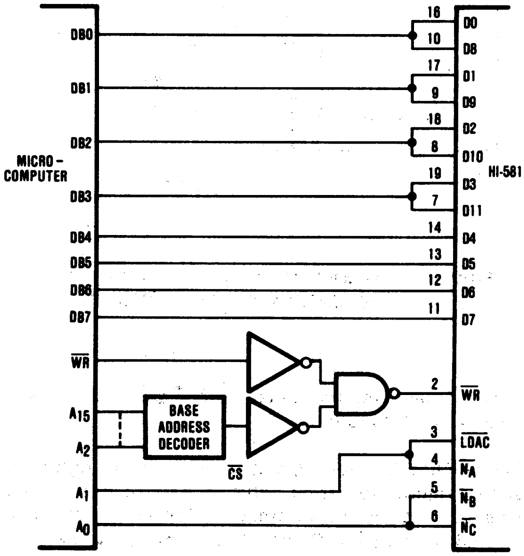

MICRO-
COMPUTER
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
WR
A15
A2
A1
A0
BASE ADDRESS DECODER
CS
16
10
17
9
18
8
19
7
14
13
12
11
2
3
4
5
6
D0
D8
D1
D9
D2
D10
D3
D11
D4
D5
D6
D7
WR
LDAC
NA
NB
NC
HI-5811

FIGURE 10. RIGHT-JUSTIFIED DATA BUS INTERFACE.

INTERFACING MULTIPLE HI-5811'S IN 8-BIT SYSTEMS

Many applications require that the outputs of several D/A converters be updated simultaneously such as automatic test systems. The interface shown in Figure 12 uses a 74LS138 decoder to decode a set of eight adjacent addresses to load the input latches of four HI-5811's. The example shows a right-justified data format.

A ninth address using A_3 causes all HI-5811's to be updated simultaneously. If a particular HI-5811 is always loaded last, for instance, D/A #4, A_3 is not needed, thus saving 8 address spaces for other uses. Incorporate A_3 into the Base Address Decoder, remove the inverter, connect the common $\overline{LDAC}$ line to $\overline{N_C}$ of D/A #4, and connect G1 of the 74LS138 to +5V.

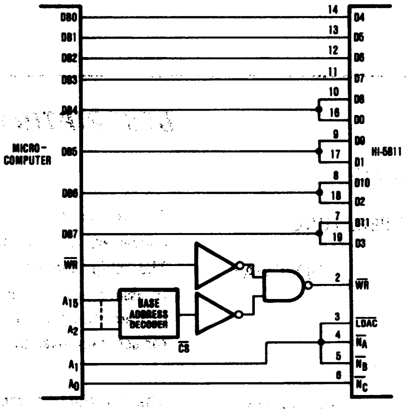
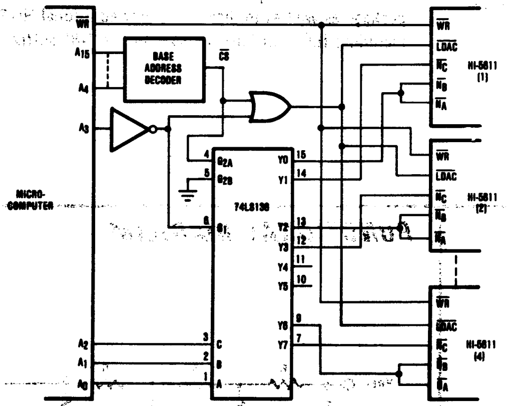

DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
WR
A15
A2
A1
A0
MICRO-COMPUTER
BASE ADDRESS DECODER
CS
14
13
12
11
10
16
9
17
8
18
7
19
2
3
4
5
6
D4
D5
D6
D7
D8
D0
D9
D1
D10
D2
D11
D3
WR
LDAC
NA
NB
NC
HI-5811

FIGURE 11. LEFT-JUSTIFIED DATA BUS INTERFACE


WR
A15
A4
A3
MICRO-COMPUTER
A2
A1
A0
BASE ADDRESS DECODER
CS
74LS138
G2A
G2B
G1
C
B
A
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
HI-5811 (1)
HI-5811 (2)
HI-5811 (4)
WR
LDAC
NC
NB
NA

ADDRESS BUS				OPERATION
A_3	A_2	A_1	A_0	
0	0	0	0	LOAD 8 LSB-D/A #1
0	0	0	1	LOAD 4 MSB-D/A #1
0	0	1	0	LOAD 8 MSB-D/A #2
0	0	1	1	LOAD 4 MSB-D/A #2
0	1	0	0	LOAD 4 MSB-D/A #3
0	1	0	1	LOAD 4 MSB-D/A #3
0	1	1	0	LOAD 8 MSB-D/A #4
0	1	1	1	LOAD 4 MSB-D/A #4
1	X	X	X	LOAD D/A LATCH ALL D/A

FIGURE 12. INTERFACING MULTIPLE HI-5811's TO AN 8-BIT BUS

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application the input latch enables lines, $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ are tied low, causing the latches to be transparent. The D/A latch, and therefore HI-5811, is selected by the address decoder and strobed by $\overline{WR}$.

Die Characteristics

Transistor Count	690
Die Size	123 X 134 mils
Thermal Constants Ceramic	θja 50°C/W
	θjc 17°C/W
Plastic	θja 62°C/W
	θjc 20°C/W
Tie Substrate to:	$-V_{CC}$
Process:	Bipolar JI

HARRIS

HI-7541

12-Bit Multiplying Monolithic Digital-to-Analog Converter

FEATURES

FULL FOUR QUADRANT MULTIPLICATION	
.01% RELATIVE ACCURACY OVER TEMPERATURE	
LOW OUTPUT CAPACITANCE	100pF MAX
TTL/CMOS COMPATIBLE	
MONOLITHIC CONSTRUCTION	
VERY LOW OUTPUT LEAKAGE CURRENT	±100nA MAX
LOW GAIN ERROR	0.1%

APPLICATIONS

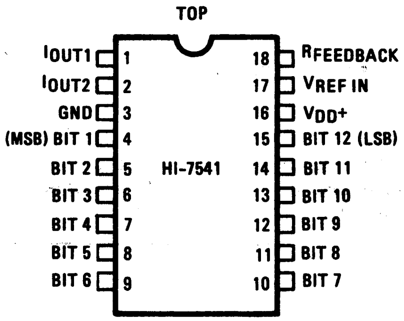
- PROGRAMMABLE GAIN AMPLIFIERS
- PROGRAMMABLE FUNCTION GENERATION

DESCRIPTION

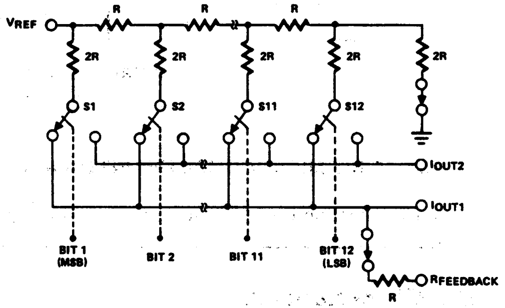
The Harris HI-7541 is a 12-Bit Monolithic Digital to Analog converter, offering full four quadrant multiplying capability. The chip features dielectrically isolated CMOS technology to assure fast settling time and freedom from latch-up. Included are thin film ladder and applications resistors, laser trimmed for accuracy over the full operating temperature range.

The HI-7541 is recommended as a high performance direct replacement for the AD7541 device. It operates on a single +5V to +15V supply and is available in an 18-pin ceramic package as well as in dice form. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix.

PINOUT


TOP
IOUT1 1
IOUT2 2
GND 3
(MSB) BIT 1 4
BIT 2 5
BIT 3 6
BIT 4 7
BIT 5 8
BIT 6 9
HI-7541
18 RFEEDBACK
17 VREF IN
16 VDD+
15 BIT 12 (LSB)
14 BIT 11
13 BIT 10
12 BIT 9
11 BIT 8
10 BIT 7

FUNCTIONAL DIAGRAM


VREF
R
R
R
2R
2R
2R
2R
2R
S1
S2
S11
S12
IOUT2
IOUT1
BIT 1 (MSB)
BIT 2
BIT 11
BIT 12 (LSB)
RFEEDBACK
R

DIGITAL INPUTS (DTL, TTL, CMOS COMPATIBLE)
LOGIC: A SWITCH IS CLOSED TO I_{OUT1} FOR ITS DIGITAL INPUT IN A HIGH (LOGIC 1) STATE.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)1

Power Supply Inputs V_{DD}	+17V
Reference Inputs VREF (Hi)	±25V
Digital Input Range Bits 1-12	V_{DD} to GND
Output Voltage (Pins 1 and 2)	-400mV to V_{DD}
Power Dissipation Derate above +75°C by12.4mW/°C.	1235mW
Operating Temperature Range	
HI-7541SD/TD	-55°C to +125°C
HI-7541AD/BD	-25°C to +85°C
HI-7541JD/JO/KD	0°C to +75°C
HI-7541SD/883 AND TD/883.	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@25°C, V_{DD} = +15V, V_{REF} = +10V Unless otherwise noted)

PARAMETER	CONDITIONS	HI-7541KN/BD/TD			HI-7541JN/AD/SD/JO/SO			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Digital Inputs	Bit ON = "Logic 1" Bit OFF = " Logic 0"							
Input Voltage								
Logic 1, V_{IH}		2.4			2.4			V
Logic 0, V_{IL}				0.8			0.8	V
Input Current								
Logic 1	V_{IN}=15V			1			1	μA
Logic 0	V_{IN}=0V			-1			-1	μA
Reference Input								
Input Resistance		7	9	12	7	9	12	KΩ
Input Voltage		-10		+10	-10		+10	V
TRANSFER CHARACTERISTICS								
Resolution	Over Full Temp. Range	12			12			Bits
Integral (2) Nonlinearity	Over Full Temp Range			±1/2			±1	LSB
Differential (2) Nonlinearity	Over Full Temp Range			±1/2			±1	LSB
Gain Error (2)	@ +25°C Over Full Temp. Range			±12.5 ±16.7			±12.5 ±16.7	LSB
Gain Tempco (2)(5)	Over Full Temp. Range			±10			±10	PPM/°C
Settling Time (2) (5) to ±1/2 LSB				1			1	μs
PSRR (2)	12.0V ≤ V_{DD} ≤ 16.0V Over Full Temp. Range			±.01 ±.02			±.01 ±.02	%FSR/°C %ΔV_{DD}
OUTPUT CHARACTERISTICS								
Output (2) Leakage Current	V_{REF} = ±10V @ +25°C Over Full Temp. Range			±50 ±200			±50 ±200	nA nA
Capacitance (2) (5)				100			100	pF
Feed Through (2)(5)	V_{REF} = 20 V_{pp} @ 10kHz			±1			±1	mVpp
POWER REQUIREMENTS								
V_{DD}	(See Fig. 6, 8 & 9)	+5	+15	+16	+5	+15	+16	V
I_{DD} (3)				2			2	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. After 30 seconds warm-up.
4. Specification's subject to change without notice.
5. Guaranteed by design, not tested.

DEFINITIONS OF SPECIFICATIONS

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00. . .0 and 11. . .1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

FEEDTHROUGH ERROR

Variation in V_{OUT} due to variation in V_{REF}, for the condition all bits OFF (zero output current).

GAIN

The gain is defined only when the MDAC is used with an output operational amplifier in which case it is V_{OUT}/V_{REF}.

POWER SUPPLY REJECTION RATIO (PSRR)

Variation in V_{OUT} due to variation in V_{DD}, expressed in %FSR/% V_{ps}.

OUTPUT CAPACITANCE

Measured capacity from I_{OUT1} or I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT

Current leakage to ground from I_{OUT1} (all bits low) or I_{OUT2} (all bits high) with no connection to the span resistor (Pin 18).

OPERATING INSTRUCTIONS

BYPASSING AND GROUNDING

For best accuracy and high frequency performance the grounding and bypass scheme shown in Figure 1 should be used. Bypass capacitors should be connected close to the HI-7541 (preferably to the device pins) and should be tantalum in parallel with a smaller ceramic type for best high frequency noise rejection.

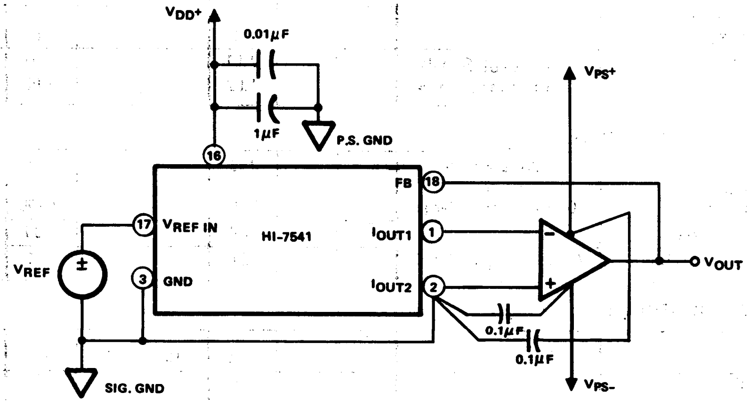
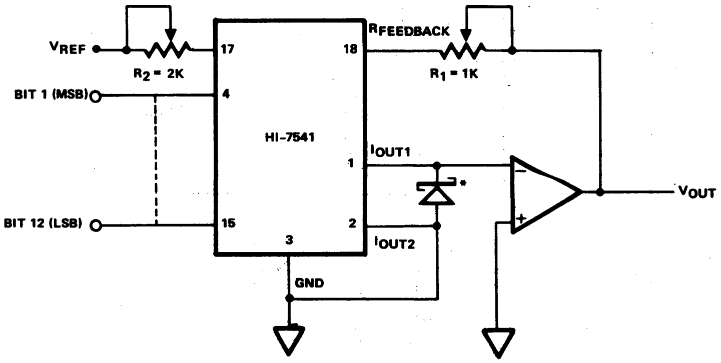


FIGURE 1

UNIPOLAR BINARY OPERATION

For most applications the HI-7541 requires an output operational amplifier, since both I_{OUT1} and I_{OUT2} should remain at ground potential to avoid linearity errors. Figure 2 shows the connections for unipolar straight binary operation. The calibration of gain will require either R_1 (to increase gain) or R_2 (to decrease gain), but not both. If both these resistors are omitted, the gain error is guaranteed not to exceed ±0.15% of full scale, over the military temperature range. See the "Offset" section for calibration of the error at zero.



*A Schottky diode to ground should be connected to IOUT1 or IOUT2, for any application in which a negative voltage greater than 400mV may be applied. This can occur with certain high speed op amps, whose inverting input may offer a low impedance to the negative supply rail during turn-on of power.

For these applications, the HI-7541 output will source excessive current and suffer damage unless it is clamped with a Schottky diode (such as the HP5082-2811 or equivalent).

FIGURE 2

CODE TABLE- UNIPOLAR OPERATION

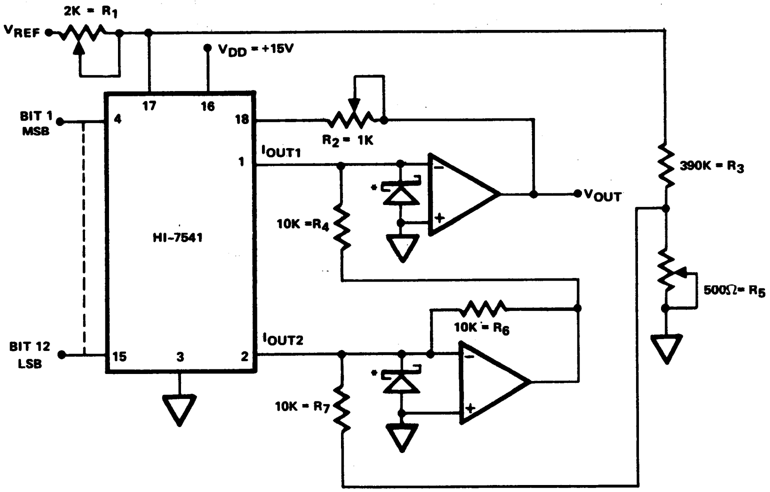
DIGITAL INPUT												NOMINAL ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}(1-2^{-12})$
1	0	0	0	0	0	0	0	0	0	0	1	$-V_{REF}(1/2+2^{-12})$
1	0	0	0	0	0	0	0	0	0	0	0	$-V_{REF}/2$
0	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}(1/2-2^{-12})$
0	0	0	0	0	0	0	0	0	0	0	1	$-V_{REF}(2^{-12})$
0	0	0	0	0	0	0	0	0	0	0	0	0

CODE TABLE - BIPOLAR (OFFSET) OPERATION

DIGITAL INPUT												NOMINAL ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}(1-2^{-11})$
1	0	0	0	0	0	0	0	0	0	0	1	$-V_{REF}(2^{-11})$
1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	1	1	1	1	$V_{REF}(2^{-11})$
0	0	0	0	0	0	0	0	0	0	0	1	$V_{REF}(1-2^{-11})$
0	0	0	0	0	0	0	0	0	0	0	0	V_{REF}

BIPOLAR (4-QUADRANT) BINARY OPERATION

Figure 3 shows the configuration for bipolar offset binary coded operation. As in the unipolar case, gain calibration requires either R_1 or R_2, but not both. The network $R_3/R_5/R_7$ assures that V_O = 0V at the zero (midrange) code 100000 000000, for which I_{OUT1} and I_{OUT2} differ by 1/2 LSB.



*A Schottky diode to ground should be connected to IOUT1 or IOUT2, for any application in which a negative voltage greater than 400mV may be applied. This can occur with certain high speed op amps, whose inverting input may offer a low impedance to the negative supply rail during turn-on of power.

For these applications, the HI-7541 output will source excessive current and suffer damage unless it is clamped with a Schottky diode (such as the HP5082-2811 or equivalent).

FIGURE 3

OFFSET AND GAIN CALIBRATION

UNIPOLAR CALIBRATION (Fig. 2)	
Step 1:	Unipolar Zero Offset Adjustment • Turn all bits OFF (00...00) • Adjust offset trimpot (See Figure 5) for V_{OUT} = 0V.
Step 2:	Unipolar Gain Adjustment • Turn all bits ON (11...11) • Adjust R_1 or R_2 for an output of $V_{OUT} = -V_{REF}(1-2^{-12})$
BIPOLAR CALIBRATION (Fig. 3)	
Step 1:	Bipolar Offset Adjustment • Set V_{REF} = +10V • Turn all bits OFF (0000...00) • Adjust R_5 so that V_{OUT} = 10V
Step 2:	Bipolar Gain Adjustment • Set V_{REF} = +10V • Turn all bits ON (1111...11) • Adjust R_1 or R_2 so that V_{OUT} = -9.99512V

SELECTING AN OPERATIONAL AMPLIFIER

The outputs I_{OUT1} and I_{OUT2} must remain very close to ground potential for the HI-7541 to maintain its accuracy. Because of this constraint, most applications require selection of a suitable output op-amp. Harris Analog Products Division offers a wide range of high performance op-amps which are well suited to a variety of applications.

COMPENSATION

In the standard configurations of Figures 1 and 2 the output capacitance of the MDAC along with the feedback resistance introduces a pole in the open loop response of the system. This pole may cause undesirable phase shift leading to excessive ringing or even oscillation. The phase shift may be compensated by placing a capacitor in the feedback loop. Figure 4 shows this scheme. The compensation is exact for RoCo = R_{FB} C_{FB}. This is a special case, however, since both Ro and Co are dependent on the digital code for a CMOS MDAC.

A practical approach is to turn all bits of the MDAC ON while applying a square wave of appropriate magnitude to the reference input. Then select a feedback capacitor which gives approximately 20% of overshoot, which is equal to a 45° Phase Margin. This form of compensation reduces the overall bandwidth of the system, which is dependent on the op amp selected.

MDAC EQUIVALENT CIRCUIT WITH COMPENSATION

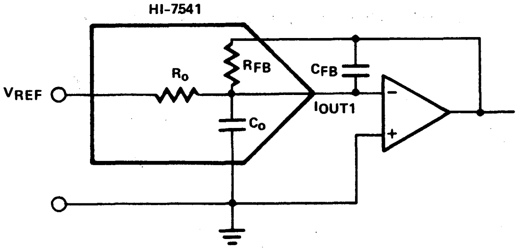


FIGURE 4

OP AMP PARAMETERS

The addition of the output amplifier has a direct effect on many of the MDAC parameters, including bandwidth, settling time, accuracy and tempco. Settling time is difficult to measure for the HI-7541 since the current outputs have almost no voltage compliance. The output settling time of the MDAC-OP AMP system can be measured; and if the settling time of the Op Amp itself is known, that of the MDAC can be estimated by the Root-Sum of Squares method;

$$T_{MDAC} = \sqrt{T^2_{MDAC/AMP} - T^2_{AMP}}$$

The bandwidth of the MDAC itself can be approximated by modeling it as a voltage source (V_{ref}) followed by a series resistance (Ro) and capacitance (Co) as in figure 4. The half-power frequency then is;

$$f = \frac{1}{2\pi RoCo}$$

If R_0 = 10KΩ and C_0 = 50pf then f = 318KHz. However, an output amplifier virtually eliminates C_0 by maintaining zero volts across it, thus extending the DAC/amplifier bandwidth almost to that of the amplifier alone.

TABLE 1 HARRIS OP AMPS
(TYPICAL AT T_A = +25°C)

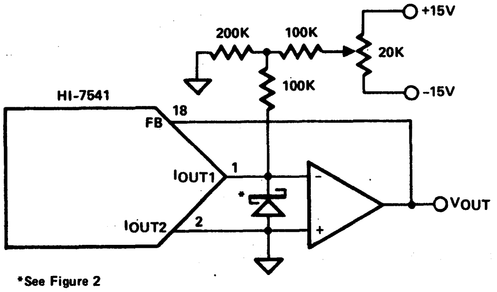
Op Amp HA-	Full Power B.W.	Offset Voltage	Offset Voltage Drift	Bias Current	C_{FB}* Compensation for 45° P.M.	Settling Time**
2600	75KHz	500μV	5μV/°C	1nA	20pf	1.5μs
2525	1.6MHz	5mV	30μV/°C	125nA	12pf	200ns
5100	150KHz	500μV	5μV/°C	20pA	18pf	1.7μs
5130	600KHz	100μV	1μV/°C	1nA	30pf	11μs
5190	6.5MHz	3mV	20μV/°C	5μA	2pf	70ns

* For standard configuration such as Figure 3. Vref equals 1KHz 10V peak to peak square wave.

** For the Op Amp alone. A_{VCL} = -1, 10V step to 0.1%.

OFFSET

The amplifier's Offset Voltage V_{OS} contributes a code dependent output error, since V_{OS} is multiplied by a gain factor (1 + R_F/R_{OUT}) in which R_{OUT} is code dependent. R_{OUT} ranges from 10kΩ to 30kΩ for nonzero input codes. R_F is 10kΩ, which leads to an output error variation of 2/3 V_{OS} (from 4/3 V_{OS} to 2 V_{OS}).



*See Figure 2

FIGURE 5

This effect applies for offset introduced at the noninverting terminal as well as V_{OS} inherent in the amplifier. Therefore, the common technique of nulling V_{OS} (due to bias current) with a resistor from the noninverting input to ground is not recommended. Instead, choose an amplifier with low V_{OS} (200μV or less) and low I_{BIAS} (75nA or less), and connect the noninverting input directly to ground. The HA-5130 and HA-5170 are recommended for these high accuracy applications.

Output Leakage Current from the HI-7541 flows through the feedback resistor to create another type of offset error. This leakage is insignificant except at high temperature, where the maximum output error is one millivolt. To null this error, inject an opposing current at the summing junction using a network as shown in Figure 5. All lead lengths connecting to $I_{OUT}1$ should be short, to minimize capacitance to ground and maintain a fast settling time.

PERFORMANCE CURVES

GAIN ERROR vs. SUPPLY VOLTAGE

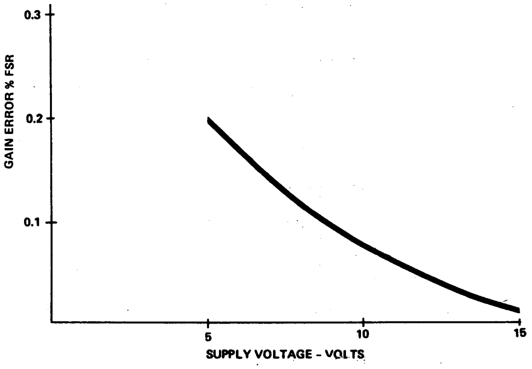


FIGURE 6

FEEDTHROUGH ERROR vs. FREQUENCY

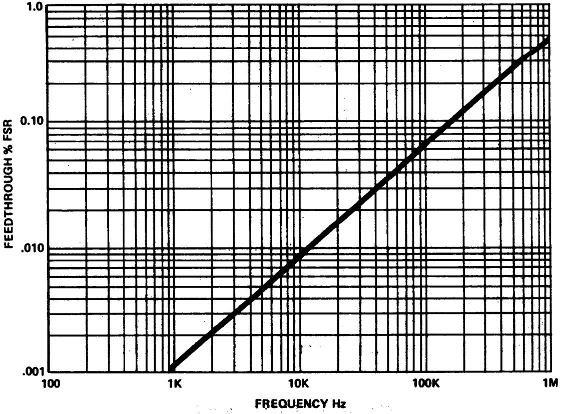


FIGURE 7

LINEARITY vs. SUPPLY VOLTAGE

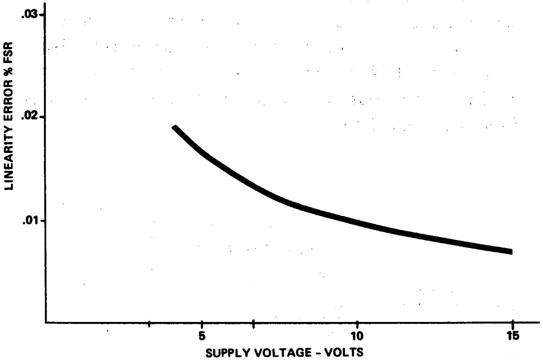


FIGURE 8

SUPPLY CURRENT vs. SUPPLY VOLTAGE

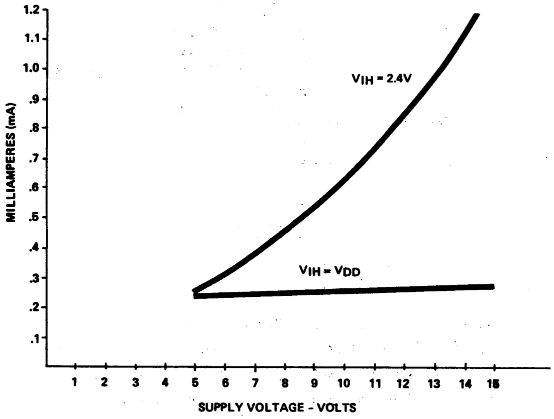


FIGURE 9

DIE CHARACTERISTICS

Transistor Count		198	Tie Substrate to:	Ground
Die Size:		111 x 99 mils	Process:	CMOS - DI
Thermal Constants;	θ_{ja}	81°C/W		
	θ_{jc}	23°C/W		

HARRIS

HI-DAC16B/ DAC16C

16-Bit D to A Converter

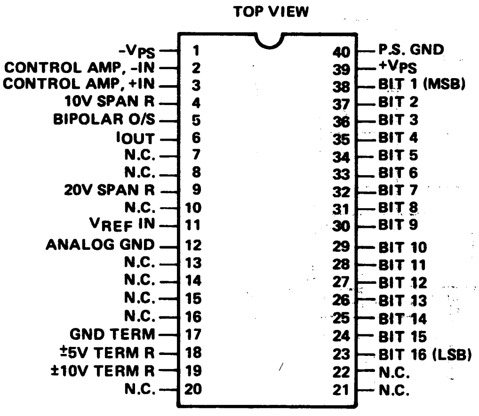
FEATURES

● 16 BIT RESOLUTION	
● MONOLITHIC DI BIPOLAR CONSTRUCTION	
● FAST SETTLING TIME	1 μs TO .003%FS
● LOW DIFF. NONLIN. DRIFT	± 0.3ppm/°C
● LOW GAIN DRIFT	± 1ppm/°C
● ON-CHIP SPAN & OFFSET RESISTORS	
● TTL/5V-CMOS COMPATIBLE	
● LOW UNIPOLAR OFFSET	≤ 1/2LSB@ +25°C
● LOW UNIPOLAR OFFSET T.C.	± 0.2ppm/°C
● EXCELLENT STABILITY	

APPLICATIONS

- HIGH RESOLUTION CONTROL SYSTEMS
- HIGH FIDELITY AUDIO RECONSTRUCTION
- PRECISION FUNCTION GENERATION AND INSTRUMENTATION

PINOUT


TOP VIEW
-VPS 1
CONTROL AMP, -IN 2
CONTROL AMP, +IN 3
10V SPAN R 4
BIPOLAR O/S 5
IOUT 6
N.C. 7
N.C. 8
20V SPAN R 9
N.C. 10
VREF IN 11
ANALOG GND 12
N.C. 13
N.C. 14
N.C. 15
N.C. 16
GND TERM 17
±5V TERM R 18
±10V TERM R 19
N.C. 20
40 P.S. GND
39 +VPS
38 BIT 1 (MSB)
37 BIT 2
36 BIT 3
35 BIT 4
34 BIT 5
33 BIT 6
32 BIT 7
31 BIT 8
30 BIT 9
29 BIT 10
28 BIT 11
27 BIT 12
26 BIT 13
25 BIT 14
24 BIT 15
23 BIT 16 (LSB)
22 N.C.
21 N.C.

DESCRIPTION

The HARRIS HI-DAC16 is a 16-bit, current output D/A converter. Single chip construction includes thin-film application resistors for use with an external op amp. These permit standard output voltage ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V. The HI-DAC16B is monotonic to 15 bits; and the HI-DAC16C to 14 bits.

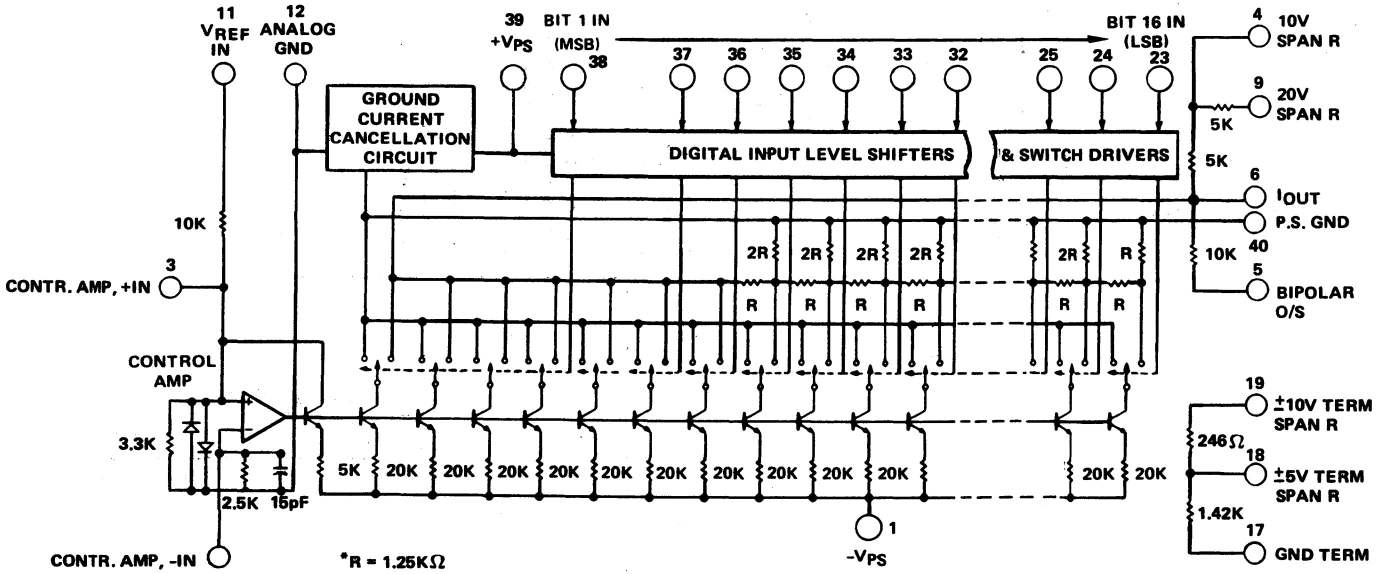
Reference and span resistors have adjacent placement on the chip for optimum match and thermal tracking. Futhermore, this layout feature helps minimize the superposition error caused by self-heating of the span resistor, reducing it to less than 1/10LSB. This and other design innovations have produced exceptionally stable operation over temperature. Typical temperature coefficients are ± 1ppm/°C for gain error and 0.3ppm/°C for differential non-linearity error.

The internal architecture is an extension of the earlier HI-562 with several major improvements. All code dependent ground currents are steered to a separate non-critical path, namely, power supply ground. This feature allows the precision ground of the converter to be sensed with virtually zero voltage drop referred to system ground. The result is the complete elimination of non-linearities due to code dependent ground currents while yielding an extremely low unipolar offset of less than 1/2LSB. Because of this separation, the user may route the precision ground some distance to the system ground without degrading converter accuracy.

The HARRIS HI-DAC16 delivers a stable, accurate output without sacrifice in speed. Settling time to within ±0.003% is one microsecond. Overall performance of this monolithic device should be attractive for applications such as high fidelity audio and high-resolution control systems.

Two accuracy grades are offered, and typical power dissipation is 465mW. Package is a 40 pin ceramic DIP. For further information, see Application Note 539.

FUNCTIONAL DIAGRAM


11
V_{REF} IN
12
ANALOG GND
GROUND CURRENT CANCELLATION CIRCUIT
39
$+V_{PS}$
BIT 1 IN (MSB)
38
37
36
35
34
33
32
25
24
23
BIT 16 IN (LSB)
DIGITAL INPUT LEVEL SHIFTERS
& SWITCH DRIVERS
4
10V SPAN R
9
20V SPAN R
5K
5K
6
I_{OUT}
P.S. GND
40
10K
5
BIPOLAR O/S
10K
3
CONTR. AMP, +IN
2R
2R
2R
2R
2R
R
R
R
R
R
R
R
CONTROL AMP
3.3K
2.5K
15pF
5K
20K
20K
20K
20K
20K
20K
20K
20K
20K
20K
20K
20K
19
±10V TERM SPAN R
246Ω
18
±5V TERM SPAN R
1.42K
17
GND TERM
1
$-V_{PS}$
CONTR. AMP, -IN
2
*R = 1.25KΩ

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	−20V
Reference Inputs	V_{REF} (Hi)	$\pm V_{ps}$
Digital Inputs	Bits 1 to 16	−1V, +12V
Outputs		$\pm V_{ps}$

Power Dissipation *	2440mW
Operating Temperature Range	
HI-DAC 16B/C	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

*Derate 24,4mW/°C above 75°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{ps} = ±15V, V_{ref} = +10V, unless otherwise specified)

PARAMETER	CONDITIONS	HI-DAC16B MIN	HI-DAC16B TYP	HI-DAC16B MAX	HI-DAC16C MIN	HI-DAC16C TYP	HI-DAC16C MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs	Bit ON "Logic 1" Bit OFF "Logic 0"							
Input Voltage	Full Temperature Range							
Logic "1"		2.0			2.0			V
Logic "0"				0.8			0.8	V
Input Current								
Logic "1"			20	500		20	500	nA
Logic "0"		-50			-50			μA
Reference Input								
Input Resistance			10			10		KΩ
Input Voltage			10			10		V
TRANSFER CHARACTERISTICS								
Resolution	Full Temperature Range		16			16		Bits
Nonlinearity	25°C		±0.0023			±0.0045		%FSR(3)
	Full Temperature Range			±0.0045			±0.009	
Differential Nonlinearity	25°C		±0.0015			±0.003		%FSR
	Full Temperature Range			±0.003			±0.006	
Relative Accuracy (5)	With 100Ω(1%) Trim Resistors							%FSR
Unipolar Gain Error	All Bits ON		±0.1	±0.25		±0.1	±0.25	
Bipolar Offset Error	All Bits OFF		±0.15	±0.43		±0.15	±0.43	
Unipolar Offset Error			±0.002	±0.05		±0.002	±0.05	
Adjustment Range	See Operating Instructions							%FSR
Gain	Using Trim Potentiometers as shown in Figure 1			±3			±3	
Bipolar Offset				±0.43			±0.43	
Temperature Stability	Drift specified with internal span resistors for voltage output							ppm of FSR/°C
Gain Drift (2)	Full Temperature Range		±1	±5		±1	±5	
Offset Drift (2)								
Unipolar Offset	All Bits OFF		±0.2			±0.2		
Bipolar Offset			±0.5			±0.5		
Differential Nonlinearity	Full Temperature Range		±0.3			±0.3		
Settling Time (2) to ±0.003%FS	All Bits ON-to-OFF or OFF-to-ON		1.0			1.0		μs

SPECIFICATIONS (Continued)

PARAMETER	CONDITIONS	HI-DAC16B MIN	HI-DAC16B TYP	HI-DAC16B MAX	HI-DAC16C MIN	HI-DAC16C TYP	HI-DAC16C MAX	UNITS
Glitch (2)	From 0111 . . . 1 to 100 . . . 0 or 100 . . . 0 to 011 . . . 1		1300			1300		mV–ns
Power Supply (2) Rejection Ratio, PSRR (3)								
$V_{ps}+$			1.5			1.5		ppm of FSR/% V_{ps}
$V_{ps}-$			1.5			1.5		
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar		-1.6	-2	-2.4	-1.6	-2	-2.4	mA
Bipolar		±0.8	±1	±1.2	±0.8	±1	±1.2	
Resistance			2.5k			2.5k		
Capacitance			10			10		pF
Output Voltage Ranges	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections							V
Unipolar			0 to +5 0 to +10			0 to +5 0 to +10		
Bipolar			±2.5 ±5 ±10			±2.5 ±5 ±10		
Compliance Limit (2)		-3		+10	-3		+10	V
Compliance Voltage (2)	Full Temperature Range		±1			±1		V
Output Noise	0.1 to 5MHz (All bits ON)		30			30		μVRMS
POWER REQUIREMENTS								
$V_{ps}+$ (7)	Full Temperature Range	13.5	+15	16.5	13.5	+15	16.5	V
$V_{ps}-$		-13.5	-15	-16.5	-13.5	-15	-16.5	
$I_{ps}+$ (4)	All Bits ON or OFF Full Temperature Range		+13	+18		+13	+18	mA
$I_{ps}-$ (4)		-25	-18		-25	-18		
Power Dissipation			465			465		mW

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impared. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
4. After 30 seconds warm-up.
5. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-DAC 16B/C accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement, or Offset Binary. (See Operation Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement *
MSB LSB			
000...000	Zero	-FS 9(Full Scale)	Zero
100...000	½FS	Zero	−FS
111...111	+FS − 1 LSB	+FS − 1 LSB	Zero − 1 LSB
011...111	½FS − 1 LSB	Zero − 1 LSB	+FS − 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H−25°C) and low ranges (+25°C−T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H −25°C) and low (+25°C −T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in −15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON–OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Calculated as the product of duration and amplitude.)

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

FIGURE 1

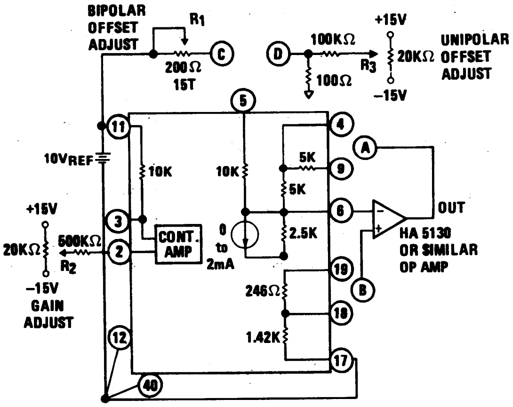


TABLE 1

	OUTPUT RANGE	CONNECTIONS			
		PIN5 to	PIN4 to	PIN9 to	PIN B to
UNIPOLAR MODE	0 to +10V	D	A	N.C.	19
	0 to +5V	D	A	PIN6	*
BIPOLAR MODE	±10V	C	N.C.	A	19
	±5V	C	A	N.C.	18
	±2.5V	C	A	6	*

*Connect an external 1.1K ohm resistor to ground.

GAIN AND ZERO CALIBRATION

The HI–DAC16B/C input reference resistor, bipolar offset resistor and span resistors are optimized for excellent tracking over temperature. LASER trimming of the reference circuit resistors corrects the unipolar Gain and Offset errors to high accuracy. The remaining error can be adjusted with trimming potentiometers. The bipolar Gain and Offset errors are greater since the LASER correction is done in the unipolar mode, however these too are easily adjusted. Figure 1 illustrates the connections for unipolar and bipolar operation. Trimming potentiometers R_1, R_2, and R_3 are required for adjustment.

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (00..0)
- Adjust R_3 for zero volts output

Step 2: Gain
- Turn all bits ON (11..1)
- Adjust R_2 for an output of FS-1 LSB

That is, adjust for:

9.999847 for +10V range
4.999924 for +5V range

BIPOLAR CALIBRATION

Step 1: Offset
Turn all bits OFF (00..0)
Adjust R_1 for an output of
−10V for ± 10V range
−5V for ± 5V range
−2.5V for ± 2.5V range

Step 2: Gain
Turn all bits ON (11..1)
Adjust R_2 for FS-1LSB output
That is, adjust for:

9.999695 for ±10V range
4.999847 for ± 5V range
2.499924 for ± 2.5V range

OTHER CONSIDERATIONS

GROUNDS

The HI-DAC16 has two ground terminals, pin 12 (REF GND) and pin 40 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 12 and 40).

The current through pin 12 is near-zero DC*, but pin 40 carries up to 1.75mA of code - dependent current from bits 1, 2, and 3. The general rule is to connect pin 12 directly to the system signal, or analog ground. Connect pin 40 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

OTHER CONSIDERATIONS (Continued)

*Current cancellation is a two-step process in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First, an auxiliary 13-bit R-2R Ladder is driven by the complement of the DAC's input code. Together the main and auxiliary ladders draw a continuous 3.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 12).

LAYOUT

Connections to pin 6 (I_{OUT}) on the HI–DAC16 are most critical for high speed performance. Output capacitance of the DAC is only 10pF, so a small additional capacitance will alter the op amp's stability and affect settling time. Connections to pin 6 should be short and few. Component leads should be short on the side connecting to pin 6.

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI–DAC16 also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 40 is sufficient, since supply current variations are small.

THERMAL EFFECTS

A consideration when using the DAC16 is Temperature Stability. In applications where full scale shift could be a problem, the use of a heat sink and/or a cooling fan is suggested. This will decrease the magnitude of the total variation by lowering the effective thermal resistance between the package and its environment. The device should be kept in a stable isothermal environment, and a warm-up time consistent with accuracy requirements should be provided.

SELECTING AN OPERATIONAL AMPLIFIER

The HI-DAC16 is a high resolution, high accuracy DAC. Many applications will require an op-amp used as a current-to-voltage converter at the DAC output. (Careful consideration should be given the choice of this amplifier as a poor selection can seriously degrade the inherent qualities of the DAC.)

The HA-5130 is an excellent choice to maintain high accuracy with an average Offset Drift of only 0.4 μV/°C leading to an error over temperature of 30 μV (0.0003% FSR for a 10V FS). Initial offset and bias current are 10 μV and 3nA respectively, while input noise current of 0.2pA/√Hz. Settling time is adequate for most audio applications. (11 μs typ. to 0.1%).

COMPOSITE AMPLIFIER

It is desirable at times to have an output amplifier which combines the qualities of those op-amps available to the designer. For instance one may wish to combine the excellent front-end characteristics of the HA-5130 with the speed of a device such as the HA-2540 (t_{settle} =250ns to 0.1%). In these instances there is the option of the composite amplifier. The basic configuration is shown in Figure 2.

COMPOSITE AMPLIFIER

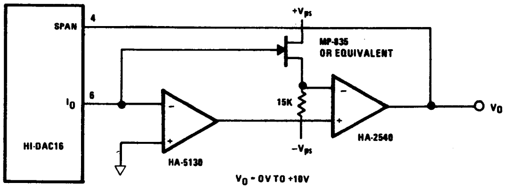


FIGURE 2

The composite amplifier may be used to achieve a compromise depending on the requirements of a design. Trade-offs in performance can be made and the following equations apply:

Offset; $V_{OFF} = \frac{V_{OFF2}}{A_{01}} + V_{OFF1}$

Bias; $I_{BIAS} = I_{BIAS2} + I_{BIAS1}$

Gain; $\frac{V_0}{V_1} = A_V(S) = A_{V2}(S)\ [1 + A_{V1}(S)]$

The amplifier A_2 should be of wide bandwidth and fast settling time.

DIE CHARACTERISTICS

Transistor Count		190
Die Size:		215 x 125 mils
Thermal Constants;	θ_{ja}	41°C/W
	θ_{jc}	11°C/W
Tie Substrate to:		Analog Ground
Process:		Bipolar - DI

*Current cancellation is a two-step process in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First, an auxiliary 13-bit R-2R Ladder is driven by the complement of the DAC's input code. Together the main and auxiliary ladders draw a continuous 3.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 12).

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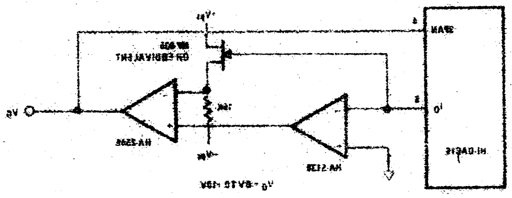

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Offset: $V_{OFF} = \frac{V_{OFF2}}{A_{V1}} + V_{OFF1}$

Bias: $I_{BIAS} = I_{BIAS1} + I_{BIAS2}$

Gain: $\frac{V_0}{V_1} = A_V(S) = A_{V1}(S)\,[1 + A_{V2}(S)]$

The amplifier A_V should be of wide bandwidth and fast settling time.

DIE CHARACTERISTICS

Transistor Count:		100
Die Size:		218 x 125 mils
Thermal Constants:	θ_{ja}	41°C/W
	θ_{jc}	11°C/W
Tie Substrate to:		Analog Ground
Process:		Bipolar - DI

Sample and Hold Amplifiers and Data Acquisition Front End

7

Product Index 7-2

Ordering Information 7-3

Standard Products Packaging Availability 7-3

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Product Information 7-5

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

[illegible]
HA-2420/2425 Fast Sample and Hold 7-10
HA-5320 High Speed Precision Monolithic Sample and Hold Amplifier 7-17
HA-5330 Very High Speed Precision Monolithic Sample and Hold Amplifier 7-24
HY-9590/91 Data Acquisition Front End Including: Multip[illegible] Hold Stages 7-28

Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H A 1 - 2420 - 2

PREFIX:
H (HARRIS)

FAMILY:
A — Analog
C — Communications
D — Digital
F — Filters
I — Interface
M — Memory
V — Analog, High Voltage
Y — Analog Hybrids

PACKAGE:
1 — Dual-In-Line, Ceramic
3 — Dual-In Line, Plastic
4 — Leadless Carriers (LCC)
4P — Plastic Leaded Carriers (PLCC)
5 — LCC Hybrid
7 — Mini-DIP, Ceramic
0 — Chip Form

PART NUMBER

TEMPERATURE:
1 — 0°C to +200°C ✱
2 — -55°C to +125°C
4 — -25°C to +85°C
5 — 0°C to +75°C
6 — 100% +25°C Probe (Dice Only)
7 — Dash-7 High Reliability Commercial Product. 0°C to +75°C
8 — Dash-8 Program
9 — -40°C to +85°C

✱ Special high temperature testing available on certain product types. Consult factory for availability.

Standard Products Packaging Availability

PACKAGE	PLASTIC DIP	CERAMIC DIP				SURFACE MOUNT LCC	SURFACE MOUNT PLCC
TEMPERATURE	-5	-2	-4	-5	-8	-8	-5
DEVICE NUMBER							
SAMPLE AND HOLD							
HA-2420		X			X	X	
HI-2425	X			X			X
HI-5320		X		X	X	X	
HI-5330		X	X	X	*	*	

* Available as MIL-STD-883 only.

Selection Guide

SAMPLE AND HOLD

Part Number	Features	Temp. Range			Package	Acquisition Time, (to 0.01%) Typ., 25°C	Charge Transfer Typ., 25°C	Aperture Time Typ., 25°C	Gain Bandwidth Product Typ., 25°C	Page
		-55°C to +125°C	0°C to +75°C	-40°C to +85°C						
HA-2420 HA-2425	Low Charge Transfer Low Droop Rate	X	X		14 Pin Cerdip, Epoxy DIP, LCC, PLCC	3.2μs	5pC	30ns	2.5MHz	7-10
HA-5320	High Speed Precision Complete-Includes Hold Capacitor	X	X		14 Pin Cerdip, LCC	1μs	0.1pC	25ns	2.0MHz	7-17
HA-5330	High Speed Precision Complete-Includes Hold Capacitor	X	X	X	14 Pin Cerdip, Com	0.5μs	0.05pC	20ns	4.5MHz	7-24

DATA ACQUISITION FRONT END

Part Number	Features	Temp. Range			Package	Acquisition Time, (to 0.01%) Typ., 25°C	Droop Rate (C_H INT.)	Gain Error Max.	Effective Aperture Delay	Aperture Uncertainty	CMRR	Page
		-55°C to +125°C	0°C to +75°C	-40°C to +85°C								
HY-9590	8-Channel Differential Mulitplexer, Programmable Gain Amplifier, Precison Sample/Hold	X	X	X	32 Pin Plastic/or Ceramic DIP	6μs	0.08μV/μs	0.01%	-25ns	0.3ns	70dB	7-28
HY-9591	16-Channel Single Ended Multiplexer, Programmable Gain Amplifier, Precision Sample/Hold	X	X	X	32 Pin Plastic/or Ceramic DIP	6μs	0.08μV/μs	0.01%	-25ns	0.3ns	70dB	7-28

HARRIS

HA-2420-1

High Temperature Sample and Hold Amplifier

FEATURES (T$_A$ = 200°C)

LOW DROOP RATE (C_H = 0.01μF)	22μV/μs
FAST ACQUISITION TIME (±0.01%)	3.2μs
HIGH SLEW RATE	7V/μs
WIDE BANDWIDTH	2.5MHz
LOW EFFECTIVE APERTURE DELAY TIME	30ns
TTL COMPATIBLE CONTROL INPUT	

APPLICATIONS

- GEOTHERMAL AND NUCLEAR INSTRUMENTATION
- OIL WELL LOGGING
- AUTOMOTIVE ENGINE MONITORING
- A TO D CONVERSION SYSTEMS
- D TO A DEGLITCHER
- AUTO ZERO SYSTEMS
- PEAK DETECTOR
- GATED OP AMP

DESCRIPTION

The HA-2420-1 is a monolithic sample-and-hold amplifier guaranteed to operate over the -55°C to +200°C temperature range. The circuit consists of a high performance operational amplifier in series with an ultra low leakage analog switch and a MOSFET input unity gain output buffer amplifier.

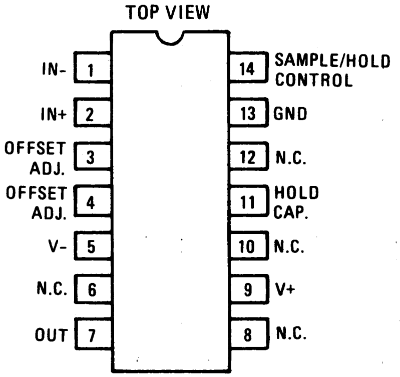
With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened, the output will remain at its last level.

Performance as a sample-and-hold at 200°C compares very favorably with other monolithic, hybrid and discrete circuits having lower temperature ranges. High slew rate, wide bandwidth, and low acquisition time provide an excellent dynamic response. The ability to operate at gains other than unity eliminate the need for an external scaling amplifier.

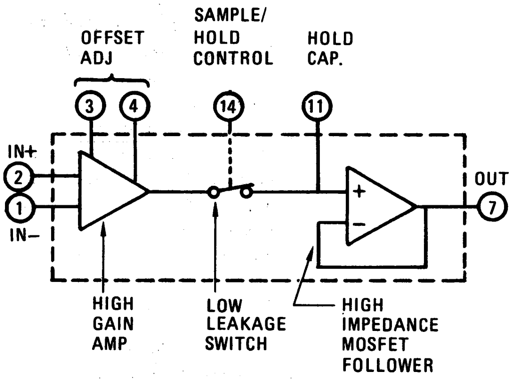
The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, multiplexed sample-and-holds, etc.

Power requirement is ± 15V. The package is a 14 pin ceramic DIP.

PINOUT


TOP VIEW
IN- 1
IN+ 2
OFFSET ADJ. 3
OFFSET ADJ. 4
V- 5
N.C. 6
OUT 7
14 SAMPLE/HOLD CONTROL
13 GND
12 N.C.
11 HOLD CAP.
10 N.C.
9 V+
8 N.C.

FUNCTIONAL DIAGRAM


OFFSET ADJ
SAMPLE/ HOLD CONTROL
HOLD CAP.
3
4
14
11
IN+
2
1
IN−
OUT
7
+
−
HIGH GAIN AMP
LOW LEAKAGE SWITCH
HIGH IMPEDANCE MOSFET FOLLOWER

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Internal Power Dissipation*	1500mW
Differential Input Voltage	±24V	Operating Temperature Range	$-55^{\circ}C \leqslant T_A \leqslant +200^{\circ}C$
Digital Input Voltage (Pin 14)	+8V, -15V	Storage Temperature Range	$-65^{\circ}C \leqslant T_A \leqslant +150^{\circ}C$
Output Current	Short Circuit Protected	*Derate 10.35mW/°C above 75°C	

ELECTRICAL CHARACTERISTICS

Test Conditions (Unless otherwise specified) $V_{SUPPLY} = \pm 15.0V$; $C_H = 1000pF$; Digital Input (Pin 14), $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold)

PARAMETER	TEMP	HA-2420-1 MIN	HA-2420-1 TYP	HA-2420-1 MAX	UNITS
INPUT CHARACTERISTICS					
*Offset Voltage	+25°C		2	4	mV
	Full		3	6	mV
*Bias Current	+25°C		50	200	nA
	Full			400	nA
*Offset Current	+25°C		10	50	nA
	Full			100	nA
Input Resistance	+25°C	5	10		MΩ
Common Mode Range	Full	±10			V
TRANSFER CHARACTERISTICS					
*Large Signal Voltage Gain (Note 1, 4)	Full	25K	50K		V/V
*Common Mode Rejection (Note 2)	Full	80	90		dB
Hold Mode Feedthrough Attenuation (Note 8)	+25°C		-76		dB
Gain Bandwidth Product (Note 3)	+25°C		2.5		MHz
OUTPUT CHARACTERISTICS					
*Output Voltage Swing (Note 1)	Full	±10			V
Output Current	+25°C	±15			mA
Full Power Bandwidth (Note 3, 4)	+25°C		100		kHz
Output Resistance (D.C.)	+25°C		.15		Ω
TRANSIENT RESPONSE					
Rise Time (Note 3, 5)	+25°C		50		ns
Overshoot (Note 3, 5)	+25°C		25		%
Slew Rate (Note 3, 6)	+25°C		7		V/μs
DIGITAL INPUT CHARACTERISTICS					
Digital Input Current (V_{IN} = 0V)	Full			0.8	mA
Digital Input Current (V_{IN} = +5.0V)	Full			20	μA
Digital Input Voltage (Low)	Full			0.8	V
Digital Input Voltage (High)	Full	2.0			V
SAMPLE/HOLD CHARACTERISTICS					
Acquisition Time to .1% 10V Step (Note 3)	+25°C		2.3		μs
Acquisition Time to .01% 10V Step (Note 3)	+25°C		3.2		μs
Aperture Time	+25°C		30		ns
Effective Aperture Delay Time	+25°C		30		ns
Aperture Uncertainty Time	+25°C		5		ns
*Drift Current (Note 3, 7)	+25°C		5	50	pA
	Full		220		nA
*Hold Step Error (Note 7)	+25°C		9	15	mV
POWER SUPPLY CHARACTERISTICS					
*Supply Current (+)	Full		5.5	7	mA
*Supply Current (-)	Full		4.5	6	mA
*Power Supply Rejection	Full	80	90		dB

NOTES:

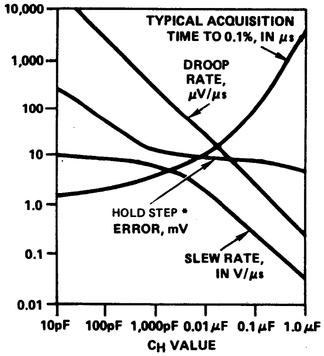
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10VDC$
3. $A_V = +1$, $R_L = 2k\Omega$, $C_L = 50pF$
4. $V_{OUT} = 20V$ peak-to-peak
5. $V_{OUT} = 200mV$ peak-to-peak
6. $V_{OUT} = 10.0V$ peak-to-peak
7. $V_{IN} = 0V$
8. $f_{IN} \leq 100kHz$

*100% Tested

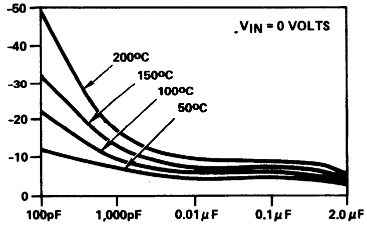
PERFORMANCE CURVES

V_{SUPPLY} = ± 15V, C_H = 1,000pF, T_A = +200°C, unless otherwise specified.

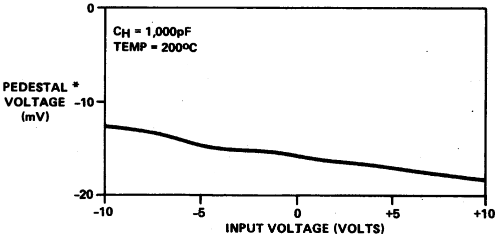
TYPICAL PERFORMANCE VS. HOLD CAPACITANCE



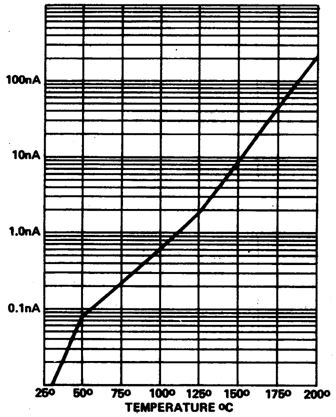
HOLD STEP VOLTAGE * VS. HOLD CAPACITANCE



HOLD STEP VOLTAGE * VS. INPUT VOLTAGE



DRIFT CURRENT VS. TEMPERATURE



*Hold step voltage is the output error following a switch from sample to hold.

APPLICATIONS

Operation of the HA-2420-1 at +200°C is similar to that of the -2 version at +125°C. Most of the maximum limits are the same, except for slight increases in supply and input bias currents, and a 55X increase in drift current. (Drift current is responsible for voltage droop error in the HOLD mode.) At high temperatures, a guard ring is essential, to counteract the increased flow of drift current from the hold capacitor. See Figure 2.

The components and materials external to this integrated circuit must carry a similar qualification for high temperature operation. TEFLON®* wire insulation and a TEFLON IC socket (if used) are recommended, along with TEFLON dielectric for the bypass and hold capacitors. In addition, the holding capacitor should have extremely high insulation resistance and low dielectric absorption.

Figure 1 shows a typical unity gain circuit, with Offset Zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420-1. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

For more applications, consult Harris Application Note 517, or factory applications group.

BASIC SAMPLE-AND-HOLD
(TOP VIEW)

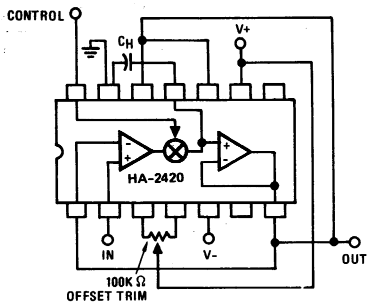


Figure 1

GUARD RING LAYOUT
(BOTTOM VIEW)

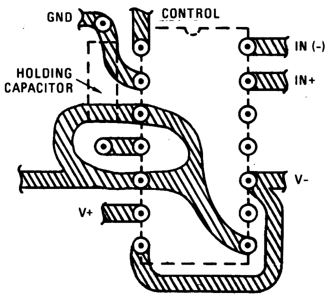


Figure 2

GLOSSARY OF TERMS

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ± 0.1% or ± 0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

EFFECTIVE APERTURE DELAY TIME (EADT):

The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

APERTURE UNCERTAINTY:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

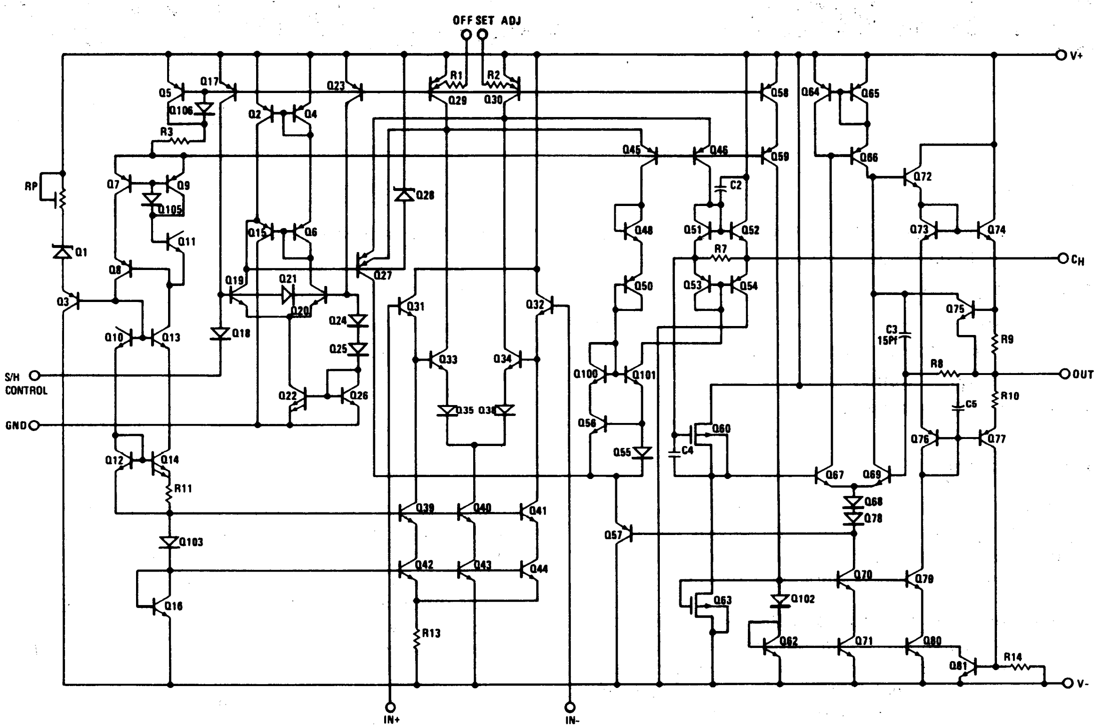
DRIFT CURRENT:

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D\ (pA) = C_H\ (pF) \times \frac{\Delta V}{\Delta T}\ (\text{Volts/sec})$$

*TEFLON is a registered trademark of Dupont Corporation

SCHEMATIC


OFFSET ADJ
V+
V-
CH
OUT
IN+
IN-
S/H CONTROL
GND
RP
R1
R2
R3
R7
R8
R9
R10
R11
R13
R14
C2
C3 15Pf
C4
C5
Q1
Q3
Q5
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q2
Q4
Q6
Q20
Q21
Q22
Q23
Q24
Q25
Q26
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Q67
Q68
Q69
Q70
Q71
Q72
Q73
Q74
Q75
Q76
Q77
Q78
Q79
Q80
Q81
Q100
Q101
Q102
Q103
Q105
Q106

DASH 1 PRODUCT FLOW

HARRIS SEMICONDUCTOR DASH 1 PRODUCT FLOW
100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND
①	Internal Visual	2010 Cond. B
②	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
③	Temperature Cycling	1010 Cond. C
④	Constant Acceleration	2001 Cond. E; Y1 plane
⑤	Seal: A Fine	1014 Cond. A or B
	B Gross	1014 Cond. C
⑥	Initial Electrical	Harris Specifications
⑦	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
⑧	Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
⑨	External Visual	2009 Sample Inspection
⑩	Lot Acceptance	Table I, Group A Elect. Tests
⑪	Final Electrical	Harris Specifications @ +200°C

HARRIS

HA-2420/25

Fast Sample and Hold

Features

- **Maximum Acquisition Time (10V Step to 0.1%) ......4μs (10V Step to 0.01%) 6μs**
- **Low Droop Rate (C_H = 1000pF) 5μV/ms**
- **Bandwidth 2.5MHz**
- **Low Effective Aperture Delay Time 30ns**
- **TTL Compatible Control Input**
- **±12V to ±15V Operation**

Applications

- **12-Bit Data Acquisition**
- **D to A Deglitcher**
- **Auto Zero Systems**
- **Peak Detector**
- **Gated Op Amp**

Description

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and MOSFET input unity gain amplifier.

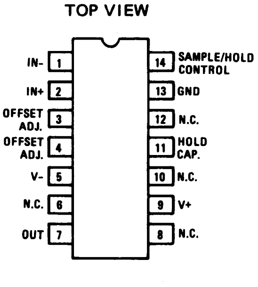
With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

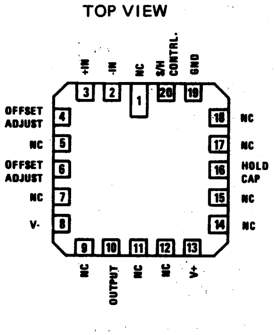
The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note number 517.

The MIL-STD-883 and the High Temperature (200°C) data sheets for this device are available on request.

Pinouts

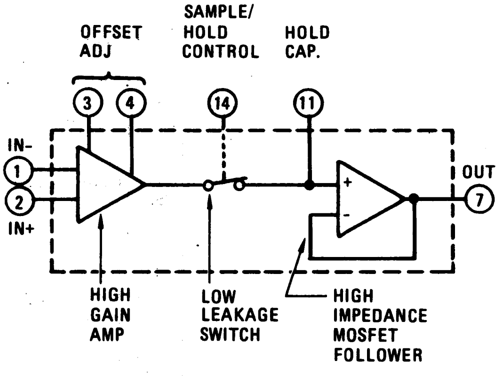

TOP VIEW
IN- 1
IN+ 2
OFFSET ADJ. 3
OFFSET ADJ. 4
V- 5
N.C. 6
OUT 7
14 SAMPLE/HOLD CONTROL
13 GND
12 N.C.
11 HOLD CAP.
10 N.C.
9 V+
8 N.C.

14 PIN DIP


TOP VIEW
+IN 3
-IN 2
NC 1
S/H CONTRL. 20
GND 19
OFFSET ADJUST 4
NC 5
OFFSET ADJUST 6
NC 7
V- 8
NC 18
NC 17
HOLD CAP 16
NC 15
NC 14
NC 9
OUTPUT 10
NC 11
NC 12
V+ 13

LEADLESS CHIP CARRIER (LCC) PACKAGE

Functional Diagram


SAMPLE/ HOLD CONTROL
OFFSET ADJ
HOLD CAP.
3
4
14
11
IN- 1
IN+ 2
+
-
OUT 7
HIGH GAIN AMP
LOW LEAKAGE SWITCH
HIGH IMPEDANCE MOSFET FOLLOWER

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals	40V
Differential Input Voltage	±24V
Digital Input Voltage (Pin 14)	+8V, -15V
Output Current	Short Circuit Protected
Power Dissipation	855mW (Note 7)

Operating Temperature Range

HA-2420-2/8	$-55^oC \leq T_A \leq +125^oC$
HA-2425-5	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

Electrical Characteristics

Test Conditions (Unless otherwise specified) $V_{SUPPLY} = \pm 15.0V$; $C_H = 1000pF$; Digital Input (Pin 14), $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold)

PARAMETER	TEMP	HA-2420-2 MIN	HA-2420-2 TYP	HA-2420-2 MAX	HA-2425-5 MIN	HA-2425-5 TYP	HA-2425-5 MAX	UNITS
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10			±10			V
*Offset Voltage	+25°C		2	4		3	6	mV
	Full		3	6		4	8	mV
*Bias Current	+25°C		40	200		40	200	nA
	Full			400			400	nA
*Offset Current	+25°C		10	50		10	50	nA
	Full			100			100	nA
Input Resistance	+25°C	5	10		5	10		MΩ
Common Mode Range	Full	±10			±10			V
TRANSFER CHARACTERISTICS								
*Large Signal Voltage Gain (Note 1, 4)	Full	25K	50K		25K	50K		V/V
*Common Mode Rejection (Note 2)	Full	-80	-90		-74	-90		dB
Hold Mode Feedthrough Attenuation (Note 9)	Full		-76			-76		dB
Gain Bandwidth Product (Note 3)	+25°C		2.5			2.5		MHz
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 1)	Full	±10			±10			V
Output Current	+25°C	±15			±15			mA
Full Power Bandwidth (Note 3, 4)	+25°C		100			100		kHz
Output Resistance (D.C.)	+25°C		.15			.15		Ω
TRANSIENT RESPONSE								
Rise Time (Note 3, 5)	+25°C		75	100		75	100	ns
Overshoot (Note 3, 5)	+25°C		25	40		25	40	%
Slew Rate (Note 3, 6)	+25°C	3.5	5		3.5	5		V/μs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full			-0.8			-0.8	mA
Digital Input Current ($V_{IN} = +5.0V$)	Full			20			20	μA
Digital Input Voltage (Low)	Full			0.8			0.8	V
Digital Input Voltage (High)	Full	2.0			2.0			V
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time to .1% 10V Step (Note 3)	+25°C		2.3	4		2.3	4	μs
Acquisition Time to .01% 10V Step (Note 3)	+25°C		3.2	6		3.2	6	μs
Aperture Time (Note 10)	+25°C		30			30		ns
Effective Aperture Delay Time	+25°C		30			30		ns
Aperture Uncertainty	+25°C		5			5		ns
*Drift Current (Note 3, 8)	+25°C		5			5		pA
	Full		1.8	4.0		0.1	1.0	nA
*Hold Step Error (Note 8)	+25°C		10	20		10	20	mV
POWER SUPPLY CHARACTERISTICS								
*Supply Current (+)	+25°C		3.5	5.5		3.5	5.5	mA
*Supply Current (-)	+25°C		2.5	3.5		2.5	3.5	mA
*Power Supply Rejection	Full	-80	-90		-74	-90		dB

NOTES:

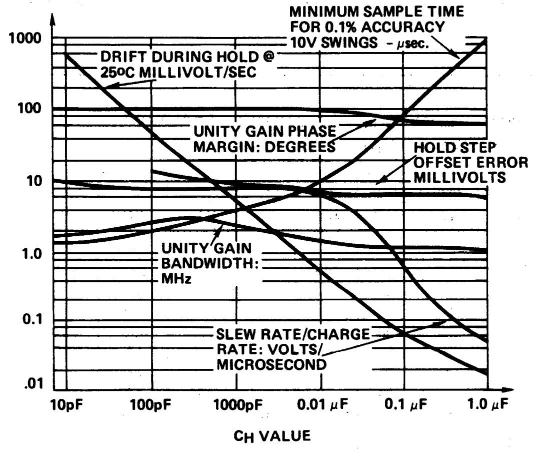
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10VDC$
3. $A_V = \pm 1, RL = 2k\Omega, C_L = 50pF$
4. $V_{OUT} = 20V$ peak-to-peak
5. $V_{OUT} = 200mV$ peak-to-peak
6. $V_{OUT} = 10.0V$ peak-to-peak
7. Derate Power Dissipation by 8.5mW/°C above +75°C Ambient temperature
8. $V_{IN} = 0V$
9. $f_{IN} \leqslant 100kHz$
10. Derived from computer simulation only; not tested.

*100% Tested for DASH 8

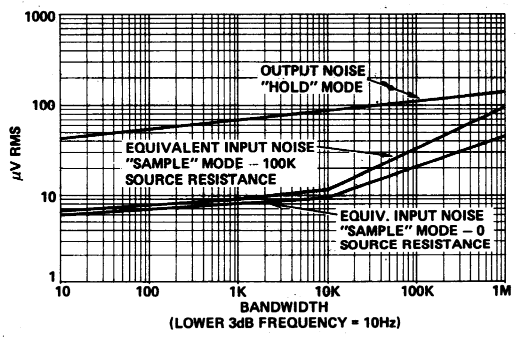
PERFORMANCE CURVES

V_{SUPPLY} = ±15VDC, T_A = +25°C, C_H = 1,000pF Unless Otherwise Specified

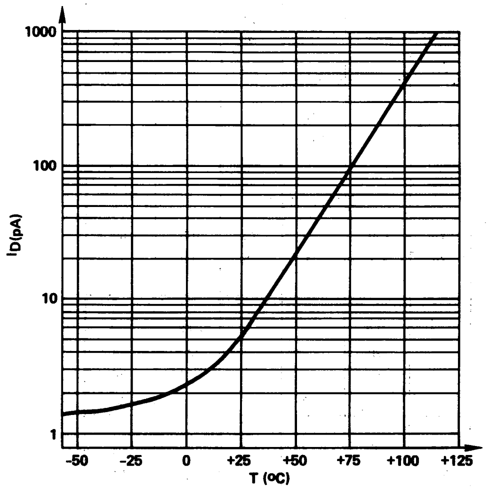
TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR



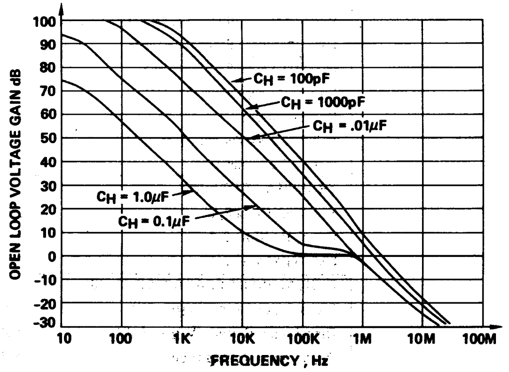
BROADBAND NOISE CHARACTERISTICS



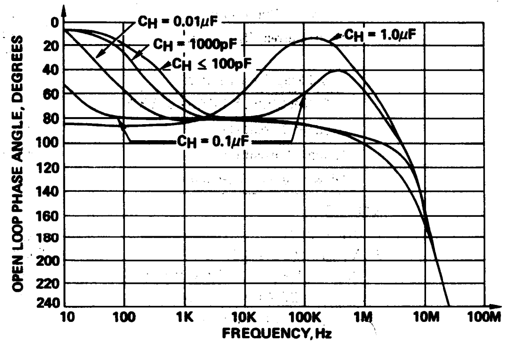
DRIFT CURRENT VS. TEMPERATURE



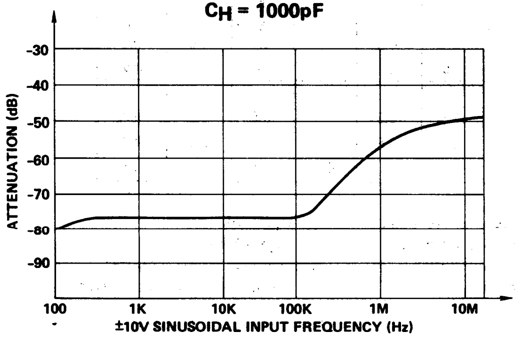
OPEN LOOP FREQUENCY RESPONSE



OPEN LOOP PHASE RESPONSE



HOLD MODE FEED THROUGH ATTENUATION CH = 1000pF



OFFSET AND GAIN ADJUSTMENT

HOLD STEP VS. INPUT VOLTAGE

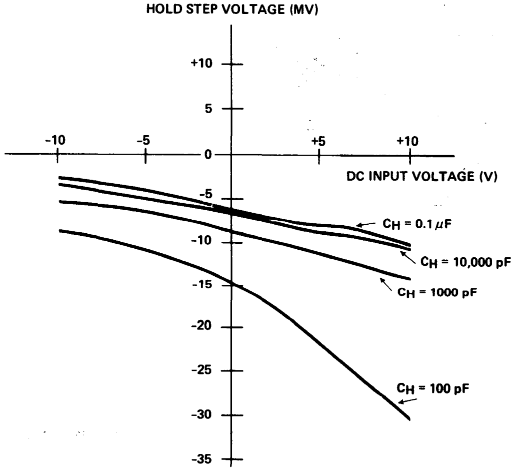


Figure 1

OFFSET ADJUSTMENT

The offset voltage of the HA-2420/2425 may be adjusted using a 100kΩ trim pot, as shown in Figure 6. The recommended adjustment procedure is:

1. Apply zero volts to the sample-and-hold input, and a square wave to the S/H control.
2. Adjust the trim pot for zero volts output in the hold mode.

GAIN ADJUSTMENT

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (C_H = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage ($V_{-10\ NOMINAL}$). Adjust the trim pot for an output hold voltage of
$$\frac{(V_{-10\ NOMINAL}) + (-10V)}{2}$$

INVERTING CONFIGURATION

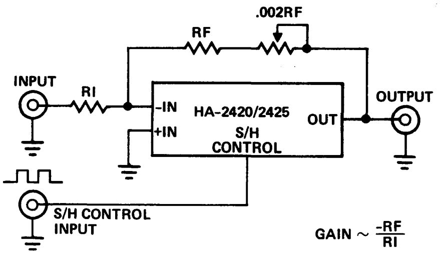

.002RF
RF
INPUT
RI
-IN
+IN
HA-2420/2425
S/H
CONTROL
OUT
OUTPUT
S/H CONTROL
INPUT
GAIN ~ -RF/RI

Figure 2

NONINVERTING CONFIGURATION

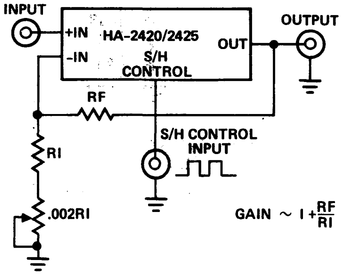

INPUT
+IN
-IN
HA-2420/2425
S/H
CONTROL
OUT
OUTPUT
RF
RI
.002RI
S/H CONTROL
INPUT
GAIN ~ 1 + RF/RI

Figure 3

TEST CIRCUITS

HOLD STEP ERROR AND DRIFT CURRENT

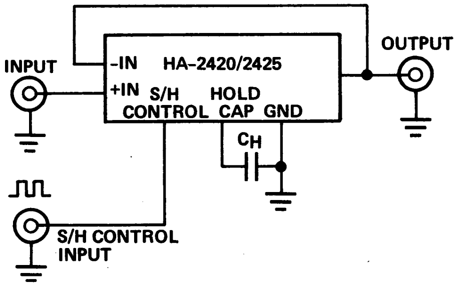
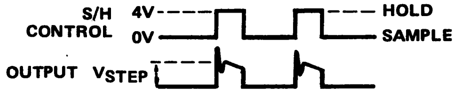

INPUT
-IN
HA-2420/2425
+IN
S/H CONTROL
HOLD CAP
GND
OUTPUT
C_H
S/H CONTROL INPUT

Figure 4

HOLD STEP ERROR TEST

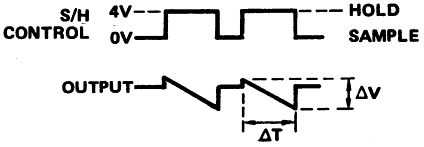
1. With a D.C. input voltage, observe the following waveforms:


S/H CONTROL
4V
0V
HOLD
SAMPLE
OUTPUT
V_{STEP}

2. Set rise/fall times of S/H Control to approximately 20 ns.

DRIFT CURRENT TEST

1. With a D.C. input voltage, observe the following waveforms:


S/H CONTROL
4V
0V
HOLD
SAMPLE
OUTPUT
ΔV
ΔT

2. Measure the slope of the output during hold, $\Delta V/\Delta t$, and compute drift current from: $I_D = C_H \Delta V/\Delta t$

HOLD MODE FEEDTHROUGH ATTENUATION

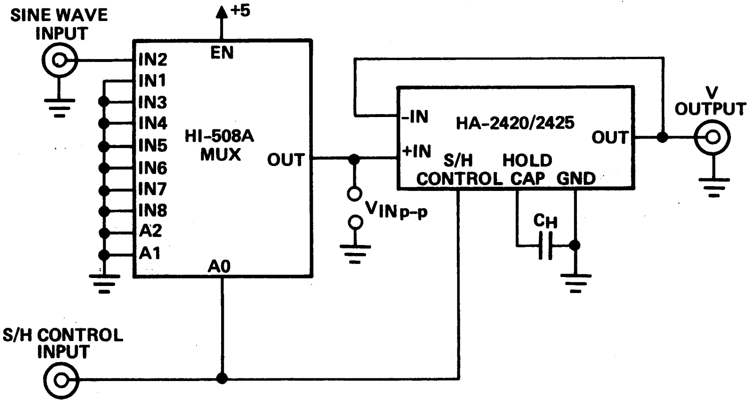

SINE WAVE INPUT
+5
EN
IN2
IN1
IN3
IN4
IN5
IN6
IN7
IN8
A2
A1
A0
HI-508A MUX
OUT
$V_{IN\,p\text{-}p}$
-IN
HA-2420/2425
+IN
OUT
S/H CONTROL
HOLD CAP
GND
C_H
V OUTPUT
S/H CONTROL INPUT

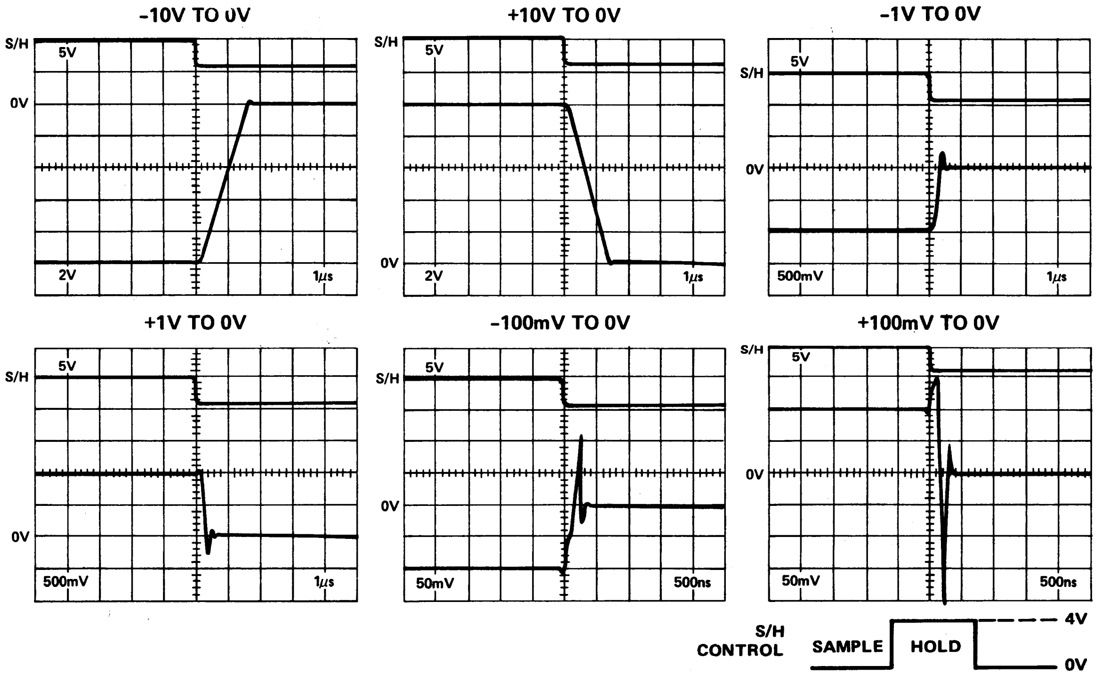
Figure 5

NOTE: Compute hold mode feedthrough attenuation from the formula:

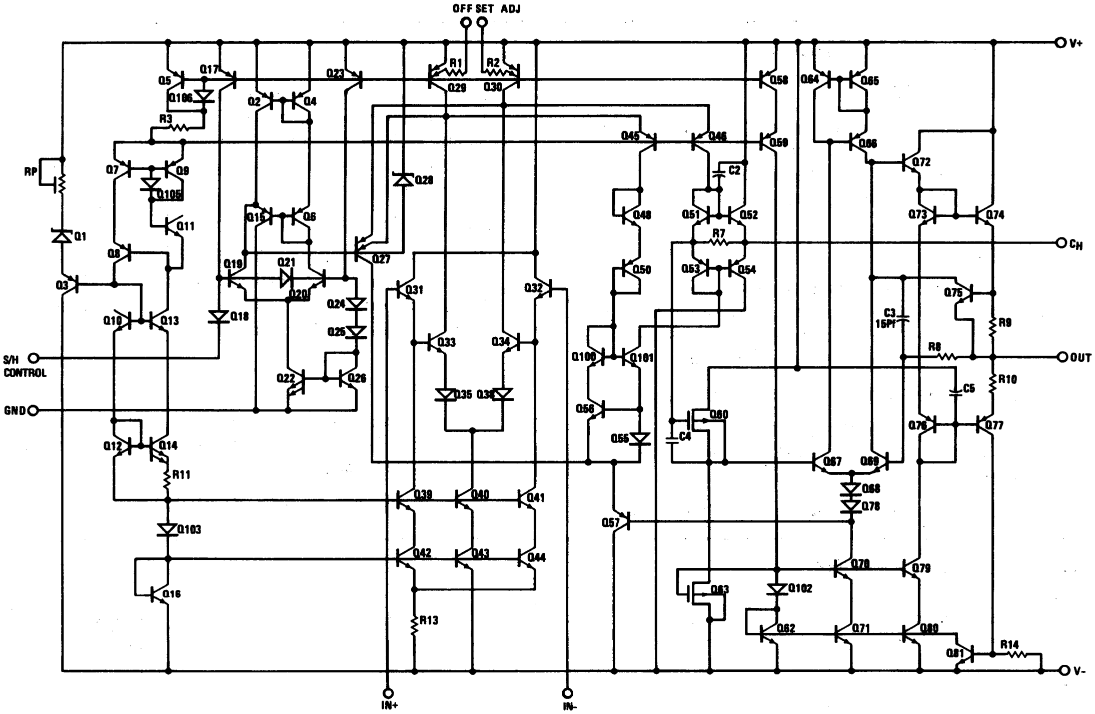
$$\text{Feedthrough Attenuation} = 20 \text{ Log } \frac{V_{OUT}\text{ HOLD}}{V_{IN}\text{HOLD}}$$

Where V_{OUT} HOLD = Peak-Peak value of output sinewave during the hold mode.

ACQUISITION TIMES (C$_H$ = 1000pF)



SCHEMATIC


OFF SET ADJ
V+
V-
C$_H$
OUT
S/H CONTROL
GND
IN+
IN-
RP
R1
R2
R3
R7
R8
R9
R10
R11
R13
R14
C2
C3 15PF
C4
C5
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
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Q100
Q101
Q102
Q103
Q105
Q106

APPLICATIONS

BASIC SAMPLE-AND-HOLD (TOP VIEW)

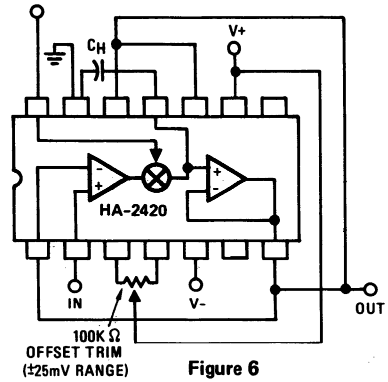


Figure 6

GUARD RING LAYOUT (BOTTOM VIEW)

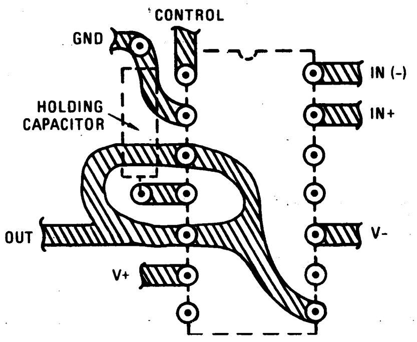


Figure 7

NOTES:

1. Figure 6 shows a typical unity gain circuit, with Offset Zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

2. The method used to reduce leakage paths on the P.C. board and the device package is shown in Figure 7. This guard ring is recommended to minimize the drift during hold mode.

3. The holding capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), Teflon, or Parlene types are recommended.

For more applications, consult Harris Application Note 517, or factory applications group.

GLOSSARY OF TERMS

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

EFFECTIVE APERTURE DELAY TIME (EADT):

The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

APERTURE UNCERTAINTY:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DRIFT CURRENT

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D(pA) = C_H\ (pF) \times \frac{\Delta V}{\Delta T}\ (\text{Volts/sec})$$

DIE CHARACTERISTICS

Transistor Count:		78	Tie Substrate to:	$-V_{SUPPLY}$
Die Dimensions:		97 x 61 mils	Process:	Bipolar, Dielectric Isolation
Thermal Constants:	θ_{ja}	117°C/W		
	θ_{jc}	46°C/W		

HARRIS

HA-5320

High Speed Precision Monolithic Sample and Hold Amplifier

FEATURES

GAIN, dc	2 x 10^6 V/V
ACQUISITION TIME	1.0 µs (0.01%)
DROOP RATE	0.08 µV/µs (25°C) 17 µV/µs (FULL TEMP)
APERTURE TIME	25ns
HOLD STEP ERROR (SEE GLOSSARY)	1.0 mV
INTERNAL HOLD CAPACITOR	
FULLY DIFFERENTIAL INPUT	
TTL COMPATIBLE	

APPLICATIONS

- PRECISION DATA ACQUISITION SYSTEMS
- D/A CONVERTER DEGLITCHING
- AUTO-ZERO CIRCUITS
- PEAK DETECTORS

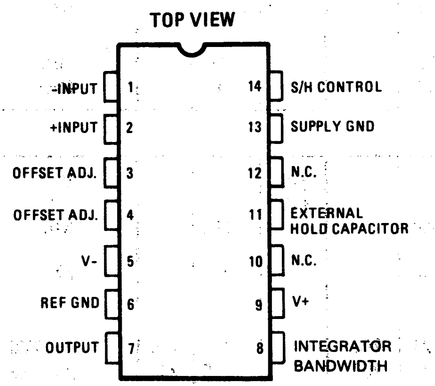
DESCRIPTION

The HA-5320 was designed for use in precision, high speed data acquisition systems.

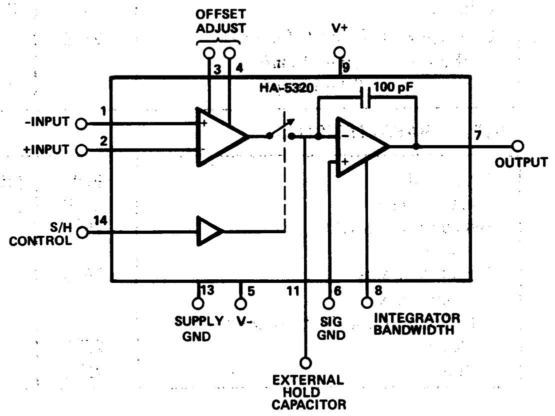
The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

This monolithic device is manufactured using the Harris Dielectric Isolation Process, minimizing stray capacitance and eliminating SCR's. This allows higher speed and latch-free operation. The HA-5320 is available in a ceramic 14-pin DIP. For further information, please see Application Note number 538.

PINOUT


TOP VIEW
-INPUT 1
+INPUT 2
OFFSET ADJ. 3
OFFSET ADJ. 4
V- 5
REF GND 6
OUTPUT 7
14 S/H CONTROL
13 SUPPLY GND
12 N.C.
11 EXTERNAL HOLD CAPACITOR
10 N.C.
9 V+
8 INTEGRATOR BANDWIDTH

FUNCTIONAL DIAGRAM


OFFSET ADJUST
V+
3
4
9
HA-5320
100 pF
-INPUT 1
+INPUT 2
7
OUTPUT
S/H CONTROL 14
13
5
11
6
8
SUPPLY GND
V-
SIG GND
INTEGRATOR BANDWIDTH
EXTERNAL HOLD CAPACITOR

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V^+ and V^- terminals	40V
Differential Input Voltage	±24V
Digital Input Voltage (Pin 14)	+8V, −15V
Output Current, continuous	±20mA (Note 2)

Internal Power Dissipation *	1.33W
Operating Temperature Range	
HA-5320-2/8	$-55^{\circ}C \leq TA \leq +125^{\circ}C$
HA-5320-5	$0^{\circ}C \leq TA \leq +75^{\circ}C$
Storage Temperature Range	$-65^{\circ}C \leq TA \leq +150^{\circ}C$

* Derate 13. 3mW/°C above 75°C

ELECTRICAL CHARACTERISTICS Test Conditions (unless otherwise specified)

V Supply = ±15V; C_H - Internal; Digital Input (Pin 14), V_{IL} = +0.8V (sample), V_{AH} = +2.0V (hold).

PARAMETER	TEMP	HA-5320-2/8			HA-5320-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10			±10			V
Input Resistance	25°C	1	5		1	5		MΩ
Input Capacitance	25°C			3			3	pF
Offset Voltage	25°C		0.2			0.5		mV
	Full			2.0			1.5	mV
Bias Current	25°C		70	200		100	300	nA
	Full			200			300	nA
Offset Current	25°C		30	100		30	300	nA
	Full			100			300	nA
Common Mode Range	Full	±10			±10			V
CMRR (Note 3)	25°C	80	90		72	90		dB
Offset Voltage T.C.	Full		5	15		5	20	μV/°C
TRANSFER CHARACTERISTICS								
Gain, dC	25°C	10^6	2×10^6		3×10^5	2×10^6		V/V
Gain Bandwidth Product (A_V = +1)	25°C							
(Note 5) CH = 100pF			2.0			2.0		MHz
CH = 1000pF			.18			.18		MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10			±10			V
Output Current	25°C	±10			±10			mA
Full Power Bandwidth (Note 4)	25°C		600			600		KHz
Output Resistance (Hold mode)	25°C		1.0			1.0		Ω
Total Output Noise, DC to 10 MHz								
Sample	25°C		125	200		125	200	μV RMS
Hold	25°C		125	200		125	200	μV RMS

SPECIFICATIONS (continued)

PARAMETER	TEMP	HA-5320-2/8 MIN	HA-5320-2/8 TYP	HA-5320-2/8 MAX	HA -5320-5 MIN	HA -5320-5 TYP	HA -5320-5 MAX	UNITS
TRANSIENT RESPONSE								
Rise Time (Note 5)	25°C		100			100		nS
Overshoot (Note 5)	25°C		15			15		%
Slew Rate (Note 6)	25°C		45			45		V/µs
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{IH}	Full	2.0			2.0			V
Input Voltage (Low), V_{IL}	Full			0.8			0.8	V
Input Current (V_{IL} = 0V)	Full			4			4	µA
Input Current (V_{IH} = +5V)	Full			0.1			0.1	µA
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time (.1%) (Note 7)	25°C		0.8	1.2		0.8	1.2	µS
Acquisition Time (.01%) (Note 7)	25°C		1.0	1.5		1.0	1.5	µS
Aperture Time (Note 8)	25°C		25			25		ns
Effective Aperture Delay Time (See Glossary)	25°C	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty	25°C		0.3			0.3		ns
Droop Rate	25°C		0.08	0.5		0.08	0.5	µV/us
Droop Rate	Full		17	100		1.2	100	µV/us
Drift Current (Note 9)	25°C		8	50		8	50	pA
Drift Current (Note 9)	Full		1.7	10		0.12	10	nA
Charge Transfer (Note 9)	25°C		0.1	0.5		0.1	0.5	pC
Hold Mode Settling Time (.01%)	Full		165	350		165	350	ns
Hold Mode Feedthrough ($10V_{p-p}$, 100kHz)	Full		2			2		mV
POWER SUPPLY CHARACTERISTICS								
Positive Supply Current (Note 10)	25°C		11	13		11	13	mA
Negative Supply Current (Note 10)	25°C		−11	−13		−11	−13	mA
Power Supply Rejection V^+	Full	80			80			dB
(Note 11) V^-	Full	65			65			dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below +20mA.
3. $V_{CM} = \pm 5V$ DC
4. $V_O = 20V_{p-p}$; $R_L = 2K\Omega$; $C_L = 50pF$; unattenuated output.
5. $V_O = 200mV_{p-p}$; $R_L = 2K\Omega$; $C_L = 50pF$.
6. $V_O = 20V$ Step; $R_L = 2K\Omega$; $C_L = 50pF$.
7. $V_O = 10V$ Step; $R_L = 2K\Omega$; $C_L = 50pF$.
8. Derived from computer simulation only; not tested.
9. $V_{IN} = 0V$, $V_{IH} = +3.5V$, $t_r < 20ns$ (V_{IL} to V_{IH})
10. Specified for a zero differential input voltage between pins 1 and 2. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ± 28mA at 20V.
11. Based on a one volt delta in each supply, ie. 15V ± 0.5V DC.

APPLYING THE HA-5320

The HA-5320 has the uncommitted differential inputs of an op amp, allowing the Sample/Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas. (Note, however, these apply to a different Sample/Hold amplifier. The HA-5320 is not necessarily plug-in compatible.)

LAYOUT

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (.01 to 0.1μF, ceramic) should be provided from each power supply terminal to the Power Gnd terminal on pin 13.

The ideal ground connections are pin 6 (Reference Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

HOLD CAPACITOR

The HA-5320 includes a 100 pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Characteristics section is based on this internal capacitor). Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

If an external hold capacitor C_H is used, then a noise bandwidth capacitor of value $0.1C_H$ should be connected from pin 8 to ground. Exact value and type are not critical.

The hold capacitor C_H should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to +85°C. Teflon®* and glass dielectrics offer good performance to +125°C and above.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

---

* Teflon is a registered trademark of Dupont Corporation.

APPLICATIONS

Figure 1 shows the HA-5320 connected as a unity gain noninverting amplifier – its most widely used configuration. As an input device for a fast successive – approximation A/D converter, it offers the highest throughput rate available from a monolithic IC sample/hold amplifier. Also, the HA-5320's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12 bit accurate output from the converter.

The application may call for an external hold capacitor C_H as shown. As mentioned earlier, $0.1C_H$ is then recommended at pin 8 to reduce output noise in the Hold mode.

The HA-5320 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

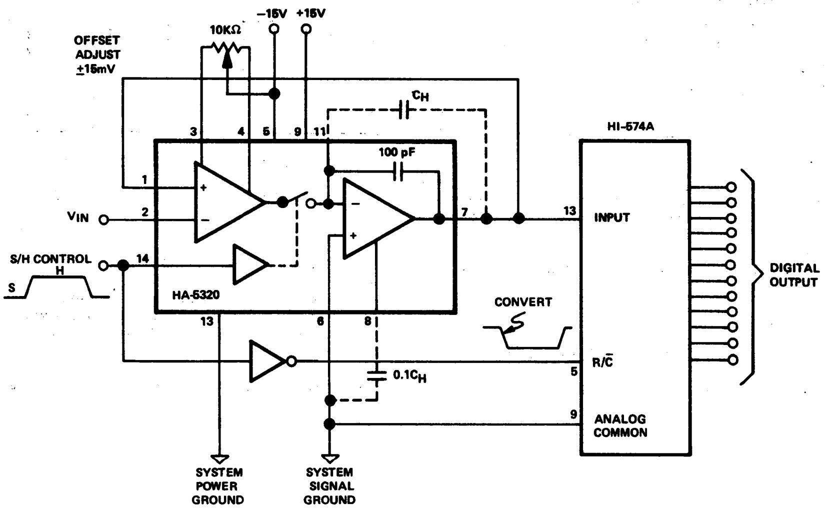


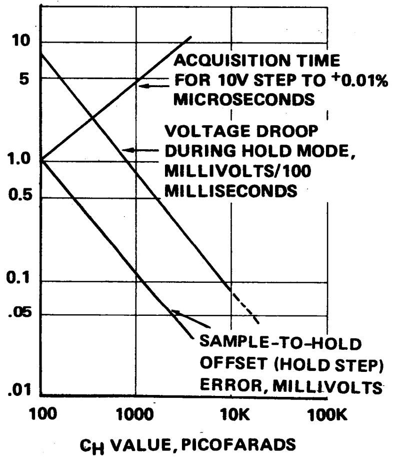
Figure 1

TYPICAL HA-5320 CONNECTIONS; NONINVERTING UNITY GAIN MODE.

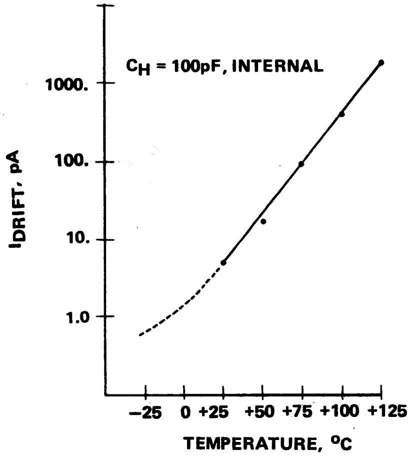
PERFORMANCE CURVES

V_{SUPPLY} = ±15VDC

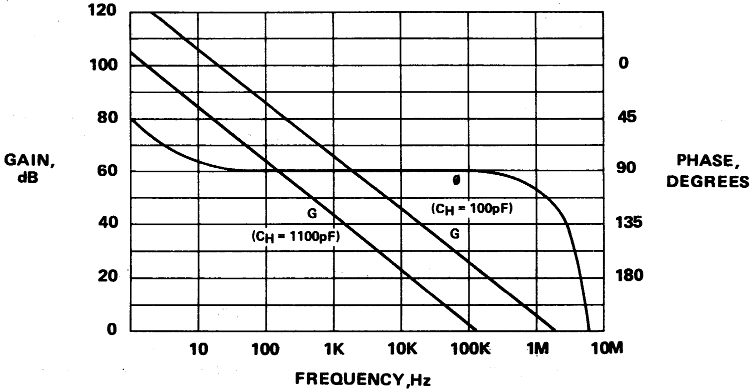
TYPICAL SAMPLE AND HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR



DRIFT CURRENT VS. TEMPERATURE

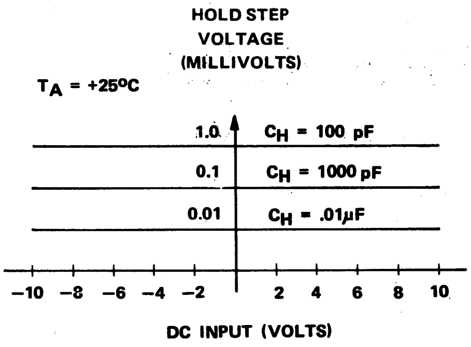


OPEN LOOP GAIN AND PHASE RESPONSE

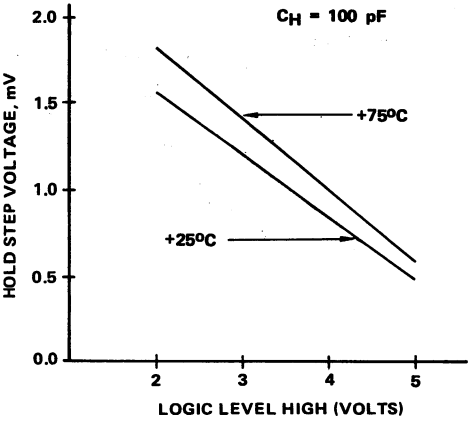


TYPICAL SAMPLE-TO-HOLD OFFSET (HOLD STEP) ERROR

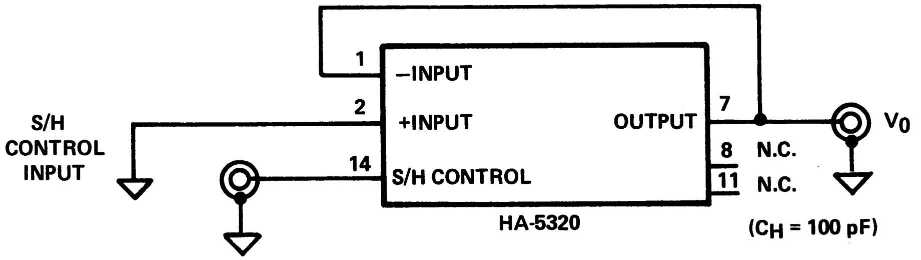
HOLD STEP vs. INPUT VOLTAGE



HOLD STEP vs. LOGIC (V_{IH}) VOLTAGE

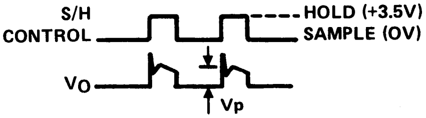


CHARGE TRANSFER AND DRIFT CURRENT


S/H
CONTROL
INPUT
1
2
14
−INPUT
+INPUT
S/H CONTROL
OUTPUT
7
8
11
N.C.
N.C.
V_O
HA-5320
(C_H = 100 pF)

CHARGE TRANSFER TEST

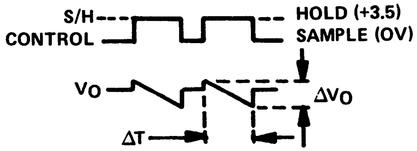
1. Observe the "hold step" voltage Vp:


S/H
CONTROL
HOLD (+3.5V)
SAMPLE (OV)
V_O
Vp

2. Compute charge transfer: $Q = V_P C_H$

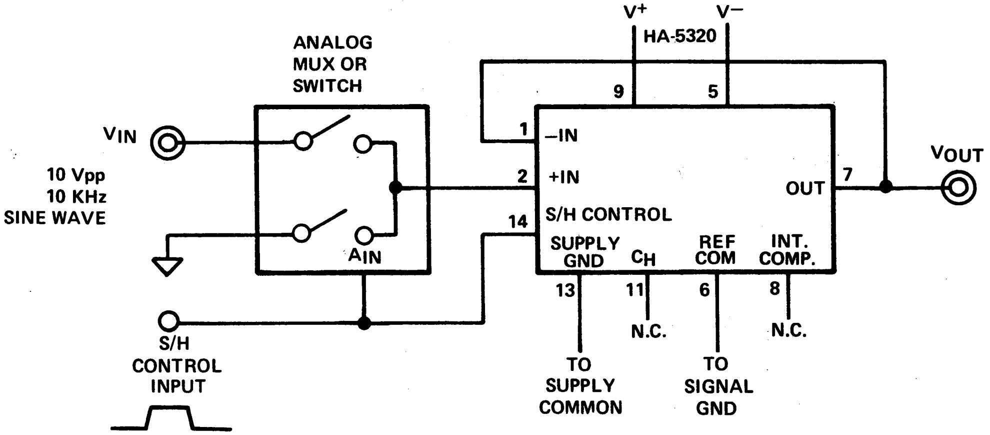
DRIFT CURRENT TEST

1. Observe the voltage "droop", $\Delta V_O/\Delta T$:


S/H
CONTROL
HOLD (+3.5)
SAMPLE (OV)
V_O
ΔV_O
ΔT

2. Measure the slope of the output during hold, $\Delta V_O/\Delta T$, and compute drift current: $I_D = C_H \Delta V_O/\Delta t$.

HOLD MODE FEED THROUGH ATTENUATION


ANALOG
MUX OR
SWITCH
V_{IN}
10 Vpp
10 KHz
SINE WAVE
A_{IN}
S/H
CONTROL
INPUT
V+
V−
HA-5320
9
5
1
2
14
−IN
+IN
S/H CONTROL
OUT
7
V_{OUT}
SUPPLY
GND
C_H
REF
COM
INT.
COMP.
13
11
6
8
N.C.
N.C.
TO
SUPPLY
COMMON
TO
SIGNAL
GND

Feedthrough in dB = $20 \log \frac{V_{OUT}}{V_{IN}}$ where:

V_{OUT} = Volts pp, Hold Mode,
V_{IN} = Volts pp.

GLOSSARY OF TERMS

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

CHARGE TRANSFER:

The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the Hold mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where:

$$\text{Charge Transfer (pC)} = C_H\ \text{(pF)} \times \text{Offset Error (V)}$$

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

HOLD STEP ERROR:

Hold Step Error is the output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{HOLD STEP (V)} = \frac{\text{CHARGE TRANSFER (pC)}}{\text{HOLD CAPACITANCE (pF)}}$$

See Performance Curves.

EFFECTIVE APERTURE DELAY TIME (EADT):

The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

APERTURE UNCERTAINTY:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DRIFT CURRENT:

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D\ \text{(pA)} = C_H\ \text{(pF)} \times \frac{\Delta V}{\Delta T}\ \text{(Volts/sec)}$$

DIE CHARACTERISTICS

Transistor Count:		175
Die Dimensions:		90.2 x 143.7 mils
Thermal Constants:	θ_{ja}	75°C/W
	θ_{jc}	15°C/W
Tie Substrate to		$-V_{Supply}$
Process:		Bipolar Dielectric Isolation

HARRIS

HA-5330

Very High Speed Precision Monolithic Sample and Hold Amplifier

Features

Very Fast Acquisition	**350ns (0.1%)** **500ns (0.01%)**
Low Droop Rate	**0.01µV/µs**
Very Low Offset	**0.2mV**
High Slew Rate	**90 V/µs**
Wide Supply Range	**±11V to ±18V**
Internal Hold Capacitor	
Fully Differential Input	
TTL/CMOS Compatible	

Applications

- **Precision Data Acquisition Systems**
- **D/A Converter Deglitching**
- **Auto-Zero Circuits**
- **Peak Detectors**

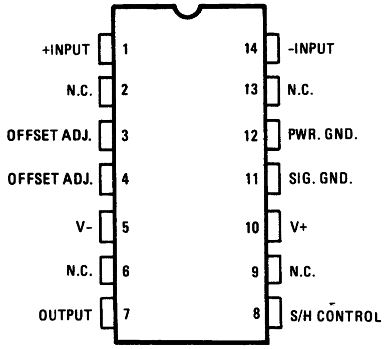
Description

The HA-5330 is a very fast sample and hold amplifier designed primarily for use with high speed A/D converters. It utilizes the Harris Dielectric Isolation process to achieve a 500ns acquisition time to 12-bit accuracy and a droop rate of 0.01 µV/µs. The circuit consists of an input transconductance amplifier capable of producing large amounts of charging current, a low leakage analog switch, and an integrating output stage which includes a 90pF hold capacitor.

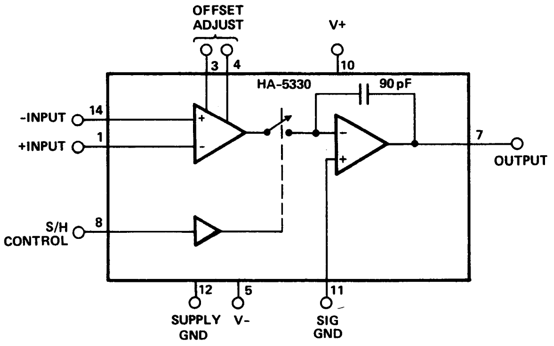
The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of V_{in}. Charge injection is held to a low value by compensation circuits and, if necessary, the resulting 0.5mV hold step error can be adjusted to zero via the Offset Adjust terminals. Compensation is also used to minimize leakage currents which cause voltage droop in the Hold mode.

The HA-5330 will operate at reduced supply voltages (to ±11V) with a reduced signal range. This monolithic device is available in a ceramic 14-pin DIP. The MIL-STD-883 data sheet for this device is available on request.

Pinout


+INPUT
1
N.C.
2
OFFSET ADJ.
3
OFFSET ADJ.
4
V-
5
N.C.
6
OUTPUT
7
14
-INPUT
13
N.C.
12
PWR. GND.
11
SIG. GND.
10
V+
9
N.C.
8
S/H CONTROL

Functional Diagram


OFFSET
ADJUST
3
4
V+
10
HA-5330
90 pF
-INPUT
14
+INPUT
1
+
-
-
+
7
OUTPUT
S/H
CONTROL
8
12
5
11
SUPPLY
GND
V-
SIG
GND

Absolute Maximum Ratings (Note 1)

Voltage between V+ and PWR/SIG GND . . . . +20V
Voltage between V− and PWR/SIG GND . . . . −20V
Voltage between PWR GND and SIG GND . . . . ±2.0V
Differential Input Voltage . . . . ±24V
Voltage between S/H Control and PWR/SIG GND . . . . +8V, −6V
Output Current, continuous . . . . ±17mA (Note 2)
Total Power Dissipation* 1.33W

* Derate 13.3 mW/°C above 75°C

Operating Temperature Range

HA-5330-2 . . . . −55°C to +125°C
HA-5330-4 . . . . −25°C to +85°C
HA-5330-5 . . . . 0°C to +75°C
Storage Temperature . . . . −65°C to +150°C

Electrical Characteristics

Test Conditions (unless otherwise specified) V Supply = ±15V ±3%; Digital Input (Pin 8): V_{IL} = +0.8V (sample): V_{IH} = +2.0V (hold); SIG GND = PWR GND

		HA-5330 -2, -4			HA-5330 -5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10			±10			V
Input Resistance (Note 3)	25°C	5	15		5	15		MΩ
Input Capacitance	25°C		3			3		pF
Offset Voltage	25°C		0.2			0.2		mV
	Full			2.0			1.5	mV
Offset Voltage T.C.	Full		1	10		1	10	µV/°C
Bias Current	25°C		±20			±20		nA
	Full			±500			±300	nA
Offset Current	25°C		20			20		nA
	Full			500			300	nA
Common Mode Range	Full	±10			±10			V
CMRR (Note 4)	Full	86	100		86	100		dB
TRANSFER CHARACTERISTICS								
Gain, DC	Full	2X10^6	2X10^7		2X10^6	2X10^7		V/V
Gain Bandwidth Product (Note 5)	25°C		4.5			4.5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10			±10			V
Output Current	Full	±10			±10			mA
Full Power Bandwidth (Note 6)	25°C		1.6			1.6		MHz
Output Resistance								
(Hold Mode)	25°C		0.2			0.2		Ω
(Sample Mode)	25°C		10^{-5}	0.001		10^{-5}	0.001	Ω
Total Output Noise, DC to 4.0 MHz								
Sample	25°C		230			230		µV RMS
Hold	25°C		190			190		µV RMS

HA-5330 Specifications

		HA-5330 -2, -4			HA-5330 -5			
PARAMETER	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSIENT RESPONSE								
Rise Time (Note 5)	25°C		70			70		ns
Overshoot (Note 5)	25°C		10			10		%
Slew Rate (Note 7)	25°C		90			90		V/µS
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{IH}	Full	2.0			2.0			V
Input Voltage (Low), V_{IL}	Full			0.8			0.8	V
Input Current ($V_{IL} = 0V$)	Full		10	40		10	40	µA
Input Current ($V_{IH} = +5V$)	Full		10	40		10	40	µA
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time (Note 8)								
(0.1%)	25°C		350			350		ns
	Full			500			500	ns
(0.01%)	25°C		500			500		ns
	Full			900			900	ns
Aperture Time (Note 3)	25°C		20			20		ns
Effective Aperture Delay Time (See Glossary)	25°C	−50	−25	0	−50	−25	0	ns
Aperture Uncertainty	25°C		0.1			0.1		ns
Droop Rate (Note 9)	25°C		0.01			0.01		µV/µs
	Full			100			10	µV/µs
Hold Step Error (Note 10)	25°C		0.5			0.5		mV
Hold Mode Settling Time (0.01%)	25°C		100	200		100	200	ns
Hold Mode Feedthrough $20V_{pp}$, 100 kHz	Full		−88			−88		dB
POWER SUPPLY CHARACTERISTICS								
Positive Supply Current	Full		18	22		18	24	mA
Negative Supply Current	Full		19	23		19	25	mA
Power Supply Rejection V+,V− (Note 11)	Full	86	100		86	100		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below ±17mA.
3. Derived from computer simulation only; not tested.
4. $V_{CM} = \pm 10V$ DC
5. $V_O = 200mV_{p\text{-}p}$; $R_L = 2K$; $C_L = 50pF$.
6. Full power bandwidth based on slew rate measurement using

$$FPBW = \frac{\text{SLEW RATE}}{2\pi V_{peak}}$$

7. $V_O = 20V$ Step; $R_L = 2K$; $C_L = 50pF$.
8. $V_O = 10V$ Step; $R_L = 2K$; $C_L = 50pF$.
9. This parameter is measured at ambient temperature extremes in a high speed test environment. Consequently, steady state heating effects from internal power dissipation are not included.
10. $V_{IN} = 0V$; $V_{IH} = +3.5V$; $t_r = 20ns$ (V_{IL} to V_{IH}). See graph.
11. Based on a three volt delta in each supply, ie. 15V = ±1.5V DC.

Applying the HA-5330

The HA-5330 has the uncommitted differential inputs of an op amp, allowing the Sample/Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas. (Note, however, these apply to a different Sample/Hold amplifier. The HA-5330 is not plug-in compatible.)

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (.01 to 0.1μF, ceramic) should be provided from each power supply terminal to the Power Gnd terminal on pin 12.

Applications

The HA-5330 is configured as a unity gain noninverting amplifier by simply connecting the output (pin 7) to the inverting input (pin 14). As an input device for a fast successive - approximation A/D converter, it offers an extremely high throughput rate. Also, the HA-5330's pedestal error is adjustable to zero by using an Offset Adjust potentiometer (10K to 50K) center tapped to V−.

The ideal ground connections are pin 11 (Signal Ground) directly to the system Signal Ground (Analog Ground), and pin 12 (Power Ground) directly to the system Supply Common.

Hold Capacitor

The HA-5330 includes a 90pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Characteristics section is based on this internal capacitor).

Output Stage

The HA-5330 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momenatry short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

Glossary of Terms

Acquisition Time:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

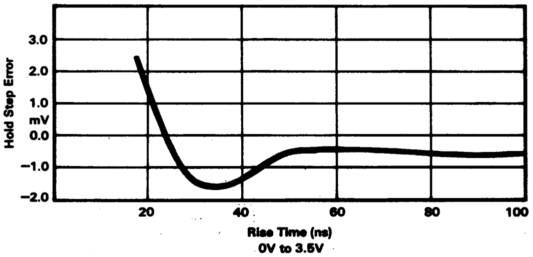
Aperture Time:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Hold Step Error:

Hold step error is the output shift due to charge transfer from the sample to the hold mode. It is also referred to as "offset step" or "pedistal error".

Hold Step Error vs S/H Control Rise Time



Effective Aperture Delay Time (EADT):

The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occured before the Hold command.

Aperture Uncertainty:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

HARRIS

HY-9590/91

ADVANCED

Data Acquisition Front End

Features

- Pin Compatible with HI-5900/5901
- Input Overvoltage Protection
- 12-Bit Accuracy
- Software Controlled Gain and Input Channel Selection
- Inverting Gains of -1, -2, -4 and -8
- 0.01% Gain Error
- Zero Offset Adjustment
- Output Track/Hold Amplifier
- 6μs Acquisition Time (typ.)
- Track/Hold Droop Rate.................................... 0.08μV/μs
- Low Power Dissipation 580mW
- Compact 32 Pin DIP
- Available Temperature Ranges:
  - Commercial (-5) .... 0°C to +75°C
  - Industrial (-9)..................................... -40°C to +85°C
  - Military (-2) .... -55°C to +125°C

Applications

- High Performance Multi-Channel Acquisition
- Status Monitoring Systems
- Process Control Systems
- Instrumentation
- High Reliability DAS's
- Military Systems

HY-9590 Features

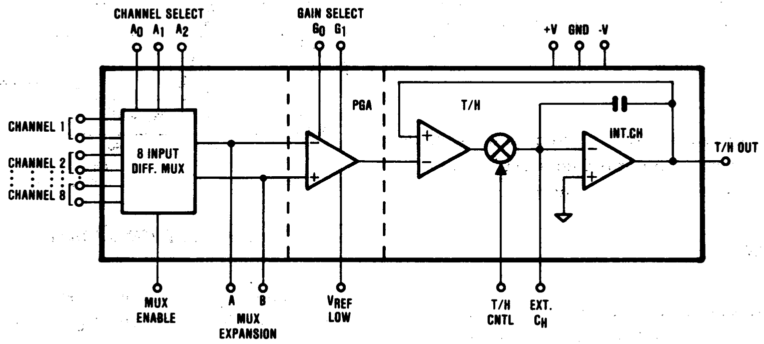
- 8 Differential Input Channels

HY-9591 Features

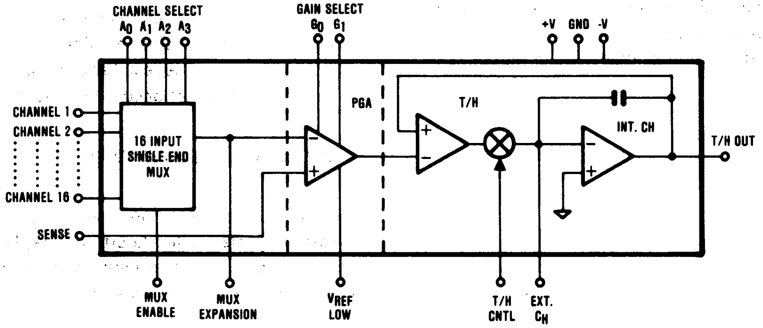
- 16 Pseudo-Differential/Single Ended Input Channels

Functional Diagrams

HY-9590


CHANNEL SELECT
A0 A1 A2
GAIN SELECT
G0 G1
+V GND -V
CHANNEL 1
CHANNEL 2
CHANNEL 8
8 INPUT DIFF. MUX
PGA
T/H
INT.CH
T/H OUT
MUX ENABLE
A B
MUX EXPANSION
VREF LOW
T/H CNTL
EXT. CH

HY-9591


CHANNEL SELECT
A0 A1 A2 A3
GAIN SELECT
G0 G1
+V GND -V
CHANNEL 1
CHANNEL 2
CHANNEL 16
SENSE
16 INPUT SINGLE END MUX
PGA
T/H
INT. CH
T/H OUT
MUX ENABLE
MUX EXPANSION
VREF LOW
T/H CNTL
EXT. CH

Description

The HY-9590 and the HY-9591 are data acquisition front end subsystems which can be used to interface multiple sensors to an Analog-to-Digital Converter (ADC) for computer processing. Both products combine an analog input Multiplexer (MUX), a Programmable Gain Instrumentation Amplifier (PGA), and a Track-and-Hold (T/H) amplifier. Adding a timing circuit and one ADC yields a complete data acquisition system.

The HY-9590 provides eight pairs of multiplexed differential inputs.

The HY-9591 has sixteen single-ended or pseudo differential channels of multiplexed inputs.

Both devices provide input fault protection. Input channel expansion can be easily implemented with external multiplexers. Both input lines of the instrumentation (PGA) amplifier are buffered by high-quality non-inverting amplifiers. These buffers isolate each line from external source impedances, preserving the high CMRR of the amplifier block. Also, the buffers provide a high input impedance for each channel.

The PGA, which includes an op amp, a laser trimmed monolithic resistor network, and a four channel differential multiplexer, offers precision inverting gain values of -1, -2, -4, and -8. The voltage gain is selected by a two bit digital word. The output of the PGA drives the Track-and-Hold amplifier, and the ground side of the PGA is isolated by a buffer amplifier to further enhance the CMRR.

The output Track/Hold amplifier is a monolithic device, internally connected for non-inverting unity gain. In the "track" mode, it operates as a high performance buffer amplifier. With the internal 100pF holding capacitor (INT C_H), the T/H has an effective aperture delay time (EADT) of -25ns. (See 1986 Harris Analog Data Book, page 7-23 for definition of EADT). External capacitance can be added to reduce droop rate and pedestal error at the expense of increased acquisition time.

The electrical differences between the HI-5900/5901 and the pin compatible HY-9590/91 are summarized below:

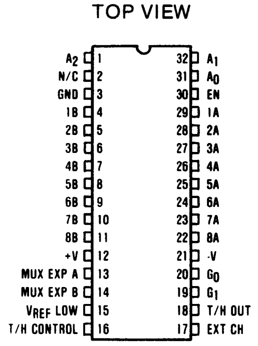
Differences Between HI-590X and HY-959X

PARAMETER	HI-5900/01	HY-9590/91
External Hold Capacitor	Required	Optional, 100pF supplied
	Tied From C_H Pin to GND	Tied From C_H Pin to T/H OUTPUT

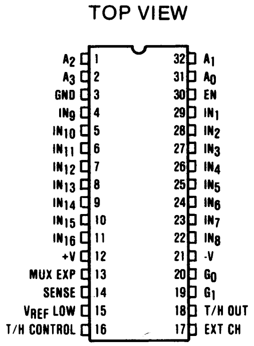
If a HY-9590/91 is intended to replace a HI-5900/01, the external hold capacitor must be either: (a) disconnected from pin 17, or (b) disconnected from ground and re-connected to pin 18 (T/H OUT). It should be noted that by using only the internal 100pF hold capacitor, the HY-9590/91 outperforms the HI-5900/01 using the standard 1000pF capacitor in pedestal error and aperture uncertainty.

The HY-9590/91 accepts the standard ±10V input range. Power requirements are ±15V with typical dissipation of 580mW. All models are packaged in a 32 pin plastic DIP with 600 mil row centers, except military temperature parts, which use a ceramic package.

Pinouts

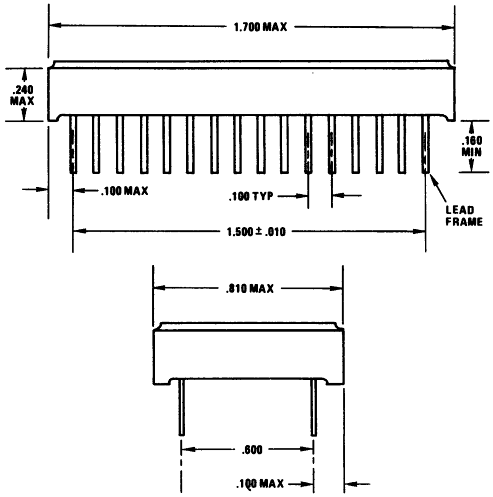

TOP VIEW
A2 1
N/C 2
GND 3
1B 4
2B 5
3B 6
4B 7
5B 8
6B 9
7B 10
8B 11
+V 12
MUX EXP A 13
MUX EXP B 14
VREF LOW 15
T/H CONTROL 16
17 EXT CH
18 T/H OUT
19 G1
20 G0
21 -V
22 8A
23 7A
24 6A
25 5A
26 4A
27 3A
28 2A
29 1A
30 EN
31 A0
32 A1

HY-9590


TOP VIEW
A2 1
A3 2
GND 3
IN9 4
IN10 5
IN11 6
IN12 7
IN13 8
IN14 9
IN15 10
IN16 11
+V 12
MUX EXP 13
SENSE 14
VREF LOW 15
T/H CONTROL 16
17 EXT CH
18 T/H OUT
19 G1
20 G0
21 -V
22 IN8
23 IN7
24 IN6
25 IN5
26 IN4
27 IN3
28 IN2
29 IN1
30 EN
31 A0
32 A1

HY-9591

Package


1.700 MAX
.240 MAX
.160 MIN
.100 MAX
.100 TYP
LEAD FRAME
1.500 ± .010
.810 MAX
.600
.100 MAX

Description

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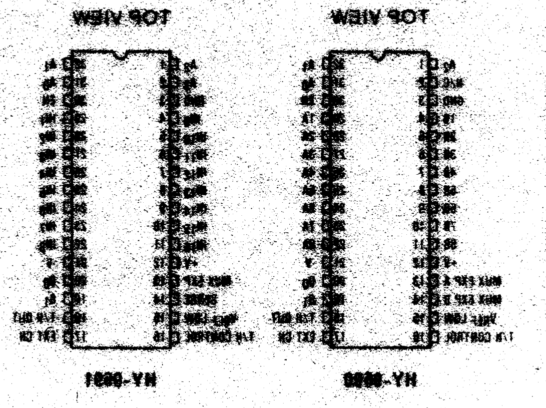
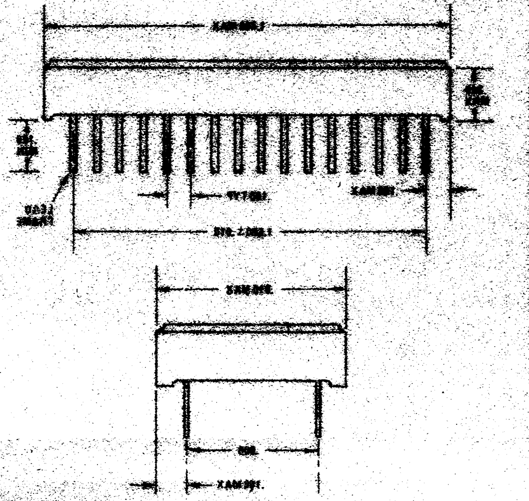
Pinouts



Package



ANALOG

Telecommunications

8

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Ordering Information 8-3

Standard Products Packaging Availability 8-3

Glossary of Telecom Terms 8-4

Telecom Line Card Glossary 8-5

Product Information 8-7

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

HC-5502A
HC-5504 Subscriber Line Interface Circuit (SLIC) 8-12
HC-5508/09 Subscriber Line Interface Circuit (SLIC) 8-17
HC-5510/5511 Monolithic CODECs 8-24
HC-5512/5512A PCM Monolithic Filters 8-33
HC-5512C PCM or CVSD Monolithic Filter 8-40
HC-5512D PCM Monolithic Filter Military T[illegible] 8-48
HC-5552/53/54/57 Monolithic Combo Family 8-57
HC-55536 All-Digital Continuously Variable Slope Delta Demodulator (CVSD) Decode Only 8-68
HC-55564 All-Digital Continuously Variable Slope Delta Modulator (CVSD) 8-72
HF-10 Universal Active Filter 8-79
HC-5560 Transcoder 8-82
HC-5580 Trunk Subscriber Line Interface Circuit (TSLIC) 8-83
HC-5581 DAA Subscriber Line Interface Circuit (DAASLIC) 8-84
HC-5590 Digital Line Transceiver 8-85
HC-5572 2400/1200/600/300 BPS Modem 8-86

Ordering Information

HARRIS PRODUCT CODE EXAMPLE

H C 3 - 5502A - 5

PREFIX:
H (HARRIS)

FAMILY:
A — Analog
C — Communications
D — Digital
F — Filters
I — Interface
M — Memory
V — Analog, High Voltage
Y — Analog Hybrids

PACKAGE:
1 — Dual-In-Line, Ceramic
2 — Metal Can
3 — Dual-In Line, Plastic
4 — Leadless Carriers
5 — LCC Hybrid
7 — Mini-DIP, Ceramic
0 — Chip Form

PART NUMBER

TEMPERATURE:
1 — 0°C to +200°C ✱
2 — -55°C to +125°C
4 — -25°C to +85°C
5 — 0°C to +75°C
6 — 100% +25°C Probe (Dice Only)
7 — Dash-7 High Reliability Commercial Product. 0°C to +75°C
8 — Dash-8 Program HA2-2520-8 (Example only)
9 — -40°C to +85°C

✱ Special high temperature testing available on certain product types. Consult factory for availability.

Standard Products Packaging Availability

PACKAGE	PLASTIC DIP 3-		CERAMIC DIP 1-					SURFACE MOUNT LCC 4-	SURFACE MOUNT PLCC 4P-
TEMPERATURE	-5	-7	-2	-5	-7	-8	-9	-8	-5
DEVICE NUMBER									
TELECOM									
HC-5502A	X	X		X	X		X		X
HC-5504	X	X		X	X		X		X
HC-5508	X								
HC-5509									X
HC-5510				X					
HC-5511				X					
HC-5512				X	X				
HC-5512A				X	X				
HC-5512C				X	X				
HC-5512D			X			X		X	
HC-55536				X					
HC-55564			X	X	X	X	X	X	
HC-5560	X								
HF-0010			X	X	X	X	X		

Glossary of Telecom Terms

BORSCHT: Acronym for functions provided by a subscriber line interface circuit. Includes Battery feed, Overvoltage protection, Ringing, Supervision, Coding, Hybrid and Test functions.

CHIP POWER DOWN: Ability to minimize device power dissipation by shutting down majority of power consuming circuitry, putting the device in an "idle" state. Not to be confused with Power Denial, which minimizes power dissipation across the 2w loop.

DC/DC CONVERTER: Converts one DC voltage to another. Commonly used in transmission equipment where different DC voltages are required throughout a system.

FAULT CURRENTS: These are loop currents that flow during loop fault conditions, i.e., shorts in the line. Integrated on the SLIC is a fault current limit circuit which protects the SLIC from excessive power.

FREQUENCY RESPONSE: A measure of the variation of the transmission performance of the SLIC with respect to frequency variations.

IDLE CHANNEL NOISE (ICN): Noise measurements must characterize the annoyance to a user of unwanted signals. ICN is a measure of these unwanted signals under idle (no signal) channel conditions.

INSERTION LOSS OR TRANS HYBRID GAIN VARIATION: Simply the gain or loss of a signal through the SLIC from 2w to 4w and from 4w to 2w.

LEVEL LINEARITY OR GAIN TRACKING: A measure of the linearity of gain over a range of signal levels at a particular frequency. (Dynamic range usually +3dBm to -55dBm).

LINE POLARITY REVERSAL: Refers to 2w side tip and ring lines. Tip lines normally more positive with respect to the ring line. Reverse polarity is used for signaling purposes on trunk lines.

LONGITUDINAL CURRENT REJECTION: Ability of SLIC to suppress currents induced in the subscriber loop by power lines, antennae, etc.

LOOP CURRENT LIMIT: This is the maximum current the SLIC will allow in the subscriber loop. It is controlled by sensing loop current across the feed resistors, and adjusting the DC bias voltage at ring feed accordingly.

LOW FREQUENCY LONGITUDINAL BALANCE: Measure of degree of match of tip to ground and ring to ground impedance in the presence of large longitudinal currents at power line frequencies (50, 60 Hz).

OVERLOAD LEVEL: Upper limit of the SLICs dynamic range where speech signals just start to clip. This parameter sets the maximum speech power level the device can handle.

PROGRAMMABLE DC FEED: Ability to control the tip feed and ring feed output DC bias voltages that establish loop current.

PSRR: Measures the SLICs ability to reject noise in the power supply. SLIC must not allow the noise to couple into the speech paths.

SURGE PROTECTION: Adequate protection of the SLIC must be provided against lightning, low frequency induction, and power contact surges. The combination of split feed resistors, a diode bridge and ability of the feed amplifiers to reject longitudinal currents afford adequate protection to the SLIC.

TRANS HYBRID LOSS: A measure of the SLICs ability to separate the bidirectional speech transmission path into distinct transmit and receive paths on the 4w side.

2W LONGITUDINAL BALANCE: A measure of the degree of balance of tip to ground and ring to ground. Mismatches result in degradation of longitudinal current suppression in on-hook and off-hook conditions.

Telecom Line Card Glossary

RING RELAY: Allows switching of AC ringing signal from ring generator to drive subscriber telephone ringer via tip or ring side.

RING RELAY DRIVER: SLIC output to drive ring relay coil.

SNUBBER NETWORK: RC network across ring relay contacts to reduce effects of inductive kickbacks to SLIC.

DC ISOLATION CAPACITOR: Blocks DC loop current from transformer.

ZENER DIODE: Secondary protection for RX and TX amplifiers.

AC HYBRID TRANSFORMER: Provides 2wire-4wire and 4wire-2wire conversion of voice signals.

BALANCING NETWORK: Provides 2wire line impedance matching and transhybrid balance.

DC FEED RESISTORS: Four 150Ω resistors that provide 600Ω of 2wire impedance and provide sense mechanism for SLIC to detect switch hook, ground key and ring trip. Also provides some high voltage protection to SLIC by dividing in half any voltage transient.

TX/RX AMPLIFIERS: Amplifies voice signal lost in hybrid transformer. Also provides impedance conversion from 2wire-4wire and 4wire-2wire.

SUPERVISION NETWORK: Monitors SLICs switch hook, ringtrip, and ground key detection functions, and flags controller.

CONTROLLER: Stores ring command, ring trip, switch hook information, etc., until system CPU or line circuit can react.

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HARRIS

HC-5502A

SLIC
Subsciber Line Interface Circuit

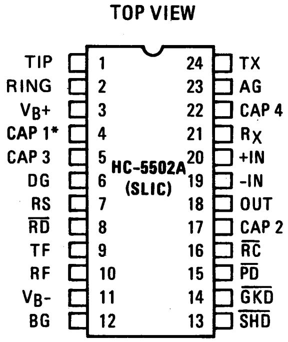
FEATURES

- MONOLITHIC INTEGRATED DEVICE
- DI HIGH VOLTAGE PROCESS
- COMPATIBLE WITH WORLDWIDE PBX PERFORMANCE REQUIREMENTS
- CONTROLLED SUPPLY OF BATTERY FEED CURRENT FOR SHORT LOOPS
- INTERNAL RING RELAY DRIVER
- LOW POWER CONSUMPTION DURING STANDBY
- SWITCH HOOK, GROUND KEY AND RING TRIP DETECTION FUNCTIONS
- SELECTIVE DENIAL OF POWER TO SUBSCRIBER LOOPS

APPLICATIONS

- SOLID STATE LINE INTERFACE CIRCUIT FOR ANALOG AND DIGITAL PBX SYSTEMS
- DIRECT INWARD DIAL (DID) TRUNKS
- VOICE MESSAGING PBX's

PINOUT


TOP VIEW
TIP 1
RING 2
VB+ 3
CAP 1* 4
CAP 3 5
DG 6
RS 7
RD 8
TF 9
RF 10
VB- 11
BG 12
HC-5502A
(SLIC)
24 TX
23 AG
22 CAP 4
21 RX
20 +IN
19 -IN
18 OUT
17 CAP 2
16 RC
15 PD
14 GKD
13 SHD

*Optional

DESCRIPTION

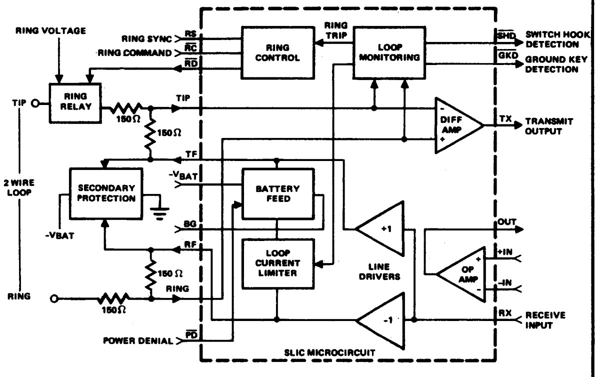
The HARRIS SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique HARRIS dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

The HARRIS SLIC is ideally suited for the design of new digital PBX systems, by eliminating bulky hybrid transformers.

SLIC is available in either a 24 pin dual-in-line plastic or ceramic package. The SLIC is also available as unpackaged die.

FUNCTIONAL DIAGRAM


RING VOLTAGE
RING SYNC
RS
RING COMMAND
RC
RD
RING CONTROL
RING TRIP
LOOP MONITORING
SHD
SWITCH HOOK DETECTION
GKD
GROUND KEY DETECTION
TIP
RING RELAY
150Ω
150Ω
TIP
DIFF AMP
TX
TRANSMIT OUTPUT
TF
2 WIRE LOOP
SECONDARY PROTECTION
-VBAT
-VBAT
BATTERY FEED
BG
RF
LOOP CURRENT LIMITER
+1
LINE DRIVERS
OUT
OP AMP
+IN
-IN
150Ω
RING
RING
150Ω
-1
RX
RECEIVE INPUT
POWER DENIAL
PD
SLIC MICROCIRCUIT

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum Continuous Supply Voltages	($V_{B}-$)	-60 to +.5 Volts
	($V_{B}+$)	-.5 to +15 Volts
	($V_{B}+ - V_{B}-$)	75 Volts
Operating Ambient Temperaure Range	(T_A)	0°C to +75°C
Storage Temperature Range (R_{SRG})		-40°C to +85°C
Thermal Resistance ($\theta_{J\text{-}A}$) (Plastic)		60°C/W
Thermal Resistance ($\theta_{J\text{-}A}$) (Ceramic)		61°C/W

RECOMMENDED OPERATING CONDITIONS

Positive Supply Voltage ($V_{B}+$)	10.8 to 13.2 Volts
Negative Supply Voltage ($V_{B}-$)	-42 to -58 Volts
Minimum High Level Logic Input Voltage	2.4 Volts
Maximum Low Level Logic Input Voltage	0.8 Volts
Loop Resistance (R_L)	200 to 1200 Ohms
Ambient Operating Temperature Range (T_A)	0°C to +75°C

ELECTRICAL CHARACTERISTICS

($V_{B}- = -48V$, $V_{B}+ = +12V$, AG = BG = DG = 0V, T_A = 25°C Unless Otherwise Stated)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	$I_{Long.} = 0$		135	174	mW
Off Hook Power Dissipation	R_{LOOP} = 600 Ohms, $I_{Long} = 0$		743	795	mW
Off Hook IB+	R_{LOOP} = 600 Ohms, $I_{Long} = 0$			4.3	mA
Off Hook IB-	R_{LOOP} = 600 Ohms, $I_{Long} = 0$			38	mA
Off Hook Loop Current	R_{LOOP} = 1200 Ohms, $I_{Long} = 0$		21		mA
Off Hook Loop Current	R_{LOOP} = 1200 Ohms, $V_{B}- = -42V$, $I_{Long} = 0$	17.5			mA
Off Hook Loop Current	R_{LOOP} = 200 Ohms, $I_{Long} = 0$	25.5	30	34.5	mA
Fault Currents					
TIP to Ground			14		mA
RING to Ground			47		mA
TIP to RING			30		mA
TIP and RING to Ground			47		mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA		0.2	0.5	V
Ring Trip Detection Period	R_{LOOP} = 600 Ohms		2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD}$ = VOL	10			mA
	$\overline{SHD}$ = VOH			5	mA
Ground Key Detection Threshold	$\overline{GKD}$ = VOL	20			mA
	$\overline{GKD}$ = VOH			10	
Dial Pulse Distortion		0		5	ms
Receive Input Impedance			90		k Ohms
Transmit Output Impedance			1		Ohm
Two Wire Return Loss	(Return Loss Referenced				
SRL LO	to 600Ω+2.16μF)		15.5		dB
ERL			24		dB
SRL HI			31		dB
Longitudinal Balance	1V Peak-Peak 200Hz - 3400Hz				
2 Wire Off Hook		58	65		dB
2 Wire On Hook		60	63		dB
4 Wire Off Hook		50	58		dB
Low Frequency Longitudinal Balance	R.E.A. Method			23	dBrnC
				-67	dBMOP

SPECIFICATIONS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss	@ 1kHz, 0dBm Input Level				
2 Wire – 4 Wire			±.05	±0.2	dB
4 Wire – 2 Wire			±.05	±0.2	dB
Frequency Response	200 – 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level		±.02	±0.05	dB
Idle Channel Noise					
2 Wire – 4 Wire			1	5	dBrnC
			-89	-85	dBMOP
4 Wire – 2 Wire			1	5	dBrnC
			-89	-85	dBMOP
Absolute Delay					
2 Wire – 4 Wire				2	μs
4 Wire – 2 Wire				2	μs
Envelope Delay					
2 Wire – 4 Wire				2	μs
4 Wire – 2 Wire				2	μs
Trans Hybrid Loss	Balance Network Set Up for 600 Ohm Termination at 1kHz	36	40		dB
Overload Level					
2 Wire – 4 Wire		+4			dBm
4 Wire – 2 Wire		+4			dBm
Level Linearity	at 1kHz				
2 Wire – 4 Wire	+3 to -40dBm			±.05	dB
	-40 to -50dBm			±.1	dB
	-50 to -55dBm			±.3	dB
4 Wire – 2 Wire	+3 to -40dBm			±.05	dB
	-40 to -50dBm			±.1	dB
	-50 to -55dBm			±.3	dB
Power Supply Rejection Ratio					
V_B+ to 2 Wire	30 – 60Hz, $R_{LOOP} = 600\Omega$	15			dB
V_B+ to Transmit		15			dB
V_B- to 2 Wire		15			dB
V_B- to Transmit		15			dB
V_B+ to 2 Wire	200 – 16kHz	30			dB
V_B+ to Transmit	$R_{LOOP} = 600\Omega$	30			dB
V_B- to 2 Wire		30			dB
V_B- to Transmit		30			dB
Logic Inputs					
Logic '0' V_{IL}				0.8	Volts
Logic '1' V_{IH}		2.0		5.5	Volts
Logic Outputs	Max Two LS Loads				
Logic '0' V_{OL}			0.1	0.5	Volts
Logic '1' V_{OH}		2.7	5.0	5.5	Volts

OVERVOLTAGE PROTECTION AND LONGITUDINAL CURRENT REJECTION

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or 30mA RMS, 15mA RMS per leg, without any performance degradation.

TABLE 1

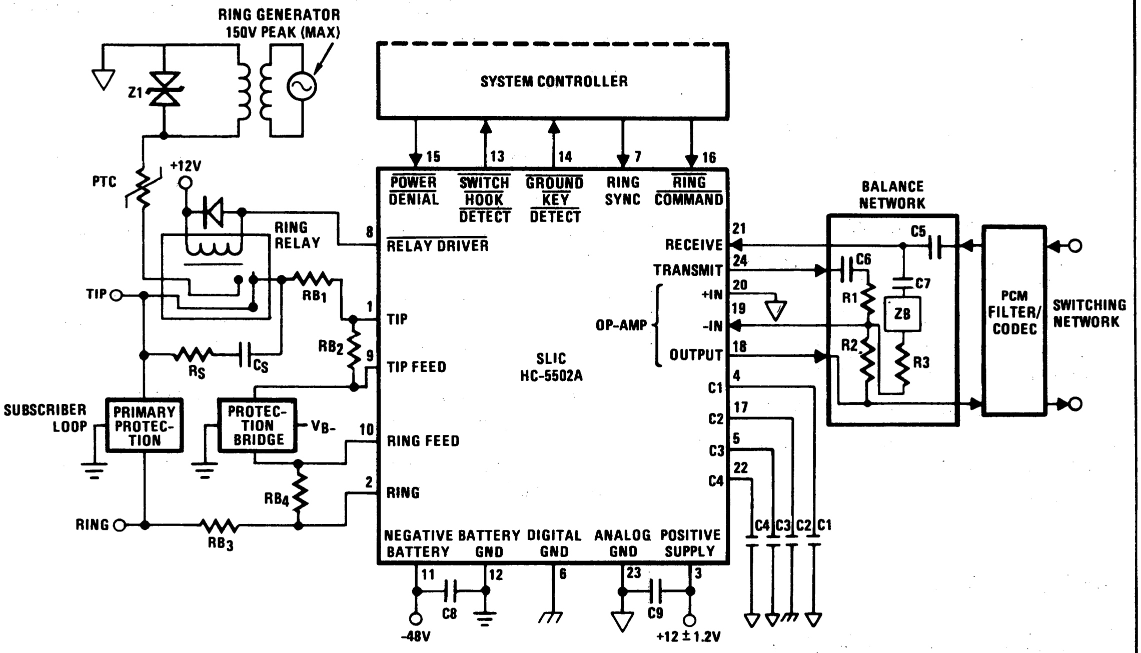
PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
Metallic Surge	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
T/GND R/GND	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
50/60Hz Current T/GND R/GND	700V rms Limited to 10A rms	11	Cycles

PIN ASSIGNMENTS

PIN NUMBER	SYMBOL	DESCRIPTION
1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay. Functions with the Ring terminal (Pin 2) to receive voice signals from the telephone and for Loop Monitoring Purposes.
2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor. Functions with the Tip terminal (Pin 1) to receive voice signals from the telephone and for loop monitoring purposes.
3	V_B+	Positive Voltage Source – Most positive supply. V_B+ is typically 12 volts with an operational range of 10.8 to 13.2 volts.
4	CAP 1	Capacitor #1 – Optional Capacitor used to improve power supply rejection. This pin should be left open if unused.
5	CAP 3	Capacitor #3 – An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering -48V supply. Typical value is 0.3µF, 30V.
6	DG	Digital Ground – To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC.
7	RS	Ring Synchronization Input – A TTL-compatible clock input. The clock is arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, tie to +5V.
8	$\overline{\text{RD}}$	Relay Driver – A low active open collector logic output. When enabled, the external ring relay is energized. Maximum $\overline{\text{RD}}$ voltage is 15 volts.
9	TF	Tip Feed- A low impedance analog output connected to the T terminal (Pin 1) through a 150Ω feed resistor. Functions with the RF terminal (Pin 10) to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
10	RF	Ring Feed - A low impedance analog output connected to the R terminal (Pin 2) through a 150Ω feed resistor. Functions with the TF terminal (Pin 9) to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.
11	V_B-	Negative Voltage Source – Most negative supply. V_B- is typically -48 volts with an operational range of -42 to -58 volts. Frequently referred to as "battery".
12	BG	Battery Ground – To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
13	$\overline{\text{SHD}}$	Switch Hook Detection – A low active LS TTL -compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
14	$\overline{\text{GKD}}$	Ground Key Detection – A low active LS TTL -compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA , and disabled if this current difference is less than 10mA.
15	$\overline{\text{PD}}$	Power Denial – A low active TTL-compatible logic input. When enabled, the loop current is limited to a maximum 2mA, the switch hook detect ($\overline{\text{SHD}}$) and ground key detect ($\overline{\text{GKD}}$) are not necessarily valid, and the relay driver ($\overline{\text{RD}}$) output is disabled.
16	$\overline{\text{RC}}$	Ring Command – A low active TTL-compatible logic input. When enabled, the relay driver ($\overline{\text{RD}}$) output goes low on the next rising edge of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{\text{PD}}$ = 0) or the subscriber is not already off-hook ($\overline{\text{SHD}}$ = 0).
17	CAP 2	Capacitor #2 – An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15µF, 10V. This capacitor is not used if ground key function is not required.
18	OUT	The analog output of the spare operational amplifier.
19	-IN	The inverting analog input of the spare operational amplifier.
20	+IN	The non-inverting analog input of the spare operational amplifier.
21	RX	Receive Input, Four Wire Side – A high impedance (90kΩ) analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the tip feed and ring feed terminals, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.
22	CAP 4	Capacitor #4 – An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near proximity power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5µF,to 1.0µF, 20V. This capacitor should be nonpolarized.
23	AG	Analog Ground – To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
24	TX	Transmit Output, Four Wire Side – A low impedance (10Ωmax) analog output which represents the differential voltage across tip and ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.

APPLICATIONS DIAGRAM

TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC


RING GENERATOR
150V PEAK (MAX)
Z1
PTC
+12V
RING RELAY
TIP
RB1
RB2
RS
CS
SUBSCRIBER LOOP
PRIMARY PROTECTION
PROTECTION BRIDGE
VB-
RB4
RING
RB3
SYSTEM CONTROLLER
15
13
14
7
16
POWER DENIAL
SWITCH HOOK DETECT
GROUND KEY DETECT
RING SYNC
RING COMMAND
8
RELAY DRIVER
1
TIP
9
TIP FEED
10
RING FEED
2
RING
SLIC
HC-5502A
OP-AMP
RECEIVE
21
TRANSMIT
24
+IN
20
-IN
19
OUTPUT
18
C1
4
C2
17
C3
5
C4
22
NEGATIVE BATTERY
BATTERY GND
DIGITAL GND
ANALOG GND
POSITIVE SUPPLY
11
12
6
23
3
C8
-48V
C9
+12 ± 1.2V
C4
C3
C2
C1
BALANCE NETWORK
C5
C6
C7
R1
ZB
R2
R3
PCM FILTER/ CODEC
SWITCHING NETWORK

TYPICAL COMPONENT VALUES

C1 = 0.5μF (Note 1)
C2 = 0.15μF, 10V
C3 = 0.3μF, 30V
C4 = 0.5μV to 1.0μF,
±10%, 20V (Should be nonpolarized)

C5 = 0.5μF, 20V
C6 = C7 = 0.5μF (10% Match Required) (Note 2), 20V
C8 = 0.01μF, 100V
C9 = 0.01μF, 20V, ±20%

R1 ⟶ R3 = 100kΩ (0.1% Match Required, 1% absolute value), ZB = 0 for 600Ω Terminations (Note 2)
$RB_1 = RB_2 = RB_3 = RB_4$ = 150Ω (0.1% Match Required, 1% absolute value)
R_S = 1KΩ, C_S = 0.1μF, 200V typically, depending on V_{Ring} and line length..
Z1 = 150V to 200V transient protector. PTC used as ring ballast.

NOTE 1: C1 is an optional capacitor used to improve +12V supply rejection. This pin must be left open if unused.

NOTE 2: To obtain the specified transhybrid loss it is necessary for the thee legs of the balance network, C6-R1-and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 and 1 μF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -10.5 to -21 volt step when the loop is closed and that too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter /CODEC.

A 0.5 μF and 100KΩ gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.

NOTE 3: Secondary protection diode bridge recommended is MDA 220 or equivalent.

**ADDITIONAL INFORMATION IS CONTAINED
IN APPLICATION NOTE 549, "THE HC-550X TELEPHONE SLICs"
BY GEOFF PHILLIPS**

HARRIS

HC-5504

SLIC
Subscriber Line Interface Circuit

FEATURES

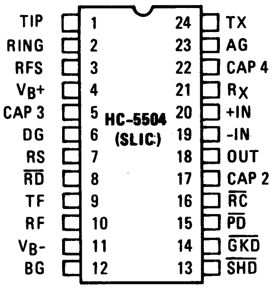
- MONOLITHIC INTEGRATED DEVICE
- DI HIGH VOLTAGE PROCESS
- COMPATIBLE WITH WORLDWIDE PBX PREFORMANCE REQUIREMENTS
- CONTROLLED SUPPLY OF BATTERY FEED CURRENT FOR SHORT LOOPS
- INTERNAL RING RELAY DRIVER
- ALLOWS INTERFACING WITH NEGATIVE SUPERIMPOSED RINGING SYSTEMS
- LOW POWER CONSUMPTION DURING STANDBY
- SWITCH HOOK GROUND KEY AND RING TRIP DETECTION FUNCTIONS
- SELECTIVE DENIAL OF POWER TO SUBSCRIBER LOOPS

APPLICATIONS

- SOLID STATE LINE INTERFACE CIRCUIT FOR ANALOG AND DIGITAL PBX SYSTEMS
- DIRECT INWARD DIAL (DID) TRUNKS
- VOICE MESSAGING PBXs

PINOUT

TOP VIEW


TIP 1
RING 2
RFS 3
VB+ 4
CAP 3 5
DG 6
RS 7
RD 8
TF 9
RF 10
VB- 11
BG 12
24 TX
23 AG
22 CAP 4
21 RX
20 +IN
19 -IN
18 OUT
17 CAP 2
16 RC
15 PD
14 GKD
13 SHD
HC-5504
(SLIC)

DESCRIPTION

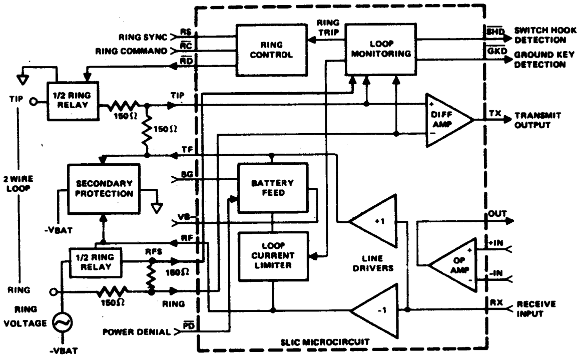
The HARRIS SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

The HARRIS SLIC is ideally suited for the design of new PBX systems, be eliminating bulky hybrid transformers.

SLIC is available in either a 24 pin dual-in-line plastic or ceramic package. The SLIC is also available in die form.

FUNCTIONAL DIAGRAM


RING SYNC
RS
RING COMMAND
RC
RD
RING CONTROL
RING TRIP
LOOP MONITORING
SHD
SWITCH HOOK DETECTION
GKD
GROUND KEY DETECTION
TIP
1/2 RING RELAY
150Ω
150Ω
TIP
DIFF AMP
TX
TRANSMIT OUTPUT
TF
2 WIRE LOOP
SECONDARY PROTECTION
BG
BATTERY FEED
-VBAT
VB
+1
OUT
RF
1/2 RING RELAY
RFS
150Ω
LOOP CURRENT LIMITER
LINE DRIVERS
OP AMP
+IN
-IN
RING
150Ω
RING
-1
RX
RECEIVE INPUT
RING VOLTAGE
POWER DENIAL
PD
SLIC MICROCIRCUIT
-VBAT

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum Continuous Supply Voltages (V_{B-})	-60 to +0.5V
(V_{B+})	-.5 to +15V
($V_{B+} - V_{B-}$)	75V
Operating Ambient Temperature Range (T_A)	0 °C to +75 °C
Storage Temperature Range (R_{SRG})	-40 °C to +85 °C
Thermal Resistance (θ_{J-A}) (Plastic)	60°C/W
Thermal Resistance (θ_{J-A}) (Ceramic)	61°C/W

RECOMMENDED OPERATING CONDITIONS

Positive Supply Voltage (V_{B+})	10.8 to 13.2V
Negative Supply Voltage (V_{B-})	-42 to -58V
Mimimum High Level Logic Input Voltage	2.4V
Maximum Low Level Logic Input Voltage	0.8V
Loop Resistance (R_L)	200 to 1200Ω
Ambient Operating Temperature Range (T_A)	0°C to +75°C

ELECTRICAL CHARACTERISTICS $V_{B-} = -48$, $V_{B+} = +12V$, AG = BG = DG = 0V, $T_A = 25$ °C Unless Otherwise Stated

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	$I_{Long.} = 0$		135	174	mW
Off Hook Power Dissipation	$R_{LOOP} = 600$ Ohms, $I_{Long.} = 0$		390	704	mW
Off Hook IB+	$R_{LOOP} = 600$ Ohms, $I_{Long.} = 0$		3	4.3	mA
Off Hook IB-	$R_{LOOP} = 600$ Ohms, $I_{Long.} = 0$		35	40	mA
Off Hook Loop Current	$R_{LOOP} = 1200$ Ohms, $I_{Long.} = 0$		21		mA
Off Hook Loop Current	$R_{LOOP} = 1200$ Ohms, $V_{B-} = -42V$, $I_{Long.} = 0$	17.5			mA
Off Hook Loop Current	$R_{LOOP} = 200$ Ohms, $I_{Long.} = 0$	36	41	48	mA
Fault Currents					
TIP to Ground			14		mA
RING to Ground			63		mA
TIP to RING			41		mA
TIP and RING to Ground			63		mA
Ring Relay Drive V_{OL}	$I_{OL} = 62mA$		0.2	0.5	V
Ring Trip Detection Period	$R_{LOOP} = 600$ Ohms		2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD} = V_{OL}$	10			mA
	$\overline{SHD} = V_{OH}$			5	mA
Ground Key Detection Threshold	$\overline{GKD} = V_{OL}$	20			mA
	$\overline{GKD} = V_{OH}$			10	mA
Dial Pulse Distortion		0		5	ms
Receive Input Impedance			90		k Ohms
Transmit Output Impedance			1		Ohm
Two Wire Return Loss	(Return Loss Referenced				
SRL LO	to 600Ω+2.16μF)		15.5		dB
ERL			24		dB
SRL HI			31		dB
Longitudinal Balance	1V Peak-Peak (200Hz-3400Hz)				
2 Wire Off Hook		58	65		dB
2 Wire On Hook		60	63		dB
4 Wire Off Hook		50	58		dB
Low Frequency Longitudinal Balance	R.E.A. Method			23	dBrnC
Insertion Loss	@ 1kHz, 0dBm Input Level			-67	dBmop
2 Wire - 4 Wire			±.05	±0.2	dB
4 Wire - 2 Wire			±.05	±0.2	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level		±.02	±0.05	dB
Idle Channel Noise					
2 Wire - 4 Wire			1	5	dBrnC
			-89	-85	dBmop
4 Wire - 2 Wire			1	5	dBrnC
			-89	-85	dBmop
Absolute Delay					
2 Wire - 4 Wire				2	μs
4 Wire - 2 Wire				2	μs

SPECIFICATIONS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Envelope Delay					
2 Wire - 4 Wire				2	μs
4 Wire - 2 Wire				2	μs
Trans Hybrid Loss	Balance Network Set Up for 600 Ohm Termination at 1kHz	36	40		dB
Overload Level					
2 Wire - 4 Wire		+4			dBm
4 Wire - 2 Wire		+4			dBm
Level Linearity	at 1kHz				
2 Wire - 4 Wire	+3 to -40dBm			±0.05	dB
	-40 to -50dBm			±0.1	dB
	-50 to -55dBm			±0.3	dB
4 Wire - 2 Wire	+3 to -40dBm			±0.05	dB
	-40 to -50dBm			±0.1	dB
	-50 to -55dBm			±0.3	dB
Power Supply Rejection Ratio					
VB+ to 2 Wire	30 – 60Hz, R_{LOOP} = 600Ω	15			dB
V_B+ to Transmit		15			dB
V_B- to 2 Wire		15			dB
V_B- to Transmit		15			dB
V_B+ to 2 Wire	200 - 16kHz	30			dB
V_B+ to Transmit	R_{LOOP} = 600Ω	30			dB
V_B- to 2 Wire		30			dB
V_B- to Transmit		30			dB
Logic Inputs					
Logic '0' V_{IL}		0.0		0.8	V
Logic '1' V_{IH}		2.0		5.5	V
Logic Outputs	Max Two LS Loads				
Logic '0' V_{OL}			0.1	0.5	V
Logic '1' V_{OH}		2.7		5.5	V

OVERVOLTAGE PROTECTION AND LONGITUDINAL CURRENT REJECTION

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage ligntning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

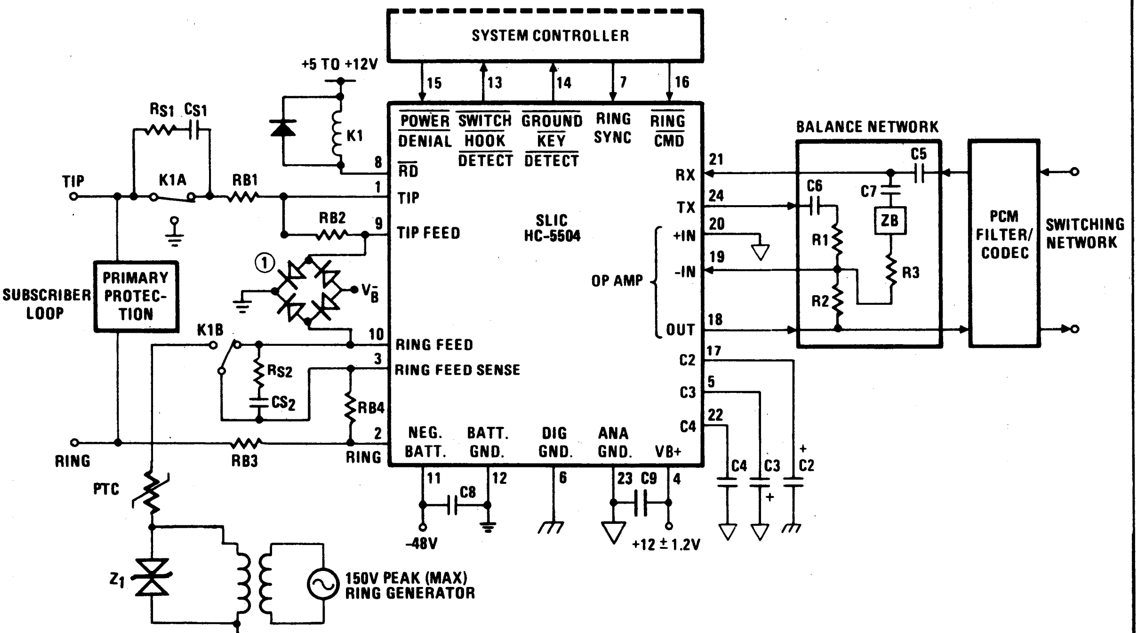
The SLIC will withstand longitudinal currents up to a maximum or 30mA RMS, 15mA RMS per leg, without any performance degradation.

TABLE 1

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
Metallic Surge	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
T/GND R/GND	10μs Rise/ 1000μs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
50/60Hz Current T/GND R/GND	700V rms Limited to 10A rms	11	Cycles

PIN ASSIGNMENTS

PIN NUMBER	SYMBOL	DESCRIPTION
1	TIP	An Analog input connected to the Tip (More Positive) side of the subscriber loop through a 150Ωfeed resistor and a ring relay. Functions with the Ring terminal (Pin 2) to receive voice signals from the telephone and for loop monitoring purposes.
2	RING	An Analog input connected to the Ring (More Negative) side of the subscriber loop through a 150Ωfeed resistor. Functions with the Tip terminal (Pin 1) to receive voice signals from the telephone and for loop monitoring purposes.
3	RFS	Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.
4	$V_{B}+$	Positive Voltage Source—Most positive supply. $V_{B}+$ is typically 12 volts with an operational range of 10.8 to 13.2 volts.
5	CAP 3	Capacitor #3—An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering −48V supply. Typical value is 0.3μF, 30V.
6	DG	Digital Ground—To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
7	RS	Ring Synchronization Input—a TTL - compatible clock input. The clock is arranged such that a positive pulse (50-500μ s) occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, then tie to +5V.
8	$\overline{\text{RD}}$	Relay Driver—a low active open collector logic output. When enabled, the external ring relay is energized. Maximum $\overline{\text{RD}}$ voltage is 15 volts.
9	TF	Tip Feed—A low impedance Analog output connected to the T terminal (Pin 1) through a 150Ω feed resistor. Functions with the RF terminal (Pin 10) to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.
10	RF	Ring Feed—A low impedance Analog output connected to the R terminal (Pin 2) through a 150Ω feed resistor. Functions with the TF terminal (Pin 9) to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.
11	$V_{B}-$	Negative Voltage Source—Most negative supply. VB− is typically −48 volts with an operational range of −42 to −58 volts. Frequently referred to as "battery."
12	BG	Battery Ground—To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
13	$\overline{\text{SHD}}$	Switch Hook Detection—A low active LS TTL-compatible logic output. This output is typically enabled for loop currents exceeding 7.5 mA and typically disabled for loop currents less than 7.5mA.
14	$\overline{\text{GKD}}$	Ground Key Detection—A low active LS TTL-compatible logic output. This output is typically enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 12.5 mA, and typically disabled if this current difference is less than 12.5mA.
15	$\overline{\text{PD}}$	Power Denial—A low active TTL-compatible logic input. When enabled, the loop current is limited to a maximum 2mA, the switch hook detect ($\overline{\text{SHD}}$)and ground key detect ($\overline{\text{GKD}}$) are not necessarily valid and the relay driver ($\overline{\text{RD}}$) output is disabled.
16	$\overline{\text{RC}}$	Ring Command—A low active TTL-compatible logic input. When enabled, the relay driver ($\overline{\text{RD}}$) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{\text{PD}}$=0) or the subscriber is not already off-hook ($\overline{\text{SHD}}$=0).
17	CAP 2	Capacitor #2—An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occuring during ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not needed if ground key function is not required and pin 17 may be left open or connected to digital ground.
18	OUT	The analog output of the spare operational amplifier. The output voltage swing is typically ±5V.
19	−IN	The inverting analog input of the spare operational amplifier.
20	+IN	The non-inverting analog input of the spare operational amplifier.
21	RX	Receive Input, Four Wire Side—A high impedance (90kΩ) analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the tip feed and ring feed terminals, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.
22	CAP 4	Capacitor #4—An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occuring when longitudinal currents are induced onto the subscriber loop from near proximity power lines and other noise sources. This capactior is also required for the proper operation of ring trip detection. Typical value is 0.5μF to 1.0μF, 20V. This capacitor should be nonpolarized.
23	AG	Analog ground—To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
24	TX	Transmit Output, Four Wire Side—A low impedance (10Ωmax) analog output which represents the differential voltage across tip and ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.


SYSTEM CONTROLLER
15
13
14
7
16
+5 TO +12V
K1
R_{S1}
C_{S1}
TIP
K1A
RB1
RB2
PRIMARY PROTEC-TION
SUBSCRIBER LOOP
①
V_B^-
K1B
R_{S2}
C_{S2}
RB4
RING
RB3
RING
PTC
Z_1
-48V
150V PEAK (MAX) RING GENERATOR
POWER DENIAL
SWITCH HOOK DETECT
GROUND KEY DETECT
RING SYNC
RING CMD
8
$\overline{RD}$
1
TIP
9
TIP FEED
SLIC HC-5504
10
RING FEED
3
RING FEED SENSE
2
NEG. BATT.
BATT. GND.
DIG GND.
ANA GND.
VB+
11
12
6
23
4
C8
C9
-48V
+12 ± 1.2V
21
RX
24
TX
20
+IN
19
-IN
OP AMP
18
OUT
17
C2
5
C3
22
C4
C4
C3
C2
BALANCE NETWORK
C5
C6
C7
ZB
R1
R2
R3
PCM FILTER/ CODEC
SWITCHING NETWORK

TYPICAL COMPONENT VALUES

C2 = 0.15μF, 10V
C3 = 0.3μF, 30V
C4 = 0.5 μF to 1.0μF 10%, 20V (Should be non-polarized)
C5 = 0.5μF, 20V
C6 = C7 = 0.5μF (10% Match Required) ②
C8 = 0.01μF, 100V
C9 = 0.01μF, 20V ± 20%
R1 = R2 = R3 = 100k (0.1% Match Required, ZB = 0 for 600Ω Terminations ②
RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required, 1% Absolute)
R_{S1} = R_{S2} = 1KΩ Typically
C_{S1} = C_{S2} = 0.1μF, 200V typically, depending on V_{RING} and Line Length.
Z_1 = 150V to 200V transient protection.
PTC used as ring generator ballast.

NOTES:

① Secondary protection diode bridge recommended is an MDA 220 or equivalent.

② To obtain the specified transhybrid loss of 40dB it is necessary for the 3 legs of the balance network, C6 - R1 and R2 and C7 - ZB - R3, to match in impedance to within 0.3%. If C6 and C7 are 1μF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -22V step when the loop is closed. Too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC. A 0.5μF and 100kΩ gives a time constant of 50msec. The uncommited op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.

ADDITIONAL INFORMATION IS CONTAINED IN
APPLICATION NOTE 549
"THE HC-550X TELEPHONE SLICs"
BY GEOFF PHILLIPS

HARRIS

HC-5508/09

PRELIMINARY

SLICs
Subscriber Line Interface Circuits

Features

- **Monolithic Integrated Device**
- **DI High Voltage Process**
- **Compatible with Worldwide PBX Performance Requirements**
- **Controlled Supply of Battery Feed Current for Short Loops**
- **Internal Ring Relay Driver and Message Waiting Relay Driver**
- **Programmable Loop Current Limit and Self-Test Function (HC-5509)**
- **Low Power Consumption During Standby**
- **Switch Hook, Ground Key, Ring Trip and Message Waiting Detection Functions**
- **Selective Denial of Power to Subscriber Loops**
- **Two On Chip Op Amps for Transhybrid Balance and 2 Wire Impedance Matching**

Applications

- **Solid State Line Interface Circuit for PBX or Central Office Systems**
- **Hotel/Motel (Message/Waiting) Switching Systems**
- **Direct Inward Dialing (DID) Trunks**
- **Voice Messaging PBX's**
- **Analog Trunk Echo Cancellor Interface**

Description

The HC-5508/09 SLICs incorporate many of the BORSHT functions on a monolithic IC. These include DC battery feed with loop current limiting, overvoltage protection, ringing, supervisory and hybrid functions. The devices are designed to maintain specified transmission performance in the presence of externally induced longitudinal currents.

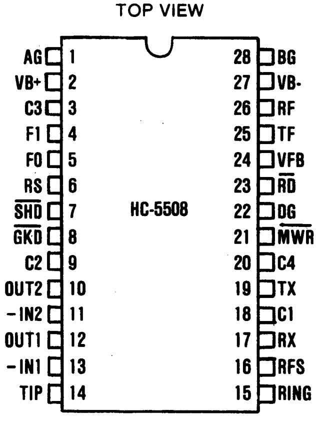
The SLICs also provide selective denial of power, a 40mA loop current limit, line fault protection, and thermal current limiting. If a PBX/CO system becomes overloaded during an emergency or is subjected to line faults, the SLICs will provide system protection by denying power to selected subscriber loops or by limiting loop current. Switch hook, ground key, ring trip, and message waiting detection functions are also incorporated into the SLIC devices.

The Harris SLICs are ideally suited for the design of PBX and CO systems, replacing bulky hybrid transformers.

The HC-5508 SLIC is available in a 28 pin Dual-In-Line plastic package, or in die form. The HC-5509 is available in a 44 pin PLCC or in a die form which allow users the option to access additional functions including a self test function and an externally programmable loop current limit.

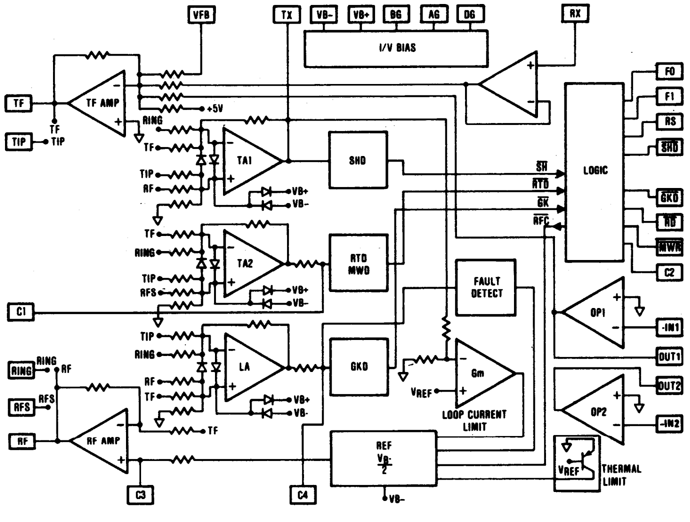
Both SLICs are ideally suited for use with the HC-5512/12A PCM filters, the HC-5510/11 PCM CODECs, and the HC-5552/3/4/7 serial interface PCM combos.

Pinout


TOP VIEW
HC-5508
AG 1
VB+ 2
C3 3
F1 4
F0 5
$\overline{RS}$ 6
$\overline{SHD}$ 7
$\overline{GKD}$ 8
C2 9
OUT2 10
-IN2 11
OUT1 12
-IN1 13
TIP 14
15 RING
16 RFS
17 RX
18 C1
19 TX
20 C4
21 $\overline{MWR}$
22 DG
23 $\overline{RD}$
24 VFB
25 TF
26 RF
27 VB-
28 BG

HC-5509
AVAILABLE IN
SURFACE MOUNT
44 PIN PLCC

Functional Diagram


VFB
TX
VB-
VB+
BG
AG
DG
RX
I/V BIAS
TF
TIP
TF AMP
+5V
RING
TA1
TA2
LA
SHD
RTD MWD
GKD
FAULT DETECT
Gm
VREF
LOOP CURRENT LIMIT
LOGIC
$\overline{SH}$
$\overline{RTD}$
$\overline{GK}$
RFC
F0
F1
$\overline{RS}$
$\overline{SHD}$
$\overline{GKD}$
$\overline{RD}$
$\overline{MWR}$
C2
OP1
-IN1
OUT1
OUT2
OP2
-IN2
C1
RING
RF
RFS
RF AMP
C3
C4
REF
$\frac{V_B-}{2}$
VB-
VREF
THERMAL LIMIT
TF
TIP
RF
RFS

Description of Pin Functions

PIN	SYMBOL	DESCRIPTION
1	AG	Analog Ground — To be connected to zero potential. Serves as a reference for the transmit output (TX) and receive input (RX) terminals.
2	V_B+	Positive Voltage Source — Most positive supply. V_B+ is typically 12 volts with an operational range of 10.8 to 13.2 volts.
3	C3	Capacitor #3 — An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering -48V supply. Typical value is 0.3μF, 30V.
4	F1	Function Address 1 — TTL and CMOS compatible input used with F0 function address line to externally select logic functions; ring command, message waiting, and loop power denial. The three selectable functions are mutually exclusive. (See Truth Table 1.)
5	F0	Function Address 0 — TTL and CMOS compatible input used with F1 function address line to externally select logic functions; ring command, message waiting, and loop power denial. The three selectable functions are mutually exclusive. (See Truth Table 1.)
6	RS	Ring Synchronization Input — A TTL compatible clock input. The clock is arranged such that a positive pulse (50-500μs) occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, then tie to +5V.
7	$\overline{SHD}$	Switch Hook Detection — A low active LS TTL compatible logic output. This output is typically enabled for loop currents exceeding 12mA and typically disabled for loop currents less than 12mA.
8	$\overline{GKD}$	Ground Key Detection — A low active LS TTL compatible logic output. This output is typically enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 15mA and typically disabled if this current difference is less than 15mA.
9	C2	Capacitor #2 — An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not needed if ground key function is not required and may be left open or connected to digital ground.
10	OUT2	The analog output of spare operational amplifier Number 2. The output voltage swing is typically ±5V.
11	-IN2	The inverting analog input of spare operational amplifier Number 2.
12	OUT1	The analog output of spare operational amplifier Number 1. The output voltage swing is typically ±5V.
13	-IN1	The inverting analog input of spare operational amplifier Number 1.
14	TIP	An analog input connected to the TIP (more positive) side of subscriber loop through a 50Ω feed resistor and a ring relay. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purposes.

Description of Pin Functions (Continued)

PIN	SYMBOL	DESCRIPTION
15	RING	An Analog input connected to the RING (more negative) side of the subscriber loop through a 50Ω feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	RFS	Senses ring side of loop for ground key detection. During Ring Injected ringing, the ring signal is inserted into the line at this node to isolate RF from the ring signal via the ring relay. For balanced or Tip Injected Ringing, the RF and RFS pins must be shorted.
17	RX	Receive Input, Four Wire Side — A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip Feed and Ring Feed terminals, which in turn drive TIP and RING through 100 ohms of feed resistance on each side of the line.
18	C1	Capacitor #1 — An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection and false message waiting detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. Typical value is 0.5μF to 1.0μF, 20V. This capacitor should be nonpolarized.
19	TX	Transmit Ouput, Four Wire Side — A low impedance (10Ωmax) analog output which represents the differential voltage across TIP and RING. Transhybrid balancing must be performed (using the SLIC microcircuit spare op amps) beyond this output to completely implement two to four wire conversion. This output is referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	C4	Capacitor #4 — An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication from occurring when longitudinal currents are induced into the subscriber loop from power lines and other noise sources. Typical value is 0.5 μF to 1.0μF, 20V. This capacitor should be nonpolarized.
21	$\overline{\text{MWR}}$	Message Waiting Relay Driver — A active low open collector logic output. Used to switch a high voltage onto the line to drive a telephone set neon lamp to indicate a message is waiting.
22	DG	Digital Ground — To be connected to zero potential. Serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
23	$\overline{\text{RD}}$	Ring Relay Driver — A active low open collector logic output. Used to switch ring signals onto the 2 wire line.
24	VFB	Feedback signal from the tip feed amplifier. To be used in conjunction with transmit output signal (TX) and the spare op-amps to accommodate 2W line impedance matching.
25	TF	Tip Feed — A low impedance analog output connected to the TIP terminal through a 50Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.
26	RF	Ring Feed — A low impedance analog output connected to the RING terminal through a 50Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.
27	V_B-	Negative Voltage Source — Most negative supply. V_B- is typically -48 volts with an operational range of -25 to -58 volts. Frequently referred to as "battery".
28	BG	Battery Ground — To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.

Absolute Maximum Ratings

Max. Continuous Supply Voltages (VB+) .....-0.5V to +15V
(VB+)-(VB-) .... +75V
Operating Ambient Temperature (TA) .... 0°C to +75°C
Storage Temperature Range (TS) ...-25°C to +125°C

Recommended Operating Conditions

Positive Power Supply (VB+) .... +12V ±5%
Negative Power Supply (VB-) .... -25V to -58V
Ambient Operating Temperature Range
(TA) .... 0°C to +75°C

Electrical Characteristics

Typical Conditions Unless Otherwise Stated:
VB- = -48V, VB+ = 12V, AG = DG = BG = 0V, TA = 25°C,
All AC Parameters are Specified at 600Ω

TABLE 1.

F1	F0	ACTION
0	0	Normal Loop Feed
0	1	$\overline{\text{RD}}$ Active
1	0	$\overline{\text{MWR}}$ Active
1	1	Loop Power Denial Active

A.C. Transmission Performance

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RX Input Impedance	300Hz to 3.4KHz	1			MΩ
4W Input Overload Level	300Hz to 3.4KHz	+4			dBm
2W Input Overload Level	300Hz to 3.4KHz	+4			dBm
2W Longitudinal Impedance	Per Lead		100		Ω
2W Return Loss					
SRL LO	200Hz to 500Hz	25	35		dB
ERL	500Hz to 2.5KHz	25	40		dB
SRL HI	2.5KHz to 3.2KHz	25	40		dB
2W Longitudinal to Metallic Balance	per ANSI/IEEE STD 455-1976				
Off Hook	300Hz to 3400Hz	55	65		dB
On Hook	10Hz to 3400Hz	60	63		dB
4W Longitudinal to Metallic Balance	per ANSI/IEEE STD 455-1976				
Off Hook	300Hz to 3400Hz	50	55		dB
Low Frequency Longitudinal Balance 2W and 4W	R.E.A. Method			-67 23	dBmop dBrnC
Longitudinal Current Capability	Per Lead			15	mArms

A.C. Transmission Performance (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss					
2W/4W, 4W/2W	0dBm @ 300Hz to 3400Hz			±0.2	dB
Level Linearity					
	Ref. to -10dBm				
2W/4W	+3 to -40dBm			±0.05	dB
	-40 to -50dBm			±0.1	dB
	-50 to -55dBm			±0.3	dB
4W/2W	+3 to -40dBm			±0.05	dB
	-40 to -50dBm			±0.1	dB
	-50 to -55dBm			±0.3	dB
Absolute Delay					
2W/4W	300Hz to 3400Hz			2	μs
4W/2W	300Hz to 3400Hz			2	μs
Envelope Delay Distortion					
2W/4W, 4W/2W	500Hz to 1KHz			2	μs
	1KHz to 2.6KHz			2	μs
	2.6KHz to 2.8KHz			2	μs
Transhybrid Loss, THL	0dBm @ 1KHz	36	40		Dβ
Total Harmonic Distortion	Ref. Level 0dBm				
2W/4W, 4W/2W, 4W/4W	300Hz to 3400Hz			-52	dB
Idle Channel Noise					
2W and 4W	C-Message			5	dBrnC
	Psophometric			-85	dBmop
	3KHz Flat			15	dBrn
Power Supply Rejection Ratio	30Hz to 200Hz				
VB+ to 2W		25			dB
VB+ to 4W	V_{NOISE} = 100mVrms	25			dB
VB- to 2W		25			dB
VB- to 4W		25			dB
VB+ to 2W	200Hz to 16KHz	30			dB
VB+ to 4W		30			dB
VB- to 2W	V_{NOISE} = 100mVrms	30			dB
VB- to 4W		30			dB

D.C. Performance

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Loop Current Limit			40	46	mA
Loop Current During Power Denial				±2	mA
Fault Currents					
TIP to Ground			40		mA
RING to Ground			60		mA
TIP and RING to Ground			100		mA
TIP to RING			40		mA
Switch Hook Detection Threshold			12		mA
Ground Key Detection Threshold			15		mA
Message Waiting Detection Threshold			15		mA
Ring Trip Detection Threshold			15		mA
Ring Trip Detection Period			2	3	Cycles
Dial Pulse Distortion			0.1		mS
Relay Driver Outputs ($\overline{RD}$, $\overline{MWR}$)					
On Current	V_{SAT} = 1.2V		50		mA
Off Leakage Current			±10		μA
Delay Time				10	μs
Rise and Fall Time	+12V to 0V			10	μs
TTL/CMOS Logic Inputs (F0, F1, RS)					
Logic '0' V_{IL}				0.8	V
Logic '1' V_{IH}		2.0		5.5	V
Input Current (F0, F1, RS)	$0V \leq V_{IN} \leq 5V$			±100	μA
Ring Synchronization (RS)					
Pulse Width		25			μs
Delay Time, Sync to Driver Off		20		20	μs
Logic Inputs					
Logic '0' V_{IL}		0.0		0.8	V
Logic '1' V_{IH}		2.0		5.5	V
Logic Outputs	Max Two LS Loads				
Logic '0' V_{IL}			0.1	0.5	V
Logic '1' V_{IH}		2.7		5.5	V
Power Dissipation					
On Hook			200		mW

Uncommitted Op Amps

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			10	15	mV
Input Offset Current				100	nA
Input Bias Current				400	nA
Differential Input Resistance			1		MΩ
Input Noise Voltage	f = 1KHz		20		nV/ Hz
Output Voltage Swing	R_L = 10KΩ		±5		V
Output Resistance				10	Ω
Small Signal GBW			1		MHz

Overvoltage Protection and Longitudinal Current Rejection

The SLIC devices, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

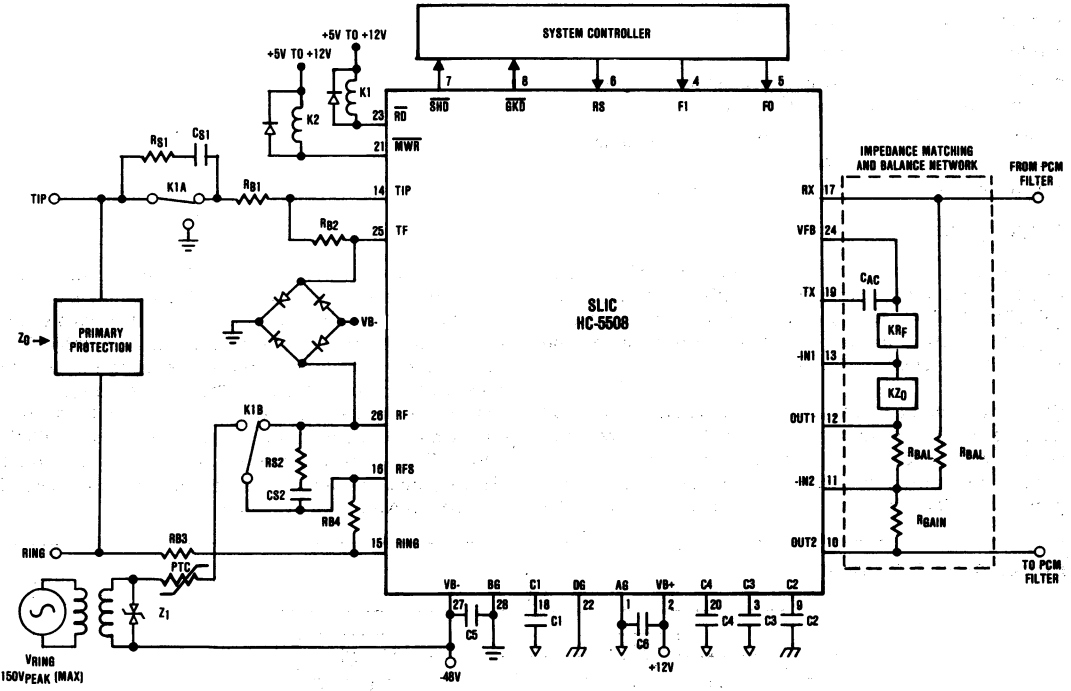
High voltage surge conditions are as specified in Table 2.

The SLICs will withstand longitudinal currents up to a maximum total of 30mArms (15mArms per leg) without any performance degradation.

TABLE 2.

PARAMETER	TEST CONDITION	PERFORMANCE (MAXIMUM)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
Metallic Surge	10µs Fall 1000µs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic) ±500 (Ceramic)	V Peak V Peak
50/60Hz Current T/GND R/GND	700V rms Limited to 10A rms	11	Cycles

Applications Diagram


SYSTEM CONTROLLER
+5V TO +12V
+5V TO +12V
K1
K2
R_{S1}
C_{S1}
K1A
R_{B1}
R_{B2}
TIP
RING
Z_0
PRIMARY PROTECTION
VB-
K1B
RS2
CS2
RB4
RB3
PTC
Z_1
V_{RING}
150VPEAK (MAX)
-48V
+12V
SLIC
HC-5508
7 SHD
8 GKD
6 RS
4 F1
5 F0
23 RD
21 MWR
14 TIP
25 TF
26 RF
16 RFS
15 RING
17 RX
24 VFB
19 TX
13 -IN1
12 OUT1
11 -IN2
10 OUT2
27 VB-
28 BG
18 C1
22 DG
1 AG
2 VB+
20 C4
3 C3
9 C2
C1
C4
C3
C2
C5
C6
C_{AC}
KR_F
KZ_0
R_{BAL}
R_{BAL}
R_{GAIN}
IMPEDANCE MATCHING AND BALANCE NETWORK
FROM PCM FILTER
TO PCM FILTER

Typical Component Values:

C1 = 0.5µF to 1µF, 20V (Nonpolarized)
C2 = 0.15µF, 10V
C3 = 0.3µF, 30V
C4 = 0.5µF - 1.0µF ± 10%, 20V (Should be Nonpolarized)
C5 = 0.01µF, 100V ±20%
C6 = 0.01µF, 20V ±20%
C_{AC} = 0.5µF, 20V
KZ_0 = 60KΩ (Z_0 = 600Ω, K = Scaling Factor)
R_{GAIN} = User Defined
R_{BAL} = 100KΩ

KR_F = 20KΩ ($R_F = 2(R_{B1} + R_{B4})$), K = Scaling Factor)
$R_{B1} = R_{B2} = R_{B3} = R_{B4}$ = 50Ω (1% Absolute, 0.1% Match Required)
$R_{S1} = R_{S2}$ = 1KΩ Typically
$C_{S1} = C_{S2}$ = 0.1µF, 200V Typically, Depending on V_{RING} and Line Length.

Z_1 = 150 to 200V Transient Protector. PTC used as Ring Generator Ballast.

Secondary Protection Diode Bridge Recommended is an MDA 220 or equivalent.

NOTE: HC-5508 applications diagram shows Ring Injected Ringing Configuration. A Balanced or Tip injected configuration may also be used. For additional applications information refer to Applications Note 549 by Geoff Phillips, "The HC-550X Telephone SLICs."

HARRIS

HC-5510/11

Monolithic CODECs

Features

- Industry Standard Pinout
- Low Power switched capacitor CMOS
- Low Operation Power .... 45mW Typical
- Low Standby Power .... 1mW Typical
- ±5V Operation
- TTL Compatible Digital Interface
- Time Slot Assignment or Alternate Fixed Time Slot Modes
- Internal Precision Reference
- Internal Sample and Hold Capacitors
- Internal Auto-Zero Circuit
- HC-5510-μ-Law Coding With Signaling Capabilities that meet Bell D3/D4 specifications
- HC-5511-A-Law Coding with Signaling Capabilities that meet CCITT specifications
- Synchronous or Asynchronous Operation

Applications

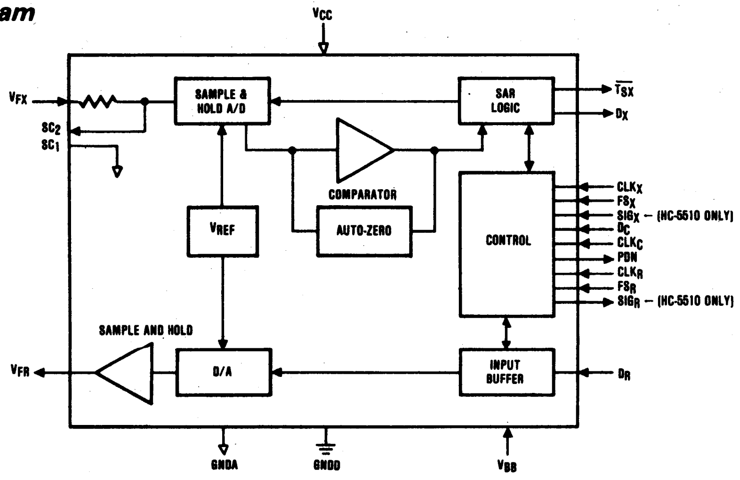
- Pulse Code Modulation Coding and Decoding for Digital PBX and Central Office Telecommunications Switching Systems
- Analog to Digital Conversion in MODEMs and Multiplexers
- Data Acquisition Systems

Description

The HC-5510 and HC-5511 are monolithic PCM CODECs implemented with double-poly CMOS technology. The HC-5510 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The HC-5511 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the HC-5510/HC-5511 may be operated in a fixed time slot mode. Both devices are ideal for use with the HC-5512/12A/12C/12D monolithic PCM filters, which provide the input anti-aliasing function for the encoder, smooth the output of the decoder, and correct for the sin x/x distortion introduced by the decoder sample and hold output. All devices may be used with the Harris Family of Subscriber Line Interface Circuits (SLICs), including the HC-5502A, HC-5504 and HC-5508. Application Notes are available.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Operating Temperature	-25°C to +125°C
Storage Temperature	-65°C to +150°C
V_{CC} with Respect to GNDD	7V
V_{CC} with Respect to V_{BB}	14V
V_{BB} with Respect to GNDD	-7V
Voltage at Any Input or Output	V_{BB} -0.3V to V_{CC} +0.3V
Lead Temperature (Soldering, 10 seconds)	300°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A = 0°C to 75°C, V_{CC} = 5.0V ± 5%, V_{BB} = -5.0V ± 5%. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = -5.0V and T_A = 25°C. All digital signals are referenced to GNDD. All analog signals are referenced to GNDA.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
DIGITAL INTERFACE						
I_I	Input Current	-10		10	μA	$0 < V_{IN} < V_{CC}$
V_{IL}	Input Low Voltage			0.6	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output Low Voltage			0.4 0.4 0.4 0.4	V V V V	D_X, I_{OL} = 4.0mA SIG_R, I_{OL} = 0.5mA $\overline{TS}_X$, I_{OL} = 3.2mA, Open Drain PDN, I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4 2.4			V V	D_X, I_{OH} = 6mA SIG_R, I_{OH} = 0.6mA
ANALOG INTERFACE						
Z_I	VF_X Input Impedance when Sampling	2.0			kΩ	Resistance in Series with Approximately 70pF
Z_O	Output Impedance at VF_R		10	20	Ω	$-3.1V < VF_R < 3.1V$
V_{OS}	Output Offset Voltage at VF_R	-25		25	mV	D_R = PCM Zero Code, HC-5510 or Alternating ±1 Code, HC-5511
I_{IN}	Analog Input Bias Current	-0.1		0.1	μA	V_{IN} = 0V
R1 x C1	DC Blocking Time Constant	4.0			ms	
C1	DC Blocking Capacitor	0.1			μF	
R1	Input Bias Resistor			160	kΩ	
POWER DISSIPATION						
I_{CC0}	Standby Current, V_{CC}		0.1	0.4	mA	
I_{BB0}	Standby Current, V_{BB}		0.03	0.1	mA	
I_{CC1}	Operating Current, V_{CC}		4.5	8.0	mA	
I_{BB1}	Operating Current, V_{BB}		4.5	8.0	mA	

A.C. Electrical Characteristics

Unless otherwise noted, the analog input is a 0dBm0, 1.02kHz sine wave. The digital input is a PCM bit stream generated by passing a 0dBm0, 1.02kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
	Absolute Level					The nominal 0dBm0 levels for the HC-5510 and HC-5511 are 1.520 Vrms and 1.525 Vrms respectively. The resulting nominal overload level is 3.096V peak for both devices. All gain measurements for the encode and decode portions of the HC-5510/HC-5511 are based on these nominal levels after the necessary sin x/x corrections are made.
G_{RA}	Receive Gain, Absolute	-0.125		0.125	dB	T = 25°C, V_{CC} = +5V, V_{BB} = -5V
G_{RAT}	Absolute Receive Gain Variation with Temperature	-0.05		0.05	dB	T = 0°C to 75°C
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	-0.07		0.07	dB	V_{CC} = 5V ±5%, V_{BB} = -5V±5%
G_{XA}	Transmit Gain, Absolute	-0.325		-0.075	dB	T = 25°C, V_{CC} = 5V, V_{BB} = -5V
G_{XAT}	Absolute Transmit Gain Variation with Temperature	-0.05		0.05	dB	T = 0°C to 75°C
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	-0.07		0.07	dB	V_{CC} = 5V ±5%, V_{BB} = -5V ±5%
G_{RAL}	Absolute Receive Gain Variation with Level	-0.3 -0.2 -0.4 -1.0		0.3 0.2 0.4 1.0	dB dB dB dB	CCITT Method 2 Relative to -10dBm0 0dBm0 to 3dBm0 -40dBm0 to 0dBm0 -50dBm0 to -40dBm0 -55dBm0 to -50dBm0
G_{XAL}	Absolute Transmit Gain Variation with Level	-0.3 -0.2 -0.4 -1.0		0.3 0.2 0.4 1.0	dB dB dB dB	CCITT Method 2 Relative to -10dBm0 0dBm0 to 3dBm0 -40dBm0 to 0dBm0 -50dBm0 to -40dBm0 -55dBm0 to -50dBm0
S/D_R	Receive Signal to Distortion Ratio	35 29 25			dBc dBc dBc	Sinusoidal Test Method Input Level -30dBm0 to 0dBm0 -40dBm0 -45dBm0
S/D_X	Transmit Signal to Distortion Ratio	35 29 25			dBc dBc dBc	Sinusoidal Test Method Input Level -30dBm0 to 0dBm0 -40dBm0 -45dBm0
N_R	Receive Idle Channel Noise			6 -84	dBnrc0 dBm0p	D_R = Steady State PCM Code HC-5510 HC-5511
N_X	Transmit Idle Channel Noise			13 -67	dBrnc0 dBm0p	HC-5510, VF_X = 0V (no signaling) HC-5511, VF_X = 0V
HD_R	Receive Harmonic Distortion			-47	dB	2nd or 3rd Harmonic
HD_X	Transmit Harmonic Distortion			-47	dB	2nd or 3rd Harmonic
$PPSR_R$	Positive Power Supply Rejection, Receive	40			dB	D_R = Steady PCM Code, V_{CC} = 5.0V_{DC} + 200mVrms, f = 1.02kHz
$PPSR_X$	Positive Power Supply Rejection, Transmit	50			dB	Input Level = 0V, V_{CC} = 5.0V_{DC} + 200mVrms, f = 1.02kHz
$NPSR_R$	Negative Power Supply Rejection, Receive	45			dB	D_R = Steady PCM Code, V_{BB} = -5.0V_{DC} +200mVrms, f = 1.02kHz
$NPSR_X$	Negative Power Supply Rejection Transmit	50			dB	Input Level = 0V, V_{BB} = -5.0V_{DC} + 200mVrms, f = 1.02kHz
CT_{XR}	Transmit to Receive Crosstalk			-75	dB	D_R = Steady PCM Code
CT_{RX}	Receive to Transmit Crosstalk			-70 -65	dB dB	Transmit Input Level = 0V HC-5510 HC-5511

Timing Specifications

Unless otherwise noted, T_A = 0°C to 75°C, V_{CC} = 5.0 ±5%, V_{BB} = -5.0 ±5%. All digital signals are referenced to GNDD and measured at V_{IL} and V_{IH} levels as indicated in the timing waveforms.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_{PC}	Period of Clock	485			ns	CLK_C, CLK_R, CLK_X
t_{RC}, t_{FC}	Rise and Fall Time of Clock			30	ns	CLK_C, CLK_R, CLK_X
t_{WCH}	Width of Clock High	165			ns	CLK_C, CLK_R, CLK_X
t_{WCL}	Width of Clock Low	165			ns	CLK_C, CLK_R, CLK_X
$t_{A/D}$	A/D Conversion Time			16	Time Slots	From End of Encoder Time Slot to Completion of Conversion
$t_{D/A}$	D/A Conversion Time			2	Time Slots	From End of Decoder Time Slot to Transition of VF_R
t_{SDC}	Set-Up Time, D_C to CLK_C	100			ns	
t_{HDC}	Hold Time, CLK_C to D_C	100			ns	
t_{SFC}	Set-Up Time, FS_X or CLK_X	100			ns	
t_{HFX}	Hold Time, CLK_X to FS_X	100			ns	
t_{DZX}	Delay Time to Enable D_X on TS Entry	25		125	ns	C_L = 150pF
t_{DDX}	Delay Time, CLK_X to D_X			125	ns	C_L = 150pF
t_{DXZ}	Delay Time, D_X to High Impedance State on TS Exit	50		165	ns	C_L = 0pF
t_{DTSL}	Delay to $\overline{TS}_X$ Low	30		185	ns	$0 \leq C_L \leq$ 150pF
t_{DTSH}	Delay to $\overline{TS}_X$ Off	30		185	ns	C_L = 0pF
t_{SSX}	Set-Up Time, SIG_X to CLK_X	100			ns	
t_{HSX}	Hold Time, CLK_X to SIG_X	100			ns	
t_{SFR}	Set-Up Time, FS_R to CLK_R	100			ns	
t_{HFR}	Hold Time, CLK_R to FS_R	100			ns	
t_{SDR}	Set-Up Time, D_R to CLK_R	40			ns	
t_{HDR}	Hold Time, CLK_R to D_R	30			ns	
t_{DSR}	Delay Time, CLK_R to SIG_R			300	ns	C_L = 100pF

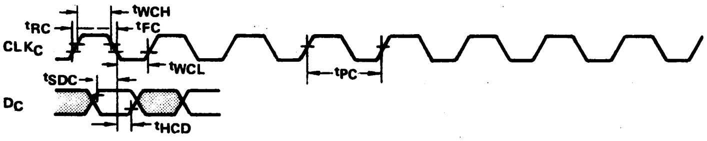
HC-5510 Pin Assignments

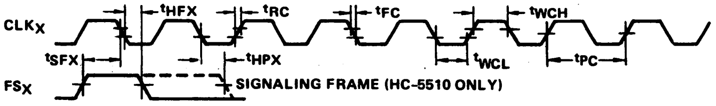
PIN NO.	SYMBOL	DESCRIPTION
1	SC1	Internally connected to GNDA.
2	SC2	Connects VF_X to an external sample / hold capacitor if fitted for use with pin compatible NMOS CODEC. Insures gain compatibility.
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin. Must be same potential as GNDD.
6	SIG_R	Receive signaling bit output. During receive signaling frames the least significant (last) bit shifted into D_R is internally latched and appears at this output-SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
7	NC	Unused
8	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
9	PDN	TTL output level which goes high when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
10	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15µs after the end of the decode time slot.
11	NC	Unused
12	NC	Unused
13	GNDD	Digital ground. All digital levels are referenced to this pin. Must be same potential as GNDA.
14	D_X	Serial PCM "Three-State" output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
15	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external "Three-State" bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
16	V_{CC}	5V (±5%) input.
17	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_X or CLK_C.
18	FS_R	Decoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.
19	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_R or CLK_C.
20	FS_X	Encoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_X to two or more cycles of CLK_X signifies a transmit signaling frame.
21	SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the least significant (last) bit of PCM data.
22	V_{BB}	-5V (±5%) input.
23	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
24	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the HC-5510/HC-5511 into the fixed time slot mode.

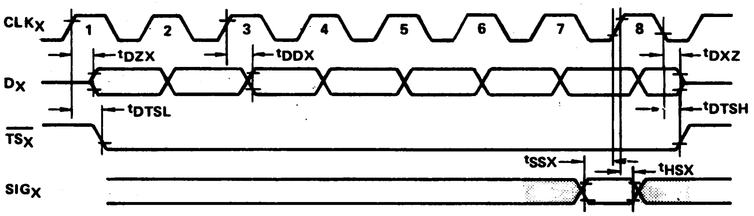
HC-5511 Pin Assignments

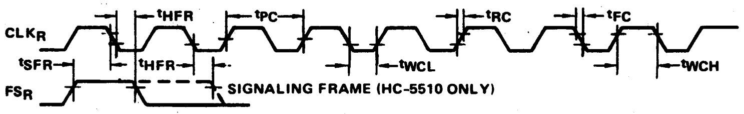
PIN NO.	SYMBOL	DESCRIPTION
1	SC1	Internally connected to GNDA.
2	SC2	Connects VF_X to an external sample / hold capacitor if fitted for use with pin compatible NMOS CODEC. Insures gain compatibility.
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin. Must be same potential as GNDD.
6	NC	Unused
7	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
8	PDN	Open drain output which turns off when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
9	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15μs after the end of the decode time slot.
10	NC	Unused
11	NC	Unused
12	GNDD	Digital ground. All digital levels are referenced to this pin. Must be same potential as GNDA.
13	D_X	Serial PCM "Three-State" output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most signficant bit first, on the rising edge of CLK_X.
14	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external "Three-State" bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
15	V_{CC}	5V (±5%) input.
16	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_X or CLK_C.
17	FS_R	Decoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_R cycle wide.
18	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536MHz, 1.544MHz, or 2.048MHz. May be asynchronous with CLK_R or CLK_C.
19	FS_X	Encoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_X cycle wide.
20	V_{BB}	-5V (±5%) input.
21	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
22	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the HC-5510/HC-5511 into the fixed time slot mode.

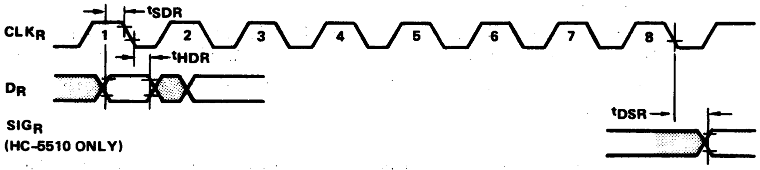
Timing Waveforms


tRC
tWCH
tFC
CLKC
tWCL
tPC
tSDC
DC
tHCD

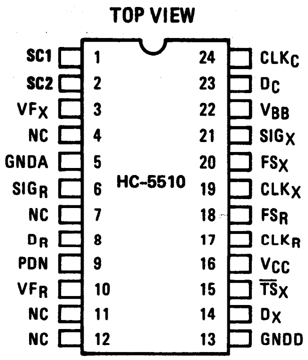

CLKX
tHFX
tRC
tFC
tWCH
tSFX
tHPX
tWCL
tPC
FSX
SIGNALING FRAME (HC-5510 ONLY)

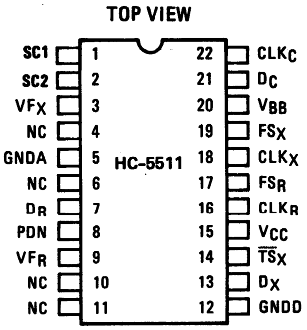

CLKX
1
2
3
4
5
6
7
8
DX
tDZX
tDDX
tDXZ
tDTSL
tDTSH
$\overline{TS}_X$
tSSX
tHSX
SIGX


CLKR
tHFR
tPC
tRC
tFC
tSFR
tHFR
tWCL
tWCH
FSR
SIGNALING FRAME (HC-5510 ONLY)


CLKR
tSDR
1
2
3
4
5
6
7
8
tHDR
DR
SIGR
(HC-5510 ONLY)
tDSR

Pinouts


TOP VIEW
HC-5510
SC1 1
SC2 2
VFX 3
NC 4
GNDA 5
SIGR 6
NC 7
DR 8
PDN 9
VFR 10
NC 11
NC 12
24 CLKC
23 DC
22 VBB
21 SIGX
20 FSX
19 CLKX
18 FSR
17 CLKR
16 VCC
15 $\overline{TS}_X$
14 DX
13 GNDD


TOP VIEW
HC-5511
SC1 1
SC2 2
VFX 3
NC 4
GNDA 5
NC 6
DR 7
PDN 8
VFR 9
NC 10
NC 11
22 CLKC
21 DC
20 VBB
19 FSX
18 CLKX
17 FSR
16 CLKR
15 VCC
14 $\overline{TS}_X$
13 DX
12 GNDD

Functional Description

Power-Up

Upon application of power, internal circuitry initializes the CODEC and places it into the power-down mode. No sequencing of 5V or -5V is required. In the power-down mode, all non-essential circuits are deactivated, the "Three-State" PCM data output D_X is placed in the high impedance state and the receive signaling output of the HC-5510, SIG_R, is reset to logical zero. Once in the power-down mode, the method of activating the HC-5510/5511 depends on the chosen mode of operation, time slot assignment or fixed time slot.

Time Slot Assignment Mode

The time slot assignment mode of operation is selected by maintaining CLK_C in a normally low state. The state of the CODEC is updated by pulsing CLK_C eight times within a period of 125μs or less. The falling edge of each clock pulse shifts the data on the D_C input into the CODEC. The first two control bits determine if the subsequent control bits B3-B8 are to specify the time slot for the encoder (B1 = 0), the decoder (B2 = 0) or both (B1 and B2 = 0) or if the CODEC is to be placed into the power-down mode (B1 and B2 = 1). The desired action will take place upon the occurrence of the second frame sync pulse following the first pulse of CLK_C. Assigning a time slot to either the encoder or decoder will automatically power-up the entire CODEC circuit. The D_X output and D_R input, however, will be inhibited for one additional frame to allow the analog circuitry time to stabilize. If separate time slots are to be assigned to the encoder and the decoder, the encoder time slot should be assigned first. This is necessary because up to four frames are required to assign both time slots separately, but only three frames are necessary to activate the D_X output. If the encode time slot has not been updated, the PCM data will appear at the output pin during the previously assigned time slot which may now be assigned to another CODEC.

Fixed Time Slot Mode

There are several ways in which the HC-5510/5511 may operate in the fixed time slot mode. The first and easiest method is to leave CLK_C disconnected or to connect CLK_C to V_{CC}. In this situation, D_C behaves as a power-down input. When D_C goes low, both encode and decode time slots are set to one on the second subsequent frame sync pulse. Time slot one corresponds to the eight CLK_X or CLK_R cycles starting one cycle from the nominal leading edge of FS_X or FS_R respectively. As in the time slot assignment mode, the D_X output is inhibited for one additional frame after the circuit is powered up. A logical "1" on D_C powers the CODEC down on the second subsequent FS_X pulse.

A second fixed time slot method is to operate CLK_C continuously. Placing a "1" on D_C will then cause the serial control register to fill up with ones. With B1 and B2 equal to "1" the CODEC will power-down. Placing a "0" on D_C will cause the serial control register to fill up with zeroes, assigning time slot one to both the encoder and decoder and powering up the device. One important restriction with this method of operation is that the rising transition of D_C must occur at least 8 cycles of CLK_C prior to FS_X. If this restriction is not followed, it is possible that on the frame prior to power-down, the encoder could be assigned to an incorrect time slot (e.g., 1, 3, 7, 15 or 31), resulting in a possible PCM bus conflict.

Serial Control Port

When the HC-5510/HC-5511 is operated in the time slot assignment mode or the fixed time slot mode with continuous clock, the data on D_C is shifted into the serial control register, bit 1 first. In the time slot assignment mode, depending on B1 and B2, the data in the RCV or XMT time slot registers is updated at the second FS_R or FS_X pulse after the first CLK_C pulse, or the CODEC is powered down. In the continuous clock fixed time slot mode, the CODEC is powered up or down at every second FS_R or FS_X pulse. The control register data is interpreted as follows:

B1	B2	ACTION
0	0	Assign Time Slot to Encoder and Decoder
0	1	Assign Time Slot to Encoder
1	0	Assign Time Slot to Decoder
1	1	Power-Down CODEC

B3	B4	B5	B6	B7	B8	TIME SLOT
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64

During the power-down command, bits 3 through 8 are ignored. Note that with 64 possible time slot assignments it is frequently possible to assign a time slot which does not exist. This can be useful to disable an encoder or decoder without powering down the CODEC.

Signaling

The HC-5510 μ-law CODEC contains circuitry to insert and extract signaling information for the PCM data. The transmit signaling frame is signified by widening the FS_X pulse from one cycle of CLK_X to two or more cycles.

When this occurs, the data present on the SIG_X input at the eighth clock pulse of the encode time slot is inserted into the last bit of the PCM data stream. A receive signaling frame is indicated in a similar fashion by widening the FS_R pulse to two or more cycles of CLK_R.

During a receive signaling frame, the last PCM bit shifted in is latched into a flip-flop and appears at the SIG_R output. This output will remain unchanged until the next signaling frame, until a power-down is executed or until power is removed from the device. Since the least significant bit of the PCM data is lost during a signaling frame, the decoder interprets the bit as a "1/2" (i.e., half way between a "0" and a "1"). This minimizes the noise and distortion due to the signaling.

Functional Description (Continued)

Encoding Delay

The encoding process begins immediately at the end of the encode time slot and is concluded no later than 17 time slots later. In normal applications, this PCM data is not shifted out until the next time slot 125μs later, resulting in an encoding delay of 125μs. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048MHz clock, the FS_X rate could be increased to 15kHz, reducing the delay from 125μs to 67μs.

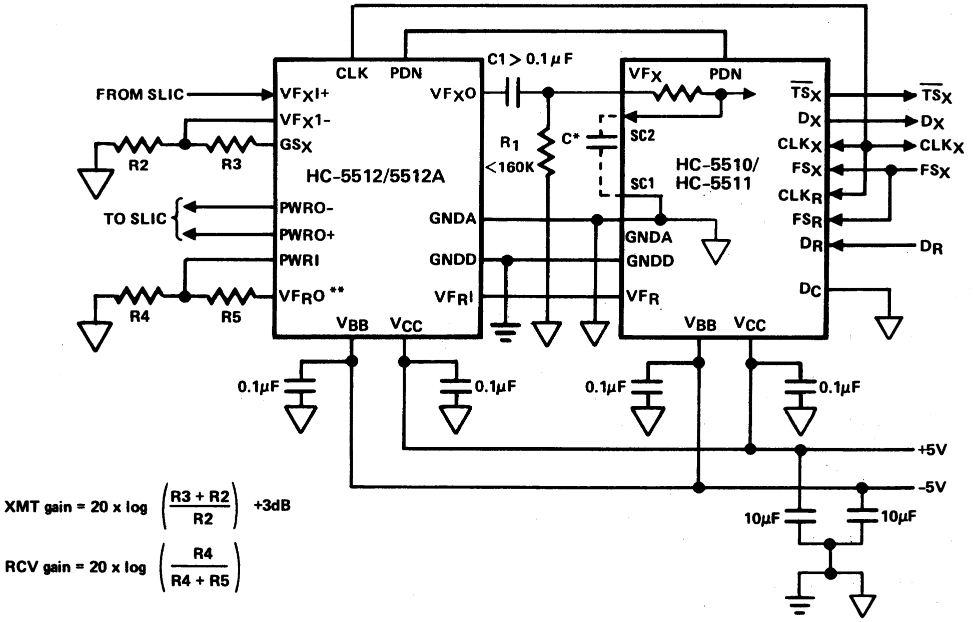
Decoding Delay

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 CLK_R cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or 81μs for a 1.544MHz system with an 8kHz frame rate or 76μs for a 2.048MHz system with an 8kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

Typical Application

A typical application of the HC-5510/11 used in conjunction with the HC-5512/12A PCM filter is shown. The values of resistor R1 and DC blocking capacitor C1, are noncritical. The capacitor value should exceed 0.1μF, R1 should be less than 160kΩ, and the product R1 x C1 should exceed 4ms.

Typical Application



FROM SLIC
TO SLIC
R2
R3
R4
R5
CLK
PDN
VFXI+
VFXI-
GSX
VFXO
HC-5512/5512A
PWRO-
PWRO+
PWRI
VFRO **
GNDA
GNDD
VFRI
VBB
VCC
C1 > 0.1μF
R1
<160K
C*
VFX
PDN
SC2
SC1
HC-5510/
HC-5511
GNDA
GNDD
VFR
VBB
VCC
TSX
DX
CLKX
FSX
CLKR
FSR
DR
DC
TSX
DX
CLKX
FSX
DR
0.1μF
0.1μF
0.1μF
0.1μF
+5V
-5V
10μF
10μF

$$\text{XMT gain} = 20 \times \log \left(\frac{R3 + R2}{R2}\right) + 3\text{dB}$$

$$\text{RCV gain} = 20 \times \log \left(\frac{R4}{R4 + R5}\right)$$

The power supply decoupling capacitors should be 0.1μF. In order to take advantage of the excellent noise performance of the HC-5510/HC5511/HC-5512, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines. The above application is configured for a fixed time slot mode of operation.

* The external sample/hold capacitor required for use with pin-compatible NMOS CODECs introduces attenuation due to the capacitive divider formed with C1. The SC pins connect VF_X to this sample/hold capacitor (via a 300 Ω resistor) to ensure gain compatibility. The HC-5510/11 itself does not require an external sample/hold capacitor.

** For use with Monolithic Slics, such as HC-5502A, HC-5504 and HC-5508. The output may be taken directly at VF_RO.

HARRIS

HC-5512/5512A

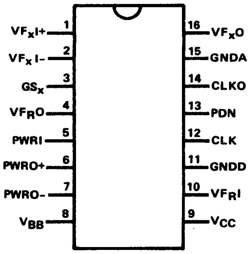
PCM Monolithic Filter

FEATURES

- EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- +5V, -5V POWER SUPPLIES
- LOW POWER CONSUMPTION:
  45mW (600Ω 0dBm LOAD)
  30mW (POWER AMPS DISABLED)
- POWER DOWN MODE: 0.5mW
- 20dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUTS PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING

PINOUT

DUAL-IN-LINE PACKAGE
TOP VIEW


VF_XI+ 1
VF_XI- 2
GS_X 3
VF_RO 4
PWRI 5
PWRO+ 6
PWRO- 7
V_{BB} 8
16 VF_XO
15 GNDA
14 CLKO
13 PDN
12 CLK
11 GNDD
10 VF_RI
9 V_{CC}

DESCRIPTION

The HC-5512/HC-5512A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

FUNCTIONAL DIAGRAM

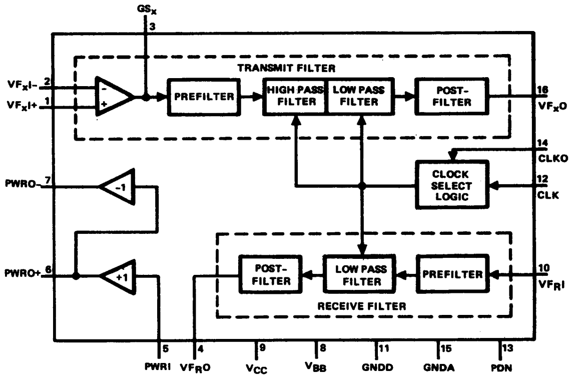

GS_X
3
TRANSMIT FILTER
VF_XI- 2
VF_XI+ 1
-
+
PREFILTER
HIGH PASS FILTER
LOW PASS FILTER
POST-FILTER
16 VF_XO
14 CLKO
CLOCK SELECT LOGIC
12 CLK
PWRO- 7
-1
PWRO+ 6
+1
POST-FILTER
LOW PASS FILTER
PREFILTER
10 VF_RI
RECEIVE FILTER
5 PWRI
4 VF_RO
9 V_{CC}
8 V_{BB}
11 GNDD
15 GNDA
13 PDN

FIGURE 1

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±7V
Power Dissipation	1W/Package
Input Voltage	±7V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	-25°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A = 0°C to 75°C, V_{CC} = 5.0V±5%, V_{BB} = -5.0V ±5%, clock frequency is 1.544MHz. Typical parameters are specified at T_A = 25°C, V_{CC} = 5.0V, V_{BB} = -5.0V. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{BB0}	V_{BB} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
I_{CC2}	V_{CC} Operating Current	Note 1		4.6	6.4	mA
I_{BB2}	V_{BB} Operating Current	Note 1		4.6	6.4	mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	$V_{BB} \leq V_{IN} \leq V_{CC}$	−10		10	μA
I_{INP}	Input Current, PDN	$V_{BB} \leq V_{IN} \leq V_{CC}$	−100			μA
I_{INO}	Input Current, CLK0	$V_{BB} \leq V_{IN} \leq V_{CC}$ -0.5V	−10		−0.1	μA
V_{IL}	Input Low Voltage, CLK, PDN		0		0.8	V
V_{IH}	Input High Voltage, CLK, PDN		2.2		V_{CC}	V
V_{ILO}	Input Low Voltage, CLK0		V_{BB}		$V_{BB}+0.5$	V
V_{IIO}	Input Intermediate Voltage, CLK0		−0.8		0.8	V
V_{IHO}	Input High Voltage, CLK0		$V_{CC}-0.5$		V_{CC}	V
TRANSMIT INPUT OP AMP						
IB_xI	Input Leakage Current, VF_xI	$V_{BB} \leq VF_xI \leq V_{CC}$	−100		100	nA
RI_xI	Input Resistance, VF_xI	$V_{BB} \leq VF_xI \leq V_{CC}$	10			MΩ
VOS_xI	Input Offset Voltage, VF_xI	$-2.5V \leq V_{IN} \leq +2.5V$	−20		20	mV
V_{CM}	Common-Mode Range, VF_xI		-2.5		2.5	V
CMRR	Common-Mode Rejection Ratio	$-2.5V \leq V_{IN} \leq 2.5V$	60			dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}		60			dB
R_{OL}	Open Loop Output Resistance, GS_x			1		kΩ
R_L	Minimum Load Resistance, GS_x		10			kΩ
C_L	Maximum Load Capacitance, GS_x				100	pF
VO_xI	Output Voltage Swing, GS_x	$R_L \geq 10k$	±2.5			V
A_{VOL}	Open Loop Voltage Gain, GS_x	$R_L \geq 10k$	5,000			V/V
F_c	Open Loop Unity Gain Bandwidth, GS_x			2		MHz

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 25°C. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT FILTER (Transmit filter input op amp set to the non-inverting unity gain mode, with VF_xI = 1.09 Vrms unless otherwise noted.)						
RL_x	Minimum Load Resistance, VF_xO	$-3.2V < V_{OUT} < 3.2V$	10			kΩ
CL_x	Load Capacitance, VF_xO				100	pF
RO_x	Output Resistance, VF_xO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_xO	f = 1 kHz, VF_xI+ = 0 Vrms	30			dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO	Same as Above	35			dB
GA_x	Absolute Gain	f = 1 kHz (HC-5512A)	2.9	3.0	3.1	dB
		f = 1 kHz (HC-5512)	2.875	3.0	3.125	dB
GR_x	Gain Relative to GA_x	Below 50 Hz			−35	dB
		50 Hz		−41	−35	dB
		60 Hz		−35	−30	dB
		200 Hz (HC-5512A)	−1.5		0	dB
		200 Hz (HC-5512)	−1.5		0.05	dB
		300 Hz to 3 kHz (HC-5512A)	−0.125		0.125	dB
		300 Hz to 3 kHz (HC-5512)	−0.15		0.15	dB
		3.3 kHz	−0.35		0.03	dB
		3.4 kHz	−0.70		−0.1	dB
		4.0 kHz		−15	−14	dB
		4.6 kHz and Above			−32	dB
DA_x	Absolute Delay at 1 kHz				230	μs
DD_x	Differential Envelope Delay from 1 kHz to 2.6 kHz				60	μs
DP_x1	Single Frequency Distortion Products				−48	dB
DP_x2	Distortion at Maximum Signal Level	0.16 Vrms, 1 kHz Signal Applied to VF_xI+, Gain = 20 dB, R_L = 10k			−45	dB
NC_x1	Total C Message Noise at VF_xO			2	5	dBrnc0
NC_x2	Total C Message Noise at VF_xO	Gain Setting Op Amp at 20 dB, Non-Inverting, Note 3 T_A = 0°C to 70°C		3	6	dBrnc0
GA_xT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain	V_{CC} = 5.0V ± 5% V_{BB} = −5.0V ± 5%		0.01		dB/V
CT_{RX}	Crosstalk, Receive to Transmit $20 \log \frac{VF_xO}{VF_RO}$	Receive Filter Output = 2.2 Vrms VF_xI+ = 0 Vrms, f = 0.2 kHz to 3.4 kHz Measure VF_xO			−70	dB
GR_xL	Gaintracking Relative to GA_x	Output Level = +3 dBm0	−0.1		0.1	dB
		+2 dBm0 to −40 dBm0	−0.05		0.05	dB
		−40 dBm0 to −55 dBm0	−0.1		0.1	dB

AC ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = 25°C. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54 Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-3.2V \le V_{IN} \le 3.2V$	−100		100	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	3	Ω
CL_R	Load Capacitance, VF_RO				100	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1 kHz	35			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	−200		200	mV
GA_R	Absolute Gain	f = 1 kHz (HC-5512A)	−0.1	0	0.1	dB
		f = 1 kHz (HC-5512)	−0.125	0	0.125	dB
GR_R	Gain Relative to Gain at 1 kHz	Below 300 Hz			0.125	dB
		300 Hz to 3.0 kHz (HC-5512A)	−0.125		0.125	dB
		300 Hz to 3.0 kHz (HC-5512)	−0.15		0.15	dB
		3.3 kHz	−0.35		0.03	dB
		3.4 kHz	−0.7		−0.1	dB
		4.0 kHz			−14	dB
		4.6 kHz and Above			−32	dB
DA_R	Absolute Delay at 1 kHz				100	μs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1 kHz			−48	dB
DP_R2	Distortion at Maximum Signal Level	2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, R_L = 10k			−45	dB
NC_R	Total C-Message Noise at VF_RO			3	5	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_xO}$	Transmit Filter Output = 2.2 Vrms VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz Measure VF_RO			−70	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3 dBm0	−0.1		0.1	dB
		+2 dBm0 to −40 dBm0	−0.05		0.05	dB
		−40 dBm0 to −55 dBm0	−0.1		0.1	dB
		Note 5				

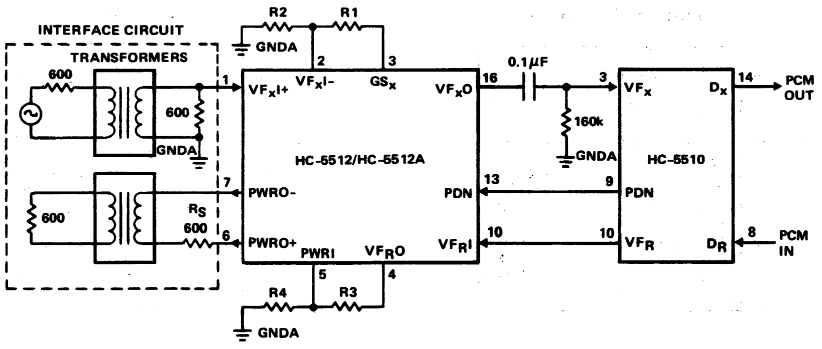
AC ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = 25^oC$. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-3.2V \le V_{IN} \le 3.2V$	0.1		3	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO +, PWRO −	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO +, PWRO −				500	pF
GA_P+	Gain, PWRI to PWRO +	$R_L = 600\Omega$ Connected Between PWRO + and PWRO −, Input Level = 0 dBm0 (Note 4)		1		V/V
GA_P-	Gain, PWRI to PWRO −			−1		V/V
GR_PL	Gaintracking Relative to 0 dBm0 Output Level	V = 2.05 Vrms, $R_L = 600\Omega$ (Notes 4, 5)	−0.1		0.1	dB
		V = 1.75 Vrms, $R_L = 300\Omega$	−0.1		0.1	dB
S/D_P	Signal/Distortion	V = 2.05 Vrms, $R_L = 600\Omega$ (Notes 4, 5)			−45	dB
		V = 1.75 Vrms, $R_L = 300\Omega$			−45	dB
VOSP	Output DC Offset, PWRO +, PWRO −	PWRI Connected to GNDA	−50		50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	45			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600Ω connected from PWRO+ to PWRO−.
Note 2: Voltage input to receive filter at 0V, VF_RO connected to PWRI, 600Ω from PWRO+ to PWRO−. Output measured from PWRO+ to PWRO−.
Note 3: The 0dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.
Note 4: The odBm0 level for the power amplifiers is load dependent. For R_L = 600Ω to GNDA the 0dBm0 level is 1.43 Vrms measured at the amplifier output for R_L = 300Ω the 0dBm0 level is 1.22Vrms.
Note 5: VF_RO connected to PWRI, input signal applied to VF_RI.

INTERFACE CIRCUIT FOR HC-5510 CODEC



Note 1: Transmit voltage gain = $\frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain) (R1 + R2 ≥ 10k).

Note 2: Receive gain = $\frac{R4}{R3 + R4}$
(R3 + R4 ≥ 10k)

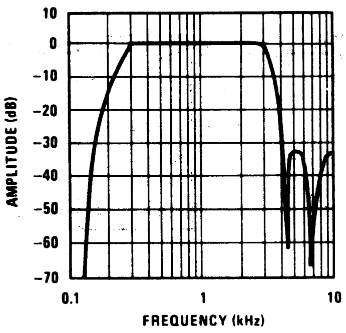
Note 3: In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

PIN ASSIGNMENTS

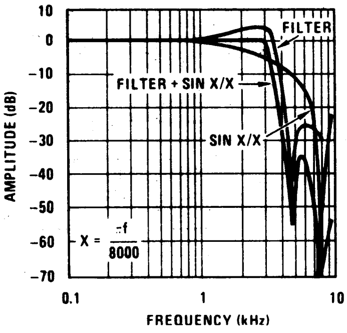
Pin No.	Name	Function
1	VF_XI+	The non-inverting input to the transmit filter stage.
2	VF_XI-	The inverting input to the transmit filter stage.
3	GS_X	The output used for gain adjustments of the transmit filter.
4	VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	PWRI	The input to the receive filter differential power amplifier.
6	PWRO +	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
7	PWRO −	The inverting output of the receive filter power amplifier. This output can be used with PWRO + to differentially drive a transformer hybrid.
8	V_{BB}	The negative power supply pin. Recommended input is −5V.
9	V_{CC}	The positive power supply pin. The recommended input is 5V.
10	VF_RI	The input pin for the receive filter stage.
11	GNDD	Digital ground input pin. All digital signals are referenced to this pin.
12	CLK	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
13	$\overline{\text{PDN}}$	The input pin used to power down the HC-5512/12A during idle periods. Logic $\bar{1}$ (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency: **CLK** — **Connect CLK0 to:** 2048 kHz — V_{CC} 1544 kHz — GNDD 1536 kHz — V_{BB} An internal pull-up is provided.
15	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
16	VF_XO	The output of the transmit filter stage.

TYPICAL PERFORMANCE CHARACTERISTICS

Transmit Filter Stage



Receive Filter Stage



FUNCTIONAL DESCRIPTION

The HC-5512/12A monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/ Select Logic *(Figure 1)*. A brief description of the operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10MΩ , a voltage gain of greater than 5,000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10kΩ load in parallel with up to 100pF. The inputs and output of the amplifier are accessible for added flexibility. Noninverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a ±3.2V peak to peak signal into a 10kΩ load in parallel with up to 100pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband reejction and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 *(Figure 2)*. The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1mW. If the PWRI pin (pin 5) is connected to V_{BB}, the power amplifier output will enter a high impedance (tri-state) mode. Otherwise, the power amplifier output will be clamped to V_{BB}.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLK0 (pin 14) to V_{CC}, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and V_{BB} selects 1.536MHz.

APPLICATIONS INFORMATION

Gain Adjust

Figure 2 shows the signal path interconnections between the HC-5512/12A and HC-5510 single channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained for the HC-5512/12A filter when operated with system peak overload voltages of ±2.5V to ±3.2V at VF_XO. When interfacing to a PCM CODEC with a peak overload voltages outside this range, further gain or attenuation may be required.

For example, the HC-5512/12A filter can be used with the HC-5510/5511 series CODEC which has a 5.5V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between GNDA and GNDD and between the GNDA traces of adjacent filters and CODECs.

HARRIS

HC-5512C

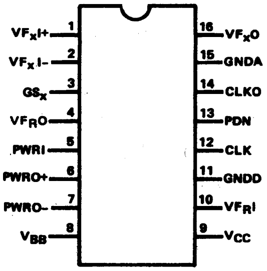
PCM or CVSD Monolithic Filter

FEATURES

- +5V, -5V POWER SUPPLIES
- LOW POWER CONSUMPTION:
  - 45mW (600Ω 0dBm LOAD)
  - 30mW (POWER AMPS DISABLED)
- POWER DOWN MODE: 0.5mW
- 20dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUTS PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING

PINOUT

DUAL-IN-LINE PACKAGE
TOP VIEW


VFXI+ 1
VFXI- 2
GSX 3
VFRO 4
PWRI 5
PWRO+ 6
PWRO- 7
VBB 8
16 VFXO
15 GNDA
14 CLKO
13 PDN
12 CLK
11 GNDD
10 VFRI
9 VCC

DESCRIPTION

The HC-5512C filter is a monolithic circuit containing both transmit and receive filters originally designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter lends itself well as a cost effective replacement of a discrete audio input/output filter for the continuously variable slope delta modulator (CVSD).

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high-pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stairstep signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

FUNCTIONAL DIAGRAM

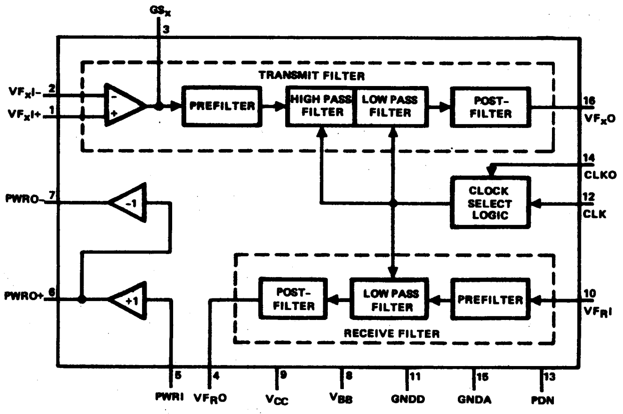

GSX
3
TRANSMIT FILTER
VFXI- 2
VFXI+ 1
PREFILTER
HIGH PASS FILTER
LOW PASS FILTER
POST-FILTER
16
VFXO
14
CLKO
CLOCK SELECT LOGIC
12
CLK
PWRO- 7
-1
PWRO+ 6
+1
POST-FILTER
LOW PASS FILTER
PREFILTER
10
VFRI
RECEIVE FILTER
5 PWRI
4 VFRO
9 VCC
8 VBB
11 GNDD
15 GNDA
13 PDN

FIGURE 1

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±7V
Power Dissipation	1W/Package
Input Voltage	±7V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{BB} = -5.0V ±5%, clock frequency is 1.544MHz. Typical parameters are specified at T_A = 25°C, V_{CC} = 5.0V, V_{BB} = -5.0V. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{BB0}	V_{BB} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	μA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.5	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.5	mA
I_{CC2}	V_{CC} Operating Current	Note 1		4.6	6.4	mA
I_{BB2}	V_{BB} Operating Current	Note 1		4.6	6.4	mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	GNDD ≤ V_{IN} ≤ V_{CC}	−10		10	μA
I_{INP}	Input Current, PDN	GNDD ≤ V_{IN} ≤ V_{CC}	−100			μA
I_{INO}	Input Current, CLK0	V_{BB} ≤ V_{IN} ≤ V_{CC} - 0.5V	−10		0	μA
V_{IL}	Input Low Voltage, CLK, PDN		0		0.8	V
V_{IH}	Input High Voltage, CLK, PDN		2.2		V_{CC}	V
V_{ILO}	Input Low Voltage, CLK0		V_{BB}		V_{BB}+0.5	V
V_{IIO}	Input Intermediate Voltage, CLK0		−0.8		0.8	V
V_{IHO}	Input High Voltage, CLK0		V_{CC}−0.5		V_{CC}	V
TRANSMIT INPUT OP AMP						
IB_xI	Input Leakage Current, VF_xI	V_{BB} ≤ VF_xI ≤ V_{CC}	−100		100	nA
RI_xI	Input Resistance, VF_xI	V_{BB} ≤ VF_xI ≤ V_{CC}	10			MΩ
VOS_xI	Input Offset Voltage, VF_xI		−20		20	mV
V_{CM}	Common-Mode Range, VF_xI		-2.5		2.5	V
CMRR	Common-Mode Rejection Ratio	-2.5V ≤ V_{IN} ≤ +2.5V	60			dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}		60			dB
R_{OL}	Open Loop Output Resistance, GS_x			1		kΩ
R_L	Minimum Load Resistance, GS_x		10			kΩ
C_L	Maximum Load Capacitance, GS_x				100	pF
VO_xI	Output Voltage Swing, GS_x	R_L ≥ 10k	±2.5			V
A_{VOL}	Open Loop Voltage Gain, GS_x	R_L ≥ 10k	3400			V/V
F_c	Open Loop Unity Gain Bandwidth, GS_x			2		MHz

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = 25^oC$. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT FILTER (Transmit filter input op amp set to the non-inverting unity gain mode, with VF_XI = 1.09 Vrms unless otherwise noted.)						
RL_x	Minimum Load Resistance	$-3.2V < V_{OUT} < 3.2V$	10			kΩ
CL_x	Load Capacitance, VF_xO				100	pF
RO_x	Output Resistance, VF_xO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_xO	$f = 1$ kHz, $VF_xI+ = 0$ Vrms	30			dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO	Same as Above	30			dB
GA_x	Absolute Gain	$f = 1$ kHz	2.8	3.0	3.2	dB
GR_x	Gain Relative to GA_x	Below 50 Hz			−35	dB
		50 Hz		−41	−35	dB
		60 Hz		−35	−30	dB
		200 Hz	−1.5		0.2	dB
		300 Hz to 3 kHz	−0.15		0.15	dB
		3.3 kHz	−0.45		0.25	dB
		3.4 kHz	−0.70		−0.1	dB
		4.0 kHz		−15	−14	dB
		4.6 kHz and Above			−32	dB
DA_x	Absolute Delay at 1 kHz				230	µs
DD_x	Differential Envelope Delay from 1 kHz to 2.6 kHz				60	µs
DP_x1	Single Frequency Distortion Products				−40	dB
DP_x2	Distortion at Maximum Signal Level	0.16Vrms,1 kHz Signal Applied to VF_xI+, Gain = 20 dB, $R_L = 10k$			−40	dB
NC_x1	Total C Message Noise at VF_xO with $V_{IN} = 0$				10	dBrnc0
NC_x2	Total C Message Noise at VF_xO with $V_{IN} = 0$	Gain Setting Op Amp at 20 dB, Non-Inverting, Note 3			10	dBrnc0
GA_xT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{RX}	Crosstalk, Receive to Transmit $20 \log \frac{VF_xO}{VF_RO}$	Receive Filter Output = 2.2 Vrms $VF_xI+ = 0$ Vrms, $f = 0.2$ kHz to 3.4 kHz Measure VF_xO			−60	dB
GR_xL	Gaintracking Relative to GA_x	Output Level = +3 dBm0	−0.1		0.1	dB
		+2 dBm0 to −40 dBm0	−0.05		0.05	dB
		−40 dBm0 to −55 dBm0	−0.1		0.1	dB

AC ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1KHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54 Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-2.5V \leq V_{IN} \leq 2.5V$	−100		100	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	3	Ω
CL_R	Load Capacitance, VF_RO				100	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1 kHz	30			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	−200		200	mV
GA_R	Absolute Gain	f = 1 kHz	−0.2	0	0.2	dB
GR_R	Gain Relative to Gain at 1 kHz	Below 300 Hz			0.125	dB
		300 Hz to 3.0 kHz	−0.15		0.15	dB
		3.3 kHz	−0.45		0.25	dB
		3.4 kHz	−0.7		−0.1	dB
		4.0 kHz			−14	dB
		4.6 kHz and Above			−32	dB
DA_R	Absolute Delay at 1 kHz				100	μs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1 kHz			−40	dB
DP_R2	Distortion at Maximum Signal Level	2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, R_L = 10k			−40	dB
NC_R	Total C-Message Noise at VF_RO				10	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_xO}$	Transmit Filter Output = 2.2 Vrms VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz Measure VF_RO			−60	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3 dBm0	−0.1		0.1	dB
		+2 dBm0 to −40 dBm0	−0.05		0.05	dB
		−40 dBm0 to −55 dBm0 Note 5	−0.1		0.1	dB

AC ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = 25°C. All parameters are specified for a signal level of 0 dBm0 at 1KHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-2.5V \le V_{IN} \le 2.5V$	0.1		3	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO+, PWRO−	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO+, PWRO−				500	pF
GA_P+	Gain, PWRI to PWRO+	$R_L = 600\Omega$ Connected Between PWRO+ and PWRO−, Input Level = 0 dBm0 (Note 4)		1		V/V
GA_P-	Gain, PWRI to PWRO−			−1		V/V
GR_PL	Gaintracking Relative to 0 dBm0 Output Level	V = 2.05 Vrms, $R_L = 600\Omega$ (Notes 4, 5)	−0.1		0.1	dB
		V = 1.75 Vrms, $R_L = 300\Omega$ (Notes 4, 5)	−0.1		0.1	dB
S/D_P	Signal/Distortion	V = 2.05 Vrms, $R_L = 600\Omega$ (Notes 4, 5)			−45	dB
		V = 1.75 Vrms, $R_L = 300\Omega$ (Notes 4, 5)			−45	dB
VOSP	Output DC Offset, PWRO+, PWRO−	PWRI Connected to GNDA	−50		50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	45			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600Ωconnected from PWRO+ to PWRO−.
Note 2: Voltage input to receive filter at 0V, VF_RO connected to PWRI, 600Ω from PWRO+ to PWRO−. Output measured from PWRO+ to PWRO−.
Note 3: The 0dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.
Note 4: The 0dBm0 level for the power amplifiers is load dependent. For $R_L = 600\Omega$ to GNDA the 0dBm0 level is 1.43 Vrms measured at the amplifier output for $R_L = 300\Omega$ the 0dBm0 level is 1.22Vrms.
Note 5: VF_RO connected to PWRI, input signal applied to VF_RI.

TYPICAL PERFORMANCE CHARACTERISTICS

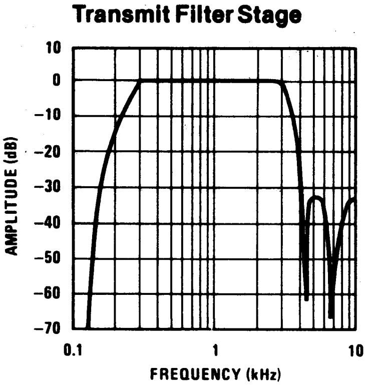


FIGURE 2

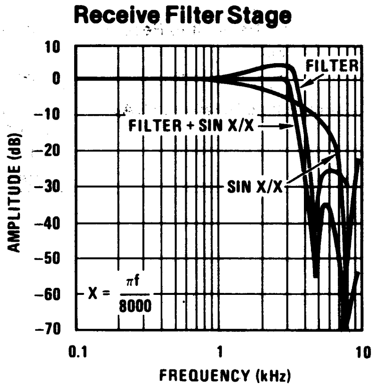


FIGURE 3

PIN ASSIGNMENTS

Pin No.	Name	Function
1	VF_XI+	The non-inverting input to the transmit filter stage.
2	VF_XI-	The inverting input to the transmit filter stage.
3	GS_X	The output used for gain adjustments of the transmit filter.
4	VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	PWRI	The input to the receive filter differential power amplifier.
6	PWRO +	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
7	PWRO −	The inverting output of the receive filter power amplifier. This output can be used with PWRO + to differentially drive a transformer hybrid.
8	V_{BB}	The negative power supply pin. Recommended input is −5V.
9	V_{CC}	The positive power supply pin. The recommended input is 5V.
10	VF_RI	The input pin for the receive filter stage.

Pin No.	Name	Function
11	GNDD	Digital ground input pin. All digital signals are referenced to this pin.
12	CLK	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
13	PDN	The input pin used to power down the HC-5512C during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency: **CLK** **Connect CLK0 to:** 2048 kHz V_{CC} 1544 kHz GNDD 1536 kHz V_{BB} An internal pull-up is provided.
15	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
16	VF_XO	The output of the transmit filter stage.

The HC-5512C monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/ Select Logic *(Figure 1)*. A brief description of the operation for each section is provided below.

Transmit filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10MΩ, a voltage gain of greater than 3,400, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10kΩ load in parallel with up to 100pF. The inputs and output of the amplifier are accessible for added flexibility. Noninverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by a least 40dB. The output of the transmit filter is capable of driving a ±2.5V peak to peak signal into a 10kΩ load in parallel with up to 100pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits in PCM applications. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 *(Figure 4)*. The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

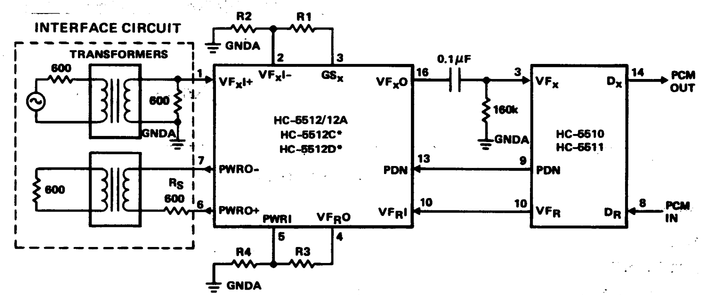
Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1mW. If the PWRI pin (pin 5) is connected to V_{BB}, the power amplifier output will enter a high impedance (tri-state) mode. Otherwise, the power amplifier output will be clamped to V_{BB}.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLKO (pin 14) to V_{CC}, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and V_{BB} selects 1.536MHz.

INTERFACE CIRCUIT FOR HC-5510 CODEC


INTERFACE CIRCUIT
TRANSFORMERS
600
600
GNDA
RS
600
600
R2
R1
GNDA
VFXI+
VFXI-
GSX
VFXO
HC-5512/12A
HC-5512C*
HC-5512D*
PWRO-
PDN
PWRO+
PWRI
VFRO
VFRI
R4
R3
GNDA
0.1µF
160k
GNDA
VFX
DX
HC-5510
HC-5511
PDN
VFR
DR
PCM OUT
PCM IN

Note 1: Transmit voltage gain = $\frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain) ($R1 + R2 \geq 10k$).

Note 2: Receive gain = $\frac{R4}{R3 + R4}$
($R3 + R4 \geq 10k$)

Note 3: In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

*Note 4: Although the HC-5512C/D may be used in some PCM telephone applications, it does not meet CCITT and D3/D4 specifications for PCM telephone transmission systems.

FIGURE 4

INTERFACE CIRCUIT FOR HC-55564 CVSD

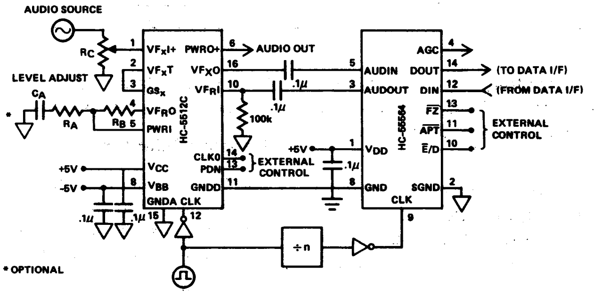

AUDIO SOURCE
RC
LEVEL ADJUST
CA
RA
RB
*
+5V
-5V
.1µ
.1µ
VFXI+
VFXT
GSX
VFRO
PWRI
VCC
VBB
GNDA
CLK
PWRO+
VFXO
VFRI
CLKO
PDN
GNDD
HC-5512C
AUDIO OUT
.1µ
.1µ
100k
EXTERNAL CONTROL
+5V
.1µ
AGC
AUDIN
DOUT
AUDOUT
DIN
FZ
APT
E/D
VDD
GND
SGND
CLK
HC-55564
(TO DATA I/F)
(FROM DATA I/F)
EXTERNAL CONTROL
÷n
*OPTIONAL
CLK. GEN.

FIGURE 5

APPLICATIONS INFORMATION

Gain Adjust

Figure 4 shows the signal path interconnections between the HC-5512C and HC-5510 single channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Figure 5 shows the signal path interconnections between the HC-5512C and the HC-55564 CVSD. For the circuit shown, the audio signal into the CVSD should be 1Vp-p over the 3.2kHz band to obtain a flat response. R_A, R_B and C_A form a simple lead lag filter at the output of the HC-5512C receive filter which introduces a pole and a zero at 3,3kHz to help compensate against the filters' inherent sin x/x characteristic. (See Figure 3). Note that the transmit side of the filter provides an inherent +3dB voltage gain, and the resistor RD, at VFRI causes a voltage loss from audio out to VFRI, owing to the 100KΩ output impedance of the CVSD at audio out. Generally, the higher the RD value used, the more thermal noise introduced to the circuit.

Optimum noise and distortion performance will be obtained for the HC-5512C filter when operated with system peak overload voltages of ±2.5V to ±3.2 at VF_XO and VF_RO. When interfacing to a PCM CODEC or CVSD with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the HC-5512/5512A/5512C/5512D filter can be used with the HC-5510/5511 series CODEC which has a 5.5V peak overload voltage, or with the HC-55564 CVSD which has a 4.0V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC or CVSD output are required in this case.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground of each filter and each CVSD should be connected to digital ground at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC, and each filter and CVSD is recommended. Ground loops should be avoided between GNDA and GNDD, between the GNDA traces of adjacent filters and CODECs, and between the analog ground traces of adjacent filters and CVSDs.

HARRIS HC-5512D

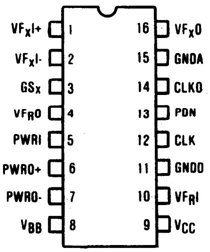
PCM or CVSD Monolithic Filter

Features

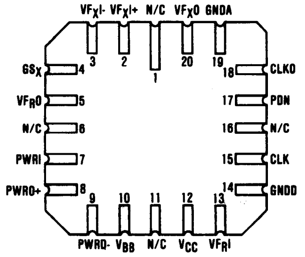
- **+5V, -5V Power Supplies**
- **Low Power Consumption:**
  - **45mW (600Ω 0dBm Load)**
  - **30mW (Power Amps Disabled)**
- **Power Down Mode:....................................... 0.5mW**
- **No External Anti-Aliasing Components**
- **Sin x/x Correction in Receive Filter**
- **50/60Hz Rejection in Transmit Filter**
- **TTL and CMOS Compatible Logic**
- **All Inputs Protected Against Static Discharge Due to Handling**
- **Military Temperature Range....... -55°C to +125°C**

Pinout

TOP VIEW
CERDIP


VFXI+ 1
VFXI- 2
GSX 3
VFRO 4
PWRI 5
PWRO+ 6
PWRO- 7
VBB 8
16 VFXO
15 GNDA
14 CLKO
13 PDN
12 CLK
11 GNDD
10 VFRI
9 VCC

BOTTOM VIEW
LCC


VFXI- VFXI+ N/C VFXO GNDA
3 2 1 20 19
GSX 4
VFRO 5
N/C 6
PWRI 7
PWRO+ 8
18 CLKO
17 PDN
16 N/C
15 CLK
14 GNDD
9 10 11 12 13
PWRO- VBB N/C VCC VFRI

Description

The HC-5512D filter is a monolithic circuit containing both transmit and receive filters originally designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter lends itself well as a cost effective replacement of a discrete audio input/output filter for CVSD/PCM/ADPCM/PAM speech filtering. Other applications include telephone line cards, modems and multiplexers.

The HC-5512D is a wider specification version of the HC-5512 that meets military requirements and most D3/D4 and CCITT specifications. To meet the Harris Military Dash -8 program (-55°C to +125°C), the HC-5512D undergoes a manufacturing process which requires more test, burn-in and inspection than the HC-5512.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

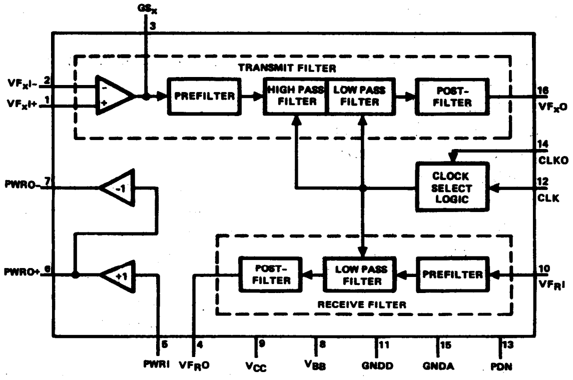
Transmit Filter Stage

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

Receive Filter Stage

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stairstep signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

Functional Diagram


GSX 3
TRANSMIT FILTER
VFXI- 2
VFXI+ 1
PREFILTER
HIGH PASS FILTER
LOW PASS FILTER
POST-FILTER
16 VFXO
14 CLKO
CLOCK SELECT LOGIC
12 CLK
PWRO- 7
-1
PWRO+ 6
+1
POST-FILTER
LOW PASS FILTER
PREFILTER
10 VFRI
RECEIVE FILTER
5 PWRI
4 VFRO
9 VCC
8 VBB
11 GNDD
15 GNDA
13 PDN

Absolute Maximum Ratings

Supply Voltages	±7V
Input Voltage	±7V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Unless otherwise noted, T_A = -55°C to +125°C, V_{CC} + 5.0V ±5%, Clock Frequency is 1.544MHz. Typical parameters are specified at T_A = + 25°C, V_{CC} = + 5.0V, V_{BB} = -5.0V. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	PDN = V_{DD}, Power Down Mode		50	200	μA
I_{BB0}	V_{BB} Standby Current	PDN = V_{DD}, Power Down Mode	-200	-50		μA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	7.0	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive	-7.0	-3.0		mA
I_{CC2}	V_{CC} Operating Current	Note 1		4.6	9.0	mA
I_{BB2}	V_{BB} Operating Current	Note 1	-9.0	-4.6		mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	GNDD $\leq V_{IN} \leq V_{CC}$	-10		10	μA
I_{INP}	Input Current, PDN	GNDD $\leq V_{IN} \leq V_{CC}$	-100		100	μA
I_{IN0}	Input Current, CLK0	GNDD $\leq V_{IN} \leq V_{CC}$ - 0.5V	-10		0	μA
V_{IL}	Input Low Voltage, CLK, PDN		0		0.8	V
V_{IH}	Input High Voltage, CLK, PDN		2.2		V_{CC}	V
V_{IL0}	Input Low Voltage, CLK0		V_{BB}		V_{BB} +0.5	V
V_{II0}	Input Intermediate Voltage, CLK0		-0.8		0.8	V
V_{IH0}	Input High Voltage, CLK0		V_{CC} -0.5		V_{CC}	V
TRANSMIT INPUT OP AMP						
IB_XI	Input Leakage Current, VF_XI	$V_{BB} \leq VF_XI \leq V_{CC}$	-100		100	nA
RI_XI	Input Resistance, VF_XI	$V_{BB} \leq VF_XI \leq V_{CC}$	10			MΩ
VOS_XI	Input Offset Voltage, VF_XI	-2.5V $\leq V_{IN} \leq$ +2.5V	-20		20	mV
V_{CM}	Common Mode Range, VF_XI		-2.5		2.5	V
CMRR	Common Mode Rejection Ratio	-2.5V $\leq V_{IN} \leq$ +2.5V	60			dB
PSRR+	Power Supply Rejection of V_{CC}		60			dB
PSRR-	Power Supply Rejection of VBB		60			dB
R_{OL}	Open Loop Output Resistance, GS_X			1		kΩ
R_L	Minimum Load Resistance, GS_X		10			kΩ
C_L	Maximum Load Capacitance, GS_X				100	pF
VO_XI	Output Voltage Swing, GS_X	$R_L \geq$ 10k	-2.5		2.5	V
A_{VOL}	Open Loop Voltage Gain, GS_X	$R_L \geq$ 10k	3000			V/V
F_C	Open Loop Unity Gain Bandwidth, GS_X			2		MHz

AC Electrical Characteristics

Unless otherwise noted, typical parameters are specified at T_A = +25°C. All parameters are specified for a signal level of 0dBm at 1kHz. The 0dBm level is assumed to be 1.54Vrms measured at the output of the transmit or receive filter.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT FILTER (Transmit filter input op amp set to the noninverting unity gain mode, with VFxI = 1.09Vrms unless otherwise noted)						
RL_X	Minimum Load Resistance	$-3.2V < V_{OUT} < 3.2V$	10			kΩ
CL_X	Load Capacitance, VF_XO				100	pF
RO_X	Output Resistance, VF_XO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_XO	f = 1kHz, VF_XI+ = 0Vrms	30			dB
PSRR2	V_{BB} Power Supply Rejection, VF_XO	Same as above	35			dB
GA_X	Absolute Gain	f = 1kHz	2.8	3.0	3.2	dB
GR_X	Gain Relative to GA_X	Below 50Hz			-35	dB
		50Hz		-41	-35	dB
		60Hz		-35	-30	dB
		200Hz	-1.5		0.15	dB
		300Hz to 3kHz	-0.15		0.15	dB
		3.3kHz	-0.35		0.15	dB
		3.4kHz	-1.0		0.0	dB
		4.0kHz		-15	-10	dB
		4.6kHz and Above			-30	dB
DA_X	Absolute Delay at 1kHz				230	μs
DD_X	Differential Envelope Delay from 1kHz to 2.6kHz				60	μs
DP_X1	Single Frequency Distortion Products				-40	dB
DP_X2	Distortion at Maximum Signal Level Level	0.16Vrms, 1kHz Signal Applied to VF_XI+, Gain = 20dB, R_L = 10k			-40	dB
NC_X1	Total C Message Noise at VF_XO with V_{IN} = 0				10	dBrnc0
NC_X2	Total C Message Noise at VF_XO with V_{IN} = 0	Gain Setting Op Amp at 20dB, Non-Inverting			10	dBrnc0
GA_XT	Temperature Coefficient of 1kHz Gain			0.0004		dB/°C
GA_XS	Supply Voltage Coefficient of 1kHz Gain			0.01		dB/V
CTR_X	Crosstalk, Receive to Transmit $20\log\frac{VF_XO}{VF_RO}$	Receive Filter Output = 2.2Vrms VF_XI+ = 0Vrms, f = 0.2kHz to 3.4kHz Measure VF_XO			-60	dB
GR_XL	Gaintracking Relative to GA_X	Output Level = +3dBm0 to -45dBm0	-0.1		0.1	dB
		-50dBm0	-0.15		0.15	dB
		-55dBm0	-0.25		0.25	dB

AC Electrical Characteristics (Continued)

Unless otherwise noted, typical parameters are specified at $T_A = +25^oC$. All parameters are specified for a signal level of 0dBm at 1kHz. The 0dBm level is assumed to be 1.54Vrms measured at the output of the transmit or receive filter.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54Vrms.)						
IB_R	Input Leakage Current, VF$_R$I	$-2.5V \leq V_{IN} \leq 2.5V$	-100		100	nA
RI_R	Input Resistance, VF$_R$I		10			MΩ
RO_R	Output Resistance, VF$_R$O			1	3	Ω
CL_R	Load Capacitance, VF$_R$O				100	pF
RL_R	Load Resistance, VF$_R$O		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF$_R$O	VF$_R$I Connected to GNDA f = 1kHz	35			dB
VOS_RO	Output DC Offset, VF$_R$O	VF$_R$I Connected to GNDA	-200		200	mV
GA_R	Absolute Gain	f = 1kHz	-0.2	0	0.2	dB
GR_R	Gain Relative to Gain at 1kHz	Below 300Hz			0.125	dB
		300Hz to 3.0kHz	-0.15		0.15	dB
		3.3kHz	-0.5		0.15	dB
		3.4kHz	-1.0		0.0	dB
		4.0kHz			-10	dB
		4.6kHz and Above			-30	dB
DA_R	Absolute Delay at 1kHz				100	µs
DD_R	Differential Envelope Delay 1kHz to 2.6kHz				100	µs
DP_R1	Single Frequency Distortion Products	f = 1kHz			-40	dB
DP_R2	Distortion at Maximum Signal Level	2.2Vrms Input to Sin x/x Filter, f = 1kHz, R_L = 10k			-40	dB
NC_R	Total C-Message Noise at VF$_R$O				10	dBrnc0
GA_RT	Temperature Coefficient of 1kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_XO}$	Transmit Filter Output = 2.2Vrms VF$_R$I = 0Vrms, f = 0.3kHz to 3.4kHz Measure VF$_R$O			-60	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3dBm0 to -45dBm0	-0.1		0.1	dB
		-50 dBm0	-0.15		0.15	dB
		-55 dBm0	-0.25		0.25	dB
		Note 3				

AC Electrical Characteristics (Continued)

Unless otherwise noted, typical parameters are specified at T_A = +25°C. All parameters are specified for a signal level of 0dBm at 1kHz. The 0dBm level is assumed to be 1.54Vrms measured at the output of the transmit or receive filter.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-2.5V \leq V_{IN} \leq 2.5V$	0.1		3	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO + PWRO-	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO + PWRO-				500	pF
$GA_{P}+$	Gain, PWRI to PWRO+	R_L = 600Ω Connected Between		1		V/V
$GA_{P}-$	Gain, PWRI to PWRO-	PWRO+ and PWRO-		-1		V/V
		Input Level = 0dBm0 (Note 2)				
GR_{PL}	Gaintracking Relative to 0dBm0	V = 2.05Vrms, R_L = 600Ω	-0.1		0.1	dB
	Output Level	V = 1.75Vrms, R_L = 300Ω (Notes 2,3)	-0.1		0.1	dB
S/D_P	Signal/Distortion	V = 2.05Vrms, R_L = 600Ω			-45	dB
		V = 1.75Vrms, R_L = 300Ω (Notes 2,3)			-45	dB
VOSP	Output DC Offset, PWRO + PWRO-	PWRI Connected to GNDA	-50		50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	45			dB

NOTES:

1. Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0dBm is delivered to 600Ω connected from PWRO+ to PWRO-.
2. The 0dBm0 level for the power amplifiers is load dependent. For R_L = 600Ω to GNDA the 0dBm0 level is 1.43Vrms measured at the amplifier output. For R_L = 300Ω the 0dBm0 level is 1.22Vrms.
3. VF_RO connected to PWRI, input signal applied to VF_RI.

Typical Performance Characteristics

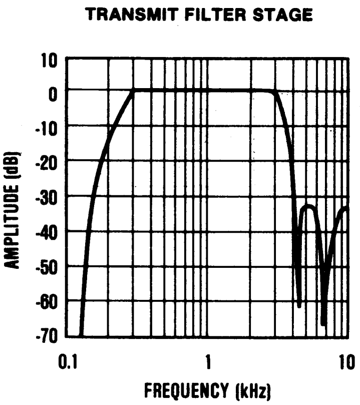


FIGURE 2.

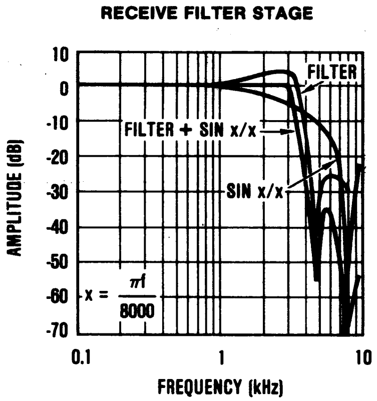


FIGURE 3.

Pin Assignments

PIN NO.	NAME	FUNCTION
1	VF_XI+	The non-inverting input to the transmit filter stage.
2	VF_XI-	The inverting input to the transmit filter stage.
3	GS_X	The output used for gain adjustments of the transmit filter.
4	VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	PWRI	The input to the receive filter differential power amplifier.
6	PWRO+	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
7	PWRO-	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
8	V_{BB}	The negative power supply pin. Recommended input is -5V.
9	V_{CC}	The positive power supply pin. Recommended input is 5V.
10	VF_RI	The input pin for the receive filter stage.
11	GNDD	Digital ground input pin. All digital signals are referenced to this pin
12	CLK	Master input clock. Input frequency can be selected as 2.048MHz, 1.544MHz or 1.536MHz.
13	PDN	The input pin used to power down the HC-5512D during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency: **CLK** — **Connect CLK0 to:** 2048kHz — VCC 1544kHz — GNDD 1536kHz — VBB An internal pull-up is provided.
15	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
16	VFxO	The output of the transmit filter stage.

Functional Description

The HC-5512D monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (Figure 1). A brief description of the operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10MΩ, a voltage gain of greater than 3,000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10kΩ load in parallel with up to 25pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a ±2.5V peak to peak signal into a 10kΩ load in parallel with up to 25pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits in PCM applications. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3 and R4 (Figure 4). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

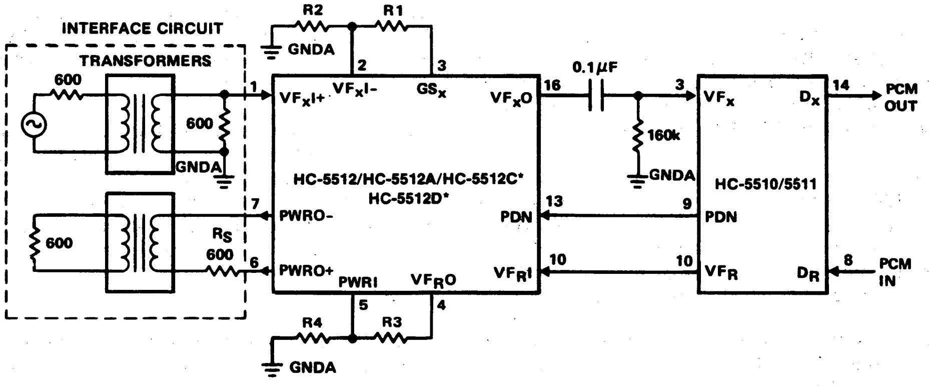
Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1mW. If the PWRI pin (pin 5) is connected to VBB, the power amplifier output will enter a high impedance (three-state) mode. Otherwise, the power amplifier output will be clamped to V_{BB}.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLKO (pin 14) to VCC, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and VBB selects 1.536MHz.

Interface Circuit for HC-5510 CODEC


INTERFACE CIRCUIT
TRANSFORMERS
600
600
GNDA
600
RS 600
R2
R1
GNDA
2
3
1
7
6
VFXI+
VFXI-
GSX
VFXO
HC-5512/HC-5512A/HC-5512C*
HC-5512D*
PWRO-
PWRO+
PWRI
VFRO
PDN
VFRI
16
13
10
5
4
R4
R3
GNDA
0.1μF
160k
GNDA
3
9
10
VFX
PDN
VFR
HC-5510/5511
DX
DR
14
8
PCM OUT
PCM IN

Note 1. Transmit voltage gain = $\frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain) ($R1 + R2 \geq 10k$).

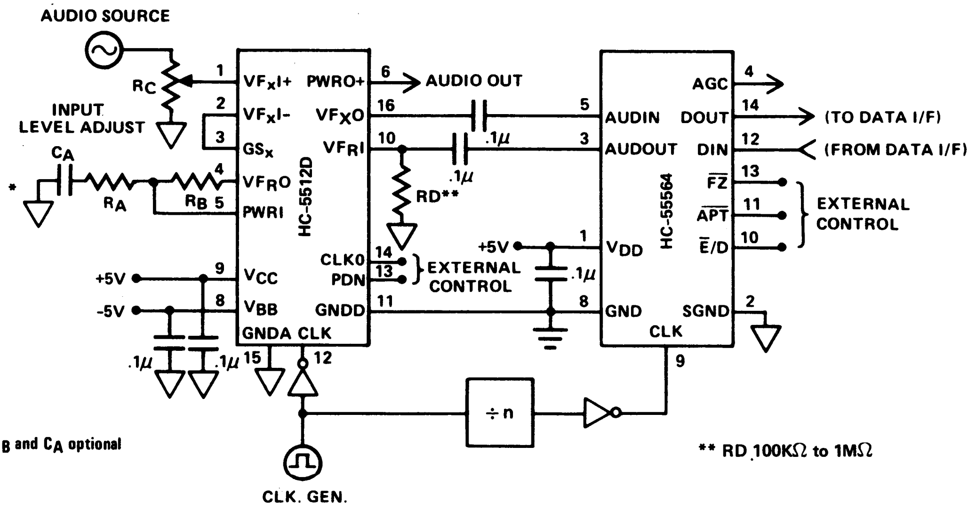
Note 2. Receive gain $\frac{R4}{R3 + R4}$
($R3 + R4 \geq 10k$)

Note 3. In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

*Note 4. The HC-5512C/HC-5512D may be used in some PCM telephone applications, it does meet most CCITT and D3/D4 specifications for PCM telephone transmission systems.

FIGURE 4.

Interface Circuit for HC-55564 CVSD


AUDIO SOURCE
RC
INPUT LEVEL ADJUST
CA
*
RA
RB
1
2
3
4
5
VFXI+
VFXI-
GSX
VFRO
PWRI
PWRO+
VFXO
VFRI
HC-5512D
6
AUDIO OUT
16
10
.1μ
.1μ
RD**
+5V
-5V
9
8
VCC
VBB
GNDA CLK
CLKO
PDN
GNDD
14
13
11
15
12
EXTERNAL CONTROL
+5V
.1μ
.1μ
.1μ
5
3
1
8
AUDIN
AUDOUT
VDD
GND
HC-55564
AGC
DOUT
DIN
FZ
APT
E/D
SGND
CLK
4
14
12
13
11
10
2
9
(TO DATA I/F)
(FROM DATA I/F)
EXTERNAL CONTROL
÷n
CLK. GEN.

*RA, RB and CA optional

** RD 100KΩ to 1MΩ

FIGURE 5.

Applications Information

Gain Adjust

Figure 4 shows the signal path interconnections between the HC-5512D and HC-5510 single channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Figure 5 shows the signal path interconnections between the HC-5512D and the HC-55564 CVSD. For the circuit shown, the audio signal into the CVSD should be 1Vp-p over the 3.2kHz band to obtain a flat response. R_A, R_B and C_A form a simple lead lag filter at the output of the HC-5512D receive filter which introduces a pole and a zero at 3.3kHz to help compensate against the filters' inherent sin x/x characteristic. (See Figure 3). Note that the transmit side of the filter provides an inherent +3dB voltage gain, and the resistor RD, at VFRI causes a voltage loss from audio out to VFRI, owing to the 100kΩ output impedance of the CVSD at audio out. Generally, the higher the RD value used, the more thermal noise introduced to the circuit.

Optimum noise and distortion performance will be obtained for the HC-5512D filter when operated with system peak overload voltages of ±2.5V to ±3.2 at VF_XO and VF_RO. When interfacing to a PCM CODEC or CVSD with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the HC-5512/12A/12C/12D filter can be used with the HC-5510/11 series CODEC which has a 5.5V peak overload voltage, or with the HC-55564 CVSD which has a 4.0V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC or CVSD output are required in this case.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground o feach filter and each CVSD should be connected to digital ground at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC, and each filter and CVSD is recommended. Ground loops should be avoided between GNDA and GNDD, between the GNDA traces of adjacent filters and CODECs, and between the analog ground traces of adjacent filters and CVSDs.

HARRIS

PRELIMINARY

HC-5552/53
HC-5554/57

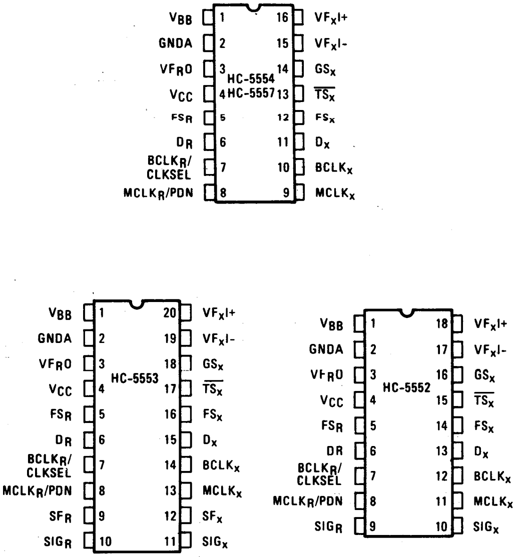
Monolithic CMOS
Serial Interface COFIDEC Family

Features

- Complete CODEC/FILTER (COFIDEC) Family
- HC-5552 - μ-Law with Short Frame Signaling (18 Pin)
- HC-5553 - μ-Law with Both Short and Long Frame Signaling (20 Pin)
- HC-5554 - μ-Law without Signaling (16 Pin)
- HC-5557 - μ-Law (16 Pin)
- Low Operation Power (60mW Typical)
- Low Standby Power (1mW Typical)
- ±5V Power Supplies
- Meets or Exceed all D3/D4 and CCITT Specifications
- TTL or CMOS Compatible Digital Interfaces
- PCM Data Serial Input/Output
- Synchronous or Asynchronous Operation
- Automatic Power-Down

Pinouts

TOP VIEW


HC-5554
HC-5557
VBB 1
GNDA 2
VFRO 3
VCC 4
FSR 5
DR 6
BCLKR/CLKSEL 7
MCLKR/PDN 8
9 MCLKX
10 BCLKX
11 DX
12 FSX
13 TSX
14 GSX
15 VFXI-
16 VFXI+
HC-5553
VBB 1
GNDA 2
VFRO 3
VCC 4
FSR 5
DR 6
BCLKR/CLKSEL 7
MCLKR/PDN 8
SFR 9
SIGR 10
11 SIGX
12 SFX
13 MCLKX
14 BCLKX
15 DX
16 FSX
17 TSX
18 GSX
19 VFXI-
20 VFXI+
HC-5552
VBB 1
GNDA 2
VFRO 3
VCC 4
FSR 5
DR 6
BCLKR/CLKSEL 7
MCLKR/PDN 8
SIGR 9
10 SIGX
11 MCLKX
12 BCLKX
13 DX
14 FSX
15 TSX
16 GSX
17 VFXI-
18 VFXI+

DUAL-IN-LINE PACKAGE

Description

The CODEC/FILTER (COFIDEC) family includes A-Law and μ-Law monolithic CODEC/FILTERS implemented with double-poly CMOS technology.

The transmit side of the device consists of:

- an amplifier with external gain adjustment
- an RC active prefilter to eliminate high frequency noise
- a switched capacitor band-pass filter including a notch filter at 55Hz to reject signals below 200Hz and above 3400Hz
- a charge redistribution coder which samples and encodes filtered signal in the companded μ-Law or A-Law PCM format
- a precision voltage reference
- an internal auto-zero network to cancel the transmit offset

The receive side of the device consists of:

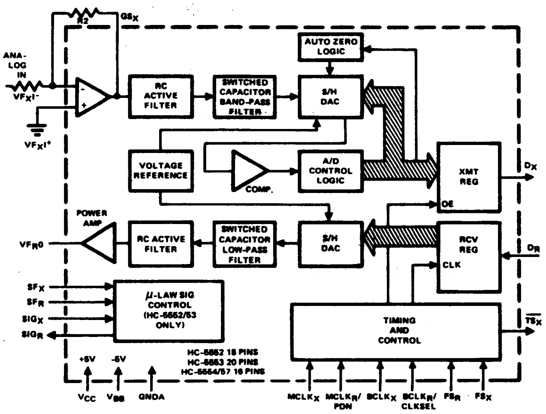
- an expanding decoder (A-Law or μ-Law) to reconstruct the analog signal
- a switched-capacitor low-pass filter which corrects for the sinx/x response of the decoder output and rejects signals above 3400Hz
- an RC active filter followed by a single ended power amplifier able to drive a 600X load
- a precision voltage reference

The PCM word is transmitted/received in a serial format compatible with industry standard.

The device is operated with two (transmit and receive) master clocks (1.536MHz, 1.544MHz or 2.048MHz) which may be asynchronous.

Also required are transmit and receive bit clock which may vary from 64KHz to 2.048MHz and transmit and receive frame sync pulses.

Functional Diagram


R2
GS_X
ANA-LOG IN
VF_XI^-
VF_XI^+
RC ACTIVE FILTER
SWITCHED CAPACITOR BAND-PASS FILTER
AUTO ZERO LOGIC
S/H DAC
VOLTAGE REFERENCE
COMP.
A/D CONTROL LOGIC
XMT REG
OE
D_X
POWER AMP
VF_R0
RC ACTIVE FILTER
SWITCHED CAPACITOR LOW-PASS FILTER
S/H DAC
RCV REG
CLK
D_R
SF_X
SF_R
SIG_X
SIG_R
μ-LAW SIG CONTROL (HC-5552/53 ONLY)
TIMING AND CONTROL
$\overline{TS_X}$
HC-5552 18 PINS
HC-5553 20 PINS
HC-5554/57 16 PINS
+5V
-5V
V_{CC}
V_{BB}
GNDA
$MCLK_X$
$MCLK_R$/ PDN
$BCLK_X$
$BCLK_R$/ CLKSEL
FS_R
FS_X

Pin Description

HC-5552 PIN #	HC-5553 PIN #	HC-5554 HC-5557 PIN #	NAME	FUNCTION
1	1	1	V_{BB}	Negative Power Supply V_{BB} = -5V ±5%.
2	2	2	GNPA	Ground Analog Ground. All signals are referenced to this pin.
3	3	3	VF_RO	Analog Output of the Receiver Filter.
4	4	4	V_{CC}	Positive Power Supply V_{CC} = +5V ±5.
5	5	5	FS_R	Receive Frame Sync Pulse. An 8KHz pulse train which enables the PCM word to be shifted into the receiver register.
6	6	6	D_R	Receive Data Input. The receiver register clocks in D_R input with bit clock falling edge following an FS_R rising edge.
7	7	7	$BCLK_R$ & CLKSEL	Bit Clock which shifts D_R data into the receiver register. May vary from 64KHz to 2.048MHz. Alternately may be a clock selection in synchronous mode. See Table 1 in Functional Description for synchronous operation.
8	8	8	$MCLK_R$ & PDN	Receive Master Clock must be 1.536, 1.544 or 2.084MHz. May be asynchronous with $MCLK_X$ and $BCLK_R$. If $MCLK_R$ is low, the COFIDEC operates in synchronous mode. If $MCLK_R$ is tied high, the COFIDEC is powered down.
	9		SF_R	When high during FS_R, SF_R indicates a receive signaling frame in long frame mode.
9	10		SIG_R	The signaling bit appears at this output after each receive signaling frame.
10	11		SIG_X	Signaling Data Input. This input is inserted in place of LSB or PCM word during signaling frame.
	12		SF_X	When high during FS_X, SF_X indicates a transmit signaling frame in long frame mode.
11	13	9	$MCLK_X$	Transmit Master Clock. Must be 1.536, 1.544 or 2.048MHz. May be asynchronous with $MCLK_R$. See table 1 in Functional Description for synchronous operation.
12	14	10	$BCLK_X$	Bit Clock. May vary from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$.
13	15	11	D_X	Three-State PCM data output enabled by FS_X.
14	16	12	FS_X	Transmit Frame Sync Pulse. An 8KHz pulse train which enables the PCM word to be shifted out through D_X with $BCLK_X$.
15	17	13	$\overline{TS_X}$	Open drain output. Pulled down durning time slot.
16	18	14	GS_X	Analog output of transmit amplifier. Used to set the gain.
17	19	15	VF_XI-	Inverting input of transmit amplifier.
18	20	16	VF_XI+	Non inverting input of transmit amplifier.

Power Up/Power Down

The COFIDEC is automatically placed into the power-down mode when V_{CC} and V_{BB} are applied to the circuit. All the analog blocks are de-activated and the D$_X$ and VF$_R$O outputs are in their high impedance state.

When a low level or a clock is applied on MCLK$_R$, the COFIDEC powers up.

During the first two frames, the D$_X$ output is in the high impedance state. To compensate rapidly for the offset of the transmit section, the auto-zero circuit is in quick capture mode during the first 512 frames and the input of the low pass filter is set to zero during the first 256 frames.

When a high level is applied on MCLK$_R$, the device goes into power down mode.

Transmit Section

The input of the transmit section is an operational amplifier whose gain can be externally adjusted. This amplifier exhibits low noise, wide bandwidth and low offset voltage (1mV typical). The input amplifier drives an anti-aliasing RC active filter. The switched capacitor band-pass filter is split into a 5th order elliptic low-pass filter and a 3rd order elliptic high-pass filter which includes a 55Hz notch filter to guarantee excellent line (50 or 60Hz) rejection. The structure of each filter is fully differential so that their performance is not affected by parasitic elements.

The A/D converter is of a companding type according to A (HC-5557) or μ (HC-5552/53/54) coding laws.

Receive Section

The receive section includes an expanding D/A converter according to A (HC-5557) or μ (HC-552/53/54) coding laws. The decoder is followed by a 5th order switched capacitor low-pass filter and an RC active filter.

As for the transmit part, the filters are fully differential. The output amplifier has a unity gain and can drive a 600Ω/500pF load.

Seperately trimmed voltage references are provided for transmit and receive sections respectively. Clocking circuits and internal power supplies are also fully independent. This arrangement greatly reduces crosstalk between the transmit and receive blocks and improves performance.

Synchronous Operation

A low level on MCLK$_R$ input presets the circuit into synchronous mode. In this case, MCLK$_X$ and BCLK$_X$ are used for both transmit and receive sections, and BCLK$_R$ is used as a master clock select. A high level or open circuit selects the normal frequency and a low level selects the alternate frequency (See Table 1 below).

TABLE 1.

BCLKR/CLKSEL	HC-5557	HC-5552/53/54
Clock	2.048MHz	1.544/1.536MHz
Low	1.536/1.544MHz	2.048MHz
High or Open	2.048MHz	1.536/1.544MHz

The bit clock BCLK$_X$ may vary from 64KHz to 2.048MHz provided that BCLK$_X$ is synchronous with MCLK$_X$. For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse of each frame.

Asynchronous Operation

Two asynchronous modes are allowed with excellent transmission performance:

1°/ MCLK$_R$ is fully independent of MCLK$_X$ and must be 2.048MHz for HC-5557 (A law) and 1.544 or 1.536MHz for HC-5552/53/54 (μ law) (freq MCLK$_X$ = freq MCLK$_R$ ± 50ppm).

2°/ If required, MCLK$_X$ can also be used as a master clock for both transmit and receive sections (MCLK$_X$ input connected externally to MCLK$_R$ input).

In both modes, BCLK$_X$ and BCLK$_R$ may operate from 64KHz to 2.048MHz. BCLK$_X$ must be synchronous with MCLK$_X$, but BCLK$_R$ may be asynchronous with MCLK$_R$ (freq BCLK$_R$ = freq MCLK$_R$ ± 50ppm).

The degradation of the signal to total distortion ration under all permitted asynchronous conditions does not exceed 0.5dB as compared to the same measurement made with fully synchronous clocks.

Data Acquisition and Transmission

In both short and long frame operation, when FS$_X$ is high, the first BCLK$_X$ rising edge enables the D$_X$ buffer and shifts the sign bit out. The other bits are shifted out with the 7 following rising edges of BCLK$_X$. The falling edge of the 8th BCLK$_X$ pulse disables the D$_X$ buffer.

Similarly, when FS$_R$ is high, the first BCLK$_R$ rising edge enables the PCM word to be latched in from D$_R$ input with the 8 following falling edges of BCLK$_R$.

Detection of Short or Long Frame Operation

A long frame of short frame operation is detected by sensing FS$_X$ on the 3rd rising edge of BCLK$_X$ after FS$_X$ low to high transition. At this time, if a high level is sensed on FS$_X$, a long frame operation is detected.

Upon power up a short frame operation is assumed.

Signaling

In transmission, the signaling bit provided by SIG$_X$ input is latched by the 8th BCLK$_X$ rising edge after FS$_X$ low to high transition and inseted in place of the LSB of the PCM word during the frame.

In reception, the signaling bit is extracted from the PCM word (LSB) in the receive register and transferred to SIG$_R$ output. The data at SIG$_R$ output will be held until next signaling frame. At the same time the decoder compensates for the loss of the LSB by setting the LSB to 1/2 to minimize noise and distortion.

* In SHORT frame, the COFIDEC senses a signaling frame when FS$_X$ (FS$_R$) is still high during the 1st falling edge of BCLK$_X$ (BCLK$_R$) after FS$_X$ (FS$_R$) low to high transition.

* In LONG frame, the frame sync pulses FS$_X$ and FS$_R$ are 3 or more bit clock periods long. A signaling frame is identified from SF$_X$ and SF$_R$ for transmit and receive sections respectively. SF$_X$ (SF$_R$) must be high for 3 or more BCLK$_X$ (BCLK$_R$) periods for a signaling frame and stay low for a non signaling frame.

NOTE: Transmit and Receive Sections must be both in LONG frame or both in SHORT frame.

HC-5553 can be used for both short and long frame signaling. For short frame use, SF$_X$ and SF$_R$ should be tied low or left open circuit.

HC-5552 is intended for short frame application only. Signaling is not possible with HC-5554 or HC-5557.

Absolute Maximum Ratings

V_{CC} to GND ....-0.3V to +7V
V_{BB} to GND ....+0.3V to -7V
Voltage at any Digital
Input or Output ....V_{CC} +0.3V to GND -0.3V
Voltage at any Analog
Input or Output ....V_{CC} +0.3V to V_{BB} -0.3V

Operating Temperature Range.................-25°C to +80°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (Soldering 10 seconds) ....+300°C

Electrical Characteristics

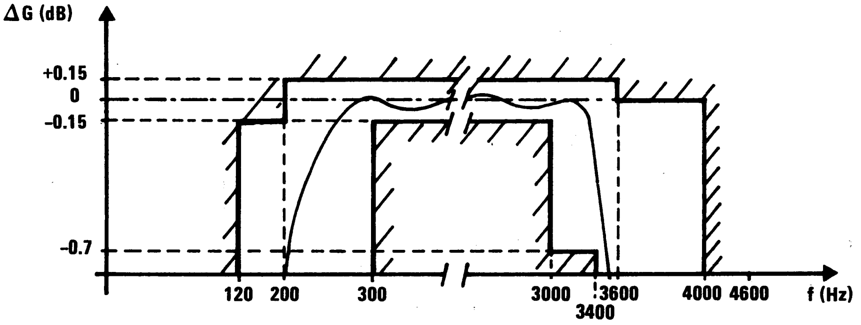
Unless otherwise specified: V_{CC} = 5.0V ± 5%, V_{BB} -5V ± 5%, GND = 0V
T_A = +0°C to +70°C: typical characteristics specified at V_{CC} = 5.0V, V_{BB} = 5.0V,
T_A = +25°C; all signals are referenced to GND.

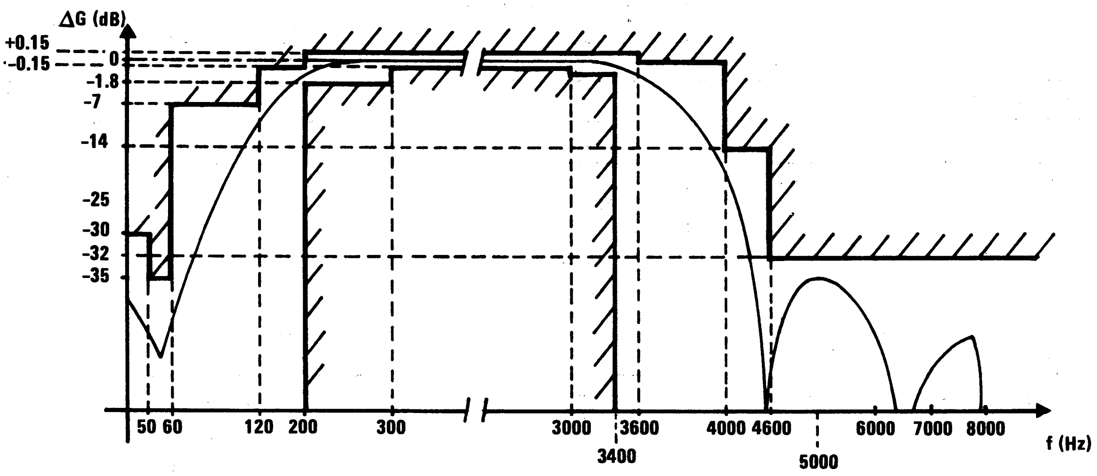
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Interface						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, I_L = 5.0mA $\overline{SIG_R}$, I_L = 1.0mA $\overline{TS_X}$, I_L = 3.2mA, Open Drain			0.4 0.4 0.4	V V V
V_{OH}	Output High Voltage	D_X, I_L = -5.0mA SIG_R, I_L = -1.0mA	2.4 2.4			V V
I_{IL}	Input Low Current (Note 1)	GND$\leq V_{IN} \leq V_{IL}$, All Digital Inputs	-10		10	μA
I_{IH}	Input High Current (Note 1)	$V_{IH} \leq V_{IN} \leq V_{CC}$	-10		10	μA
I_{OZ}	Output Current in High Impedance State	D_X, GND $\leq V_O \leq V_{CC}$	-10		10	μA
Analog Interface with Transmit Input Amplifier (All Devices)						
I_IXA	Input Leakage Current	-2.5V $\leq$ V $\leq$ +2.5V, VF_XI+ or VF_XI-	-200		200	nA
R_IXA	Input Resistance	-2.5V $\leq$ V $\leq$ +2.5V, VF_XI+ or VF_XI-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Level	GS_XR_L = 10kΩ	±2.8	±4.2		V
A_VXA	Voltage Gain	VF_XI+ to GS_X	5000			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		-20	1	20	mV
$V_{CM}XA$	Common-Mode Voltage		-2.5		+2.5	V
CMRRXA	Common-Mode Rejection Ratio		60	80		dB
PSRRXA	Power Supply Rejection Ratio		60	70		dB
Analog Interface with Receive Filter (All Devices)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	VF_RO = ±2.5V	600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		-100		100	mV
Power Dissipation (All Devices)						
I_{CCO}	Power-Down Current			0.15	.5	mA
I_{BBO}	Power-Down Current			0.05	0.3	mA
I_{CC1}	Active Current			6	9	mA
I_{BB1}	Active Current			6	9	mA

NOTE: 1). SFX, SFR: Internal pull down (2 μ A typical)
BCLR: Internal pull up (2 μ A typical)

Transmission Characteristics (Continued) Unless otherwise specified: T_A = +0°C to +70°C, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%, GND = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transmit Section Transfer Characteristics						
G_{XR}	Transmit Gain Relative to Gain at 820Hz (0dBm0)	f = 50Hz — 60Hz			-35	dB
		f = 60Hz — 120Hz			-7	dB
		f = 120Hz — 200Hz			-0.15	dB
		f = 200Hz — 300Hz	-1.8		+0.15	dB
		f = 300Hz — 3000Hz	-0.15		+0.15	dB
		f = 3000Hz — 3400Hz	-0.7		+0.15	dB
		f = 3400Hz — 3600Hz			+0.15	dB
		f = 3600Hz — 4000Hz			0	dB
		f = 4000Hz — 4600Hz			-14	dB
		f = 4600Hz and Up			-32	dB



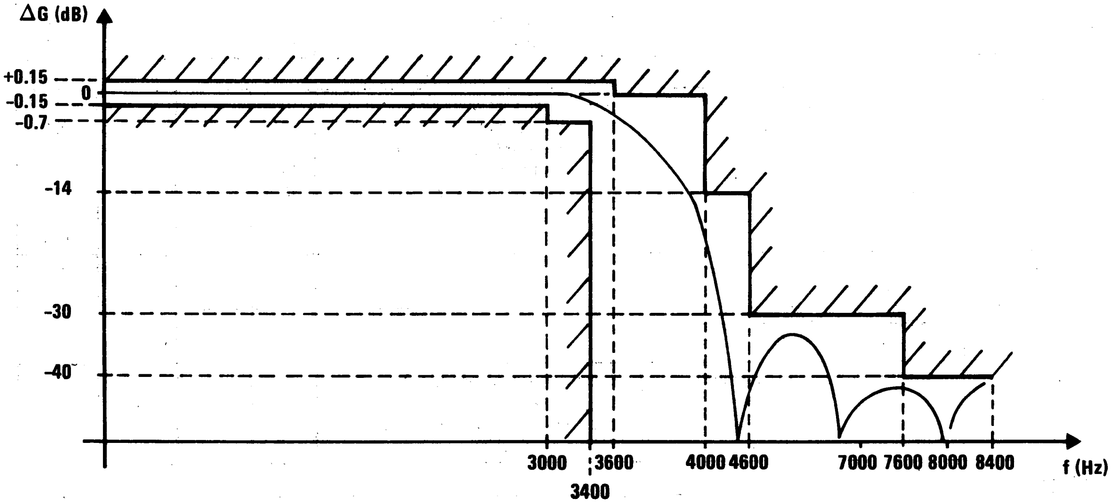


Transmission Characteristics (Continued) Unless otherwise specified: T_A = +0°C to +70°C, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%, GND = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Amplitude Response						
	Absolute Levels	Nominal 0dB0 levels is 4dBm (600Ω) 0dBm0 (All devices)		1.2277		Vrms
	Maximum Overload Levels	HC-5552, HC-5553, HC-5554 (3.17dBm0) HC-5557 (3.14dBm0)		2.501 2.492		V_{DC} V_{DC}
G_{XA}	Transmit Gain, Absolute	T_A = +25°C, V_{CC} = 5V, V_{BB} = -5V Input at GS_X = 0dBm0 at 1020Hz	0.15		0.15	dB
G_{XATV}	Absolute Transmit Gain Variation with Temperature and Supply Voltage	T_A = +0°C to +70°C V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%			±0.15	dB
G_{XRL}	Transmit Gain Variations with level	Sinusoidal Test Method Reference Level = -10dBm0 VF_XI+ = -40dBm0 to +3dBm0 VF_XI+ = -50dBm0 to -40dBm0 VF_XI+ = -55dBm0 to -50dBm0	0.2 -0.4 -1.2		0.2 0.4 1.2	dB dB dB
GRA	Receive Gain, Absolute	T_A = +25°C, V_{CC} = 5V, V_{BB} = -5V Input = Digital Code Sequence for 0dBm0 Signal at 1020Hz	-0.15		0.15	dB
G_{RATV}	Absolute Receive Gain Variation with Temperature and Supply Voltage	T_A = +0°C to +70°C V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%			±0.15	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method Reference Input PCM Code Corresponds to an Ideally Encoded = 10dBm0 Signal PCM Level Level = -40dBm0 to +3dBm0 PCM Level = -50dBm0 to -40dBm0 PCM Level = -55dBm0 to -50dBm0	0.2 -0.4 -1.2		+0.2 +0.4 +1.2	dB dB dB
V_{RO}	Receive Ouput Drive Level	R_L = 600Ω	-2.5		2.5	V
Envelope Delay Distortion with Frequency						
D_{XA}	Transmit Delay, Absolute	f = 1600Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500Hz — 600Hz f = 600Hz — 800Hz f = 800Hz — 1000Hz f = 1000Hz — 1600Hz f = 1600Hz — 2600Hz f = 2600Hz — 2800Hz f = 2800Hz — 3000Hz		140 100 50 20 60 80 140	220 145 75 50 100 110 200	μs μs μs μs μs μs μs
D_{RA}	Receive Delay, Absolute	f = 750Hz		160	180	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500Hz — 1600Hz f = 1600Hz — 260Hz f = 2600Hz — 2800Hz f = 2800Hz — 3000Hz		40 90 120 140	60 120 140 175	μs μs μs μs

Transmission Characteristics (Continued) Unless otherwise specified: T_A = +0°C to +70°C, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%, GND = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Receive Section Transfer Characteristics						
G_{RR}	Receive Gain Relative to Gain at 820Hz (0dBm0)	f = 0Hz — 3000Hz f = 3000Hz — 3400Hz f = 3400Hz — 3600Hz f = 3600Hz — 4000Hz f = 4000Hz — 4600Hz	-0.15 -0.7		+0.15 +0.15 +0.15 0 -14	dB dB dB dB dB
SOS	Spurious Out-of-Band Signals at the channel output	Image Signals at VF_RO: f = 4600Hz — 7600Hz f = 7600Hz — 8400Hz			-30 -40	dB dB



Transmission Characteristics (Continued)

Unless otherwise specified: T_A = +0°C to +70°C, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%, GND = 0V, f = 1.02kHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity gain non-inverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Noise						
N_{XC}	Transmit Idle Channel Noise, C Message Weighted	HC-5552, HC-5553, HC-5554 VF_XI+ = 0V		12	15	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	HC-5557 (Note 1)		-74	-69	dBm0p
		VF_XI+ = 0V (Note 2)		-70	-67	dBm0p
N_{RC}	Receive Idle Channel Noise, C Message Weighted	HC-5552, HC-5553, HC-5554 PCM Code equals alternating Positive and Negative Zero		8	11	dBrnC0
N_{RP}	Receive Idle Channel Noise, P Message Weighted	HC-5557 PCM Code equals Positive Zero		-82	-79	dBm0p
N_{RS}	Noise, Single Frequency	f = 0KHz to 100KHz, Loop Around Measurment, VF_XI+ = 0Vrms			-53	dBm0
Power Supply Rejection						
$PPSR_X$	Positive Power Supply Rejection Transmit	VF_XI+ = 0Vrms V_{CC} = 5.0V_{DC} + 100mVrms f = 0 — 50KHz	40			dBC
$NPSR_X$	Negative Power Supply Rejection Transmit	VF_XI+ = 0Vrms V_{BB} = -5.0V_{DC} + 100mVrms f = 0 — 50KHz	40			dBC
$PPSR_R$	Positive Power Supply Rejection Receive	PCM Code equals Positive Zero V_{CC} = 5.0V_{DC} + 100mVrms f = 0 — 4000Hz	40			dBC
		f = 0 — 50KHz	25			dB
$NPSR_R$	Negative Power Supply Rejection Receive	PCM Code equals Positive Zero V_{BB} = -5.0V_{DC} + 100mVrms f = 0 — 4000Hz	40			dBC
		f = 0 — 50KHz	25			dB
Distortion						
$STD_{X/R}$	Signal to Total Distortion Transmit or Receive Channel	Sinusoidal Test Method Level = 3.0dBm0	33			dBC
		= 0dBm0 to -30dBM0	36			dBC
		= -40dBm0 XMT	29			dBC
		RCV	30			dBC
		= -55dBm0 XMT	14			dBC
		RCV	15			dBC
SFD_X	Single Frequency Distortion Transmit				-46	dB
SFD_R	Single Frequency Distortion Receive				-46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_XI+ = -4dBm0 to -21dBm0, two frequencies in the range 300Hz to 3400Hz			-41	dB
Crosstalk						
CT_{X-R}	Transmit to Receive Crosstalk 0dBm0 Transmit Level	f = 300Hz — 3400Hz D_R = Steady PCM Code		-90	-75	dB
CT_{R-X}	Receive to Transmit Crosstalk 0dBm0 Receive Level	f = 300Hz — 3400Hz VF_XI+ = 0V		-90	-70	dB

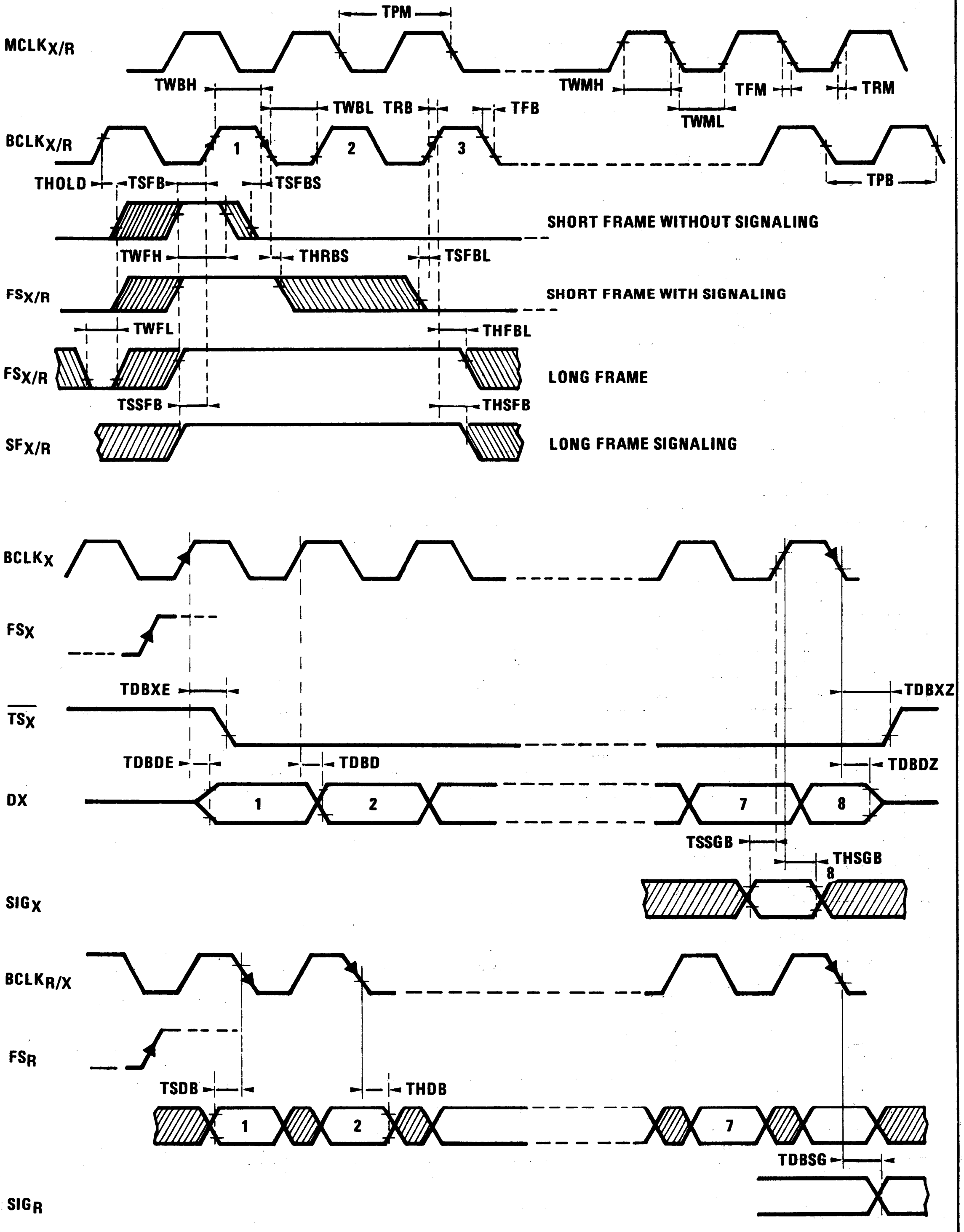
NOTE: 1). Quantization Noise, measured by extrapolation from the distortion result.

2). Idle Channel Noise, due to alternating sign bit of a perfectly zeroed encoder.

Timing Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clocks						
1/TPM	Frequency of Master Clock	Depends on the Device used and the $BCLK_R$/CLKSEL pin Selection		1.536 1.544 2.048		MHz MHz MHz
TWMH	Width of Master Clock High	VIH = 2.2V	160			ns
TWML	Width of Master Clock Low	VIL = 0.6V	160			ns
TRM	Rise Time of Master Clock				50	ns
TFM	Fall Time of Master Clock				50	ns
TPB	Period of Bit Clock		488		15625	ns
TWBH	Width of Bit Clock High	VIH = 2.2V	160			ns
TWBL	Width of Bit Clock Low	VIL = 0.6V	160			ns
TRB	Rise Time of Bit Clock	TPB = 488ns			50	ns
TFB	Fall Time Bit Clock	TPB = 488ns			50	ns
Frame Sync Pulses						
TSFB	Frame Sunc High Set up before 1st Bit Clock rising		50			ns
THOLD	Frame Sunc Low Hold after Bit Clock rising		50			ns
TWFH	Width of Frame Sync High		100			ns
TSFBS	Frame Sync Low Set up before 1st Bit Clock falling	Short Frame without Signaling	100			ns
THFBS	Frame Sync High Hold after 1st Bit Clock falling	Short Frame with Signaling	100			ns
TSFBL	Frame Sync Low Set up before 3rd Bit Clock rising	Short Frame with Signaling	100			ns
THFBL	Frame Sync High Hold after 3rd Bit Clock rising	Long Frame	100			ns
TWFL	Width of Frame Sync Low	Long Frame and 64KBit/s	100			ns
TSSFB	$SF_{X/R}$ Set up before 1st Bit Clock rising	Long Frame Signaling	0			ns
THSFB	$SF_{X/R}$ Hold after 3rd Bit Clock rising	Long Frame Signaling	100			ns
Data						
TDBXE	Delay from 1st Bit Clock rising to $\overline{TSX}$ Low	Load = 150pF + 2 LSTTL loads	20		140	ns
TDBXZ	Delay from 8th Bit Clock falling to $\overline{TS_X}$ disabled		50		165	ns
TDBDE	Delay from 1st Bit Clock rising to Data output enabled	Load = 150pF + 2 LSTTL loads	20		165	ns
TDBD	Delay from Bit Clock rising to Data output valid	Load = 150pF + 2 LSTTL loads			180	ns
TDBDZ	Delay from 8th Bit Clock falling to Data output disabled		50		165	ns
TSSGB	SIG_X, Set up before 8th Bit Clock rising		50			ns
THSGB	SIG_X, Hold after 8th Bit Clock rising		100			ns
TSDB	Data input Set up before Bit Clock falling		50			ns
THDB	Data input Hold after Bit Clock falling		50			ns
TDBSG	Delay from 8th Bit Clock falling to SIG_R valid	Load = 50pF + 2 LSTTL loads	300			ns

Timing Diagrams

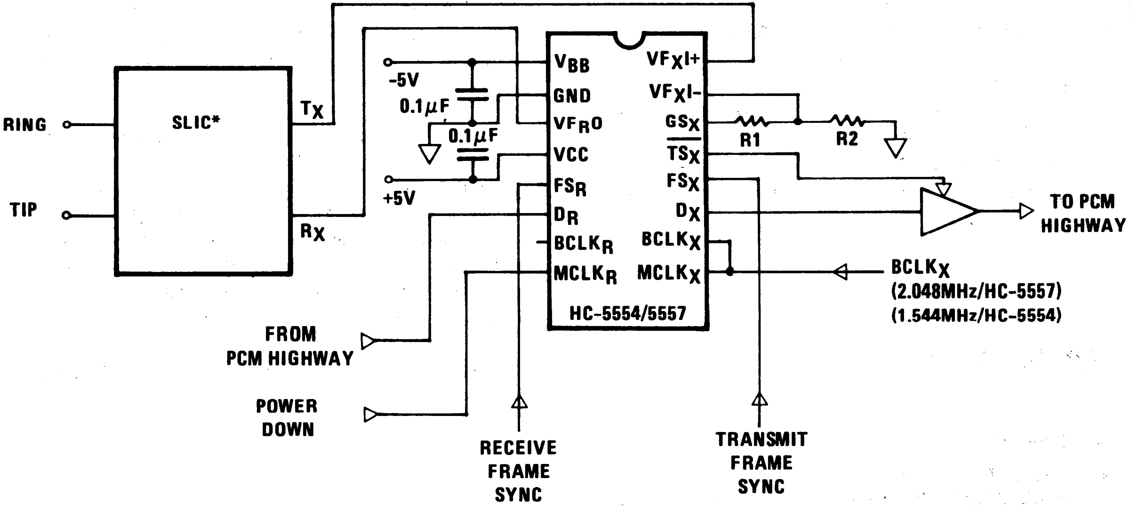

TPM
MCLKX/R
TWMH
TFM
TRM
TWML
TWBH
TWBL
TRB
TFB
BCLKX/R
1
2
3
TPB
THOLD
TSFB
TSFBS
SHORT FRAME WITHOUT SIGNALING
TWFH
THRBS
TSFBL
FSX/R
SHORT FRAME WITH SIGNALING
TWFL
THFBL
FSX/R
LONG FRAME
TSSFB
THSFB
SFX/R
LONG FRAME SIGNALING
BCLKX
FSX
TDBXE
TDBXZ
TSX
TDBDE
TDBD
TDBDZ
DX
1
2
7
8
TSSGB
THSGB
8
SIGX
BCLKR/X
FSR
TSDB
THDB
1
2
7
TDBSG
SIGR

Operating Instructions

Ground should be applied to the device before any other connection. Although V_{CC} and V_{BB} can be connected in any order, one should check that voltages on all inputs and on supply rails stay within absolute maximum ratings even for very short periods to avoid any latch-up. All ground connections to each device should meet at a common point as close as possible to the GND pin.

Two 0.1μF decoupling capacitors are required from the common ground point to V_{CC} and V_{BB}.

The ground point of each COFIDEC should be tied to a common card ground in star formation, rather than via a ground bus.


RING
TIP
SLIC*
TX
RX
-5V
0.1μF
0.1μF
+5V
VBB
GND
VFRO
VCC
FSR
DR
BCLKR
MCLKR
VFXI+
VFXI-
GSX
TSX
FSX
DX
BCLKX
MCLKX
HC-5554/5557
R1
R2
TO PCM HIGHWAY
BCLKX
(2.048MHz/HC-5557)
(1.544MHz/HC-5554)
FROM PCM HIGHWAY
POWER DOWN
RECEIVE FRAME SYNC
TRANSMIT FRAME SYNC

*HC-5502A, HC-5504, HC-5508 OR TRANSFORMER

TYPICAL SYNCHRONOUS APPLICATION

NOTICE:

Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specfications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

For maintenance of performance and reliability, Harris Semiconductor strongly recommends that the "I.C. Handling Procedures", located in Section 1 of the current Analog Products Data Book, be followed closely by any activity involved with I. C Products.

HARRIS

HC-55536

All-Digital Continuous Variable Slope Delta Demodulator (CVSD)

FEATURES

- REQUIRES FEWER EXTERNAL PARTS
- LOW POWER DRAIN: 1.5mW FROM SINGLE 3.0-7.0V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- FILTER RESET BY DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION

APPLICATIONS

- SPEECH SYNTHESIS
- AUDIO MANIPULATIONS; DELAY LINES, ECHO GENERATION/SUPPRESSION, SPECIAL EFFECTS, ETC.
- PAGERS

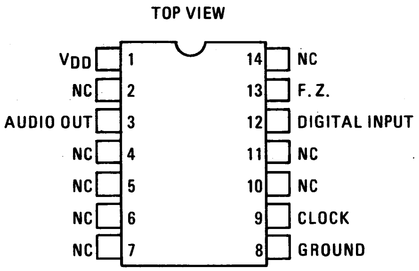
DESCRIPTION

The HC-55536 is a CMOS integrated circuit used to convert serial NRZ digital data to an analog (voice) signal. Conversion is by delta demodulation, using the continuously variable slope (CVSD) method.

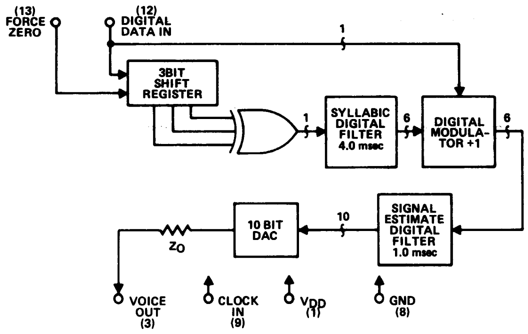
While signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by digital filters which use very low power and require no external timing components. This digital approach allows inclusion of many desirable features, which otherwise would be difficult to implement. Internal time constants are optimized for a 16K bit/sec data rate. However, the device is usable from 9K bits/sec to above 64K bits/sec.

The HC-55536 is available in a 14 pin ceramic DIP package. Chips are available, probe tested at +25°C.

PINOUT AND PIN DESCRIPTION


TOP VIEW
VDD 1
NC 2
AUDIO OUT 3
NC 4
NC 5
NC 6
NC 7
14 NC
13 F.Z.
12 DIGITAL INPUT
11 NC
10 NC
9 CLOCK
8 GROUND

FUNCTIONAL DIAGRAM


(13) FORCE ZERO
(12) DIGITAL DATA IN
1
3BIT SHIFT REGISTER
1
SYLLABIC DIGITAL FILTER 4.0 msec
6
DIGITAL MODULATOR +1
6
SIGNAL ESTIMATE DIGITAL FILTER 1.0 msec
10
10 BIT DAC
Z0
VOICE OUT (3)
CLOCK IN (9)
VDD (1)
GND (8)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage at any Pin	GND -0.3V to V_{DD} +0.3V	Operating Temperature (-5)	0°C to 75°C
Maximum V_{DD} Voltage	+7.0V		
Minimum V_{DD} Voltage	+3.0V	Storage Temperature Range	-65°C to +150°C
Operating V_{DD} Range	+3.0V to +7.0V		

ELECTRICAL CHARACTERISTICS V_{DD} = +5.0V; Bit Rate = 16K Bits/sec; T_A = +25°C.

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Clock Sampling Rate		16	64	K Bits/Sec	(1)
Clock Duty Cycle	30		70	%	
Supply Voltage	+3.0		+7.0	V	
Supply Current		0.3	1.5	mA	
Logic "1" Input, V_{IH}	3.5	4.5		V	(2)
Logic "0" Input, V_{IL}			1.5	V	(2)
Audio Output Voltage		0.5	1.2	V_{RMS}	(3)
Audio Output Impedance		150		kΩ	(4)
Syllabic Filter Time Constant		4.0		ms	(5)
L.P. Signal estimate Filter Time Conatant		0.94		ms	(5)
Step Size Ratio		24		dB	(6)
Resolution		0.1		%	(7)
Minimum Step Size		0.2		%	(8)
Slope Overload		Fig. 1		–	(9)
Signal/Noise Ratio	25			dB	
Quieting Pattern Amplitude		10		mV_{p-p}	(10)
Clamping Threshold		0.75		F. S.	(11)

NOTES:

1. There is one NRZ data bit per clock period. Clock must be phased with digital data such that a positive clock transition occurs in the middle of each received data bit.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate and changes with negative clock transitions.
3. As mentioned elsewhere, this output includes a DC bias of VDD/2. Therefore an AC coupling capcitor (min. 4.7 f) is required unless the output filter also includes this bais.
4. Presents approximately 150kr in series with recovered audio boltage. Zero-signal reference is $V_{DD}/2$.
5. Note that filter time constants are inversely proportional to clock rate.
6. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.
7. Minimum quantization voltage level expressed as a percentage of supply voltage.
8. The minimum step size between levels is twice the resolution.
9. For large signal amplitudes or high frequencies, the encoder may become slope-overloaded. Figure 1 shows the frequency response at various signal levels, measured with a 3kHz low-pass filter having a 130dB/octave roll-off to -50dB.
10. The "quieting" pattern or idle-channel audio output steps at 1/2 the bit rate, changing state on negative clock transitions.
11. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

FIG. 1. Illustrates the frequency response of the HC-55536 for varying input levels. To prevent slope overload (slew rate limiting) do not exceed the 0dB boundary. The frequency response is directly proportional to the sampling rate. The output levels were measured after filtering.

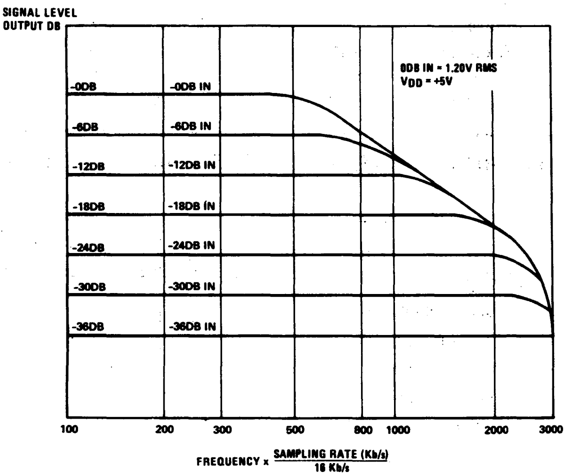


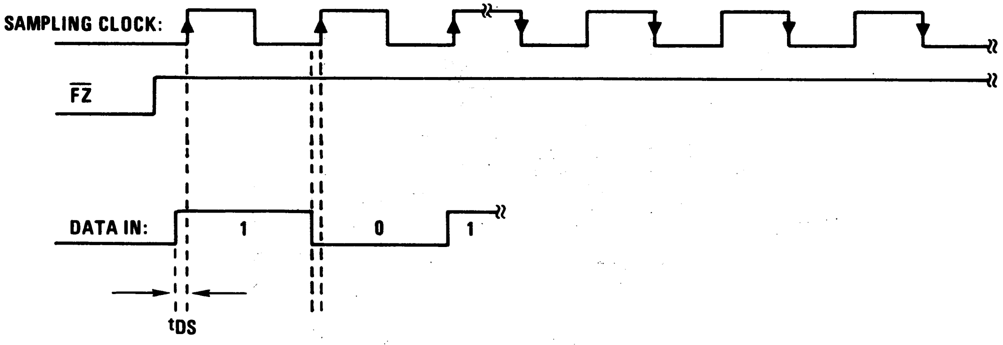
Figure 1 — Transfer Function for CVSD at 16KB

PIN ASSIGNMENT

PIN 14-LEAD D.I.P.	SYMBOL	DESCRIPTION
1	V_{DD}	Positive supply voltage.
2	N.C.	*No internal connection is made to these pins.
3	Audio Out	Recovered audio out. Presents approximately 150Kr source with DC offset of $V_{DD}/2$ should be externally AC couples.
4	N.C.	*No internal connection is made to these pins.
5	N.C.	*No internal connection is made to these pins.
6,7	N.C.	*No internal connection is made to these pins.
8	Digital Gnd.	Logic ground.
9	Clock	Sampling rote clock must be synchronized with the digital input data such that the data is valid at the positive clock transition.
10	N.C.	*No internal connection is made to these pins.
11	N.C.	*No internal connection is made to these pins.
12	Digital In	Input for the received seriai NRZ digital NRZ data.
13	$\overline{FZ}$	Active low logic input. Activation this input resets the internal logic and forces the recovered audio output into the "quieting" condition.
14	N.C.	

*NOTE: No active input should be left in a "floating condition".

TIMING WAVEFORMS



t_{DS}: DATA SET UP TIME, 100ns TYPICAL

Figure 3 – CVSD Timing Diagram

HARRIS

HC-55564

Continuously Variable Slope Delta-modulator (CVSD)

Features

- **All Digital**
- **Requires Few External Parts**
- **Low Power Drain: 1.5mW Typical From Single 3.0V-7V Supply**
- **Time Constants Determined by Clock Frequency; No Calibration or Drift Problems; Automatic Offset Adjustment**
- **Half Duplex Operation Under Digital Control**
- **Filter Reset Under Digital Control**
- **Automatic Overload Recovery**
- **Automatic "Quiet" Pattern Generation**
- **AGC Control Signal Available**

Applications

- **Voice Transmission Over Data Channels (Modems)**
- **Voice/Data Multiplexing (Pair Gain)**
- **Voice Encryption/Scrambling**
- **Voicemail**
- **Audio Manipulations: Delay Lines, Time Compression, Echo Generation/Suppression, Special Effects, Etc.**
- **Pagers/Satellites**
- **Data Aquisition Systems**
- **Voice I/O For Digital Systems and Speech Synthesis Requiring Small Size, Low Weight, and Ease of Reprogrammability**

Description

The HC-55564 is a half duplex modulator/demodulator CMOS integrated circuit used to convert voice signals into serial NRZ digital data and to reconvert that data into voice. The conversion is by delta-modulation, using the Continuously Variable Slope (CVSD) method of modulation/de-modulation.

While the signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by very low power digital filters which require no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The fundamental advantages of delta-modulation, along with its simplicity and serial data format, provide an efficient (low data rate/low memory requirements) method for voice digitization. The device may be easily configured with the HC-5512C/12D PCM/CVSD filter.

The HC-55564 is usable from 9K bits/sec to above 64Kbps. The unit is available in a 14 pin ceramic DIP or LCC package in commerical, industrial, and military temperature ranges including the Harris High Rel Dash 7 and Dash 8 programs. Application Notes 607 and 576 are available, as are Demonstation Boards.

Functional Diagram

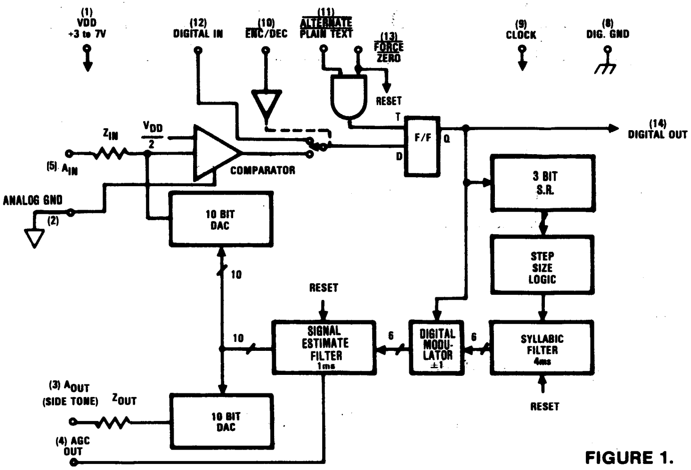
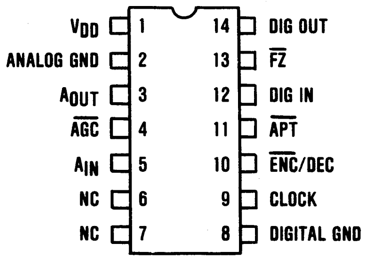
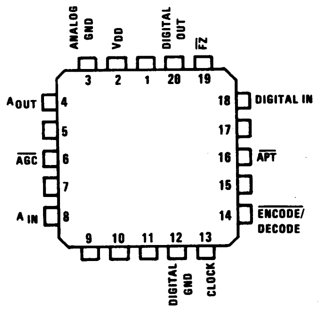

(1) VDD +3 to 7V
(12) DIGITAL IN
(10) ENC/DEC
(11) ALTERNATE PLAIN TEXT
(13) FORCE ZERO
(9) CLOCK
(8) DIG. GND
RESET
T
F/F
Q
D
(14) DIGITAL OUT
Z_{IN}
$\frac{V_{DD}}{2}$
(5) A_{IN}
COMPARATOR
ANALOG GND
(2)
10 BIT DAC
3 BIT S.R.
STEP SIZE LOGIC
10
RESET
10
SIGNAL ESTIMATE FILTER 1ms
6
DIGITAL MODU-LATOR ±1
6
SYLLABIC FILTER 4ms
RESET
(3) A_{OUT} (SIDE TONE)
Z_{OUT}
10 BIT DAC
(4) AGC OUT

FIGURE 1.

Pinouts

TOP VIEWS





Pin Assignments

PIN # 14-PIN DIP	PIN # 20-PIN LCC	SYMBOL	DESCRIPTION
1	2	V_{DD}	Positive supply voltage. Voltage range is +3.0V to +7.0V.
2	3	Analog Gnd	Analog Ground connection to D/A ladders and comparator.
3	4	A_{OUT}	Audio Out recovered from 10 bit DAC. May be used as side tone at the transmitter. Presents approximately 150 kilohm source with DC offset of $V_{DD}/2$. Within ±2dB of Audio Input. Should be externally AC coupled.
4	6	$\overline{AGC}$	Automatic Gain Control output. A logic low level will appear at this output when the recovered signal excursion reaches one-half of full scale value. In each half cycle full scale is $V_{DD}/2$. The mark-space ratio is proportional to the average signal level.
5	8	A_{IN}	Audio Input to comparator. Should be externally AC coupled. Presents approximately 280 kilohms in series with $V_{DD}/2$.
6,7	1,5,7,9, 10,11, 15,17	NC	No internal connection is made to these pins.
8	12	Digital Gnd	Logic ground. 0V reference for all logic inputs and outputs
9	13	Clock	Sampling rate clock. In the decode mode, must be synchronized with the digital input data such that the data is valid at the positive clock transition. In the encode mode, the digital data is clocked out on the negative going clock transition. The clock rate equals the data rate.
10	14	$\overline{\text{Encode}}$/ Decode	A single CVSD can provide half-duplex operation. The encode or decode function is selected by the logic level applied to this input. A low level selects the encode mode, a high level the decode mode.
11	16	$\overline{APT}$	Alternate Plain Text input. Activating this input causes a digital quieting pattern to be transmitted, however; internally the CVSD is still functional and a signal is still available at the A_{OUT} port. Active low.
12	18	Digital In	Input for the received digital NRZ data.
13	19	$\overline{FZ}$	Force Zero input. Activating this input resets the internal logic and forces the digital output and the recovered audio output into the "quieting" condition. An alternating 1-0 pattern appears at the digital output at ½ the clock rate. When this is decoded by a receive CVSD, a 10mVp-p inaudible signal appears at audio output. Active low.
14	20	Digital Out	Output for transmitted digital NRZ data.

NOTE: No active input should be left in a "floating condition."

Absolute Maximum Ratings

Voltage at Any Pin .... GND -0.3V to V_{DD} +0.3V
Maximum V_{DD} Voltage .... +7.0V
Minimum V_{DD} Voltage .... +3.0V
Operating V_{DD} Range .... +3.0V to +7.0V

Operating Temperature

Storage Temperature .... -65°C to +150°C
Operating Temperature ....-55°C to +125°C

Electrical Characteristics

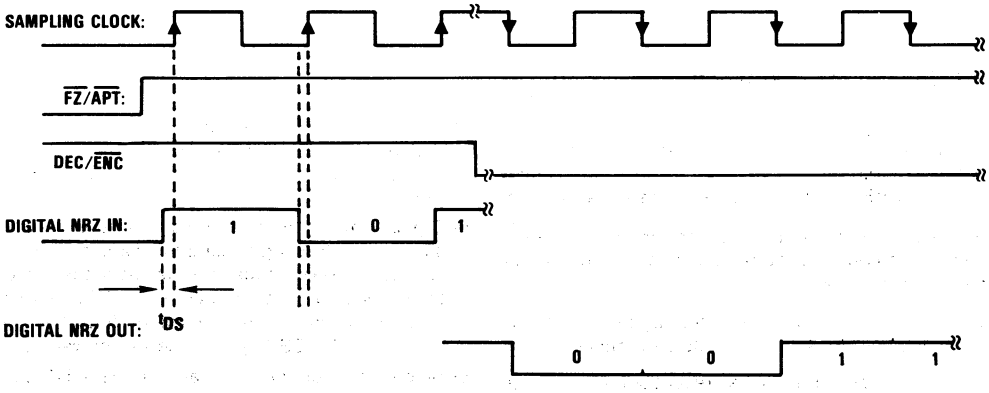
Unless otherwise noted, T_A = 25°C, V_{DD} = +5.0V, Sampling Rate = 16Kbps, AG = DG = 0V, A_{IN} = 1.2Vrms.

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS	CONDITIONS
CLK	Sampling Rate	9	16	64	Kbps	Note 1
I_{DD}	Supply Current		0.3	1.5	mA	
V_{IH}	Logic '1' Input	3.5			V	Note 2
V_{IL}	Logic '0' Input			1.5	V	Note 2
V_{OH}	Logic '1' Output	4.0			V	Note 3
V_{OL}	Logic '0' Output			0.4	V	Note 3
	Clock Duty Cycle	30		70	%	
A_{IN}	Audio Input Voltage		0.5	1.2	Vrms	AC coupled. Note 4
A_{OUT}	Audio Output Voltage		0.5	1.2	Vrms	AC coupled. Note 5
Z_{IN}	Audio Input Impedance		280		kΩ	Note 6
Z_{OUT}	Audio Output Impedance		150		kΩ	Note 6
A_{E-D}	Transfer Gain	-2.0		+2.0	dB	No Load. Audio In to Audio Out.
A_E	Encode Gain		.34		dB	
A_D	Decode Gain		1.23		dB	
t_{SF}	Syllabic Filter Time Constant		4.0		mS	Note 7
t_{SE}	Signal Estimate Filter Time Constant	1.0			mS	Note 7
	Resolution		0.1		%	Note 8
	Minimum Step Size		0.2		%	Note 9
V_{QP}	Quieting Pattern Amplitude		10		mVp-p	FZ = 0V or APT = 0V, or A_{IN} = 0V. Note 10
V_{AL}	$\overline{AGC}$ Lo Threshold		1.24		Vp-p	Note 11
V_{AH}	$\overline{AGC}$ Hi Threshold		3.85		Vp-p	Note 11
V_{CTH}	Clamping Threshold		0.75		F.S.	Note 12

NOTES:

1. There is one NRZ (Non-Return Zero) data bit per clock period. Data is clocked out on the negative clock edge. Data is clocked into the CVSD on the positive going edge (see Figure 2). Clock may be run at less than 9Kbps and greater than 64Kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.
3. Logic outputs are CMOS compatible at supply voltage and will withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions. Each output will drive two LS TTL loads.
4. Recommended voice input range for best voice performance. Should be externally AC coupled.
5. May be used for side-tone in encode mode. Should be externally AC coupled. Varies with aduio input level by ±dB.
6. Presents series impedance with audio signal. Zero signal reference is approximatey $V_{DD}/2$.
7. Note that filter time constants are inversely proportional to clock rate. Both filters approximate single pole responses.
8. Minimum quantization voltage level expressed as a percentage of supply voltage.
9. The minimum step size between levels is twice the resolution.
10. The "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.
11. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative), i.e. at $V_{DD}/2$ ±25% of V_{DD}.
12. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

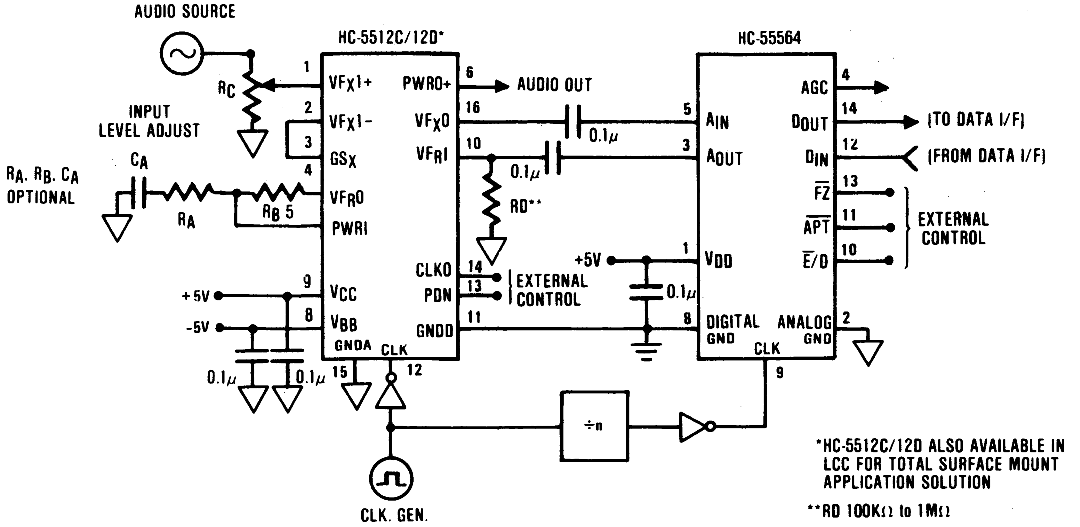
Timing Waveforms



t_{DS}: DATA SET UP TIME, 100ns TYPICAL

FIGURE 2. CVSD TIMING DIAGRAM

Interface Circuit for HC-55564 CVSD


AUDIO SOURCE
HC-5512C/12D*
HC-55564
RC
INPUT LEVEL ADJUST
CA
RA, RB, CA OPTIONAL
RA
RB 5
1
2
3
4
VFX1+
VFX1-
GSX
VFRO
PWRI
PWRO+
VFXO
VFRI
6
16
10
AUDIO OUT
0.1μ
0.1μ
RD**
+5V
CLKO
PDN
14
13
EXTERNAL CONTROL
9
8
VCC
VBB
+5V
-5V
GNDA
CLK
GNDD
11
0.1μ
0.1μ
15
12
÷n
CLK. GEN.
5
3
1
8
AIN
AOUT
VDD
DIGITAL GND
CLK
9
AGC
DOUT
DIN
FZ
APT
E/D
ANALOG GND
4
14
12
13
11
10
2
(TO DATA I/F)
(FROM DATA I/F)
EXTERNAL CONTROL
0.1μ

*HC-5512C/12D ALSO AVAILABLE IN LCC FOR TOTAL SURFACE MOUNT APPLICATION SOLUTION

**RD 100KΩ to 1MΩ

FIGURE 3.

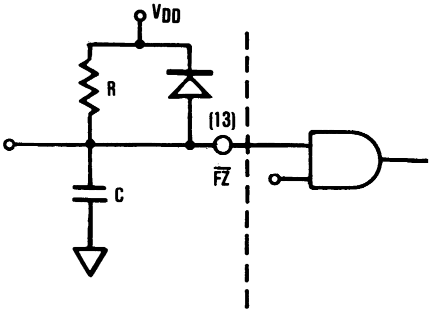
CVSD Hookup for Evaluation

The circuit in Figure 3 is sufficient to evaluate the voice quality of the CVSD, since when encoding the feedback signal at the audio output pin is the reconstructed audio input signal. CVSD design considerations are as follows;

1) Care should be taken in layout to maintain isolation between analog and digital signal paths for proper noise consideration.

2) Power supply decoupling is necessary as close to the device as possible. A 0.1uf should be sufficient.

3) Ground, then power, must be present before any input signals are applied to the CVSD. Failure to observe this may cause a latchup condition which may be destructive. Latchup may be removed by cycling the power off/on. A power-up reset circuit may be used that strobes Force Zero (Pin 13) during power-up as follows:



4) Analog (signal) ground (Pin 2) should be externally tied to Pin 8 and power ground. It is recommended that the A_{IN} and A_{OUT} ground returns connect only to Pin 2.

5) Digital inputs and outputs are compatible with standard CMOS logic using the same supply voltage. All unused logic inputs must be tied to the appropriate logic level for desired operation. TTL outputs will require 1K Ohm pull-up resistors. Pins 4 and 14 will each drive CMOS logic or one low power TTL input.

6) Since the Audio Out pins are internally DC biased to $V_{DD}/2$, AC coupling is required. In general, a value of 0.1μf is sufficient for AC coupling of the CVSD audio pins to a filter circuit.

7) The AGC output may be externally integrated to drive an AGC pre-amp, or it could drive an LED indicator through a buffer to indicate proper speaking volume.

Figures 4, 5, and 6 illustrate the typical frequency response of the HC-55564 for varying input levels and for varying sampling rates. To prevent slope overload (slew limiting), the 0dB boundry should not be exceeded. The frequency response is directly proportional to the sampling clock rate. The flat bandwidth at 0dB doubles for every 16kHz increase in sampling rate. The output levels were measured in the encode mode, without filtering, from A_{IN} to A_{OUT}, at V_{DD} = +5V. 0dB = 1.2Vrms.

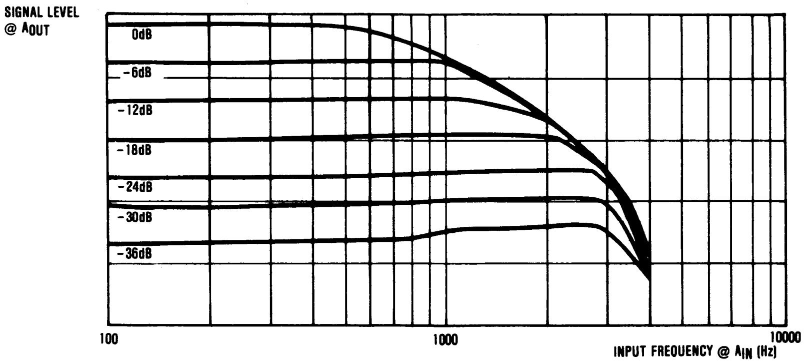


FIGURE 4. TRANSFER FUNCTION FOR CVSD AT 16Kbps

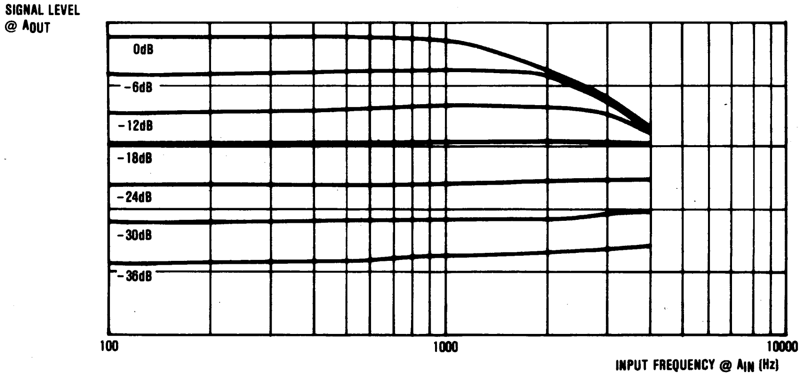


FIGURE 5. TRANSFER FUNCTION FOR CVSD AT 32Kbps

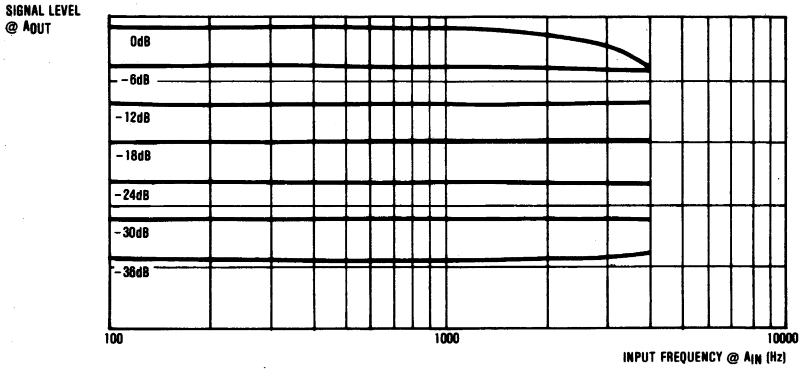
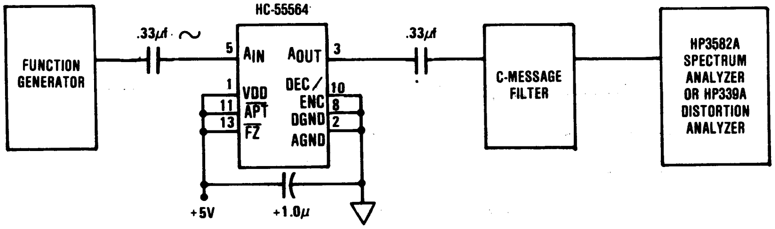


FIGURE 6. TRANSFER FUNCTION FOR CVSD AT 64Kbps

The following typical performance distortion graphs wererealized with the test configuration of Figure 7. The measurement vehicle for Total Harmonic Distortion (THD) was an HP-339A distortion measurement set, and for 2nd and 3rd harmonic distortion, an HP-3582A spectrum analyzer. All measurement conditions were at V_{DD} = +5V, and 2nd and 3rd harmonic distortion measurements were C-message filtered. 0dB = 1.2Vrms.



FUNCTION GENERATOR
.33μf
HC-55564
5
AIN
AOUT
3
1
VDD
DEC/
10
11
APT
ENC
8
13
FZ
DGND
2
AGND
+5V
+1.0μ
.33μf
C-MESSAGE FILTER
HP3582A SPECTRUM ANALYZER OR HP339A DISTORTION ANALYZER

FIGURE 7. TEST AND MEASUREMENT CIRCUIT

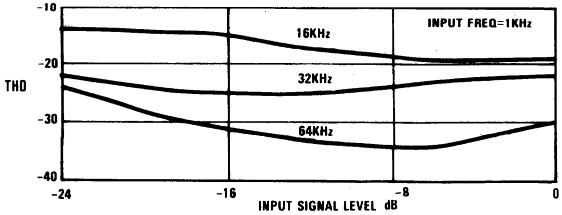


FIGURE 8. CVSD SIGNAL LEVEL VERSUS TOTAL HARMONIC DISTORTION

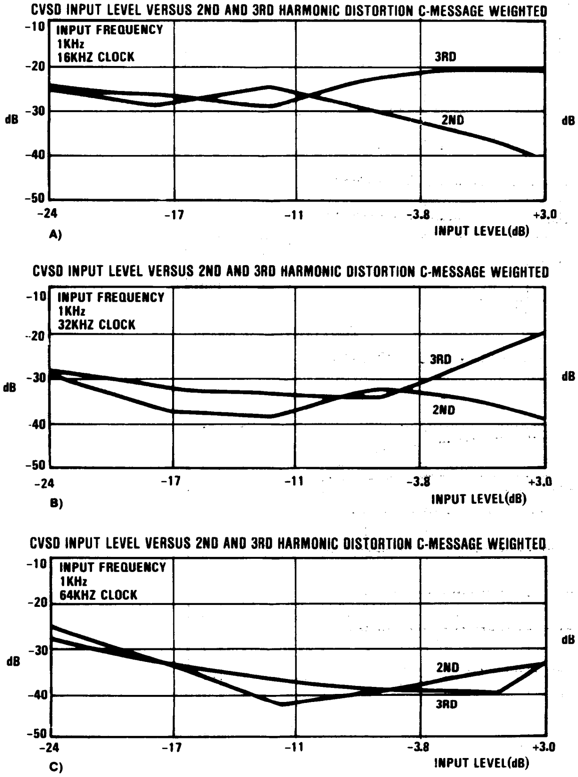


FIGURE 9A, B, C. CVSD INPUT LEVEL VERSUS 2ND AND 3RD HARMONIC DISTORTION

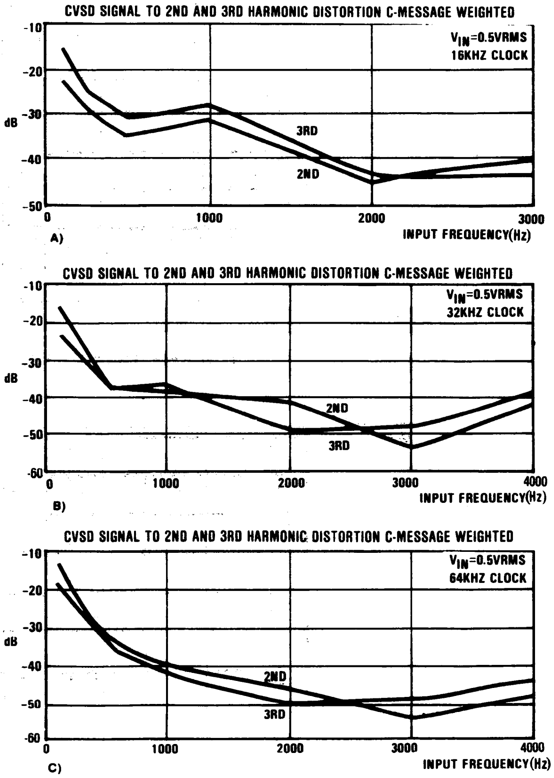


FIGURE 10A, B, C. CVSD INPUT FREQUENCY VERSUS 2ND AND 3RD HARMONIC DISTORTION

HARRIS

HF-10

PRELIMINARY

Universal Active Filter

Features

- Industry Standard Pinout
- Low Crosstalk .... -60dB
- Low Clock Feed Through...2mVrms
- Low Standby Current...500μA
- Clock to Center Frequency Ratio Accuracy ±2%
- Filter Cutoff Frequency Stability Directly Dependent on External Clock Quality
- Separate High-pass (or Notch or All-Pass), Band-Pass, Low-pass Outputs
- f_O x Q Range up to 50kHz Minimum
- Operates to f_O = 20kHz Minimum
- Specifications Guaranteed for T_A from -55°C to +125°C

Applications

- General Purpose Audio-Band Filtering
- Real-Time Programming
  - ▶ Prototyping
  - ▶ Dynamic Reconfiguration
- High Q Applications
- Precision Filtering at Low Q
- Precision Oscillators
- Extended Temperature
- Voice Response Systems
  - ▶ Modems
  - ▶ Tone Generators
- Data Acquisition Systems
- Building Block for Precision Higher-Order Filters (Directly Cascadable)

Description

The HF-10 consists of two fully independent second order switched capacitor CMOS filter sections. Each second order section is a modified state-variable filter. In each section there are three operational amplifiers and an additional "summing node". The extra summing node is a direct benefit of the switched capacitor design approach. This provides increased versatility as compared to the classical continuous-time active filter. The transfer function of each section is tailored by the user's choice of feedback configuration, external resistor values, and external clock rate.

The HF-10 topology is very useful since it produces three different, but related, transfer functions simultaneously. Each transfer function has the same pole locations but different zero locations. One of the outputs is either a notch, all-pass, or high-pass signal, depending on the feedback configuration chosen by the user; the other outputs are band-pass and low-pass signals. The center frequency of the complex pole pair, f_O, is determined by the external clock frequency and the state of the "50/100/CL" input. This value can also be scaled by a function of the external resistor values depending on the feedback configuration. The other important filter characteristics, such as gain, Q, etc. are determined by functions of external resistor values. Any of the classical filter configurations (Butterworth, Bessel, Cauer/Elliptic, Chebyshev, etc.) can be realized.

The second order sections can be used separately with the constraint that the clock input for each section be driven by signals of the same level (i.e., either TTL or CMOS logic levels), and that the two clock signals share the same digital ground. If it is desired that a fourth order function be realized, the two sections can be cascaded. The "L Sh" (level shift) input is used in conjunction with the clock inputs to allow compatibility with either TTL or CMOS clock levels.

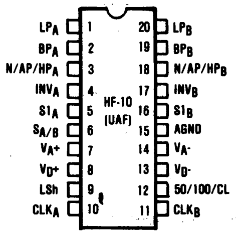
The HF-10 can be powered-down by connecting the "50/100/CL" input to V_D-. This disables the reference current generators for the operational amplifiers and the clock level shifters.

The HF-10 provides a number of advantages over other universal active filters: higher accuracy at frequency extremes; superior clock feedthrough suppression; significantly lower crosstalk; better performance over -55°C to +125°C; drives smaller impedance to higher peak output voltage; and capable of precision oscillator applications (phase is continuous when frequency is changed).

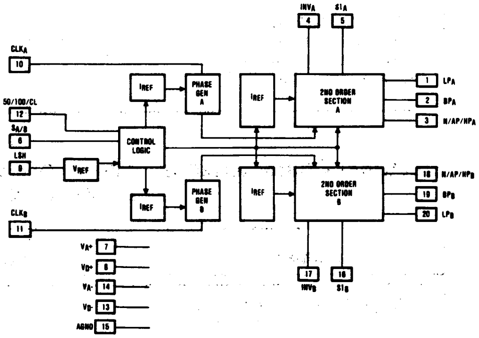
The device is available in a 20 pin ceramic package in commercial and military temperature ranges. Application note is available.

Pinout

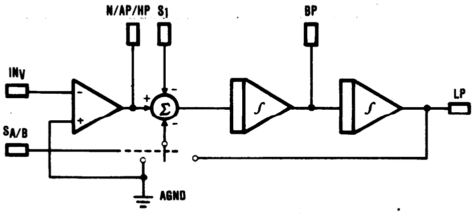
TOP VIEW



System Block Diagram



Filter Block Diagram



HF-10 Specifications

Absolute Maximum Ratings

Supply Voltages .... ±6.5 Volts
Power Dissipation 300mW
Operating Temperature .... -55°C to +125°C
Storage Temperature .... +150°C
Lead Temperature (Soldering, 10 Sec.) .... 300°C
Output Loading .... RLOAD ≧ 3.5KΩ
CLOAD ≦ 100pF

Electrical Characteristics (Complete Filter) ±4.5V < V_S < ±5.5V, -55°C < T_A < +125°C, Refer to Figure 1.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	f_o XQ < 50kHz	50		20K	Hz
Clock to Center Frequency Ratio					
f_{CLK}/f_o = 50	Pin 12 = V_D+, Q = 10 f_o XQ < 50kHz			±2%	
f_{CLK}/f_o = 100	Pin 12 = AGND, Q = 10 f_o XQ < 50kHz			±2%	
Q Range	f_o XQ < 50kHz	0.5		100	
Q Accuracy (Q Deviation from an Ideal Continuous Filter)					
f_{CLK}/f_o = 50	Pin 12 = V_D+, Q ≤ 20 f_o XQ < 50kHz			±4%	
f_{CLK}/f_o = 100	Pin 12 = AGND, Q ≤ 20 f_o XQ < 50kHz			±3%	
f_o XQ Product		50K			Hz
f_o Temperature Coefficient					
f_{CLK}/f_o = 50	T_A = 25°C Pin 12 = V_D+, f_o XQ < 50kHz External Clock Temperature Independent			±100	ppm/°C
f_{CLK}/f_o = 100	Pin 12 = AGND, f_o XQ < 50kHz External Clock Temperature Independent			±100	ppm/°C
Q Temperature Coefficient	T_A = 25°C f_o XQ < 50kHz, Q Setting Resistors Temperature Independent			±500	ppm/°C
Crosstalk	INV_A = 0dBm @ 1kHz INV_B = 0V		-60		dB
Clock Feedthrough	See Figure 2		2	5	mVrms
Clock Frequency	Min @ f_{CLK}/f_o = 50, Max @ f_{CLK}/f_o = 100	2.5		2048	kHz
Power Supply Current	T_A = 25°C		13		mA
Standby Current	Pin 12 = V_A-		500		µA

Electrical Characteristics (Internal Operational Amplifiers) ±4.5V < V_S < ±5.5V, -55°C < T_A < +125°C, Refer to Figure 1

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Swing (Pins 1, 2, 3, 18, 19, 20)	R_{LOAD} = 3.5KΩ	±3.5			V
Op Amp Gain-BW Product		2.5	3.8		MHz
Op Amp Slew Rate		5	15		V/µs
Power Supply Rejection Ratio (PSRR)	DC Only	40			dB

Pin Assignments

SYMBOL	DESCRIPTION
LP, BP, N/AP/HP (A or B)	Low-pass, band-pass, notch or all-pass or high-pass outputs of each second order section.
INV (A or B)	Inverting input of the summing op amp of each filter.
S1 (A or B)	Inverting summing input pin used in most filter configurations.
$S_{A/B}$	Activates a switch connecting one of the inputs of the filter's second summer to either analog ground ($S_{A/B}$ low to V_A-) or to the low-pass output of the circuit ($S_{A/B}$ high to V_A+). This allows flexibility in the various modes of operation of the I. C.
V_A+, V_D+	Analog positive supply and digital positive supply. These pins are internally connected through the I.C. substrate and therefore, V_A+ and V_Dx should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.
V_A-, V_D-	Analog and digital negative supply respectively. The same comments as for V_A+, V_D+ apply here.
L Sh	Level shift pin. Accommodates various clock levels with dual or single supply operation. With dual ±5V supplies, the HF-10 can be driven with CMOS clock levels (±5V), and the "L Sh" pin should be tied either to the system ground or to the negative supply pin. If the same supplies as above are used and TTL clock levels, derived from a 0V to 5V supply, are used, the "L Sh" pin should be tied to the system ground. For single supply operation (0V and 10V), the V_D- and V_A- pins should be connected to the system ground, the AGND pin should be biased at 5V, and the "L Sh" pin should also be tied to the system ground. This will accommodate both CMOS and TTL clock levels.
CLK (A or B)	Clock inputs for each switched capacitor filter building block. Should both be of the same level (TTL or CMOS). The level shift (L Sh) pin description discusses how to accommodate their levels. The duty cycle of the clock should preferably be close to 50%, especially when clock frequencies above 200kHz are used. This allows the maximum time for the op amps to settle, yielding optimum filter operation.
50/100/CL	By tying this pin to V_D+, a 50:1 clock to filter center frequency operation is obtained. Tying at mid-supplies (i. e., analog ground with dual supplies) allows the filter to operate at a 100:1 clock to center frequency ratio. When tied to VD-, a simple current limiting circuit is triggered to limit the overall supply current. The filtering action is then aborted.
AGND	Analog ground pin. Should be connected to the system ground for dual supply operation or biased at mid-supply for single supply operation. The Non-inverting inputs of the filter op amps are connected to the AGND pin so a "clean" ground is mandatory.

Note: All pins are protected against static discharge.

Typical Filter Configuration

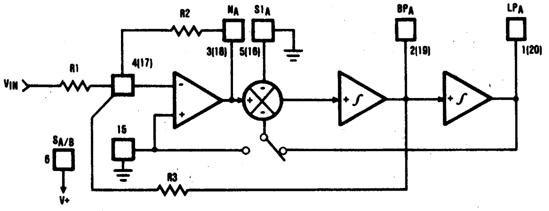

R2
NA
S1A
BPA
LPA
R1
4(17)
3(18)
5(16)
2(19)
1(20)
VIN
SA/B
6
15
R3
V+

FIGURE 1.

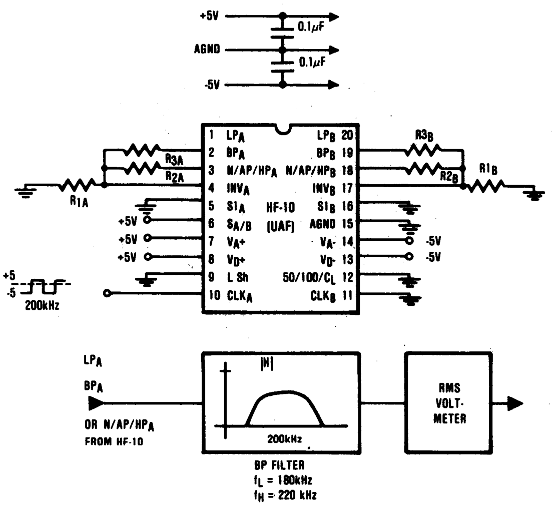

+5V
0.1µF
AGND
0.1µF
-5V
1 LPA
2 BPA
3 N/AP/HPA
4 INVA
5 S1A
6 SA/B
7 VA+
8 VD+
9 L Sh
10 CLKA
HF-10
(UAF)
LPB 20
BPB 19
N/AP/HPB 18
INVB 17
S1B 16
AGND 15
VA- 14
VD- 13
50/100/CL 12
CLKB 11
R3A
R2A
R1A
R3B
R2B
R1B
+5V
+5V
+5V
-5V
-5V
+5
-5
200kHz
LPA
BPA
OR N/AP/HPA
FROM HF-10
|H|
200kHz
BP FILTER
fL = 180kHz
fH = 220 kHz
RMS
VOLT-
METER

FIGURE 2. MEASURING CHANNEL A CLOCK FEEDTHROUGH

HARRIS

HC-5560

ADVANCE

Transcoder

Features

- Single 5V Supply .... 10mA Max.
- Mode Selectable Coding Including:
  - ▸ AMI (T1, T1C)
  - ▸ B8ZS (T1)
  - ▸ B6ZS (T2)
  - ▸ HDB3 (PCM30)
- North American and European Compatibility
- Simultaneous Encoding and Decoding
- Asynchronous Operation
- Loop Back Control
- Transmission Error Detection
- Alarm Indication Signal
- Replaces CD22103, MJ1440, MJ1471 and TCM2201 Transcoders

Applications

- North American and European PCM Transmission Lines where Pseudo Ternary Line Code Substitution Schemes are Desired
- Any Equipment that Interfaces T1, T1C, T2 or PCM30 Lines Including Multiplexers, Channel Service Units, (CSUs) Echo Cancellors, Digital Cross-Connects (DSXs), T1 Compressors, etc.

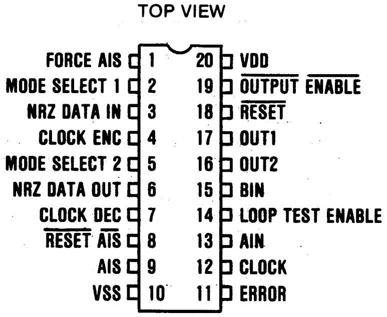
Description

The HC-5560 digital line transcoder provides encoding and decoding of pseudo ternary line code substitution schemes. Unlike other industry standard transcoders, the HC-5560 provides four worldwide compatible mode selectable code substitution schemes, including HDB3 (High Density Bipolar 3), B6ZS, B8ZS (Bipolar with 6 or 8 Zero Substitution), and AMI (Alternate Mark Inversion).

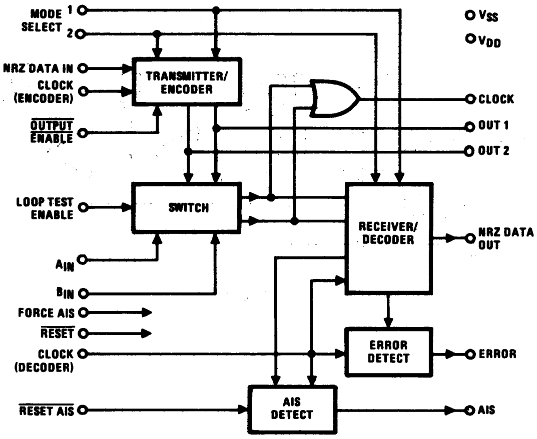
The HC-5560 is fabricated in CMOS and operates from a single 5V supply. All inputs and outputs are TTL compatible. The HC-5560 is available in 20 pin dual-in-line ceramic packages over the commercial temperature range, 0°C to +70°C.

The HC-5560 is ideally suited for use with the HC-5562 Receive Line Interface Unit (RLIU). Application Note Number 573 is available.

Pinout


TOP VIEW
FORCE AIS 1
MODE SELECT 1 2
NRZ DATA IN 3
CLOCK ENC 4
MODE SELECT 2 5
NRZ DATA OUT 6
CLOCK DEC 7
RESET AIS 8
AIS 9
VSS 10
20 VDD
19 OUTPUT ENABLE
18 RESET
17 OUT1
16 OUT2
15 BIN
14 LOOP TEST ENABLE
13 AIN
12 CLOCK
11 ERROR

Functional Diagram


MODE SELECT 1
2
NRZ DATA IN
CLOCK (ENCODER)
OUTPUT ENABLE
TRANSMITTER/ ENCODER
VSS
VDD
CLOCK
OUT 1
OUT 2
LOOP TEST ENABLE
SWITCH
RECEIVER/ DECODER
NRZ DATA OUT
AIN
BIN
FORCE AIS
RESET
CLOCK (DECODER)
ERROR DETECT
ERROR
RESET AIS
AIS DETECT
AIS

HC-5580

PRELIMINARY

Trunk Subscriber Line Interface Circuit — TSLIC

Features

- Meets FCC Part 68 Isolation and Most Signal Transmission Requirements
- Requires No External Transformers or Optoisolators
- Externally Programmable Termination Impedance
- Simple Interface to Data and Voice Systems
- Single Supply Operation from 5V to 15V
- Fully Integrated, Using Dielectric Isolation

Applications

- Trunk Interfaces for Private Branch Exchanges (PBXs), Automatic Call Distributors (ACDs), Remote Switching Units (RSUs), Least Cost Routing Systems (LCRs), Hybrid Key Systems, and Remote Line Testers.

Description

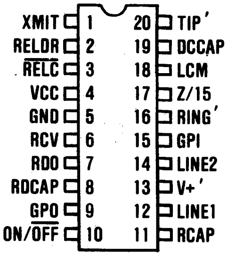
The Harris Trunk Subscriber Line Interface Circuit (TSLIC) incorporates into a single integrated circuit, the line interface on the terminal, private switching exchange, or subscriber end of the public switched telephone network.

Using the Harris dielectric isolation process, the TSLIC bridges the required isolation boundary without need for transformers or optoisolators.

The on-chip functions include on/off hook mode control, ring detection, hybrid, relay driver, loop current monitor, and a general purpose detector. The DC termination characteristic includes loop current limiting to minimize power dissipation. The off-hook AC termination impedance is externally set, giving complex or resistive line matching capability. The device can be interfaced to both loop-start and ground-start trunk lines.

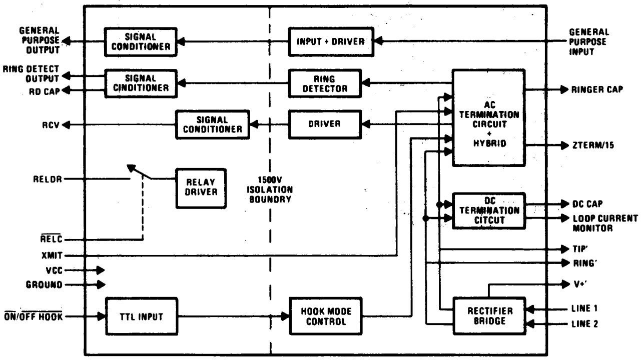
Pinout

TOP VIEW



XMIT 1
RELDR 2
$\overline{\text{RELC}}$ 3
VCC 4
GND 5
RCV 6
RDO 7
RDCAP 8
$\overline{\text{GPO}}$ 9
ON/$\overline{\text{OFF}}$ 10
20 TIP'
19 DCCAP
18 LCM
17 Z/15
16 RING'
15 GPI
14 LINE2
13 V+'
12 LINE1
11 RCAP

Functional Diagram



GENERAL PURPOSE OUTPUT
SIGNAL CONDITIONER
INPUT + DRIVER
GENERAL PURPOSE INPUT
RING DETECT OUTPUT
RD CAP
SIGNAL CINDITIONER
RING DETECTOR
AC TERMINATION CIRCUIT + HYBRID
RINGER CAP
RCV
SIGNAL CONDITIONER
DRIVER
ZTERM/15
RELDR
RELAY DRIVER
1500V ISOLATION BOUNDRY
DC TERMINATION CITCUT
DC CAP
LOOP CURRENT MONITOR
$\overline{\text{RELC}}$
XMIT
VCC
GROUND
TIP'
RING'
V+'
$\overline{\text{ON/OFF HOOK}}$
TTL INPUT
HOOK MODE CONTROL
RECTIFIER BRIDGE
LINE 1
LINE 2

HARRIS

PRELIMINARY

HC-5581

DAA Subscriber Line Interface Circuit — DAASLIC

Features

- Meets FCC Part 68 Isolation and Most Signal Transmission Requirements
- Requires No External Transformer or Optoisolators
- Externally Programmable Termination Impedance
- Simple Interface to Data and Voice Systems
- Single Supply Operation from 5V to 15V
- Fully Integrated, Using Dielectric Isolation

Applications

- Data Access Arrangement (DAA)
- Telephone Answering Machines
- Facsimile Machines
- Modems and Multiplexers

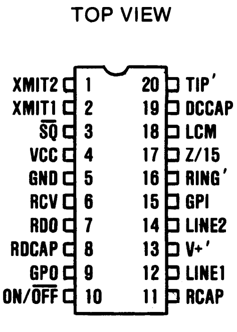
Description

The Harris Data Access Arrangement Subscriber Line Interface Circuit (DAASLIC) incorporates into a single integrated circuit, the line interface on the terminal or subscriber end of the public switched telephone network.

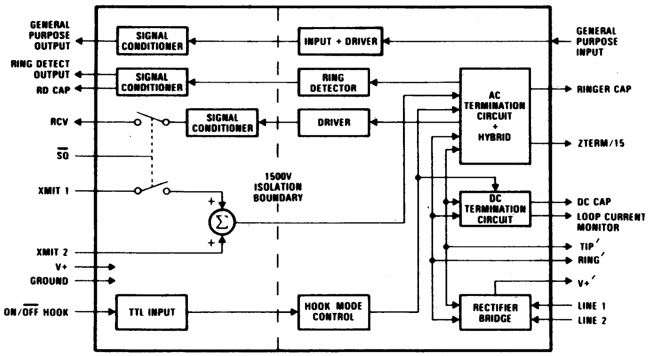
Using the Harris dielectric isolation process, the DAASLIC bridges the required isolation boundary without need for transformers or optoisolators.

The on-chip functions include on/off-hook mode control, ring detection, hybrid, dual transmit inputs, squelch, loop current monitor, and a general purpose detector. The DC termination characteristic includes loop current limiting to minimize power dissipation. The off-hook AC termination impedance is externally set, giving complex or resistive line matching capability.

Pinout


TOP VIEW
XMIT2 1
XMIT1 2
$\overline{SQ}$ 3
VCC 4
GND 5
RCV 6
RDO 7
RDCAP 8
GPO 9
ON/$\overline{OFF}$ 10
20 TIP'
19 DCCAP
18 LCM
17 Z/15
16 RING'
15 GPI
14 LINE2
13 V+'
12 LINE1
11 RCAP

Functional Diagram


GENERAL PURPOSE OUTPUT
RING DETECT OUTPUT
RD CAP
RCV
$\overline{SQ}$
XMIT 1
XMIT 2
V+
GROUND
ON/$\overline{OFF}$ HOOK
SIGNAL CONDITIONER
SIGNAL CONDITIONER
SIGNAL CONDITIONER
Σ
TTL INPUT
1500V ISOLATION BOUNDARY
INPUT + DRIVER
RING DETECTOR
DRIVER
HOOK MODE CONTROL
AC TERMINATION CIRCUIT + HYBRID
DC TERMINATION CIRCUIT
RECTIFIER BRIDGE
GENERAL PURPOSE INPUT
RINGER CAP
ZTERM/15
DC CAP
LOOP CURRENT MONITOR
TIP'
RING'
V+'
LINE 1
LINE 2

HC-5590

ADVANCE INFORMATION

Digital Line Transceiver — DLT

Features

- **Monolithic Integrated Device**
- **Data Rates up to 160K Bits/s will Support Two B and One D Channel with Additional Overhead for Frame and Handshake Information**
- **Full Duplex Transmission using AMI Line Code Adaptive Hybrid Techniques**
- **On Chip Clock Recovery Circuit Allows the Device to be Operated in Either a Master or Slave Mode**
- **Low Idle Power Dissipation Using State-of-the-art CMOS Technology**
- **Line Interface Driver**
- **Synchronous Serial Mode Allows External Protocol Generation with DLT Transparently Receiving/Transmitting**

Applications

- **Integrated Voice and Data Transmission**
- **Secure Voice and Data Terminals**
- **Integrated Digital Services Network (ISDN) U-Interface**

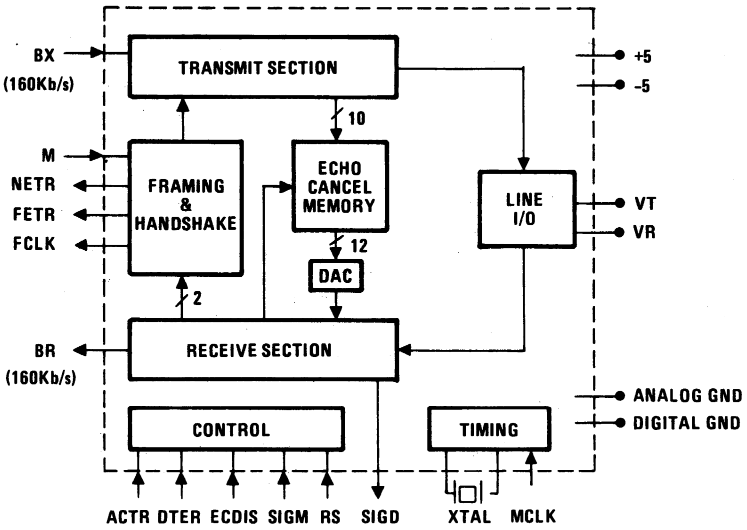
Description

The Harris Digital Line Transceiver (DLT) implements a complete full duplex data transmission system using an echo cancellation technique. Data rates up to 160KB/s can be accommodated. Functions of the circuit can be divided into three groups:
—transmit
—receive
—control/interface
The transmit functions include scrambler, bipolar coder and transmit filter. The receive functions and receive filter, $\sqrt{f}$ equalizer, echo canceller, detector, timing recovery and descrambler.

Transmitted and received bit streams are synchronous. Both are locked to a master clock running at 3.88MHz (for a 160KB/s data rate). The subscriber DLT extracts the clock from the received signal and locks its own transmitter to the recovered clock.

Block Diagram

HC-5590 DLT BLOCK DIAGRAM


BX
(160Kb/s)
TRANSMIT SECTION
10
+5
-5
M
NETR
FETR
FCLK
FRAMING & HANDSHAKE
ECHO CANCEL MEMORY
LINE I/O
VT
VR
12
DAC
2
BR
(160Kb/s)
RECEIVE SECTION
ANALOG GND
DIGITAL GND
CONTROL
TIMING
ACTR
DTER
ECDIS
SIGM
RS
SIGD
XTAL
MCLK

HARRIS

HC-5572

ADVANCE INFORMATION

Modem Signal Processor

Features

- **Monolithic Integrated Device**
- **CCITT V.22 BIS/V.22 and BELL 212A Compatible**
- **Adaptive and Compromise Equalizers Ensure Modem Performance Over Poor Telephone Line Conditions**
- **Microprocessor-Compatible Interface Bus**
- **Programmable Mode Selection**
- **Answer Tone Generation and Detection**
- **CCITT V.25 2100Hz Tone Generation and Detection**
- **State-of-the-art CMOS Technology, Ensuring Low Power Dissipation**

Description

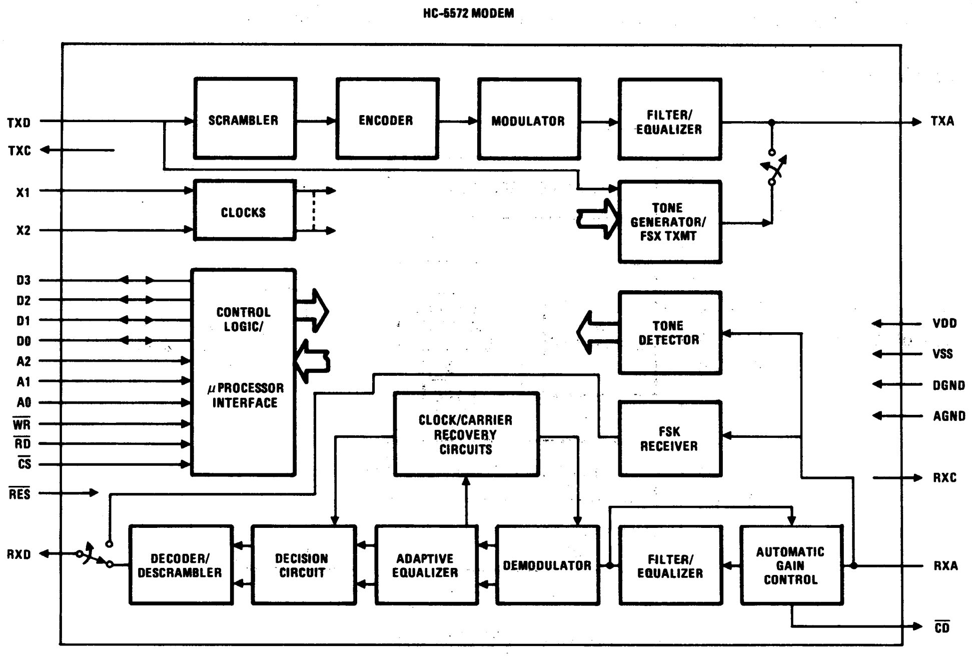
The Harris Modem Signal Processor is a single chip synchronous voiceband modem intended for use in switched or leased lines. It is programmable for operation at 2400, 1200, 600, or 300 bits per second (BPS), full duplex (FDX) data transmission compatible with CCITT V.22 BIS, V.22 or BELL 212A specifications.

Switched capacitor techniques are used in the HC-5572 to perform various signal processing functions. Adaptive and compromise equalizers are included to ensure the modem's performance over poor telephone line conditions.

The telephone line interface with the HC-5572 can be accomplished with either a solid-state terminal SLIC, such as the Harris HC-5580, or through a transformer-based Data Access Arrangement (DAA).

The HC-5572 is fabricated using CMOS technology. All digital input and output signals are TTL compatible. Power supply requirements are ±5V.

Functional Diagram


HC-5572 MODEM
TXD
TXC
X1
X2
D3
D2
D1
D0
A2
A1
A0
WR
RD
CS
RES
RXD
SCRAMBLER
ENCODER
MODULATOR
FILTER/ EQUALIZER
TXA
CLOCKS
TONE GENERATOR/ FSX TXMT
CONTROL LOGIC/
μPROCESSOR INTERFACE
TONE DETECTOR
VDD
VSS
DGND
AGND
CLOCK/CARRIER RECOVERY CIRCUITS
FSK RECEIVER
RXC
DECODER/ DESCRAMBLER
DECISION CIRCUIT
ADAPTIVE EQUALIZER
DEMODULATOR
FILTER/ EQUALIZER
AUTOMATIC GAIN CONTROL
RXA
CD

Quality & Reliability

9

The Total Approach to Quality 9-2

Harris Standard Flows 9-2

Quality Beginning to End 9-6

Electrical Screening and Test Procedures 9-9

Harris and The JAN Program 9-12

Burn-In Circuit Index 9-13

Burn-In Circuit Drawings 9-15

Harris Quality and Reliability

Harris Takes the Total Approach to Quality

Quality and reliability do not occur by accident in microcircuit manufacturing. They can be achieved only as a result of precise design, capable manufacturing methods, carefully controlled production processes and accurate screening and testing. Quality and reliability must be totally designed and built into the product. They are not characteristics that can be added after manufacture. They must be part and parcel of the flow from the original design through final assembly and test.

The major steps affecting microcircuit reliability and quality are:

- Initial circuit selection and design.
- Selection of package materials and design.
- Die layout and geometry.
- Raw material inspection and QC.
- Wafer/die production process and controls.
- Die/package assembly and controls.
- Screening and test procedures.

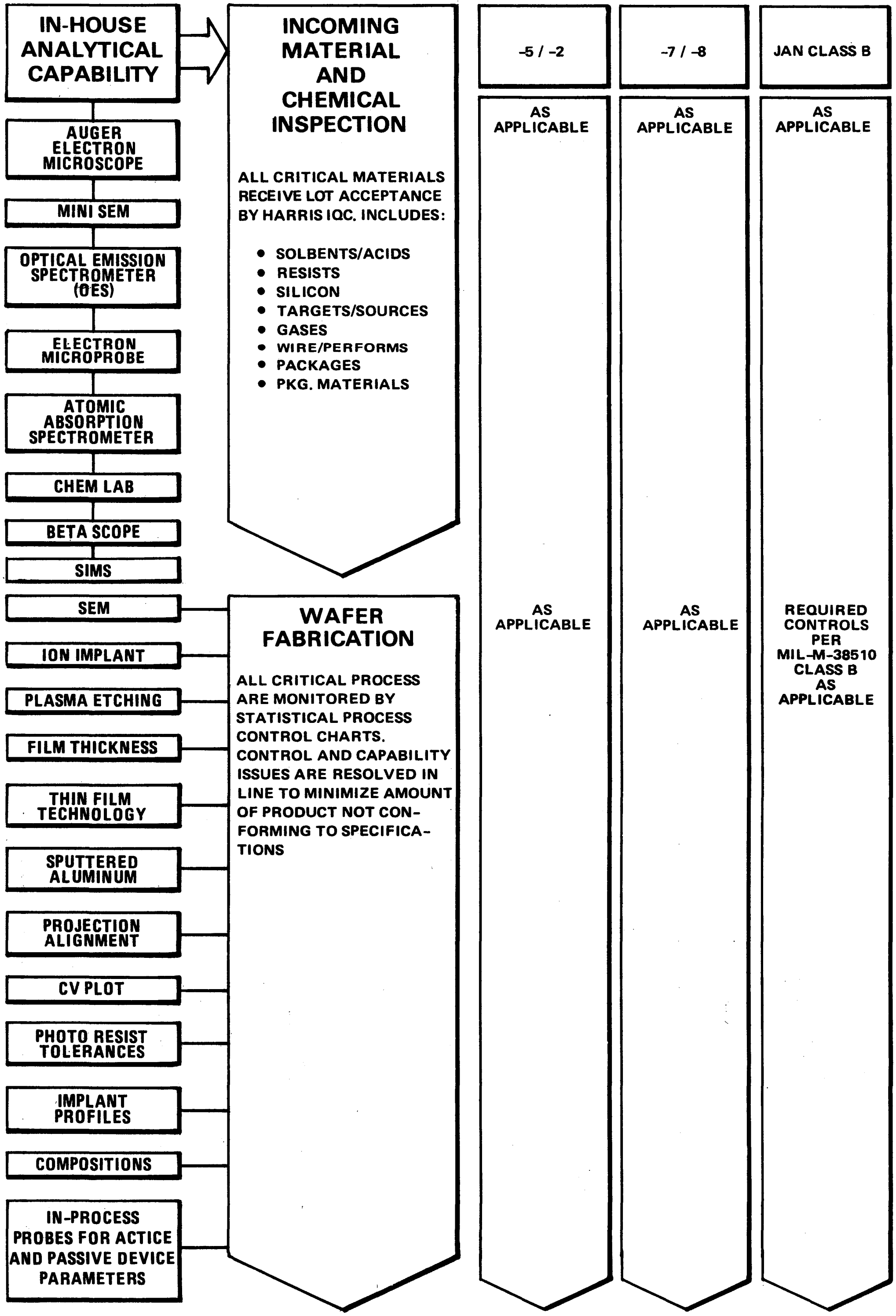
Harris Standard Flows

Harris Semiconductor offers a variety of standard product flows which cover the myriad of application environments our customers experience. These flows run the gambet of low cost commercial parts to fully qualified JAN microcircuits. All of these grades have one thing in common. They result from meticulous attention to quality, starting with design decisions made during product development and ending with the labeling of shipping containers for delivery to our customers. The standard flows offered are:

Dash 5 -	Electrical performance guaranteed from 0°C to +75°C.
Dash 7 -	Dash 5 plus 96 hours of burn-in to reduce infant mortality risk in customer applications.
Dash 2 -	Electrical performance guaranteed from -55°C to +125°C.
Dash 8 -	Electrical performance guaranteed from -55°C to +125°C plus 160 hours of burn-in with PDA of 5%. 100% preseal visual per Mil Std 883C Method 2010.
JAN Class B -	Fully qualified and certified microcircuit manufactured per Mil M 38510 requirements.

Details of the individual process requirements are contained in the flow charts which follow.

Harris Semiconductor Standard Processing Flows


IN-HOUSE ANALYTICAL CAPABILITY
AUGER ELECTRON MICROSCOPE
MINI SEM
OPTICAL EMISSION SPECTROMETER (OES)
ELECTRON MICROPROBE
ATOMIC ABSORPTION SPECTROMETER
CHEM LAB
BETA SCOPE
SIMS
SEM
ION IMPLANT
PLASMA ETCHING
FILM THICKNESS
THIN FILM TECHNOLOGY
SPUTTERED ALUMINUM
PROJECTION ALIGNMENT
CV PLOT
PHOTO RESIST TOLERANCES
IMPLANT PROFILES
COMPOSITIONS
IN-PROCESS PROBES FOR ACTICE AND PASSIVE DEVICE PARAMETERS
INCOMING MATERIAL AND CHEMICAL INSPECTION
WAFER FABRICATION
-5 / -2
-7 / -8
JAN CLASS B
AS APPLICABLE
AS APPLICABLE
AS APPLICABLE
AS APPLICABLE
AS APPLICABLE
REQUIRED CONTROLS PER MIL-M-38510 CLASS B AS APPLICABLE

INCOMING MATERIAL AND CHEMICAL INSPECTION

ALL CRITICAL MATERIALS RECEIVE LOT ACCEPTANCE BY HARRIS IQC. INCLUDES:

- SOLBENTS/ACIDS
- RESISTS
- SILICON
- TARGETS/SOURCES
- GASES
- WIRE/PERFORMS
- PACKAGES
- PKG. MATERIALS

WAFER FABRICATION

ALL CRITICAL PROCESS ARE MONITORED BY STATISTICAL PROCESS CONTROL CHARTS. CONTROL AND CAPABILITY ISSUES ARE RESOLVED IN LINE TO MINIMIZE AMOUNT OF PRODUCT NOT CONFORMING TO SPECIFICATIONS

(1) T_A = -55°C to +125°C for all grades except DASH-7 (DASH-7 T_A = 0°C to +75°C)

Harris Semiconductor Standard Processing Flows
(continued)

LASER TRIMMING AT BOTH PACKAGE AND WAFER LEVELS

HIGH/ROOM TEMP PROBE TEST

DIE ATTACH CONTROL

WIRE BOND CONTROL

PRE-SEAL WASH IN LAMINAR FLOW

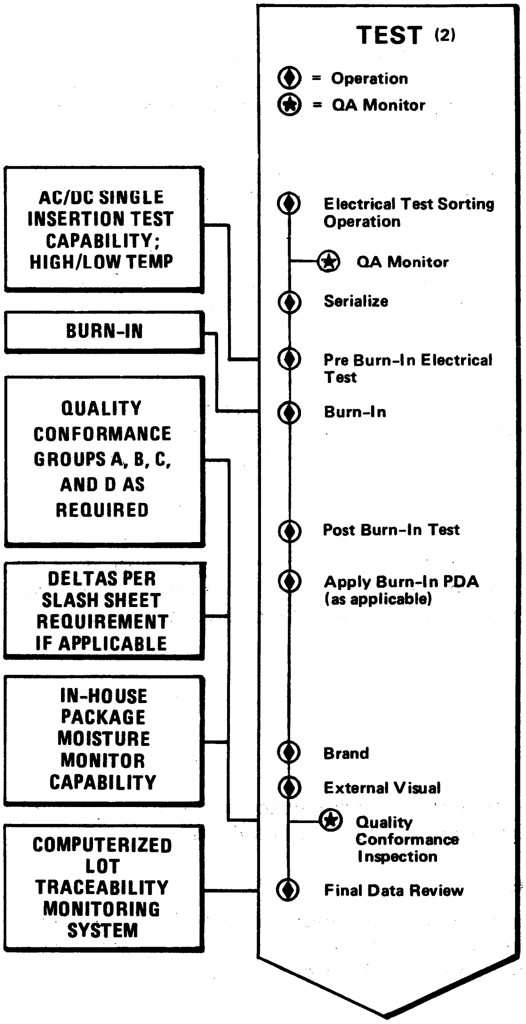
PRE-SEAL VISUAL INSPECTION IN CLASS 100 LAMINAR FLOW

PARTICLE IMPACT NOISE DETECTION (PIND) AS REQUIRED

	-5 / -2	-7 / -8	JAN Class B
PROBE/DICE PREPARATION	VISUAL INSPECTION WITH QC MONITOR	VISUAL INSPECTION WITH QC MONITOR	VISUAL INSPECTION PER MIL-STD-883. METHOD 2010. CONDITION B, WITH QC MONITOR
ASSEMBLY (1)			
◆ = Operation ★ = QA Monitor			
◆ Lead Frame Clean	YES	YES	YES
◆ Die and Frame Attach Control	YES	YES	YES
◆ Wire Bond	YES	YES	YES
★ QA Wire Bond Control	4-HOUR	4-HOUR	4-HOUR
◆ Pre-Seal Clean	AS REQUIRED	AS REQUIRED	YES
◆ Pre-Seal Inspect	YES	YES	PER MIL-STD-883 METHOD 2010, CONDITION B
★ QA Pre-Seal Inspect	YES	YES	YES
(GSI) GSI Inspect	NO	NO	YES
◆ Cerdip Sealing	YES	YES	YES
★ QA Seal Control	YES	YES	YES
◆ Stabilization Bake	NO	AS APPLICABLE	YES
◆ Temperature Cycle	YES	YES	YES
◆ Centrifuge	YES	YES	YES
◆ Tin-Plating	YES	YES	YES
★ QA Tin-Plating Inspect	YES	YES	YES
◆ Fine Leak Test	YES	AS APPLICABLE	YES
◆ Gross Leak Test	YES	AS APPLICABLE	YES
◆ PIND Test 100%	AS APPLICABLE	AS APPLICABLE	AS APPLICABLE
◆ Frame Removal	YES	YES	YES
◆ Load Shipping Tubes	YES	YES	YES
★ QA Final Inspect	YES	YES	YES
★ QA Documentation Inspect	NO	NO	YES

(1) Example for a Cerdip package part.

Harris Semiconductor Standard Processing Flows (continued)


TEST (2)
◆ = Operation
★ = QA Monitor
AC/DC SINGLE INSERTION TEST CAPABILITY; HIGH/LOW TEMP
BURN-IN
QUALITY CONFORMANCE GROUPS A, B, C, AND D AS REQUIRED
DELTAS PER SLASH SHEET REQUIREMENT IF APPLICABLE
IN-HOUSE PACKAGE MOISTURE MONITOR CAPABILITY
COMPUTERIZED LOT TRACEABILITY MONITORING SYSTEM

TEST (2)	-5 / -2	-7 / -8	JAN Class B
◆ Electrical Test Sorting Operation	YES	YES	YES
★ QA Monitor	YES	YES	NO
◆ Serialize	NO	NO	Group A and C Samples Only
◆ Pre Burn-In Electrical Test	NO	YES	YES
◆ Burn-In	NO	DASH-8: 160 HR @ +125°C DASH 7: 96 HR @ +125°C	160 HR @ +125°C, OR PER SLASH SHEET
◆ Post Burn-In Test	NO	YES	YES
◆ Apply Burn-In PDA (as applicable)	NO	No for -7 5% for -8	PER SLASH SHEET
◆ Brand	YES	YES	YES
◆ External Visual	YES	YES	YES
★ Quality Conformance Inspection	GROUP A	GROUP A	GROUP A, B, C, D
◆ Final Data Review	NO	NO	YES

Package & Ship or Stock

(2) -5 / -7 0°C to +75°C
-2 / -8 / JAN -55°C to +125°C

Advantages of Standard Flows

Wherever feasible, and in accordance with good value engineering practice, the IC user should specify device grades based on one of the five standard Harris manufacturing flows. These are more than adequate for the overwhelming majority of applications and may be utilized quite effectively if the user engineer bases his designs on the standard data book or slash sheet (as applicable) electrical limits.

Some of the more important advantages gained by using standard as opposed to custom flows are as follows:

- Lower cost than the same or an equivalent flow executed on a custom basis. This results from the higher efficiency achieved with a constant product flow and the elimination of such extra cost items as special fixturing, test programs, additional handling, and added documentation.
- Faster delivery. The manufacturer often can supply many items from inventory and, in any case, can establish and maintain a better product flow when there is no need to restructure process and/or test procedures.
- Increased confidence in the devices. A continuing flow of a given product permits the manufacturer to monitor trends which may bear on end-product performance or reliability and to implement corrective action, if necessary.
- Reduction of risk. Since each product is processed independent of specific customer orders, the manufacturer absorbs production variability within its scheduling framework without major impact on deliveries. In a custom flow, a lot failure late in the production cycle can result in significant delays in delivery due to the required recycling time.

Despite the advantages of using standard flows, there are cases where a special or custom flow is mandatory to meet design or other requirements. In such cases, the Harris Marketing groups stand ready to discuss individual customer needs and, where indicated, to accomodate appropriate custom flows.

Quality Beginning to End

There are several significant elements which comprise Harris Semiconductor's approach to quality that don't show on a process flow chart. Some of these are as follows:

INITIAL CIRCUIT SELECTION AND DESIGN

Once operational characteristics and parameter limits have been defined there are many different circuit configurations capable of conforming to them. Harris designers are tasked to choose those which are capable of meeting the required performance specifications with maximum reliability.

Powerful computer aided design (CAD) techniques are applied in developing the original concepts and detailed schematics, with computer modeled circuit simulation used to corroborate projected product performance. Monte Carlo methods, and other simulation techniques are also used, as appropriate to achieve specific objectives.

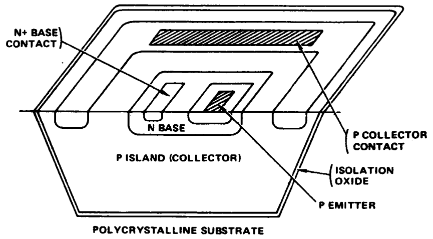
Regardless of the circuit approach selected, high reliability, top performance, and maximum potential yield to the required specifications are the governing criteria.

Individual active device types and component values are selected to provide optimum circuit performance and to minimize sensitivity to parametric changes which may occur with aging or as a result of environmental conditions.

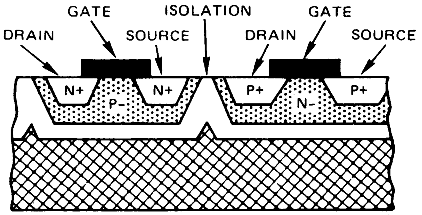
Since most Harris products are sold into military, industrial and commercial end use applications most circuits are designed to meet military temperature range requirements at the outset. This results in more capable products introduced to all segments of the marketplace.

Die Layout and Geometry

Conformance with good layout practice is a must, for consistently reliable devices cannot be assembled from poorly designed chips. Therefore, the IC layout phase at Harris is controlled by ground rules which establish the "do's" and "don'ts" for each manufacturing process. These rules define dimensions and toleranced to insure product immunity to process variations, while maximizing product reliability under worst-case stress conditions. Computerized ground rule software packages are used by the chip designers to assure dimensional adherence of diffusion windows as well as interconnect width and spacing. Automatic checkout procedures confirm that the product conforms to the established ground rules.



Cross-sectional view of high-frequency PNP device formation in the DI process.



Dielectric isolation eliminates latch-up by placing a silicon-dioxide isolation barrier between devices. This separates all active elements, eliminating interface junctions that cause parasitic SCRs.

Raw Material Inspection and QC

Acknowledging that Hi-Rel, high performance devices can be manufactured only by using top quality materials, Harris subjects incoming materials, piece parts and supplies to documented tests and inspections. The techniques used are selected for optimum evaluation of the materials checked to ensure full compliance with Harris internal specifications. Close coordination with the suppliers is maintained to assure a reliable supply of quality materials.

Wafer Die Production Process and Controls

Harris has a wide range of state-of-the-art wafer and die processing capabilities, permitting the circuit designer to choose the optimum production technique for each type of device.

Depending on specific design and performance specifications, devices, may be fabricated using either conventional or complementary bipolar, CMOS, combined bipolar and CMOS, NMOS or PMOS construction. Two complementary vertical bipolar processes are available, offering frequency responses two orders of magnitude higher than conventional fabrication techniques.

Regardless of the process involved, statistical process control charts are employed to maximize the visibility of wafer lot variability during production. These charts take the form of $\overline{X}$/R charts for variables data and $\overline{C}/\overline{p}$ charts for attributes data. Typical process control points include diffusion, thin film, photo resist steps as well as inspection points or electrical device measurements. The goal of the control charts is three fold:

- Isolate and eliminate special causes of variability to preclude the production of wafers with a process which is not operating correctly.
- Define the natural limits of variability in a process to determine its capability in light of engineering expectation.
- Provide a reference baseline for process enhancements or changes to improve capability or reduce cost.

With high reliability an integral part of its manufacturing philospohy, Harris Semiconductor does not have separate production lines for standard and JAN devices. Rather, all Harris devices of a given type are manufactured on the same line. Product grades are selected by the application of screening tests and inspection from the same generic process flows in wafer fab.

Die/Package Assembly and Controls

Each major process operation (mount, bond, seal, trim) is carefully monitored by in-process quality control steps. In addition, many mechanical and environmental tests are implemented during the die/package assembly stage. The specific controls and tests utilized at each step are in strict compliance with the applicable standards for the device reliability class designation.

Burn-In

100% burn-in is a screening procedure used when applicable to detect devices subject to infant mortality failure modes. Biases are applied to simulate worst-case operational conditions, permitting the identification and elimination of marginal units.

The applied voltage levels, operational state, temperature and test period vary with the type of device and reliability class, as governed by the applicable standards. Electrical test of the device is performed both prior to and after the burn-in period.

Electrical Screening and Test Procedures

While many factors are critical in the production of I. C. devices, the electrical screening and test procedures, are critical to matching product performance to customer need. All products receive 100% electrical test per the data sheet requirements for each product type. In addition product lots received a battery of QA inspections and tests to assure compliance with Harris production standards.

Reliability Assessment and Enhancement

At Harris, realibility assurance is a dynamic program with the primary and ultimate goal of securing full product performance throughout its usage life. Each manufacturing phase from original design to final packaging is subject to continuous review, analysis, and evaluation, with modifications introduced as needed to improve product performance and reliability. There are three important sources of reliability data:

1. Initial qualification
2. Add on life
3. Field failure history

New Products/Processes/Packages

Two requirements are imposed on the product development phase of new circuits and processes. First is the use of proper process methodology, design techniques, and layout practices. New designs are reviewed throughout the course of their development for conformance to the constraints defined by process ground rules. These rules document the results of years of experimentation and experience and reflect a relatively conservative approach to process capability and technology. Second is demonstration of reliability performance of a new product or process through a series of stress tests designed to accelerate typical failure mechanisms in integrated circuits. Qualification requirements are illustrated in Table I for a variety of product/process/package maturity conditions. These tests are executed by the Harris Reliability organization for each new product/package/process before circuits are committed to the marketplace. Failure rate predictions are made based on test results. More importantly, failure analysis results are fed back into design and process engineering organizations to generate corrective action (if applicable) and enhance product performance. Each new product entry must meet minimum failure rate standards to qualify for sale to customers.

"Add On"

An important source of reliability information is performance of established products through extended life testing under worst-case operating conditions. Failure rate predictions for specific products or product types are available on request via Harris Semiconductor Reliability bulletins;

Accelerated life test are utilized to estimate the expected field failure rate of our products. Life tests are conducted periodically on regular production samples. Sample sizes are typically 200 units which are operated at 125°C at nominal supply voltages and with forcing and loading conditions simulating typical application environments. Where possible, operating conditions are structured to provide maximum thermal and electrical acceleration of the natural failure mechanisms found in I. C. devices.

All rejected devices are carefully analyzed and activation energies are assigned based on the observed failure mechanisms. There rates are then computed based on thermal derating factors per the Arrhenius equation. The results are reported in the Harris Reliability bulletins based on derating to +55°C operations and nominal supply conditions. Failure rates are reported at the 60% confidence level and the 95% confidence level.

Finally, life tests are monitored at mid-point intervals to assure that failure rates are decreasing and that no wearout mechanisms are at work.

TABLE 1. TEST MATRIX

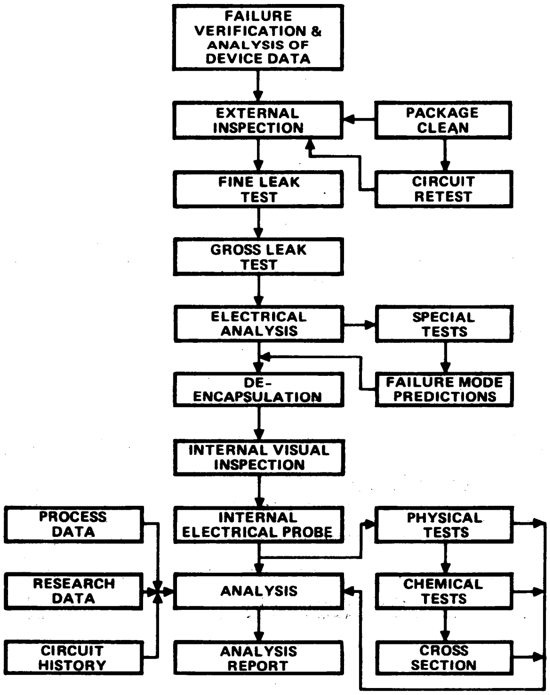
Design Package Process	New New New	New New Est.	New Exist New	New Exist Est.	Exist New New	Exist New Est.	Exist Exist New	Exist Exist Est.
Abuse Tests 20 Units	X	X	X	X	X		X	X
Max. Ratings 20 Units: No Failures	X		X	X	X		X	X
86/86 or Autoclave 50 Units: No Failures	X	X	X		X	X	X	
Constr. Analysis 5 Units: No Failures	X	X	X	X	X	X	X	X
Centrifuge 50 Units: No Failures	X	X			X	X		
Ele. Charac. 20 Units: No Failures	X	X	X	X	X		X	X
ESD Immunity 20 Units: No Failures	X	X	X	X	X		X	X
Fig. Test 20 Units: No Failures	X	X	X	X	X		X	
HTOL Sample Groups	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)
Latch-up 20 Units: No Failures	X	X	X	X	X			
Lead Integrity 20 Units: No Failures	X	X			X	X	X	X
Mech. Charac. 20 Units: No Failures	X	X			X	X		
Mech. Schock 50 Units: No Failures	X	X			X	X		
Moisture Resist 50 Units: No Failures	X	X			X	X		
θja/θjc 20 Units	X	X			X	X		
Solvent Resistance 4 Units: No Failures	X	X			X	X		
Solderability 20 Units: No Failures	X	X			X	X		
Temperature Cycling 50 Units: No Failures	X	X			X	X		
Thermal Shock 50 Units: No Failures	X	X			X	X		
Vibration 50 Units: No Failures	X	X			X	X		

Field Failures

The final source of continued reliability assessment and enhancements is the analysis of defects on products returned by our customer.

An exhaustive analysis of device failures is a requirement of the Harris reliability program. After failure confirmation by electrical test, the device is processed through the standard failure analysis procedure outlined below.

FAILURE ANALYSIS FLOW


FAILURE VERIFICATION & ANALYSIS OF DEVICE DATA
EXTERNAL INSPECTION
PACKAGE CLEAN
FINE LEAK TEST
CIRCUIT RETEST
GROSS LEAK TEST
ELECTRICAL ANALYSIS
SPECIAL TESTS
DE-ENCAPSULATION
FAILURE MODE PREDICTIONS
INTERNAL VISUAL INSPECTION
PROCESS DATA
INTERNAL ELECTRICAL PROBE
PHYSICAL TESTS
RESEARCH DATA
ANALYSIS
CHEMICAL TESTS
CIRCUIT HISTORY
ANALYSIS REPORT
CROSS SECTION

Harris and the JAN Program

Harris Semiconductor became an active participant in the JAN program as the first microcircuit manufacturer to JAN-qualify a PROM, receiving a QPL-2 qualification in 1972 and the higher level QPL-1 qualification in 1974 for the military version of the HPROM-0512, as defined by MIL-M-38510, Slash Sheet 201. Since this initial effort, Harris has received JAN line certification for production lines supplying dielectrically isolated (DI) operational amplifiers, analog switches, analog multiplexers, and junction isolated op amps.

Harris will continue to pursue further line certification and part qualification efforts, offering users an ever-expanding line for JAN-qualified devices.

JAN-Qualified Devices

TYPE	FUNCTION	MIL-M-38510/	QPL-1
HA2-2600	High Performance Operational Amplifier	12202BGC	Now Qualified
HA2-2620	Very Wide Band, Uncompensated Op Amp	12203BGC	Now Qualified
HA2-2500	Precision High Slew Rate Op Amp	12204BGC	Now Qualified
HA2-2510	High Slew Rate Op Amp	12205BGC	Now Qualified
HA2-2520	High Slew Rate Uncompensated Op Amp	12206BGC	Now Qualified
HA1-4741	Quad Operational Amp	11003BCB	Now Qualified
HI-201	Quad SPST CMOS Analog Switch	12302BEB	Now Qualified

Burn-In Circuit Index

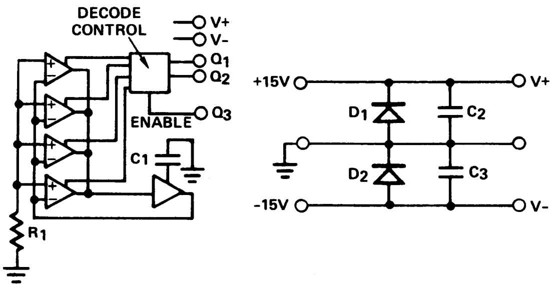
		DRAWING NUMBER
HA-OP07	Precision Operational Amplifier	4
HA-OP27	Ultra-Low Noise, Precision Operational Amplifier	5
HA-OP37	Ultra-Low Noise, Precision, High-Speed Operational Amplifier	5
HA-2400/04/05	PRAM, Four Channel Operational Amplifiers	1
HA-2406	Digitally Selected 4 Channel Operational Amplifier	1
HA-2420/25	Fast Sample and Hold Operational Amplifiers	2
HA-2420 (LCC)	Fast Sample and Hold Operational Amplifiers	3
HA-2500/02/05	Precision High Slew Rate Operational Amplifiers	4
HA-2510/12/15	High Slew Rate Operational Amplifiers	4
HA-2520/22/25	Uncompensated High Slew Rate Operational Amplifiers	4
HA-2539	Very High Slew Rate Wideband Operational Amplifiers	5
HA-2540	Wideband, Fast Settling Operational Amplifiers	5
HA-2541	Wideband, Fast Settling, Unity Gain Stable Operational Amplifiers	5
HA-2542	Wideband, High Slew Rate, High Output Current Operational Amplifiers	5
HA-2544	Video Operational Amplifiers	4
HA-2600/02/05	Wideband, High Impedance Operational Amplifiers	4
HA-2620/22/25	Very Wideband, Uncompensated Operational Amplifiers	4
HA-2630/35	High Performance Current Booster	6
HA-2640/45	High Voltage Operational Amplifiers	7
HA-2650/55	Dual High Performance Operational Amplifiers	8
HA-2720/25	Wide Range Programmable Operational Amplifiers	10
HA-4600/02/05	High Performance Quad Operational Amplifiers	11
HA-4741	Quad Operational Amplifier	11
HA-4900/02/05	Precision Quad Comparators	12
HA-5002	Monolithic, Wideband, High Slew Rate, High Output Current Buffer	13
HA-5033	Video Buffer	6
HA-5101	Low Noise, High Performance Operational Amplifier	4
HA-5102	Low Noise, High Performance Operational Amplifiers	8, 9
HA-5104	Low Noise, High Performance Operational Amplifers	11
HA-5111	Low Noise, High Performance Operational Amplifiers	5
HA-5112	Low Noise, High Performance Operational Amplifiers	9
HA-5114	Low Noise, High Performance Operational Amplifiers	14
HA-5130/35	Precision Operational Amplifiers	4
HA-5134	Precision Quad Operational Amplifiers	11
HA-5141	Ultra-Low Power Operational Amplifier	4
HA-5142	Ultra-Low Power Operational Amplifier	8, 9
HA-5144	Ultra-Low Power Operational Amplifier	11
HA-5147	Ultra-Low Noise, Precision High Slew Rate, Wideband Operational Amplifier	5
HA-5151	Low Power Operational Amplifier	4
HA-5152	Low Power Operational Amplifier	8, 9
HA-5154	Low Power Operational Amplifier	11
HA-5160/62	Wideband, JFET Input, High Slew Rate, Uncompensated Operational Amplifier	4
HA-5170	Precision JFET Input Operational Amplifier	4
HA-5180	Low Bias Current, Low Power JFET Input Operational Amplifier	4
HA-5190/95	Wideband, Fast Settling Operational Amplifiers	5
HA-5320	High Speed Precision Monolithic Sample and Hold Amplifier	15
HA-5330	Very High Speed Precision Monolithic Sample and Hold Amplifier	16
HC-5502A	Subscriber Line Interface Circuit (SLIC)	17
HC-5504	Subscriber Line Interface Circuit (SLIC)	18
HC-5508	Subscriber Line Interface Circuit (SLIC)	19
HC-5510	PCM CODEC	20
HC-5511	PCM CODEC	21
HC-5512/5512A	PCM Monolithic Filter	22
HC-5512C	PCM or CVSD Monolithic Filter	22
HC-5512D	PCM or CVSD Monolithic Filter	22
HC-5554	Monolithic CMOS Serial Interface COFIDEC Family	23
HC-5557	Monolithic CMOS Serial Interface COFIDEC Family	23
HC-55564	All-Digital Continuously Variable Slope Delta Modulator (CVSD)	24
HF-10	Universal Active Filter	25
HI-200	Dual SPST CMOS Analog Switch	26
HI-200 (LCC)	Dual SPST CMOS Analog Switch	27

Burn-In Index (Continued)

		DRAWING NUMBER
HI-201	Quad SPST CMOS Analog Switch	28
HI-201HS	High Speed Quad SPST CMOS Analog Switch	28
HI-300	Dual SPST CMOS Analog Switch	29
HI-301	SPDT CMOS Analog Switch	29
HI-302	Dual DPST CMOS Analog Switch	29
HI-303	Dual SPDT CMOS Analog Switch	30
HI-304	Dual SPST CMOS Analog Switch	30
HI-305	SPDT CMOS Analog Switch	30
HI-306	Dual DPST CMOS Analog Switch	30
HI-307	Dual SPDT CMOS Analog Switch	38
HI-381	Dual SPST CMOS Analog Switch	31
HI-384	Dual DPST CMOS Analog Switch	32
HI-387	SPDT CMOS Analog Switch	31
HI-390	Dual SPDT CMOS Analog Switch	32
HI-506/507	Single 16/Differential 8 Channel CMOS Analog Multiplexers	34
HI-506A/507A	16 Channel CMOS Analog Multiplexers with Overvoltage Protection	34
HI-506/507 (LCC)	Single 16/Differential 8 Channel CMOS Analog Multiplexers	35
HI-506A/507A (LCC)	16 Channel CMOS Analog Multiplexers with Overvoltage Protection	35
HI-506LA/507LA	Single 16/Differential 8 Channel CMOS Analog Multiplexers with Latches and Overvoltage Protection	36
HI-508/508A	8 Channel Single-Ended Multiplexer	37
HI-508/508A (LCC)	8 Channel Single-Ended Multiplexer	38
HI-508LA/509LA	Single 8/Differential 4 Channel CMOS Analog Multiplexers with Latches and Overvoltage Protection	39
HI-509/509A	4 Channel Differential Multiplexers	40
HI-509/509A (LCC)	4 Channel Differential Multiplexers	41
HI-516	16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer	42
HI-516 (LCC)	16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer	43
HI-518	8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer	44
HI-524	4 Channel Video Multiplexer	45
HI-539	Monolithic, Four Channel, Low Level, Differential Multiplexer	40
HI-562A	12-Bit High Speed Monolithic Digital-to-Analog Converter	46
HI-562A (LCC)	12-Bit High Speed Monolithic Digital-to-Analog Converter	47
HI-565A	High Speed Monolithic Digital-to-Analog Converter with Reference	48
HI-574A	Fast, Complete 12-Bit A/D Converter with Microprocessor Interface	49
HI-674A	12μs, Complete 12-Bit A/D Converter with Microprocessor Interface	49
HI-1818A	Low Resistance 8 Channel CMOS Analog Multiplexer	50
HI-1828A	Low Resistance 8 Channel CMOS Analog Multiplexer	51
HI-5040	Low Resistance SPST Switch	33
HI-5041	Low Resistance Dual SPST Switch	33
HI-5042	Low Resistance SPDT Switch	33
HI-5043	Low Resistance Dual SPDT Switch	33
HI-5044	Low Resistance DPST Switch	33
HI-5045	Low Resistance Dual DPST Switch	33
HI-5046	Low Resistance DPDT Switch	33
HI-5046A	Low Resistance DPDT Switch	33
HI-5047	Low Resistance 4 PST Switch	33
HI-5047A	Low Resistance 4 PST Switch	33
HI-5048	Low Resistance Dual SPST Switch	33
HI-5049	Low Resistance Dual DPST Switch	33
HI-5050	Low Resistance SPDT Switch	33
HI-5051	Low Resistance Dual SPDT Switch	33
HI-5610	10-Bit High Speed Monolithic Digital-to-Analog Converter	52
HI-5618A/5618B	8-Bit High Speed Digital-to-Analog Converters	53
HI-5660/5660A	High Speed Monolithic Digital-to-Analog Converter	54
HI-5687 (I)	Wide Temperature Range Monolithic 12-Bit Digital-to-Analog Converter	55
HI-5687 (V)	Wide Temperature Range Monolithic 12-Bit Digital-to-Analog Converter	56
HI-7541	12-Bit Multiplying Monolithic Digital-to-Analog Converter	57
HI-7541 (LCC)	12-Bit Multiplying Monolithic Digital-to-Analog Converter	58
HV-1000	Induction Motor Energy Saver	59
HY-9574	Sampling 12-Bit A/D Converter with 8/16-Bit Microprocessor Interface	60
HY-9590/91	Data Acquisition Front End	61

1

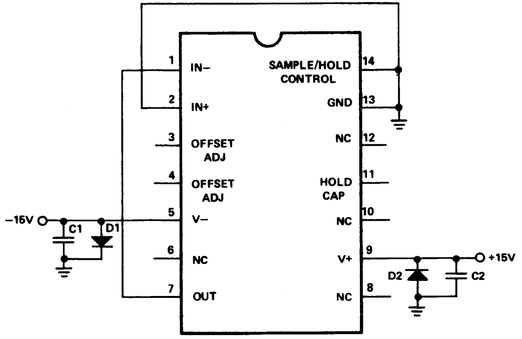
HA-2400/04/05, HA-2406


DECODE
CONTROL
V+
V-
Q_1
Q_2
ENABLE
Q_3
C1
R_1
+15V
V+
D_1
C_2
D_2
C_3
-15V
V-

NOTES:
R_1 = 100K ± 5%
C_1 = 910pF
C_2, C_3 = 0.01 μF
D_1, D_2 = IN 4002
Q_1 = 100KHz
Q_2 = 50KHz
Q_3 = 25KHz

2

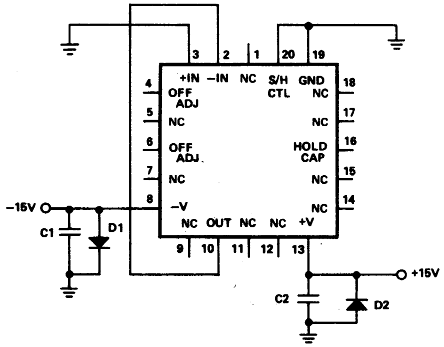
HA-2420/25


1
IN–
2
IN+
3
OFFSET
ADJ
4
OFFSET
ADJ
5
V–
6
NC
7
OUT
SAMPLE/HOLD
CONTROL
14
GND
13
NC
12
11
HOLD
CAP
10
NC
9
V+
8
NC
–15V
C1
D1
+15V
D2
C2

NOTES:
C1, C2 = .01 μF
D1, D2 = IN4002

3

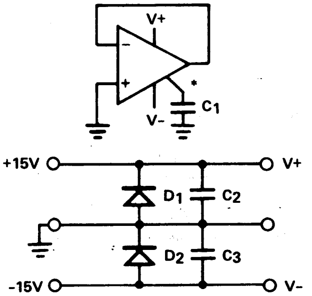
HA-2420 (LCC)


3
2
1
20
19
+IN
–IN
NC
S/H
CTL
GND
NC
18
4
OFF
ADJ
5
NC
NC
17
6
OFF
ADJ.
HOLD
CAP
16
7
NC
NC
15
8
–V
NC
14
NC
OUT
NC
NC
+V
9
10
11
12
13
–15V
C1
D1
+15V
C2
D2

NOTES:
C1, C2 = 0.01 μF
D1, D2 = IN 4002

4

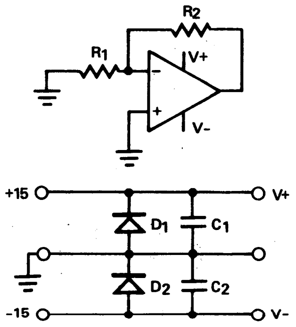
HA-2500/02/05; HA-2510/12/15; HA-2520/22/25; HA-2544; HA-2600/02/05; HA-2620/22/25; HA-5101; HA-5130/35; HA-5141; HA-5151; HA-5160/62; HA-5170; HA-5180; HA-OP07


V+
–
+
*
C1
V-
+15V
V+
D_1
C_2
D_2
C_3
-15V
V-

NOTES:
C_1,= 0.01 μF
C_2, C_3 = 0.01 μF
D_1, D_2 = IN 4002

5

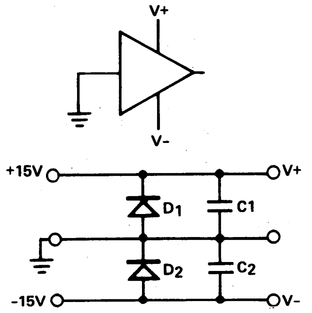
HA-2539; HA-2540; HA-2541; HA-2542; HA-5111; HA-5147; HA-5190/95; HA-OP27; HA-OP37


R2
R1
–
+
V+
V-
+15
V+
D_1
C_1
D_2
C_2
-15
V-

NOTES:
R_1 = 1K ± 5%
R_2 = 10K ± 5%
C_1, C_2 = 0.01 μF
D_1, D_2 = IN 4002

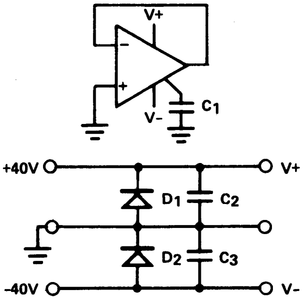
6

HA-2630/35; HA-5033


V+
V-
+15V
V+
D_1
C1
D_2
C2
-15V
V-

NOTES:
C_1, C_2 = 0.01 μF
D_1, D_2 = IN 4002

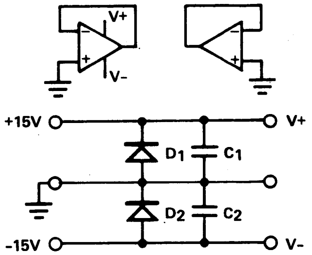
7 HA-2640/45



V+
V-
C1
+40V
V+
D1
C2
D2
C3
-40V
V-

NOTES:
$C_1 = 0.01\mu F$
$C2, C_3 = 0.01\mu F$
D_1, D_2 = IN 4002

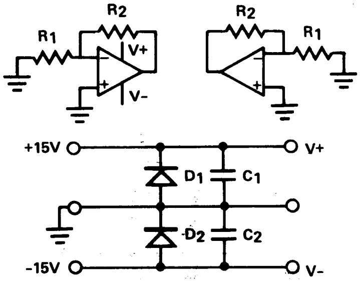
8 HA-2650/55; HA-5102; HA-5142; HA-5152 (MINI DIP)



V+
V-
+15V
V+
D1
C1
D2
C2
-15V
V-

NOTES:
$C_1, C_2 = 0.01\mu F$
D_1, D_2 = IN 4002

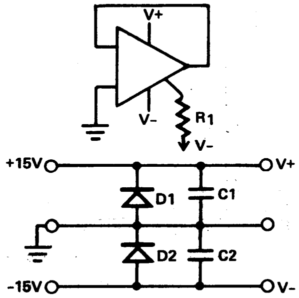
9 HA-2650/55; HA-5102; HA-5112; HA-5142; HA-5152 (METAL CAN)



R2
R1
V+
V-
R2
R1
+15V
V+
D1
C1
D2
C2
-15V
V-

NOTES:
$R_1 = 1K \pm 5\%$
$R_2 = 10K \pm 5\%$
$C_1, C_2 = 0.01\mu F$
D_1, D_2 = IN 4002

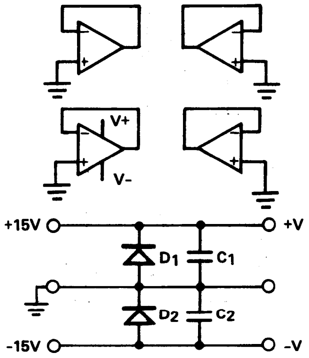
10 HA-2720/25



V+
V-
R1
V-
+15V
V+
D1
C1
D2
C2
-15V
V-

NOTES:
$C_1, C_2 = 0.01\mu F$
D_1, D_2 = IN 4002

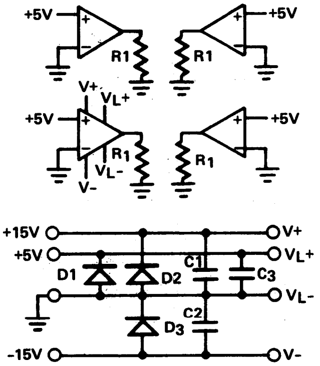
11 HA-4600/02/05; HA-4741; HA-5104; HA-5134; HA-5144; HA-5154



V+
V-
+15V
+V
D1
C1
D2
C2
-15V
-V

NOTES:
$C_1, C_2 = 0.01\mu F$
D_1, D_2 = IN 4002

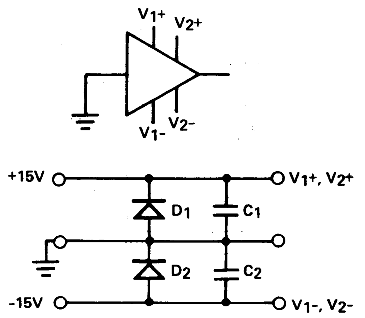
12 HA-4900/02/05



+5V
R1
R1
+5V
V+
VL+
+5V
R1
VL-
V-
R1
+5V
+15V
V+
+5V
VL+
D1
D2
C1
C3
VL-
C2
D3
-15V
V-

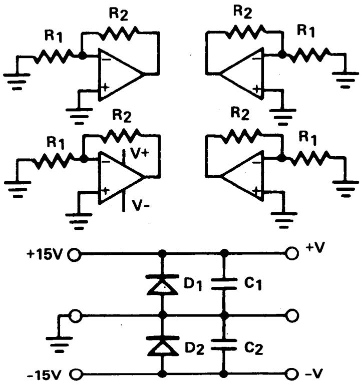
NOTES:
$R_1 = 5K \pm 5\%$
$C_1, C_2, C_3 = 0.01\mu F$
D_1, D_2, D_3 = IN 4004

13 HA-5002


V1+
V2+
V1-
V2-
+15V
V1+, V2+
D1
C1
D2
C2
-15V
V1-, V2-

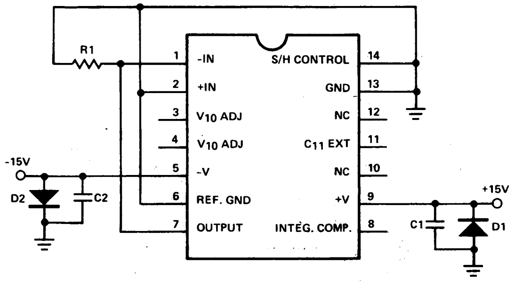
NOTES:
$C_1, C_2 = 0.01\mu F$
D_1, D_2 = IN 4002

14 HA-5114


R1
R2
V+
V-
+15V
+V
D1
C1
D2
C2
-15V
-V

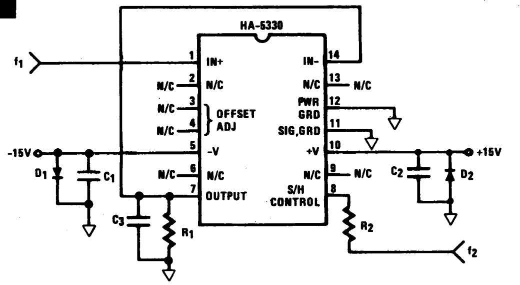
NOTES:
$R_1 = 1K \pm 5\%$ $C_1, C_2 = 0.01\mu F$
$R_2 = 10K \pm 5\%$ D_1, D_2 = IN 4002

15 HA-5320

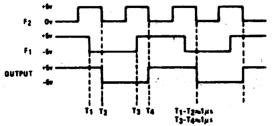

R1
1 -IN
2 +IN
3 V10 ADJ
4 V10 ADJ
5 -V
6 REF. GND
7 OUTPUT
14 S/H CONTROL
13 GND
12 NC
11 C11 EXT
10 NC
9 +V
8 INTEG. COMP.
-15V
D2
C2
+15V
C1
D1

NOTES:
R1 = 10KΩ
D1 =D2 = IN4002
C1 = C2 = 0.01 μF

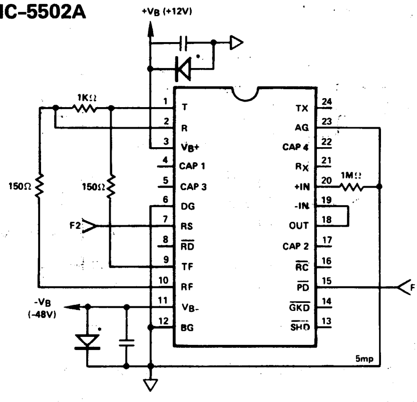
16 HA-5330


HA-5330
f1
1 IN+
2 N/C
3 OFFSET ADJ
4 OFFSET ADJ
5 -V
6 N/C
7 OUTPUT
14 IN-
13 N/C
12 PWR GRD
11 SIG.GRD
10 +V
9 N/C
8 S/H CONTROL
N/C
-15V
+15V
D1
C1
C2
D2
C3
R1
R2
f2

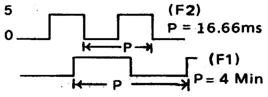
NOTES:
$R_1 = 510\Omega$,5%, ½ Watt
$C_1 = C_2 = .1\mu f$
C_3 = 47pf, 10%, 50V
$D_1 = D_2$ = IN 4002 or Equiv.
$R_2 = 0\Omega$ or Jumper wire
f_2 = 250KHz, TTL Levels, 50% Duty Cycle
f_1 = 125KHz, +5V to -5V levels, 50% Duty Cycle


F2
+5v
0v
F1
+5v
-5v
OUTPUT
+5v
-5v
T1
T2
T3
T4
T1-T2≈1μs
T3-T4≈1μs

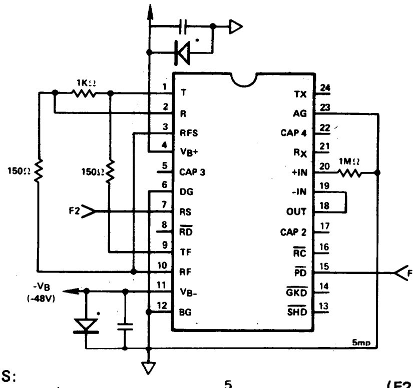
17 HC-5502A


+VB (+12V)
1KΩ
150Ω
150Ω
F2
-VB (-48V)
1 T
2 R
3 VB+
4 CAP 1
5 CAP 3
6 DG
7 RS
8 RD
9 TF
10 RF
11 VB-
12 BG
24 TX
23 AG
22 CAP 4
21 RX
20 +IN
19 -IN
18 OUT
17 CAP 2
16 RC
15 PD
14 GKD
13 SHD
1MΩ
F1
5mp

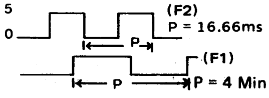
NOTES:
All Resistors ±10%
All Pin not specified leave open
F2 = 60 Hz, 0-5V Square Wave
F1 = 1/240 Hz 0-5V Square Wave


5
0
(F2)
P = 16.66ms
P
(F1)
P
P = 4 Min

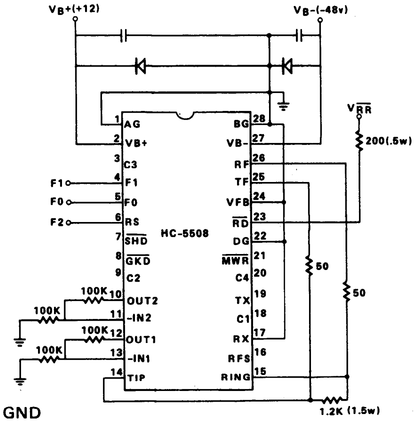
18 HC-5504


+VB (+12V)
1KΩ
150Ω
150Ω
F2
-VB (-48V)
1 T
2 R
3 RFS
4 VB+
5 CAP 3
6 DG
7 RS
8 RD
9 TF
10 RF
11 VB-
12 BG
24 TX
23 AG
22 CAP 4
21 RX
20 +IN
19 -IN
18 OUT
17 CAP 2
16 RC
15 PD
14 GKD
13 SHD
1MΩ
F1
5mp

NOTES:
All Resistors ±10%
All Pin not specified leave open
F2 = 60 Hz, 0-5V Square Wave
F1 = 1/240 Hz, 0-5V Square Wave


5
0
(F2)
P = 16.66ms
P
(F1)
P
P = 4 Min

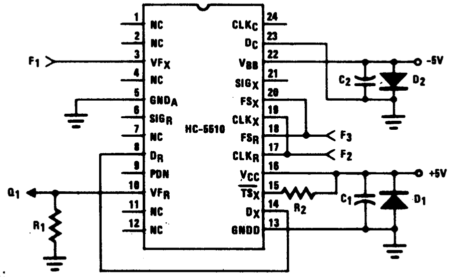
19 HC-5508



VB+(+12)
VB-(-48v)
VRR
200(.5w)
1 AG
2 VB+
3 C3
4 F1
5 F0
6 RS
7 SHD
8 GKD
9 C2
10 OUT2
11 -IN2
12 OUT1
13 -IN1
14 TIP
BG 28
VB- 27
RF 26
TF 25
VFB 24
RD 23
DG 22
MWR 21
C4 20
TX 19
C1 18
RX 17
RFS 16
RING 15
HC-5508
F1
F0
F2
100K
100K
100K
100K
50
50
1.2K (1.5w)

NOTES:
F0 = F1 = GND
F2 = +5V
V_{RR} = +5 or +12

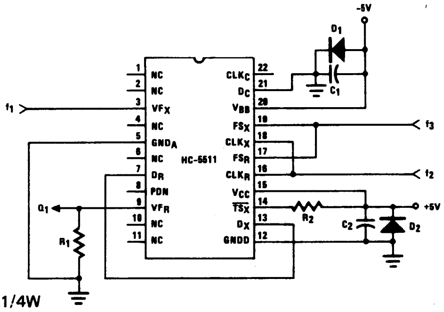
20 HC-5510



1 NC
2 NC
3 VFX
4 NC
5 GNDA
6 SIGR
7 NC
8 DR
9 PDN
10 VFR
11 NC
12 NC
CLKC 24
DC 23
VBB 22
SIGX 21
FSX 20
CLKX 19
FSR 18
CLKR 17
VCC 16
TSX 15
DX 14
GNDD 13
HC-5510
F1
F3
F2
Q1
R1
R2
C1
C2
D1
D2
-5V
+5V

PARTS:
R_1=10KΩ,1/4W
R_2=15KΩ,1/4W
C_1=C_2= .01μf (Per Socket)
D_1=D_2= IN4002 or Equiv. (Per Board)
F_1=1KHz; 5V p-pi Square Wave
F_2=2MHz; TTL Levels; 50% Duty Cycle
F_3=8KHz; TTL Levels; 1μs Wide at Logic Sync. to F_2.

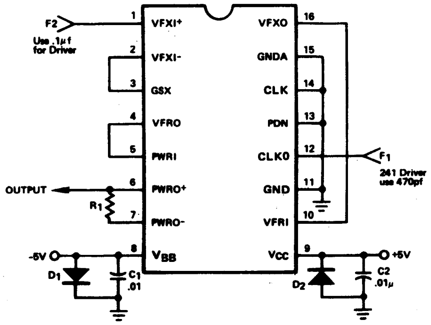
21 HC-5511



-5V
D1
C1
1 NC
2 NC
3 VFX
4 NC
5 GNDA
6 NC
7 DR
8 PDN
9 VFR
10 NC
11 NC
CLKC 22
DC 21
VBB 20
FSX 19
CLKX 18
FSR 17
CLKR 16
VCC 15
TSX 14
DX 13
GNDD 12
HC-5511
f1
f3
f2
Q1
R1
R2
C2
D2
+5V

PARTS:
R_1=10KΩ,1/4W
R_2=15KΩ,1/4W
C_1=C_2= .01μf (Per Socket)
D_1=D_2= IN4002 or Equiv. (Per Board)
F_1=1KHz; 5V p-pi Square Wave
F_2=2MHz; TTL Levels; 50% Duty Cycle
F_3=8KHz; TTL Levels; 1μs Wide at Logic Sync. to F_2.

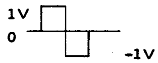
22 HC-5512; HC-5512A; HC-5512C; HC-5512D



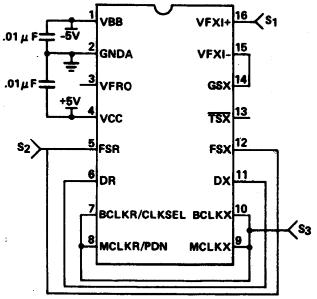
F2
Use .1μf for Driver
1 VFXI+
2 VFXI-
3 GSX
4 VFRO
5 PWRI
6 PWRO+
7 PWRO-
8 VBB
VFXO 16
GNDA 15
CLK 14
PDN 13
CLKO 12
GND 11
VFRI 10
VCC 9
F1
241 Driver use 470pf
OUTPUT
R1
-5V
D1
C1 .01
+5V
D2
C2 .01μ

NOTES:
F1 = TTL, 50% Duty Cycle
F1 = 100 KHz
F2 = 2.0V p-p @≅100 Hz,
C1, C2 = .01 μf

D1, D2 = IN4002
R1 = 600Ω



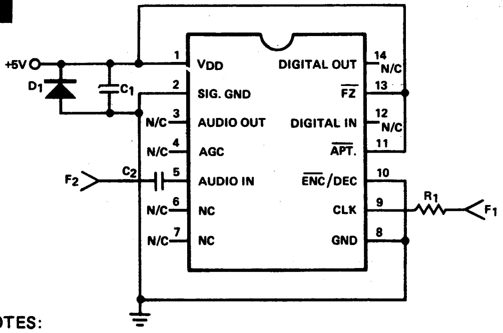
23 HC-5554; HC-5557



.01μF
-5V
.01μF
+5V
1 VBB
2 GNDA
3 VFRO
4 VCC
5 FSR
6 DR
7 BCLKR/CLKSEL
8 MCLKR/PDN
VFXI+ 16
VFXI- 15
GSX 14
TSX 13
FSX 12
DX 11
BCLKX 10
MCLKX 9
S1
S2
S3

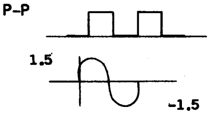
NOTES:
S1 = 1KHz, 5.0Vp-p Sine Wave
S2 = 8KHz, 1μs Wide, +5V to Gnd.
S3 = 1.5MHz Clock, +5V to Gnd

24 HC-55564

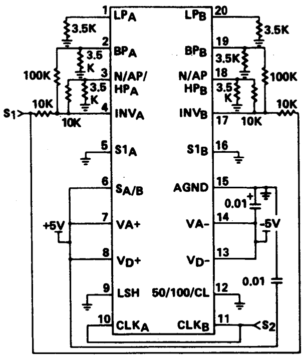


+5V
D1
C1
1 VDD
2 SIG. GND
N/C 3 AUDIO OUT
N/C 4 AGC
5 AUDIO IN
N/C 6 NC
N/C 7 NC
DIGITAL OUT 14 N/C
FZ 13
DIGITAL IN 12 N/C
APT. 11
ENC/DEC 10
CLK 9
GND 8
F2
C2
R1
F1

NOTES:
F1 - 16kHz , TTL Levels, 50% Duty Cycle, Square Wave
F2≃200 Hz (approximate), 3V, P-P
Sine wave (or triangular wave)
C1 = .01 μf
C2 = .1 μf
D1 = IN4002
R1 = 10KΩ ±10%, ¼Watt

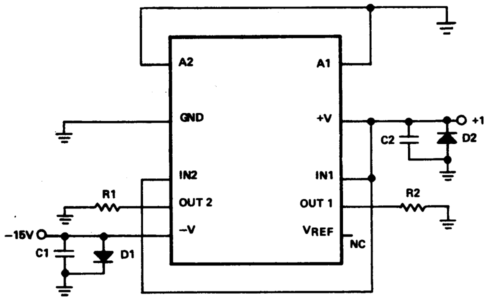


25 HF-10


1 LP_A
LP_B 20
3.5K
3.5K
2 BP_A
BP_B 19
3.5 K
3.5K
100K
3 N/AP/ HP_A
N/AP HP_B 18
3.5 K
3.5 K
100K
10K
10K
S1
4 INV_A
INV_B 17
10K
10K
5 S1_A
S1_B 16
6 S_A/B
AGND 15
0.01
+5V
7 VA+
VA- 14
-5V
8 V_D+
V_D- 13
0.01
9 LSH
50/100/CL 12
10 CLK_A
CLK_B 11
S2

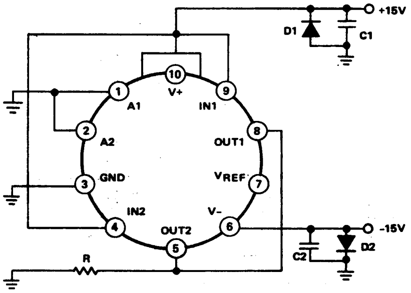
NOTES:
S1 = 1KHz, 5.0Vp-p Sine Wave
S2 = 100KHz, Clock, +5V to Gnd
All Caps are in μF

26 HI-200


A2
A1
GND
+V
+15V
C2
D2
IN2
IN1
R1
OUT 2
OUT 1
R2
-15V
-V
VREF
NC
C1
D1

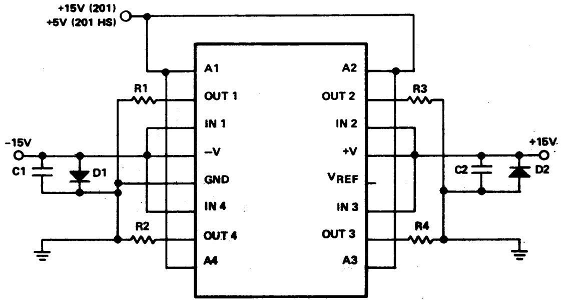
NOTES:
R1, R2 = 1kΩ
C1, C2 = .01 μF
D1, D2 = IN4002

27 HI-200 (CAN)


+15V
D1
C1
10
V+
1
A1
9
IN1
2
A2
8
OUT1
3
GND
7
VREF
IN2
V-
4
OUT2
6
-15V
5
C2
D2
R

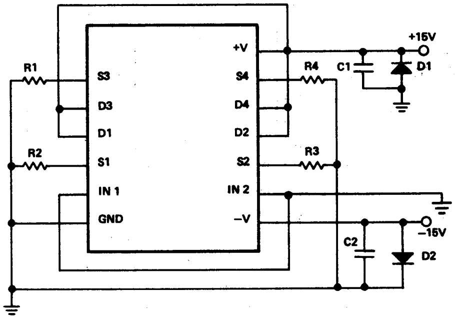
NOTES:
C1 = C2 = 0.01 μF
R = 10KΩ ±5%,
D1 = D2 = IN4002

28 HI-201; HI-201HS


+15V (201)
+5V (201 HS)
A1
A2
R1
OUT 1
OUT 2
R3
IN 1
IN 2
-15V
-V
+V
+15V
C1
D1
C2
D2
GND
VREF
IN 4
IN 3
R2
OUT 4
OUT 3
R4
A4
A3

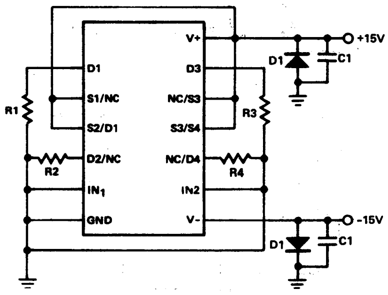
NOTES:
R1, R2, R3, R4 = 10kΩ, 5%,
C1, C2 = .01μF
D1, D2 = IN4002

29 HI-300; HI-301; HI-302


+15V
+V
R1
S3
S4
R4
C1
D1
D3
D4
D1
D2
R2
S1
S2
R3
IN 1
IN 2
GND
-V
-15V
C2
D2

NOTES:
R1, R2, R3, R4 = 10kΩ, 5%,
C1, C2 = .01μF
D1, D2 = IN4002

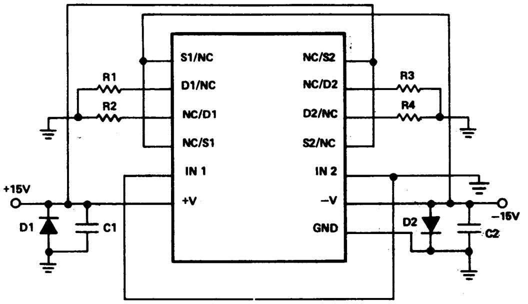
30 HI-303; HI-304; HI-305; HI-306; HI-307


V+
+15V
D1
D3
D1
C1
R1
S1/NC
NC/S3
R3
S2/D1
S3/S4
D2/NC
NC/D4
R2
R4
IN1
IN2
GND
V-
-15V
D1
C1

NOTES:
R1 to R4 = 10KΩ
C1 = 0.01 μF
D1 = IN4002

31

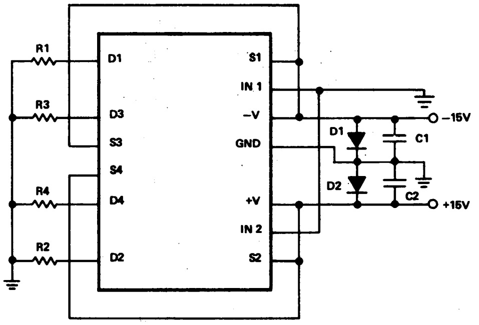
HI-381; HI-387


S1/NC
D1/NC
NC/D1
NC/S1
IN 1
+V
NC/S2
NC/D2
D2/NC
S2/NC
IN 2
−V
GND
R1
R2
R3
R4
+15V
D1
C1
D2
C2
−15V

NOTES:
R1 – R4 = 10kΩ, ±5%,
C1 – C2 = .01μF
D1 – D2 = IN4002

32

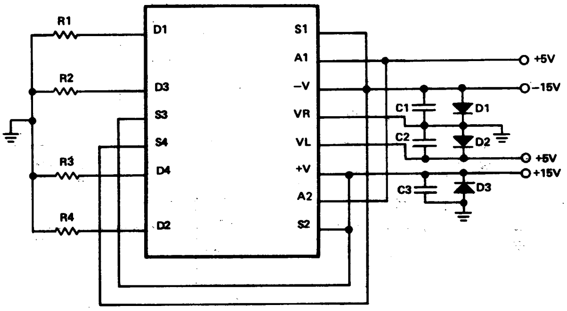
HI-384; HI-390


D1
D3
S3
S4
D4
D2
S1
IN 1
−V
GND
+V
IN 2
S2
R1
R3
R4
R2
D1
C1
D2
C2
−15V
+15V

NOTES:
R1 – R4 = 10kΩ, ±5%,
C1 – C2 = .01μF
D1 – D2 = IN4002

33

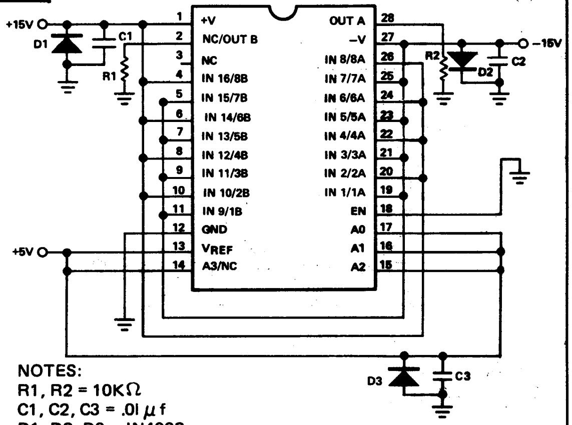
HI-5040 Through HI-5051


D1
D3
S3
S4
D4
D2
S1
A1
−V
VR
VL
+V
A2
S2
R1
R2
R3
R4
+5V
−15V
C1
D1
C2
D2
+5V
+15V
C3
D3

NOTES:
R1 – R4 = 10kΩ, 5%,
C1, C2, C3 = .01μF
D1, D2, D3 = IN4002

34

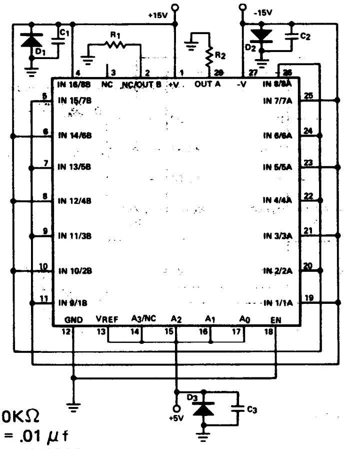
HI-506/507; HI-506A/507A; HI-546/547


+15V
D1
C1
R1
+5V
1 +V
2 NC/OUT B
3 NC
4 IN 16/8B
5 IN 15/7B
6 IN 14/6B
7 IN 13/5B
8 IN 12/4B
9 IN 11/3B
10 IN 10/2B
11 IN 9/1B
12 GND
13 VREF
14 A3/NC
28 OUT A
27 −V
26 IN 8/8A
25 IN 7/7A
24 IN 6/6A
23 IN 5/5A
22 IN 4/4A
21 IN 3/3A
20 IN 2/2A
19 IN 1/1A
18 EN
17 A0
16 A1
15 A2
R2
D2
C2
−15V
D3
C3

NOTES:
R1, R2 = 10KΩ
C1, C2, C3 = .01 μf
D1, D2, D3 = IN4002

35

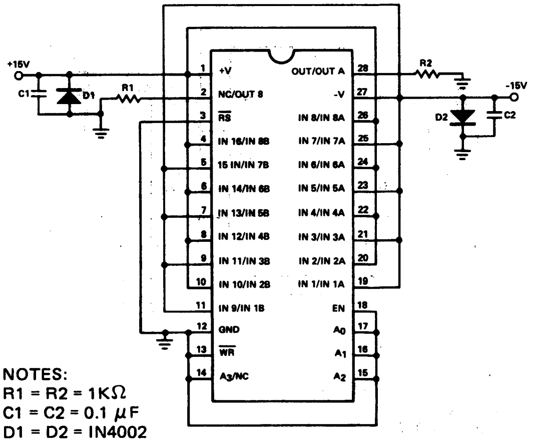
HI-506/507(LCC); HI-506A/507A (LCC)


+15V
−15V
D1
C1
R1
R2
D2
C2
4 IN 16/8B
3 NC
2 NC/OUT B
1 +V
28 OUT A
27 −V
26 IN 8/8A
5 IN 15/7B
6 IN 14/6B
7 IN 13/5B
8 IN 12/4B
9 IN 11/3B
10 IN 10/2B
11 IN 9/1B
25 IN 7/7A
24 IN 6/6A
23 IN 5/5A
22 IN 4/4A
21 IN 3/3A
20 IN 2/2A
19 IN 1/1A
12 GND
13 VREF
14 A3/NC
15 A2
16 A1
17 A0
18 EN
D3
C3
+5V

NOTES:
R1, R2 = 10KΩ
C1, C2, C3 = .01 μf
D1, D2, D3 = IN4002

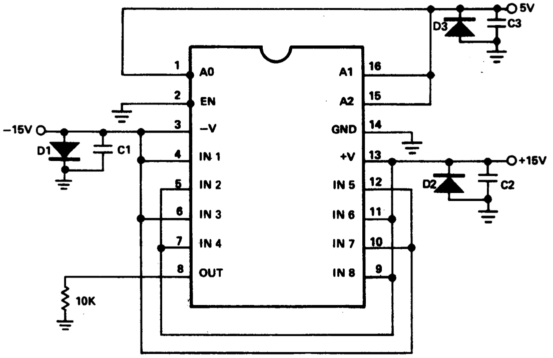
36

HI-506LA/507LA


+15V
C1
D1
R1
1 +V
2 NC/OUT 8
3 RS
4 IN 16/IN 8B
5 15 IN/IN 7B
6 IN 14/IN 6B
7 IN 13/IN 5B
8 IN 12/IN 4B
9 IN 11/IN 3B
10 IN 10/IN 2B
11 IN 9/IN 1B
12 GND
13 WR
14 A3/NC
28 OUT/OUT A
27 -V
26 IN 8/IN 8A
25 IN 7/IN 7A
24 IN 6/IN 6A
23 IN 5/IN 5A
22 IN 4/IN 4A
21 IN 3/IN 3A
20 IN 2/IN 2A
19 IN 1/IN 1A
18 EN
17 A0
16 A1
15 A2
R2
-15V
D2
C2

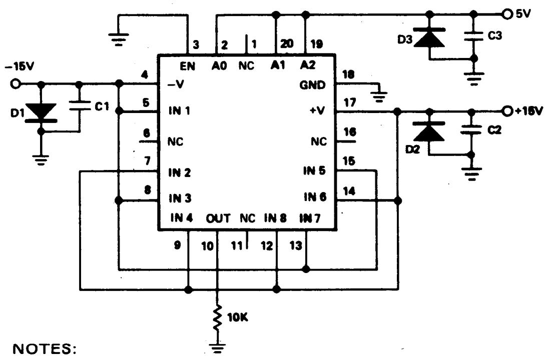
NOTES:
R1 = R2 = 1KΩ
C1 = C2 = 0.1 μF
D1 = D2 = IN4002

37 HI-508/508A; HI-548


5V
D3
C3
-15V
D1
C1
+15V
D2
C2
10K
1 A0
2 EN
3 -V
4 IN 1
5 IN 2
6 IN 3
7 IN 4
8 OUT
16 A1
15 A2
14 GND
13 +V
12 IN 5
11 IN 6
10 IN 7
9 IN 8

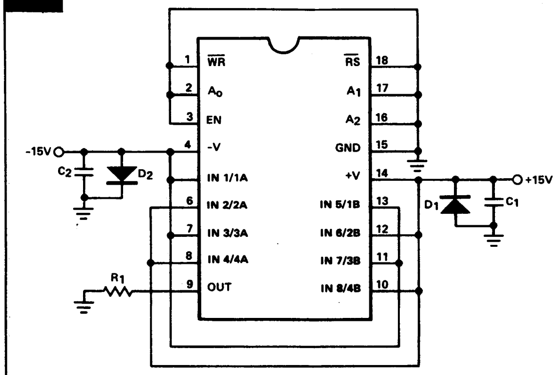
NOTES:
R1 = 10kΩ
C1, C2, C3 = .01 μf
D1, D2, D3 = IN4002

38 HI-508/508A (LCC)


5V
D3
C3
-15V
D1
C1
+15V
D2
C2
10K
3 EN
2 A0
1 NC
20 A1
19 A2
4 -V
5 IN 1
6 NC
7 IN 2
8 IN 3
18 GND
17 +V
16 NC
15 IN 5
14 IN 6
9 IN 4
10 OUT
11 NC
12 IN 8
13 IN 7

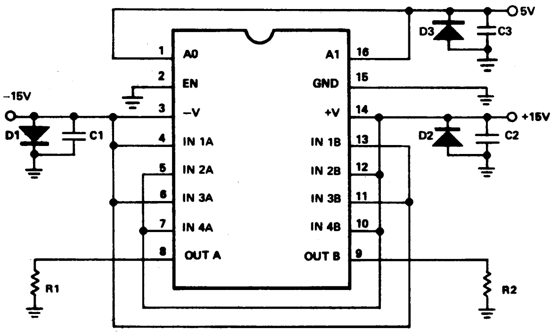
NOTES:
R1 = 10kΩ
C1, C2, C3 = .01 μf
D1, D2, D3 = IN4002

39 HI-508LA/509LA


-15V
C2
D2
+15V
D1
C1
R1
1 WR
2 A0
3 EN
4 -V
5 IN 1/1A
6 IN 2/2A
7 IN 3/3A
8 IN 4/4A
9 OUT
18 RS
17 A1
16 A2
15 GND
14 +V
13 IN 5/1B
12 IN 6/2B
11 IN 7/3B
10 IN 8/4B

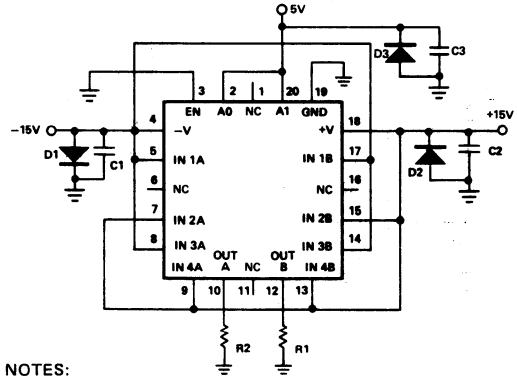
NOTES:
R1 = 1KΩ
C1 = C2 = 0.1 μF
D1 = D2 = IN4002

40 HI-509/509A; HI-539; HI-549


5V
D3
C3
-15V
D1
C1
+15V
D2
C2
R1
R2
1 A0
2 EN
3 -V
4 IN 1A
5 IN 2A
6 IN 3A
7 IN 4A
8 OUT A
16 A1
15 GND
14 +V
13 IN 1B
12 IN 2B
11 IN 3B
10 IN 4B
9 OUT B

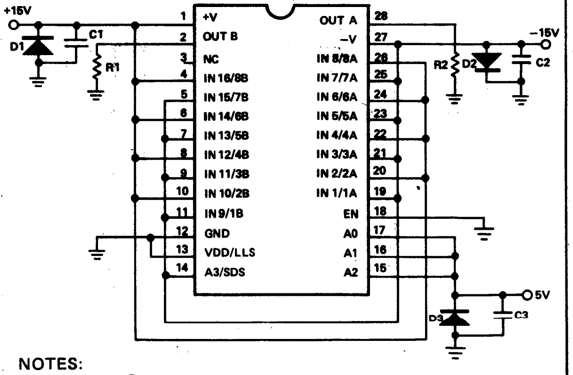
NOTES:
R1, R2 = 10kΩ
C1, C2, C3 = .0l μf
D1, D2, D3 = IN4002

41 HI-509/509A (LCC); HI-549 (LCC)


5V
D3
C3
-15V
D1
C1
+15V
D2
C2
R2
R1
3 EN
2 A0
1 NC
20 A1
19 GND
4 -V
5 IN 1A
6 NC
7 IN 2A
8 IN 3A
18 +V
17 IN 1B
16 NC
15 IN 2B
14 IN 3B
9 IN 4A
10 OUT A
11 NC
12 OUT B
13 IN 4B

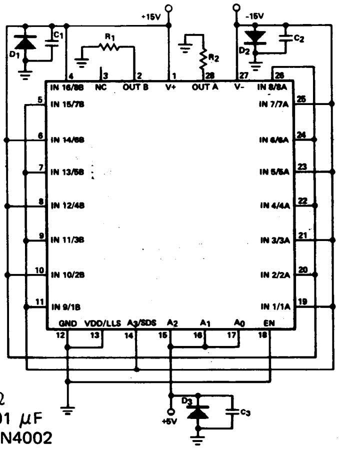
NOTES:
R1, R2 = 10kΩ
C1, C2, C3 = .01 μf
D1, D2, D3 = IN4002

42 HI-516


+15V
D1
C1
R1
-15V
R2
D2
C2
5V
D3
C3
1 +V
2 OUT B
3 NC
4 IN 16/8B
5 IN 15/7B
6 IN 14/6B
7 IN 13/5B
8 IN 12/4B
9 IN 11/3B
10 IN 10/2B
11 IN9/1B
12 GND
13 VDD/LLS
14 A3/SDS
28 OUT A
27 -V
26 IN 8/8A
25 IN 7/7A
24 IN 6/6A
23 IN 5/5A
22 IN 4/4A
21 IN 3/3A
20 IN 2/2A
19 IN 1/1A
18 EN
17 A0
16 A1
15 A2

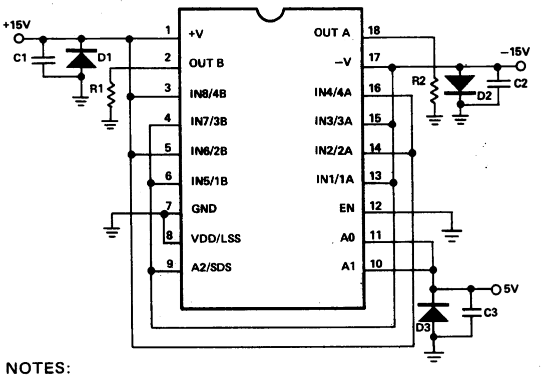
NOTES:
R1, R2 = 10kΩ
D1, D2, D3 = IN4002
C1, C2, C3 = .01 μF

43 HI-516 (LCC)


+15V
-15V
D1
C1
R1
R2
D2
C2
4 IN 16/8B
3 NC
2 OUT B
1 V+
28 OUT A
27 V-
26 IN 8/8A
5 IN 15/7B
6 IN 14/6B
7 IN 13/5B
8 IN 12/4B
9 IN 11/3B
10 IN 10/2B
11 IN 9/1B
25 IN 7/7A
24 IN 6/6A
23 IN 5/5A
22 IN 4/4A
21 IN 3/3A
20 IN 2/2A
19 IN 1/1A
12 GND
13 VDD/LLS
14 A3/SDS
15 A2
16 A1
17 A0
18 EN
D3
C3
+5V

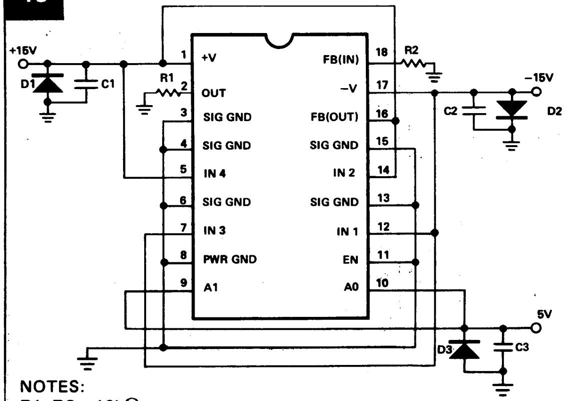
NOTES:
R1, R2 = 10kΩ
C1, C2, C3 = .01 μF
D1, D2, D3 = IN4002

44 HI-518


+15V
C1
D1
R1
1 +V
2 OUT B
3 IN8/4B
4 IN7/3B
5 IN6/2B
6 IN5/1B
7 GND
8 VDD/LSS
9 A2/SDS
18 OUT A
17 –V
16 IN4/4A
15 IN3/3A
14 IN2/2A
13 IN1/1A
12 EN
11 A0
10 A1
–15V
R2
D2
C2
5V
C3
D3

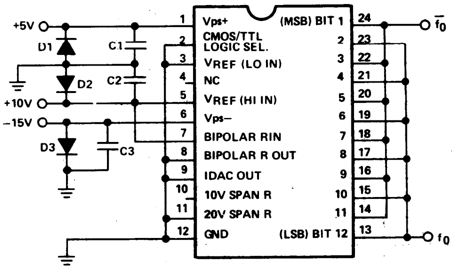
NOTES:
R1, R2 = 10kΩ
C1, C2, C3 = .01 μF
D1, D2, D3 = IN4002

45 HI-524


+15V
D1
C1
R1
1 +V
2 OUT
3 SIG GND
4 SIG GND
5 IN 4
6 SIG GND
7 IN 3
8 PWR GND
9 A1
18 FB(IN)
17 –V
16 FB(OUT)
15 SIG GND
14 IN 2
13 SIG GND
12 IN 1
11 EN
10 A0
R2
–15V
C2
D2
5V
D3
C3

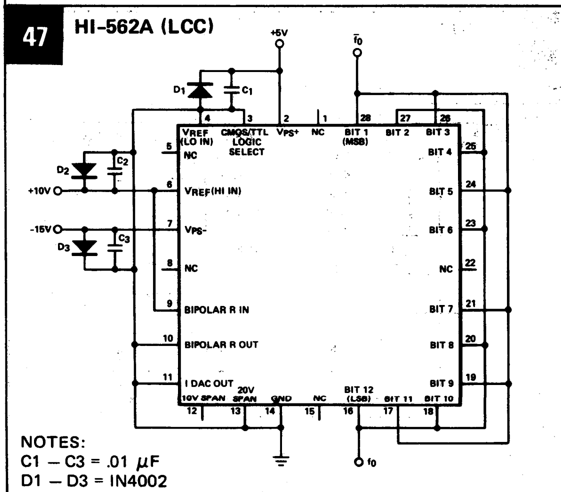
NOTES:
R1, R2 = 10kΩ
C1, C2, C3 = .01 μF
D1, D2, D3 = IN4002

46 HI-562A


+5V
D1
C1
D2
C2
+10V
–15V
D3
C3
1 Vps+
2 CMOS/TTL LOGIC SEL.
3 VREF (LO IN)
4 NC
5 VREF (HI IN)
6 Vps–
7 BIPOLAR RIN
8 BIPOLAR R OUT
9 IDAC OUT
10 10V SPAN R
11 20V SPAN R
12 GND
(MSB) BIT 1
(LSB) BIT 12
24
23
22
21
20
19
18
17
16
15
14
13
f̄0
f0

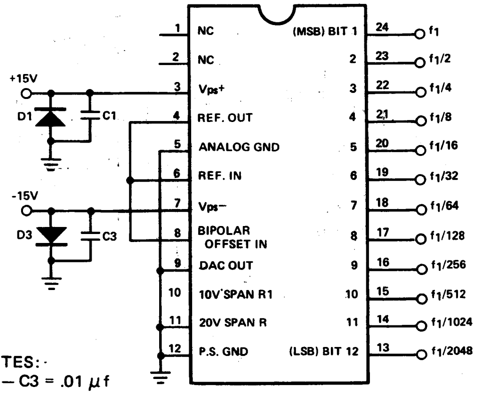
NOTES:
C1 – C3 = .01 μF
D1 – D3 = IN4002
f_0 = 100 KHz, 50% Duty Cycle

47 HI-562A (LCC)


+5V
f̄0
D1
C1
4 VREF (LO IN)
3 CMOS/TTL LOGIC SELECT
2 VPS+
1 NC
28 BIT 1 (MSB)
27 BIT 2
26 BIT 3
5 NC
6 VREF(HI IN)
7 VPS-
8 NC
9 BIPOLAR R IN
10 BIPOLAR R OUT
11 I DAC OUT
12 10V SPAN
13 20V SPAN
14 GND
15 NC
16 BIT 12 (LSB)
17 BIT 11
18 BIT 10
25 BIT 4
24 BIT 5
23 BIT 6
22 NC
21 BIT 7
20 BIT 8
19 BIT 9
D2
C2
+10V
-15V
D3
C3
f0

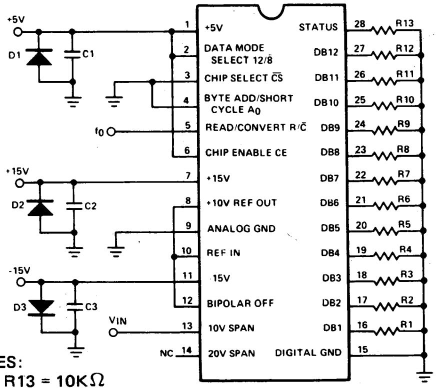
NOTES:
C1 – C3 = .01 μF
D1 – D3 = IN4002
f_0 = 100 KHz, 50% Duty Cycle

48 HI-565A


+15V
D1
C1
-15V
D3
C3
1 NC
2 NC
3 Vps+
4 REF. OUT
5 ANALOG GND
6 REF. IN
7 Vps–
8 BIPOLAR OFFSET IN
9 DAC OUT
10 10V SPAN R1
11 20V SPAN R
12 P.S. GND
(MSB) BIT 1
(LSB) BIT 12
24 f1
23 f1/2
22 f1/4
21 f1/8
20 f1/16
19 f1/32
18 f1/64
17 f1/128
16 f1/256
15 f1/512
14 f1/1024
13 f1/2048

NOTES:
C1 – C3 = .01 μf
D1 – D3 = IN4002
f_1 = 100 KHz

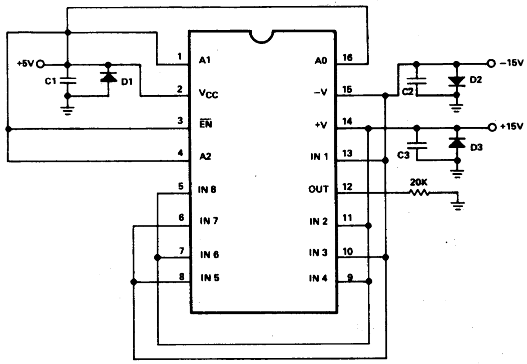
49 HI-574A/674A



+5V
D1
C1
+15V
D2
C2
-15V
D3
C3
f0
VIN
NC
1 +5V
2 DATA MODE SELECT 12/8
3 CHIP SELECT CS
4 BYTE ADD/SHORT CYCLE A0
5 READ/CONVERT R/C
6 CHIP ENABLE CE
7 +15V
8 +10V REF OUT
9 ANALOG GND
10 REF IN
11 15V
12 BIPOLAR OFF
13 10V SPAN
14 20V SPAN
28 STATUS R13
27 DB12 R12
26 DB11 R11
25 DB10 R10
24 DB9 R9
23 DB8 R8
22 DB7 R7
21 DB6 R6
20 DB5 R5
19 DB4 R4
18 DB3 R3
17 DB2 R2
16 DB1 R1
15 DIGITAL GND

NOTES:
R1 – R13 = 10KΩ
C1 – C3 = 0.1 μF
D1 – D3 = IN4002
V_{IN} = Triangle Wave Form, +5V to -5V. 1KHz
f_o = 10 KHZ, 90% Duty Cycle, 0V to 5V

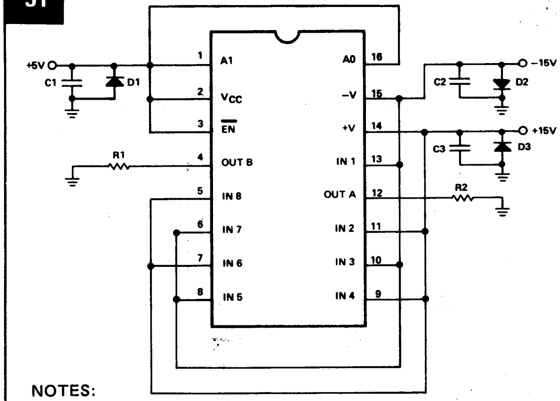
50 HI-1818A



+5V
C1
D1
1 A1
2 VCC
3 EN
4 A2
5 IN 8
6 IN 7
7 IN 6
8 IN 5
16 A0
15 –V
14 +V
13 IN 1
12 OUT
11 IN 2
10 IN 3
9 IN 4
C2
D2
–15V
C3
D3
+15V
20K

NOTES:
C1, C2, C3 = .01μF
D1, D2, D3 = IN4002

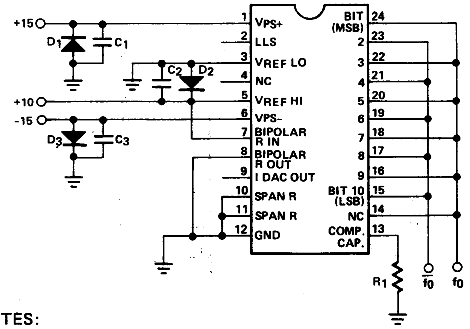
51 HI-1828A



+5V
C1
D1
R1
1 A1
2 VCC
3 EN
4 OUT B
5 IN 8
6 IN 7
7 IN 6
8 IN 5
16 A0
15 –V
14 +V
13 IN 1
12 OUT A
11 IN 2
10 IN 3
9 IN 4
C2
D2
–15V
C3
D3
+15V
R2

NOTES:
R1, R2 = 20kΩ
C1, C2, C3 = .01μF
D1, D2, D3 = IN4002

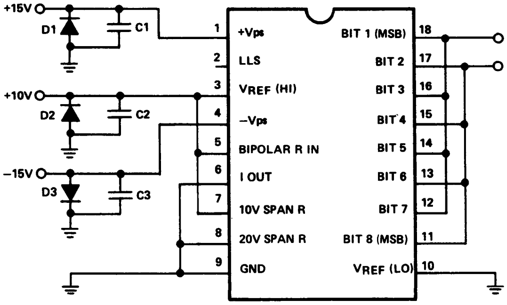
52 HI-5610



+15
D1
C1
C2
D2
+10
-15
D3
C3
1 VPS+
2 LLS
3 VREF LO
4 NC
5 VREF HI
6 VPS-
7 BIPOLAR R IN
8 BIPOLAR R OUT
9 I DAC OUT
10 SPAN R
11 SPAN R
12 GND
BIT (MSB) 24
2 23
3 22
4 21
5 20
6 19
7 18
8 17
9 16
BIT 10 (LSB) 15
NC 14
COMP. CAP. 13
R1
f0
f0

NOTES:
R1 = 50kΩ
D2, D3, D1 = IN4002
C2, C3, C1 = 0.01 μF
f_o = 1KHz, 50% Duty Cycle

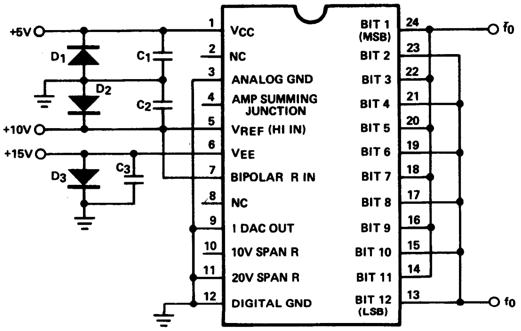
53 HI-5618A/5618B



+15V
D1
C1
+10V
D2
C2
–15V
D3
C3
1 +Vps
2 LLS
3 VREF (HI)
4 –Vps
5 BIPOLAR R IN
6 I OUT
7 10V SPAN R
8 20V SPAN R
9 GND
18 BIT 1 (MSB)
17 BIT 2
16 BIT 3
15 BIT 4
14 BIT 5
13 BIT 6
12 BIT 7
11 BIT 8 (MSB)
10 VREF (LO)
f1
f1

NOTES:
D1 – D3 = IN4002 or Similar
C1 – C3 = .1 μF
f1= 100 KHz, TTL Level, 50% Duty Cycle

54 HI-5660/5660A

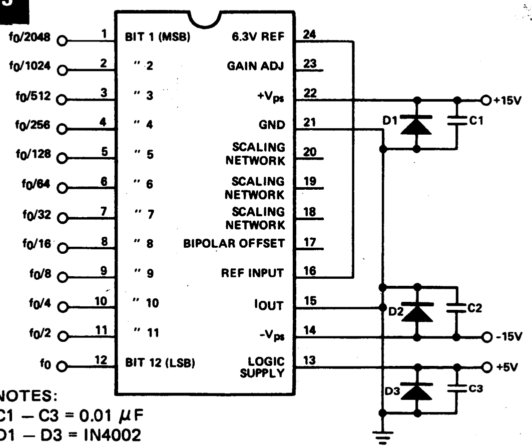


+5V
D1
C1
D2
C2
+10V
+15V
D3
C3
1 VCC
2 NC
3 ANALOG GND
4 AMP SUMMING JUNCTION
5 VREF (HI IN)
6 VEE
7 BIPOLAR R IN
8 NC
9 I DAC OUT
10 10V SPAN R
11 20V SPAN R
12 DIGITAL GND
24 BIT 1 (MSB)
23 BIT 2
22 BIT 3
21 BIT 4
20 BIT 5
19 BIT 6
18 BIT 7
17 BIT 8
16 BIT 9
15 BIT 10
14 BIT 11
13 BIT 12 (LSB)
f0
f0

NOTES:
C1 – C3 = .01μf
D1 – D3 = IN4002
f_o = 100 KHz, 50% Duty Cycle

55

HI-5687 (I)

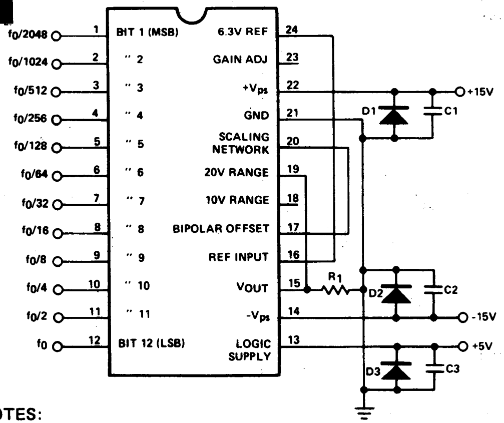


f0/2048 1 BIT 1 (MSB)
f0/1024 2 " 2
f0/512 3 " 3
f0/256 4 " 4
f0/128 5 " 5
f0/64 6 " 6
f0/32 7 " 7
f0/16 8 " 8
f0/8 9 " 9
f0/4 10 " 10
f0/2 11 " 11
f0 12 BIT 12 (LSB)
24 6.3V REF
23 GAIN ADJ
22 +Vps
21 GND
20 SCALING NETWORK
19 SCALING NETWORK
18 SCALING NETWORK
17 BIPOLAR OFFSET
16 REF INPUT
15 IOUT
14 -Vps
13 LOGIC SUPPLY
+15V
-15V
+5V
D1
D2
D3
C1
C2
C3

NOTES:
C1 – C3 = 0.01 μF
D1 – D3 = IN4002
f_O = 100KHz (TTL Logic Levels)

56

HI-5687 (V)

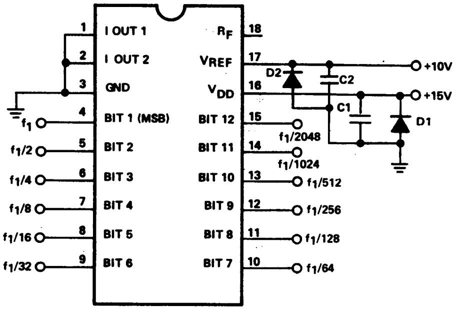


f0/2048 1 BIT 1 (MSB)
f0/1024 2 " 2
f0/512 3 " 3
f0/256 4 " 4
f0/128 5 " 5
f0/64 6 " 6
f0/32 7 " 7
f0/16 8 " 8
f0/8 9 " 9
f0/4 10 " 10
f0/2 11 " 11
f0 12 BIT 12 (LSB)
24 6.3V REF
23 GAIN ADJ
22 +Vps
21 GND
20 SCALING NETWORK
19 20V RANGE
18 10V RANGE
17 BIPOLAR OFFSET
16 REF INPUT
15 VOUT
14 -Vps
13 LOGIC SUPPLY
R1
+15V
-15V
+5V
D1
D2
D3
C1
C2
C3

NOTES:
C1 – C3 = 0.01 μF
D1 – D3 = IN4002
R1 = 2.0 KΩ
f_O = 100 KHz, (TTL Logic Level)

57

HI-7541

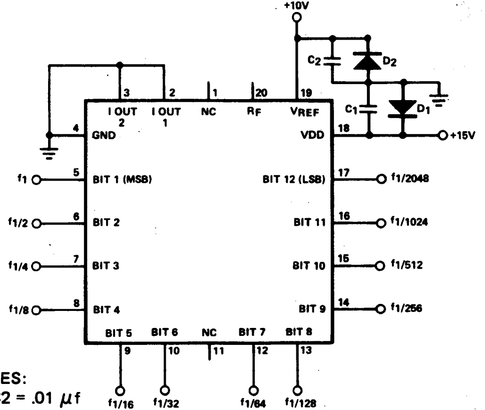


1 I OUT 1
2 I OUT 2
3 GND
f1 4 BIT 1 (MSB)
f1/2 5 BIT 2
f1/4 6 BIT 3
f1/8 7 BIT 4
f1/16 8 BIT 5
f1/32 9 BIT 6
18 RF
17 VREF
16 VDD
15 BIT 12 f1/2048
14 BIT 11 f1/1024
13 BIT 10 f1/512
12 BIT 9 f1/256
11 BIT 8 f1/128
10 BIT 7 f1/64
+10V
+15V
D1
D2
C1
C2

NOTES:
C1, C2 = .01 μf, D1, D2 = IN4002
f1 = 100kHz
Square Wave, TTL Level (0-5V)

58

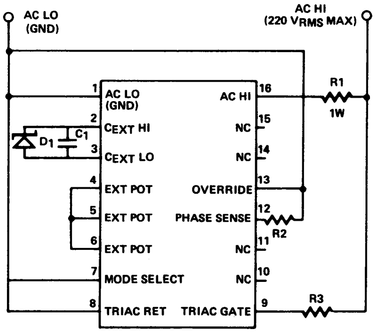
HI-7541 (LCC)



+10V
C2
D2
C1
D1
+15V
3 I OUT 2
2 I OUT 1
1 NC
20 RF
19 VREF
4 GND
18 VDD
f1 5 BIT 1 (MSB)
f1/2 6 BIT 2
f1/4 7 BIT 3
f1/8 8 BIT 4
17 BIT 12 (LSB) f1/2048
16 BIT 11 f1/1024
15 BIT 10 f1/512
14 BIT 9 f1/256
9 BIT 5 f1/16
10 BIT 6 f1/32
11 NC
12 BIT 7 f1/64
13 BIT 8 f1/128

NOTES:
C1, C2 = .01 μf
D1, D2 = IN4002
f1 = 100kHz
Square Wave, TTL Level (0-5V)

59 HV-1000



AC LO (GND)
AC HI (220 V_{RMS} MAX)
R1
1W
AC LO (GND)
AC HI
C_{EXT} HI
NC
C_{EXT} LO
NC
D_1
C_1
EXT POT
OVERRIDE
EXT POT
PHASE SENSE
R2
EXT POT
NC
MODE SELECT
NC
TRIAC RET
TRIAC GATE
R3

NOTES:

R1 = 5KΩ, 1W, 5%

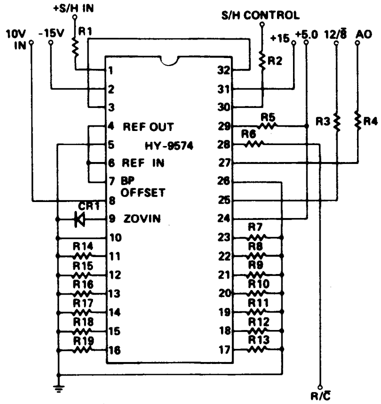
R2 = 100KΩ, ½W, 5%

R3 = 500KΩ, ½W, 5%

C1 = 0.47μF

D1 = 12V Zener, ¼W

60 HY-9574



+S/H IN
S/H CONTROL
10V IN
-15V
R1
R2
+15
+5.0
12/$\overline{8}$
AO
REF OUT
HY-9574
REF IN
BP OFFSET
ZOVIN
CR1
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R/$\overline{C}$

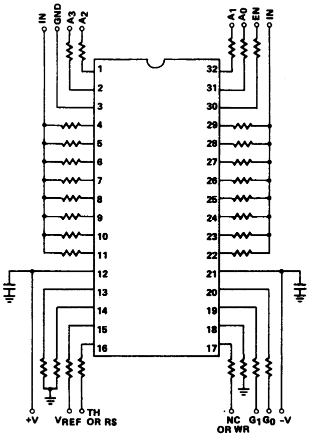
NOTES:

R1 through R6 = 10KΩ ± 10% ¼ Watt

R7 through R19 = 5KΩ ± 10% ¼ Watt

CR1 = IN 4001 or Equivalent

61 HY-9590; HY-9591; HY-9595; HY-9596



IN
GND
A3
A2
A1
A0
EN
IN
+V
V_{REF}
TH OR RS
NC OR WR
G_1
G_0
-V

NOTES:

R = 4.7K ± 10%

C = 0.1μF, 50V

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ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

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514	The HA-2400 PRAM Four Channel Operational Amplifier	HA-2400 Programmable Analog Microcircuit description, frequency compensation, applications (analog multiplexer, non-inverting programmable gain amplifier, inverting programmable gain amplifier, programmable attenuator, programmable adder-subtractor, phase selector, phase detector, synchronous rectifier, balanced modulator, integrator, ramp generator, track and hold, sample and hold, sine wave oscillator, multivibrator, active filter, programmable power supply, comparator, multiplying D/A converter).	10-14
515	Operational Amplifier Stability: Input Capacitance Considerations	Input capacitance and stability, capacitive feedback compensation, guidelines for compensation requirements.	10-21
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520	CMOS Analog Multiplexers And Switches; Application Considerations	Switch selection criteria, datasheet definitions, care and feeding of multiplexers and switches, digital interface, practical multiplexer applications alternative to CMOS switches and multiplexers.	10-37
521	Getting The Most Out Of CMOS Devices For Analog Switching Jobs	CMOS versus bipolar device performances, over voltage and channel interaction conditions, JI technology and latch-up, floating-body JI technology, fool-proof CMOS analog multiplexer, other DI benefits.	10-46
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524	Digital To Analog Converter High Speed ADC Applications	To use of High Speed DAC's in tracking, servo, and successive approximation Analog to Digital Converters. Design ideas for Data Acquisition Systems.	10-56
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529	Microprocessor Interface Methods For High-Speed Data Acquisition Systems	Applications for the HI-574A family and HY-9590/9591. Data Acquistion Systems, Microprocessor interfacing and a software flowchart.	10-68
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534	Additional Information On The HI-300 Series Switch	"ON" resistance, leakage currents, switching speeds, power supply requirements, internal switch operation and schematics, single supply operation, charge injection, power supplies conditions and protective circuitry.	10-82
535	Design Considerations For A Data Acquisition System (DAS)	A collection of guidelines for the design of a Data Acquisition System. Includes Signal Conditioning, Transducers, Single-Ended vs. Differential Signal Paths, Low Level Signals, Filters, Programmable Gain Amplifiers, Sampling Rate, and computer interfacing.	10-87
538	Monolithic Sample/Hold Combines Speed And Precision	Description and electrical specifications for the HA-5320 Sample/Hold Amplifiers, explanation of errors sources, and HA-5320 applications.	10-93
539	A Monolithic 16 Bit D/A Converter	Detailed description of the HI-DAC16 D-A Converter, chip photo and schematic, plus applications and interface considerations.	10-100
540	HA-5170 Precision Low Noise J-FET Input Operational Amplifier	Internal design and technology, J-FET noise discussion, trimming of offset voltage, single Op Amp instrumentation amplifier, sine wave oscillator, high impedance transducers interface, current source/sink and current sense circuits.	10-105
541	Using HA-2539 Very High Slew-Rate Wideband Operational Amplifier	Prototyping considerations, output short circuit protection, offset voltage adjustment,frequency compensation, composite amplifier scheme DC error reduction, boosting output current, increasing output signal swing, cascade amplifier, video gain block, high frequency oscillator, wideband signal splitter.	10-109
542	Using The HV-1000 Induction Motor Energy Saver	What is an IMES? IMES application; HV-1000 algorithm; load anticipation; basic circuit application of HV-1000; measuring power savings; handling precautions and reliability.	10-113
543	New High Speed Switch Offers Sub-50ns Switching Times	Application enhancement using the HI-201HS, high speed multiplexers, high speed sample and hold, analog switch and Op Amp circuitry, integrator with start/reset, low pass filter with select break frequency, amplifier with programmable gain, future applications.	10-122
544	Micropower Op Amp Family	Operation, noise performance, applications (remote sensor loop transmitter, charge pool power supply, low power microphone preamplifier, AGC with squelch control, Wein bridge oscillator, bar code scanner, monostable multivibrator).	10-129
545	New Multiplexers Simplify System Design	Description and applications for the Harris HI-50XL family of latched overvoltage protected multiplexers.	10-135
548	A Designer's Guide For The HA-5033 Video Buffer	Operation, video performance, video parameter specifications, Y parameters, applications (flash converter pre-driver, coaxial line driver, video gain block, high speed sample and hold, audio drivers, crystal oscillator).	10-142

Application Note Abstracts (Continued)

AN#	TITLE	ABSTRACTS	PAGE
549	The HC-550X Telephone Subscriber Line Interface Circuit	Complete description of device functionality and applications of SLIC.	10-154
550	Using the HA-2541	Protyping guidelines, thermal considerations and heat sinking, performance enhancements, applications (Wein bridge oscillator, high power gain stage, video stage with clamp, multiplexer/demultiplexer, disk drive write amplifier, gain programmable amp, composite amp).	10-173
552	Using the HA-2542	Prototyping guidelines, thermal considerations and heat sinking, performance enhancements, applications (multi-channel security system, unbalanced coaxial driver, flash converter driver, programmable power supply, bridge load driver, high current stage, differential line driver, DC motor speed control).	10-179
553	Using the HA-5147	Construction and operation, low noise design applications (Instrumentation amplifier bridge sensor, multiplexer, precision threshold detector, audio driver, NAB amplifier, multivibrator, programmable gain stage, log amp, professional mixer).	10-184
554	Low Noise Family HA-5102/04/12/14	Low noise design, operation, applications (Electronic scales, programmable attentuator, Baxandal Circuit, RIAH amplifier, NAB preamplifier, microphone amplifier, standard and simple Biquads, professional mixer.	10-192
555	Ultra Low Bias Amplifier, HA-5180	Construction, layout hints, low noise design, applications (Sample and Hold, precision sample and hold, pH probe, light sensor, photo diode sensor, precision integrator, time, atomic partical counter circuit).	10-199
560	Applying the HY-9590 Analog Data Acquisition Signal Processor	Describes use of the HY-9594 Signal Processor. Includes a description of the input Multiplexer, Programmable Gain Instrumentation Amplifier, and the Track and Hold Amplifier, plus a Data Acquisition System application.	10-206
570	Understanding CODEC Timing	Describes in detail CODEC timing sequences and modes of operation.	10-210
571	Using Ring Sync with HC-5502A and HC-5504 SLICs	Describes use of the SLICs Ring Synchronization pin and why you should use it.	10-213
573	The HC-5560 Digital Line Transcoder	Full functional and applications description of HC-5560 transcoder and line codes.	10-215
574	Understanding PCM Coding	The process of converting analog voice signals into Time Division Multiplexed (TDM) Pulse Code Modulated (PCM) format is described and illustrated.	10-221
576	HC-5512C PCM Filter Cleans Up CVSD CODEC Signals	Description of application of PCM Filter as an I/O filter for the CVSD.	10-224
607	Delta Modulation For Voice Transmission	Introduction to delta modulation coding technique, 4 general applications, including digital transmission encryption, voice scrambling, and audio delay. Also CVSD evaluation guidelines.	10-226

APP NOTE
FOR YOUR INFORMATION

No. 508

Harris Analog

TEST PROCEDURES FOR OPERATIONAL AMPLIFIERS

By G. G. Miler

The offset voltage of the amplifier under test (A.U.T.) is measured as follows:

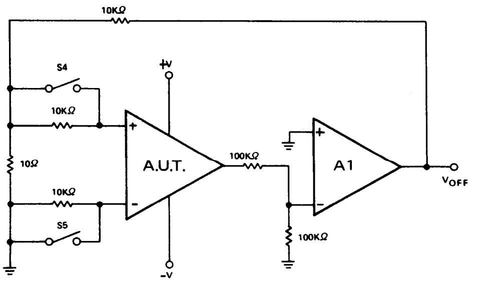
1. Set + and -V to the desired supply voltage and close S4 and S5.
2. Measure the voltage at V_{OFF}.

The offset voltage is equal to (V_{OFF}) (10^{-3}). The feedback amplifier, A1, drives the input of the A.U.T. so that the output is at ground reference, V_{OFF} is driven to 1000 times the voltage necessary to compensate for the offset voltage.

The bias current is measured as follows:

1. Measure the offset voltage, V_{OFF1}, as above.
2. Open S4 and measure V_{OFF2}.
3. The plus input current is equal to (V_{OFF2} — V_{OFF1}) x 10^{-7}.
4. Close S4 and open S5 and measure V_{OFF4}.
5. The minus input current is equal to (V_{OFF4} – V_{OFF1}) x 10^{-7}.

TEST CIRCUIT FOR MEASUREMENT OF OFFSET VOLTAGE, BIAS CURRENT, AND OFFSET CURRENT 10KΩ

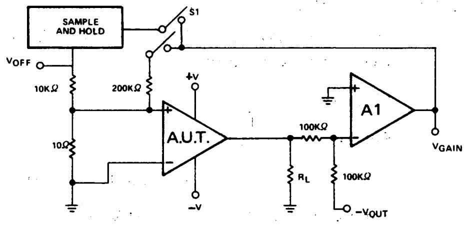


The bias current is equal to the average of the plus and minus input currents.

The input offset current is measured as follows:

1. Measure the offset voltage, V_{OFF1}, as above.
2. Open S4 and S5 and measure V_{OFF2}.
3. The offset current is equal to (V_{OFF2} — V_{OFF1}) x 10^{-7}.

TEST CIRCUIT FOR MEASURING OPEN LOOP VOLTAGE GAIN



The open loop voltage gain is measured as follows:

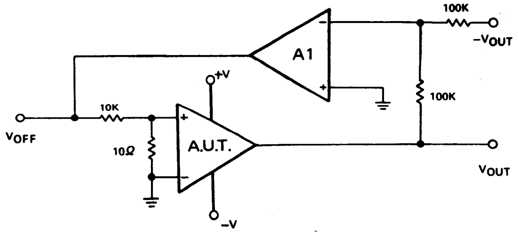
1. Set the +V and -V supply voltages to the desired value and set $-V_{OUT}$ to ground.
2. Close S1 so that the sample and hold will null the offset voltage.
3. S1 can be opened when the circuit stabilizes. The sample and hold will maintain the voltage which nulls the offset voltage.
4. Set $-V_{OUT}$ to the desired output voltage, $-V_4$ and measure V_{GAIN4}.
5. Set $-V_{OUT}$ to another output voltage, $-V5$ and measure V_{GAIN5}.

6. The gain is equal to

$$\left[\frac{V4 - V5}{V_{GAIN4} - V_{GAIN5}}\right] \times 20{,}000.$$

-V_{OUT} can be first set to zero and then to −10 volts. This gives the gain in the plus direction. The gain in the minus direction can be determined by using zero and +10 volts. The average gain can be determined by using output voltages of −10 and +10 volts.

TEST CIRCUITS FOR MEASUREMENT OF COMMON MODE REJECTION RATIO AND POWER SUPPLY REJECTION RATIO



Common Mode Rejection Ratio:

1. Set +V to +20 VDC, -V to -10 VDC, V_{OUT} +5 VDC by applying -5 VDC to -V_{OUT}.
2. Measure V_{OFF2}.
3. Set +V to +10 VDC, -V to -20 VDC, V_{OUT} to -5 VDC by applying +5 VDC to -V_{OUT}.
4. Measure $| V_{OFF2} - V_{OFF4} | < 1.0$ VDC.

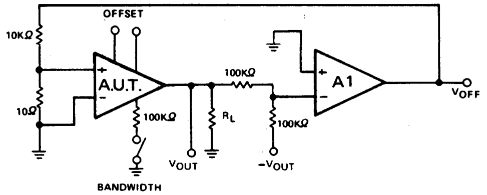
The +1.0 volt limit corresponds to a rejection ratio of 80 dB.

Power Supply Rejection Ratio:

1. Set +V to +20 VDC, -V to 15 VDC, V_{OUT} to ground by grounding -V_{OUT}.
2. Measure V_{OFF2}.
3. Set +V to +10 VDC.
4. Measure $| V_{OFF2} - V_{OFF4} | < 1.0$ VDC.
5. Set +V to +15 VDC, -V to -10 VDC.
6. Measure V_{OFF6}.
7. Set -V to -20 VDC.
8. Measure $| V_{OFF6} - V_{OFF8} | < 1.0$ VDC.

The ±1.0 volt limit corresponds to a rejection ratio of 80 dB.

TEST CIRCUITS FOR MEASURING OUTPUT VOLTAGE/CURRENT, POWER DISSIPATION, AND CONTINUITY CHECKS

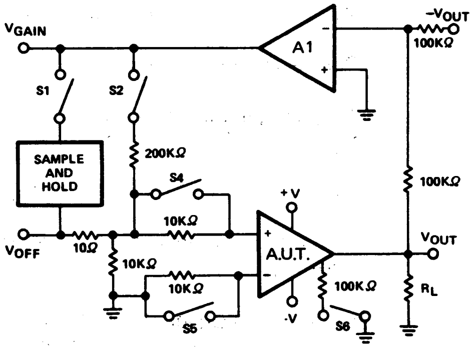


The output voltage/current is measured by connecting a load resistor, R_L, to the output of the A.U.T. The value of R_L is chosen to yield an output current which is the minimum acceptable output current at the desired output voltage. The amplifier under test is programed to a voltage greater than the desired output voltage by applying an equal but opposite polarity voltage to =V_{OUT}. The output voltage, V_{OUT}, is measured to see if it reaches the desired output voltage. This test is performed driving the output positive and driving the output negative.

The power dissipation is measured by driving the output voltage to zero by grounding −V_{OUT} and measuring the current in one of the power supply leads.

The continuity of the bandwidth control point is checked by applying −5V to −V_{OUT} and grounding the bandwidth control point through a 100K resistor. V_{OUT} should be less than one volt. There is a known relationship between the voltage at the bandwidth control point and the output voltage, V_{OUT}. This relationship depends on the device type. The continuity of the offset control points is determined by measuring the voltage at these points. These voltages will be slightly less than the positive supply voltage for the HA-2600 and the HA-2500.

SIMPLIFIED SCHEMATIC OF THE COMPLETE D.C. TEST CIRCUIT FOR OPERATIONAL AMPLIFIERS



APP NOTE

FOR YOUR INFORMATION

No. 509

Harris Analog

A SIMPLE COMPARATOR USING THE HA-2620

G. G. Miller

The input current and impedance of a comparator circuit frequently loads the source and reference signals enough to cause significant errors. This problem is frequently eliminated by using a high impedance operational amplifier between the signal and the comparator. Figure 1 shows a simple circuit in which the operational amplifier is used as a comparator which is capable of driving approximately ten logic gates. The input impedance of the HA-2620 is typically 500 MΩ. The input current is typically 1 nA. The minimum output current of 15 mA is obtainable with an output swing of up to ±10 volts.

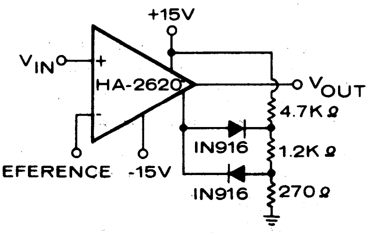


FIGURE 1 - HIGH IMPEDANCE COMPARATOR

The bandwidth control point is a very high impedance point having the same voltage as the amplifier output. The output swing can be conveniently limited by clamping the swing of the bandwidth control point. The maximum current through the clamp diodes is approximately 300 μA. The switching time is dependent on the output voltage swing and the stray capacitance at the bandwidth control point.

Figure 2 shows the waveforms for the comparator. The stray capacitance at the bandwidth control point can be reduced considerably below that of the breadboard circuit; this would improve the switching time. The switching time begins to increase more rapidly as the overdrive is reduced below 10 mV and is approximately 1 μs for an overdrive of 5 mV. Dependable switching can be obtained with an overdrive as small as 1 mV. However, the switching time increases to almost 12 μs.

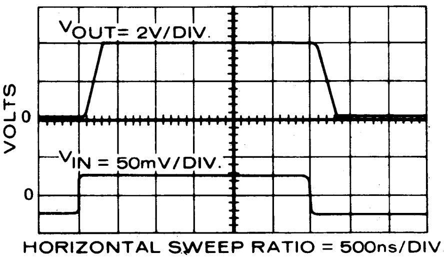


FIGURE 2 - WAVEFORMS FOR HA-2620 COMPARATOR

A common mode range of ±11 volts and a differential input range of ±12 volts makes the HA-2620 a very versatile comparator. The HA-2620 can sink or supply a minimum of 15 mA. The ability to externally clamp the output to any desired range makes the HA-2620 a very flexible comparator which is capable of driving unusual loads.

APP NOTE

FOR YOUR INFORMATION

No. 514

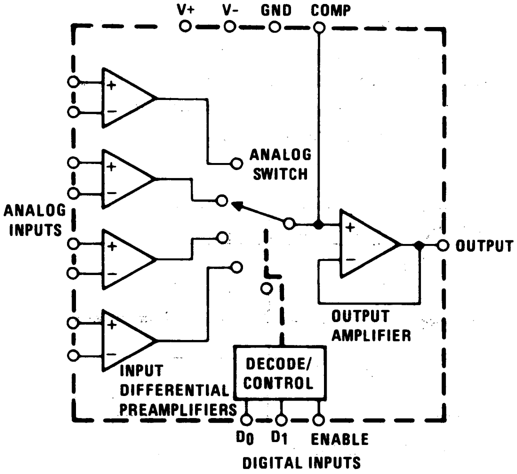
Harris Analog

THE HA-2400 PRAM FOUR CHANNEL OPERATIONAL AMPLIFIER

By Don Jones

INTRODUCTION

Harris Semiconductor has announced a new linear device, the HA-2400/HA-2405 Four Channel Operational Amplifier. This combines the functions of an analog switch and a high performance operational amplifier, and makes practical a large number of new linear circuit applications.



A functional diagram of the HA-2400 is shown above. There are four preamplifier sections, one of which is selected through the DTL/TTL compatible inputs and connected to the output amplifier. The selected analog input terminals and the output terminal form a high performance operational amplifier.

In actuality, the circuit consists of four conventional op-amp input circuits connected in parallel to a conventional op-amp output circuit. The decode/control circuitry furnishes operating current only to the selected input section.

CIRCUIT CONNECTIONS

These input control the selection of the amplifier input channels in accordance with the truth table below:

GAIN, VOLTS/VOLT		C_{COMP} pF	BANDWIDTH (TYPICAL) (-3dB), MHz	SLEW RATE (TYPICAL) VOLTS/μs
NON-INVERTING	INVERTING			
1	–	15	8.0	15
2	1	7	8.0	20
3	2	4	8.0	22
5	4	3	6.0	25
8	7	2	5.0	30
>10	>9	0	40 ÷ GAIN	50

The digital inputs can be driven with any DTL or TTL circuit which uses a standard +5.0V supply.

COMPENSATION

Frequency compensation for closed loop stability is recommended for closed loop gains less than 10. This is accomplished by connection of a single external capacitor from Pin 12 to A. C. ground (the V+ supply is recommended). The following table shows the minimum suggested compensation for various closed loop gains, with the resultant bandwidth and slew rate. Obviously, when the four channels are connected with different feedback networks, the channel with the lowest closed loop gain will govern the required compensation.

D_0	D_1	ENABLE	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4
L	L	H	ON	OFF	OFF	OFF
H	L	H	OFF	ON	OFF	OFF
L	H	H	OFF	OFF	ON	OFF
H	H	H	OFF	OFF	OFF	ON
L or H	L or H	L	OFF	OFF	OFF	OFF

$0V \leq L \leq +0.8V$ $+2.0V \geq H \geq +5.0V$

Compensation capacitors of greater value can be used to obtain lower bandwidth, greater phase margin, and reduced overshoot, at the expense of proportionately reduced slew rate.

External lead-lag networks could also be used to optimize bandwidth and/or slew rate at a particular gain.

APPLICATIONS

Any circuit function which can be constructed using a conventional operational amplifier can also be constructed using any channel of the HA-2400. Similar or different networks can be wired from the output to each channel input pair. The device can therefore be used to select and condition different input signals, or to select between different op-amp functions to be performed on a single input signal.

To wire a particular op-amp function to a channel, simply connect the appropriate network between the two inputs for that channel and the common output in the same manner as in wiring a conventional op-amp. It is often possible to design with fewer external components than would be required in wiring four separate op-amps (see Application Numbers 2 and 3 on the following pages). It should be remembered that the networks for unselected channels may still constitute a load at the amplifier output and the signal input, as if the unselected input terminals were disconnected from the network.

If offset adjustment is required, it can generally be accomplished by resistive summation at either of the inputs for each channel (see Application Number 8).

The analog input terminals of the OFF channels draw the same bias current as the ON inputs. The maximum differential input voltage of these terminals must be observed and their voltage levels must never exceed the supply voltages.

When the Enable input is held low, all four input channels are disconnected from the output. When this occurs, the output voltage will generally slowly drift towards the negative supply. If a zero volt output condition is required, one channel should be wired as a voltage follower with its positive input grounded.

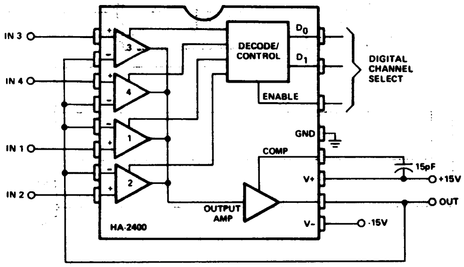
The amplifier output impedance remains low, even when the inputs are disabled; so it is not generally practical to wire the outputs of two or more devices directly together. The compensation pins of two devices, however, could be wired together to produce a switch with one output and more than four input channels.

The voltage at the compensation pin is about 0.7V more positive than the output signal, but has a very high source impedance. Maximum current from this pin is about 300μA, which makes it a convenient point for limiting the output swing through clamping diodes and divider networks (see Application Number 13).

Even if the application only requires a single channel to be switched on and off, it is often more economical to use the HA-2400, rather than a separate analog switch and high performance op-amp. Unused analog channel inputs should be grounded. Unused digital inputs may be wired to ground for a permanent "low" input, or either left open or wired to +5.0V for a permanent "high" input.

Illustrated on the following pages are a few of the thousands of possible applications for the Four Channel Operational Amplifier. These will give the reader a general impression of how the units can be connected; and probably will help generate many other ideas for applications. Also included are some "challenges" for the reader to modify the illustrated designs to perform different functions.

APPLICATION NO. 1



ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

This circuit is used for analog signal selection or time division multiplexing. As shown, the feedback signal places the selected amplifier channel in a voltage follower (non-inverting unity gain) configuration, and provides very high input impedance and low output impedance. The single package replaces four input buffer amplifiers, four analog switches with decoding, and one output buffer amplifier.

For low level input signals, gain can be added to one or more channels by connecting the (–) inputs to a voltage divider between output and ground. Bandwidth is approximately 8 MHz, and the output will slew from one level to another at about 15.0V per microsecond.

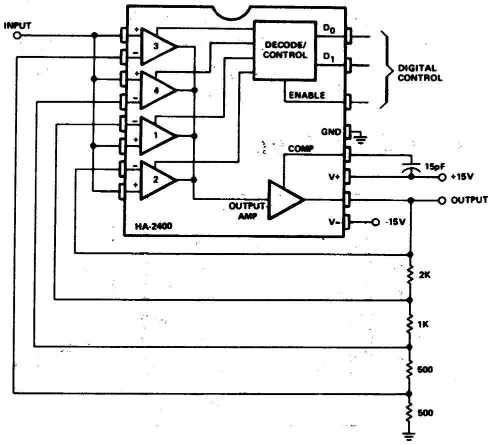
Expansion to multiplex 5 to 12 channels can be accomplished by connecting the compensation pins of two or three devices together, and using the output of only one of the devices. The Enable input on the unselected devices must be low.

Expansion to 16 or more channels is accomplished in a straightforward manner by connecting outputs of 4 four-channel multiplexers to the inputs of another four-channel multiplexer.

Differential signals can be handled by two identical multiplexers addressed in parallel.

Inverting amplifier configurations can also be used, but the feedback resistors may cause crosstalk from the output to unselected inputs.

APPLICATION NO. 2


INPUT
3
4
1
2
DECODE/
CONTROL
D0
D1
DIGITAL
CONTROL
ENABLE
GND
COMP
15pF
+15V
V+
OUTPUT
OUTPUT
AMP
HA-2400
V-
-15V
2K
1K
500
500

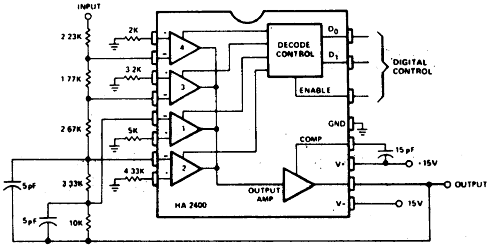
AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN

This is a non-inverting amplifier configuration with feedback resistors chosen to produce a gain of 0, 1, 2, 4, or 8 depending on the Digital Control inputs.

Comparators at the output could be used for automatic gain selection for auto-ranging meters, etc.

CHALLENGE: Design a circuit using only two HA-2400's which can be programmed to any of 16 different gains.

APPLICATION NO. 3

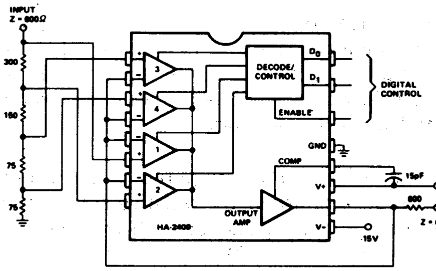

INPUT
2 23K
1 77K
2 67K
3 33K
10K
5pF
5pF
2K
3 2K
5K
4 33K
4
3
1
2
DECODE
CONTROL
D0
D1
DIGITAL
CONTROL
ENABLE
GND
COMP
15 pF
+15V
V+
OUTPUT
AMP
OUTPUT
HA 2400
V-
15V

AMPLIFIER, INVERTING PROGRAMMABLE GAIN

The circuit above can be programmed for a gain of 0, –1, –2, –4 or –8.

This could also have been accomplished with one input resistor and one feedback resistor per channel in the conventional manner, but this would require eight resistors rather than five.

APPLICATION NO. 4

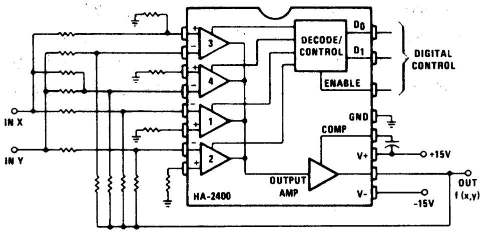

INPUT
Z = 600Ω
300
150
75
75
3
4
1
2
DECODE/
CONTROL
D0
D1
DIGITAL
CONTROL
ENABLE
GND
COMP
15pF
+15V
V+
600
OUTPUT
Z = 600Ω
OUTPUT
AMP
HA-2400
V-
-15V

ATTENUATOR PROGRAMMABLE

This circuit performs the function of dividing the input signal by a selected constant (1, 2, 4, 8, or ∞ as illustrated). To multiply by a selected constant, see circuit No. 2. While T, π, or L sections could be used in the input attenuator, this is not necessary since the amplifier loading is negligible and a constant input impedance is maintained. The circuit is thus much simpler and more accurate than the usual method of constructing a constant impedance ladder and switching sections in and out with analog switches.

Two identical circuits may be used to attenuate a balanced line.

APPLICATION NO. 5

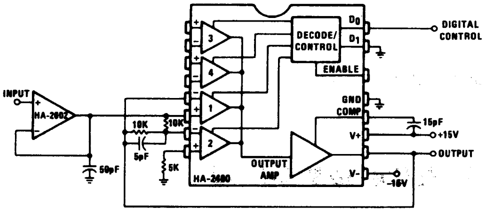

DECODE/
CONTROL
D0
D1
DIGITAL
CONTROL
ENABLE
IN X
IN Y
GND
COMP
V+
+15V
OUTPUT
AMP
OUT
f (x,y)
HA-2400
V-
-15V

ADDER/SUBTRACTOR PROGRAMMABLE FUNCTION

The circuit shown above can be programmed to give the output functions $-K_1X$, $-K_2Y$, $-(K_3X + K_4Y)$, or $K_5X - K_6Y$. Obviously, many other functions of one or more variables can be constructed, including combinations with analog multiplier or logarithmic modules.

This device opens up many new design approaches in digitally controlled analog computation or signal manipulation.

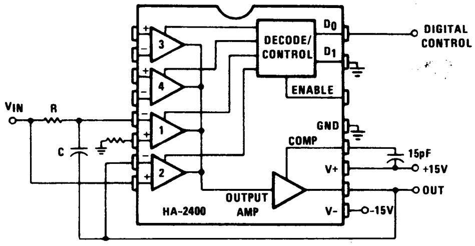
APPLICATION NO. 6


INPUT
HA-2602
50pF
10K
10K
5pF
5K
DECODE/
CONTROL
D0
D1
DIGITAL
CONTROL
ENABLE
GND
COMP
15pF
V+
+15V
OUTPUT
AMP
OUTPUT
HA-2400
V-
-15V

PHASE SELECTOR/PHASE DETECTOR/
SYNCHRONOUS RECTIFIER/BALANCED MODULATOR

This circuit passes the input signal at unity gain, either unchanged, or inverted depending on the Digital Control input. A buffered input is shown, since low source impedance is essential. Gain can be added by modifications to the feedback networks. Signals up to 100 kHz can be handled with 20.0V peak-to-peak output. The circuit becomes a phase detector by driving the Digital Control input with a reference phase at the same frequency as the input signal, the average D. C. output being proportional to the phase difference, with zero volts at $^{+}90^{\circ}$. By connecting the output to a comparator, which in turn drives the Digital Control, a synchronous full-wave rectifier is formed. With a low frequency input signal and a high frequency digital control signal, a balanced (surpressed carrier) modulator is formed.

APPLICATION NO. 7

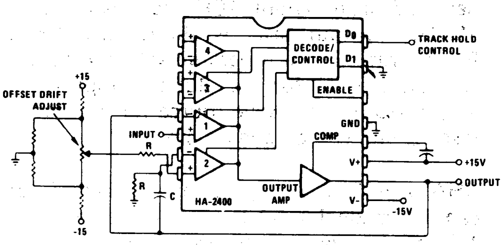

DECODE/
CONTROL
D0
D1
DIGITAL
CONTROL
ENABLE
VIN
R
C
GND
COMP
15pF
V+
+15V
OUT
OUTPUT
AMP
HA-2400
V-
-15V

INTEGRATOR/RAMP GENERATOR
WITH INITIAL CONDITION RESET

It is difficult in practice to set the initial conditions accurately in an integrator. This usually requires wiring contacts of a mechanical relay across the capacitor - - leakage currents of solid state switches produce integration inaccuracy. The scheme shown above eliminates these reliability and accuracy problems.

Channel 1 is wired as a conventional integrator, Channel 2 as a voltage follower. When Channel 2 is switched on, the output will follow V_{IN}, and C will discharge to maintain zero volts across it. When Channel 1 is then switched on the output will initially be at the instantaneous value of V_{IN}, and then will commence integrating towards the opposite polarity. This circuit is particularly suitable for timing ramp generation using a fixed D. C. input. Many variations are possible, such as programmable time constant integrators.

APPLICATION NO. 8

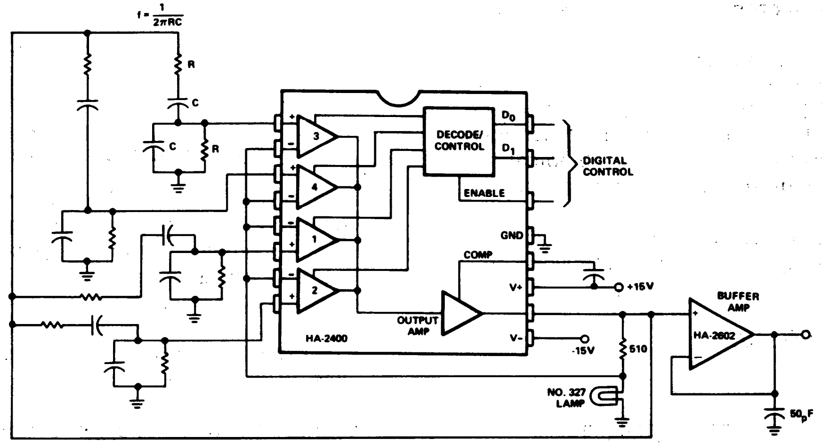

DECODE/
CONTROL
D0
D1
TRACK HOLD
CONTROL
ENABLE
+15
OFFSET DRIFT
ADJUST
INPUT
R
R
C
GND
COMP
V+
+15V
OUTPUT
OUTPUT
AMP
HA-2400
V-
-15V
-15

TRACK AND HOLD/SAMPLE AND HOLD

Channel 1 is wired as a voltage follower and is turned on during the track/sample time. If the product of R x C is sufficiently short compared to the period of maximum output frequency, or sample time, C will charge to the output level. Channel 2 is an integrator with zero input signal. When Channel 2 is then turned on, the output will remain at the voltage across C.

An even simpler circuit can be made by wiring one channel as an amplifier, choosing the compensation capacitor to yield the minimum required bandwidth or slew rate. When the Enable input is pulled low, the output will tend to remain at its last level, because of the charge remaining on the compensating capacitor.

APPLICATION NO. 9

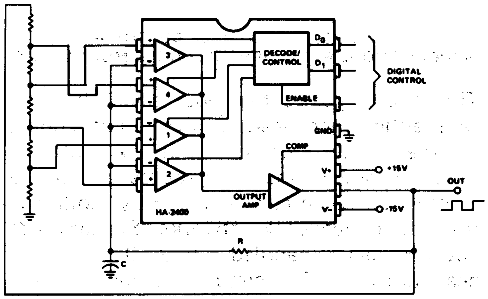

f = 1/2πRC
R
C
C
R
3
4
1
2
DECODE/ CONTROL
D0
D1
ENABLE
DIGITAL CONTROL
GND
COMP
V+
+15V
OUTPUT AMP
HA-2400
V-
-15V
510
NO. 327 LAMP
BUFFER AMP
HA-2602
50pF

SINE WAVE OSCILLATOR PROGRAMMABLE FREQUENCY

Any oscillator which can be constructed using an op-amp, such as the twin-T, phase shift, crystal controlled types, etc. can be made programmable by using the HA-2400. Illustrated above is a Wien Bridge type, which is very popular for signal generators, since it is easily tunable over a wide frequency range, and has a very low distortion sine wave output. The frequency determining networks can be designed from about 10Hz to greater than 1MHz. Output level is about 6.0V RMS. By substituting a programmable attenuator (Circuit No. 4) for the Buffer Amplifier, a very versatile sine wave source for automatic testing, etc. can be constructed.

CHALLENGE: A high Q, narrow band filter can be made by feeding back greater than 1/3 of the output to the negative input. Design a circuit using the HA-2400 and an RC network which can be programmed either to generate or to detect an audio tone of the same frequency. Such a circuit would be quite useful for data communications.

APPLICATION NO. 10

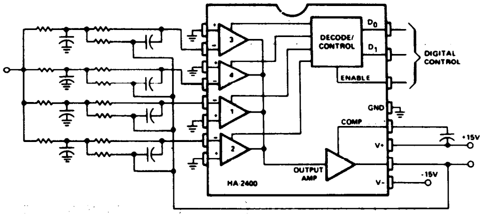

3
4
1
2
DECODE/ CONTROL
D0
D1
ENABLE
DIGITAL CONTROL
GND
COMP
V+
+15V
OUT
OUTPUT AMP
HA-2400
V-
-15V
R
C

MULTIVIBRATOR, FREE RUNNING, PROGRAMMABLE FREQUENCY

This is the simplest of any programmable oscillator circuit, since only one stable timing capacitor is required. The output square wave is about 25.0V peak-to-peak and has rise and fall times of about 0.5 μs. If a programmable attenuator circuit (No. 4) is placed between the output and the divider network, 16 frequencies can be produced with two HA-2400's and still only one timing capacitor.

A precision programmable square-triangle generator can also be constructed by adapting circuit described in Harris Application Note 507 to the HA-2400.

APPLICATION NO. 11


DECODE/
CONTROL
D0
D1
ENABLE
DIGITAL
CONTROL
GND
COMP
V+
V-
+15V
-15V
OUTPUT
AMP
HA 2400
3
4
1
2

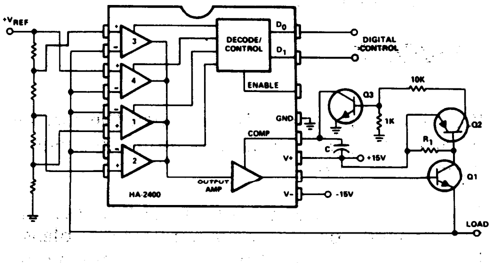
ACTIVE FILTER PROGRAMMABLE

Shown above is a second order low pass filter with programmable cutoff frequency. This circuit should be driven from a low source impedance since there are paths from the output to the input through the unselected networks.

Virtually any filter function which can be constructed with a conventional op-amp can be made programmable with the HA-2400.

A useful variation would be to wire one channel as a unity gain amplifier, so that one could select the unfiltered signal, or the same signal filtered in various manners. These could be cascaded to provide a wide variety of programmable filter functions.

APPLICATION NO. 12

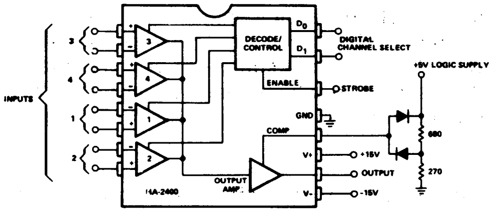

+VREF
DECODE/
CONTROL
D0
D1
DIGITAL
CONTROL
ENABLE
GND
COMP
V+
V-
10K
Q3
1K
Q2
R1
C
+15V
Q1
-15V
OUTPUT
AMP
HA 2400
LOAD
3
4
1
2

POWER SUPPLY PROGRAMMABLE

Many systems require one or more relatively low current voltage sources which can be programmed to a few predetermined levels. It is no longer necessary to purchase a programmable power supply with far more capability than needed. The circuit shown above produces positive output levels, but could be modified for negative or bipolar outputs. Q1 is the series regulator transistor, selected for the required current and power capability. R1, Q2 and Q3 form an optional short circuit protection circuit, with R1 chosen to drop about 0.7V at the maximum output current. The compensation capacitor, C. should be chosen to keep the overshoot, when switching, to an acceptable level.

CHALLENGE: Design a supply using only two HA-2400's which can be programmed to 16 binary weighted (or 10 BCD weighted) output levels.

APPLICATION NO. 13


INPUTS
3
4
1
2
DECODE/
CONTROL
D0
D1
DIGITAL
CHANNEL SELECT
+5V LOGIC SUPPLY
ENABLE
STROBE
GND
COMP
680
V+
+15V
OUTPUT
270
V-
-15V
OUTPUT
AMP
HA-2400

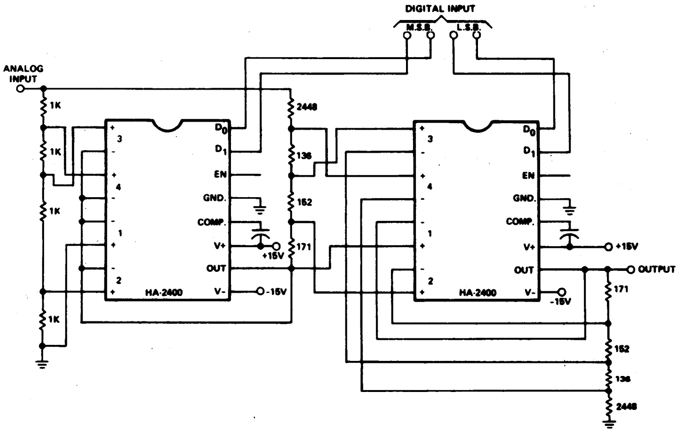
COMPARATOR, FOUR CHANNEL

When operated open loop without compensation, the HA-2400 becomes a comparator with four selectable input channels. The clamping network at the compensation pin limits the output voltage to allow DTL or TTL digital circuits to be driven with a fanout of up to ten loads.

Output rise and fall times will be about 100ns for differential input signals of several hundred millivolts, but will be in the microsecond region for small differential signals.

The circuit can be used to compare several signals against each other or against fixed references; or a single signal can be compared against several references. A "window comparator", which assures that a signal is within a voltage range, can be formed by monitoring the output polarity while rapidly switching between two channels with different reference inputs and the same signal input.

APPLICATION NO. 14



MULTIPLYING D TO A CONVERTER

The circuit above performs the function, $V_{OUT} = V_{IN} \cdot \frac{N}{16}$, where N is the binary number from 0 to 15 formed by the digital input. If the analog input is a fixed D.C. reference, the circuit is a conventional 4-bit D to A. The input could also be a variable or A.C. signal, in which case the output is the product of the analog signal and the digital signal.

The circuit on the left is a programmable attenuator with weights of 0, 1/4, 1/2 or 3/4. The circuit on the right is a non-inverting adder which adds weights to the first output of 0, 1/16, 1/8 or 3/16.

If four quadrant multiplication is required, place the Phase Selector circuit (No. 6) in series with either the analog input or output. The D_0 input of that stage becomes the + or – sign bit of the digital input.

MORE CHALLENGES

One of our favorite college textbooks paused at each climactic point with a statement to the effect that, "Proof of the following theorem is omitted, and is suggested as an exercise for the student."

The following is a list of some additional applications in which we believe the HA-2400 will prove very valuable. The "proofs", at present, remain as exercises for our ingenious readers.

- A to D Converter, Dual Slope Integrating
- Active Filter, State Variable Type with Programmable Frequency and/or Programmable "Q"
- Amplifier with Programmable D.C. Level Shift
- Chopper Amplifiers
- Crossbar Switches
- Current Source, Programmable
- F.M. Stereo Modulator
- F.S.K. Modem
- Function Generators, Programmable
- Gyrator, Programmable
- Monostable Multivibrator, Programmable
- Multiplier, Pulse Averaging
- Peak Detector with Reset
- Resistance Bridge Amplifier/Comparator with Programmable Range
- Sense Amp/Line Receiver with Programmable Threshold
- Spectrum Analyzer, Scanning Type
- Sweep Generator, Programmable
- Switching Regulator
- Touch-Tone™ Generator/Detector (Use Harris HD-0165 Keyboard Encoder I.C.)

FEEDBACK

We believe we have only scratched the surface of possible applications for a multiple channel operational amplifier.

If you have a solution for any of the previous "challenges" or any new application, please let us know. Anything from a one word description to a tested design will be welcome.

APP NOTE

FOR YOUR INFORMATION

No. 515

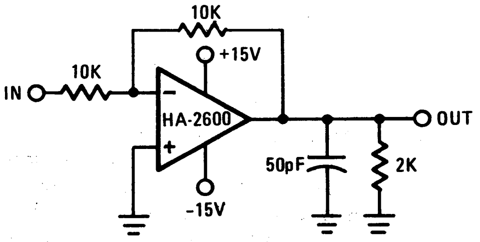
Harris Analog

OPERATIONAL AMPLIFIER STABILITY: INPUT CAPACITANCE CONSIDERATIONS

By Don Jones

This is the first in a series of notes dealing with stabilization and optimization of A.C. response in operational amplifiers. One of the more common difficulties in applying operational amplifiers will be discussed.

Let's consider the unity gain inverting amplifier circuit shown below:



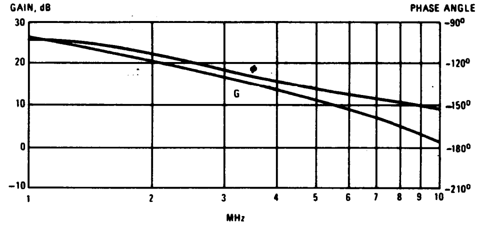
This appears to be a straightforward application with reasonable component values.

But, with the input grounded, the circuit output shows an oscillation at about 5 MHz.

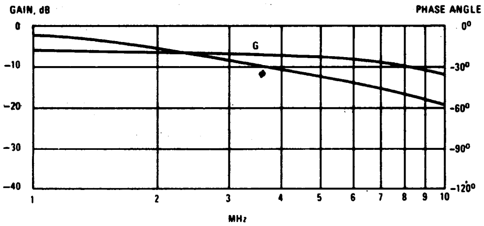
Even more surprising, if the same device is connected as a voltage follower with the same load, it is perfectly stable. Since the inverting amplifier has 6 dB less feedback than the voltage follower, shouldn't it be more stable?

The culprit here is capacitance at the amplifier inverting input. The HA-2600 in the TO-99 can has an input capacitance of about 2 or 3 pF. When soldered on a P.C. card, or inserted in a socket, wiring capacitance might add another 3 to 6 pF. With only 5K effective resistance at this point, 5 to 10 pF seems pretty negligible, doesn't it? But let's find out.

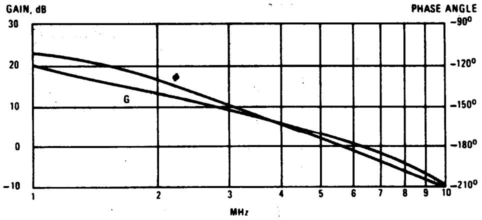
The open loop amplitude and phase response characteristics of the amplifier between 1 and 10 MHz looks like this:



The characteristics of the feedback network alone with 5 pF capacitance to ground looks like this:

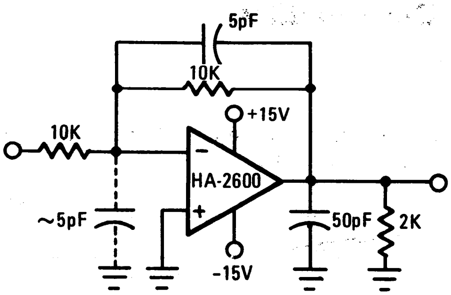


Combining these two graphs by algebraically adding the dB gains together and adding the phase shifts together gives us the open loop response at the summing point:



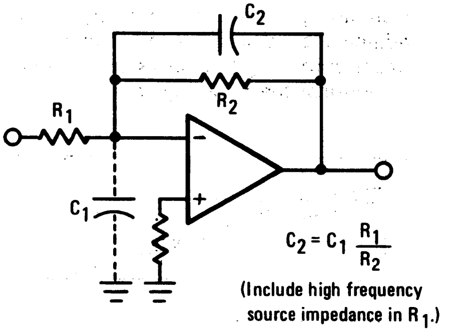
We can see that on the composite response curves, the phase shift crosses 180° at 5.5 MHz, and that there is still about +2 dB of gain at this frequency. Therefore, closing the loop automatically creates an oscillator.

How can we overcome this effect? If we add a capacitor across the feedback resistor, we can cancel the effects of the input capacitance:

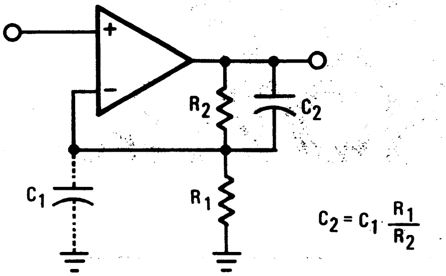


If the feedback capacitance matches the input capacitance, the response curves of the feedback network alone will be a flat -6 dB and 0° across the frequency band. The composite curves will then show a bandwidth of 7.5 MHz and a positive phase margin of 33°. So the circuit will now be quite stable. It's amazing how much difference that small capacitance can make.

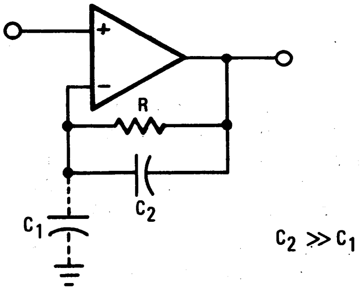
The general scheme for compensation of various circuit types is shown below:


C_2
R_2
R_1
C_1
$C_2 = C_1 \frac{R_1}{R_2}$
(Include high frequency source impedance in R_1.)

INVERTING AMPLIFIER



NON-INVERTING AMPLIFIER



FOLLOWER WITH FEEDBACK RESISTOR

It's not really necessary to know the exact value of stray capacitance, C_1 - for most layouts, about 5 to 10 pF is a good guess. Unless you are trying to squeeze out the last Hz of frequency response, it doesn't hurt to guess on the high side. At higher gains, where C_2 calculates out to less than 1 or 2 pF, it isn't necessary to use C_2 - but it won't disturb anything if you do use it.

If you are uncertain about whether compensation is necessary, check the pulse response or frequency response of the closed loop stage. Hook a pulse generator to the input, and adjust the amplitude for about a 200 millivolt step at the output - if the output overshoot is less than 40% of the step, the circuit will be stable. Alternately, check the small signal frequency response of the stage - if the high frequency peaking is less than +6 dB, more than the low frequency gain, the circuit is stable. Of course, you can increase the compensation capacitor if you need even smoother response.

The phenomena we have described are not peculiar to any one amplifier type. Wideband amplifiers require a little more care in the design of feedback networks; but the same type oscillations will show up on 741 type amplifiers with higher feedback resistor values.

APP NOTE
FOR YOUR INFORMATION
No. 517
Harris Analog

APPLICATIONS OF A MONOLITHIC SAMPLE-AND-HOLD/GATED OPERATIONAL AMPLIFIER

By Don Jones

INTRODUCTION

The sample-and-hold or track-and-hold function is very widely used in linear systems. Until recently, this function was available only in modular or hybrid circuits; or perhaps most frequently the circuit was constructed by the user from an analog switch, a capacitor, and a very low bias current operational amplifier.

A high quality sample-and-hold circuit must meet certain requirements:

(1) The holding capacitor must charge up and settle to its final value as quickly as possible.

(2) When holding, the leakage current at the capacitor must be as near zero as possible to minimize voltage drift with time.

(3) Other sources of error must be minimized.

Design of a sample-and-hold, particularly the user built variety, involves a number of compromises in the above requirements. The amplifier or other device feeding the analog switch must have high current capability and be able to drive capacitive loads with stability. The analog switch must have both low ON resistance and extremely low OFF leakage currents. But, leakage currents of most analog switches (except the dielectrically isolated types) run to several hundred nanoamperes at elevated temperatures. The analog switch must have very low coupling between the digital input and analog output, because any spikes generated at the instant of turn-off will change the charge on the capacitor. The output amplifier must have extremely low bias current over the temperature range, and also must have low offset drift and sufficient slew rate; a combination satisfied by only a few available amplifiers.

THE HA-2420/2425

The HA-2420/2425 is the first complete monolithic sample-and-hold integrated circuit. A functional diagram is shown in Figure 1.

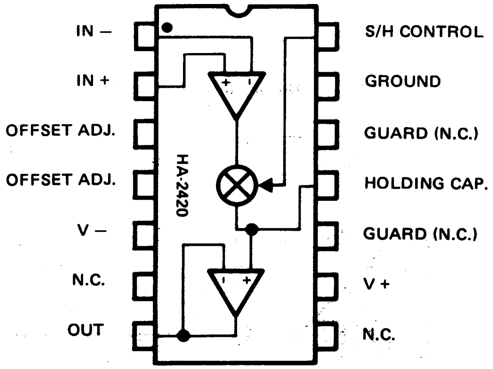


Figure 1 — HA-2420/2425 Functional Diagram

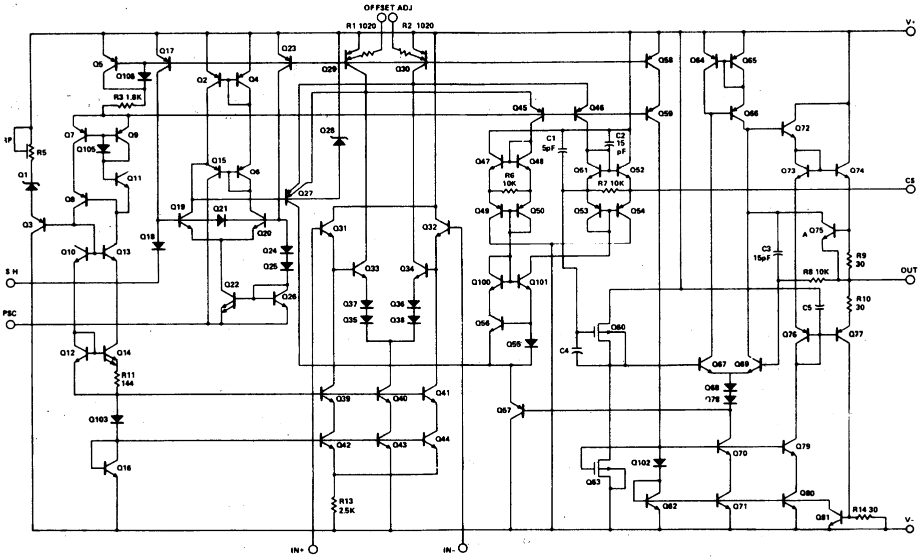
The input amplifier stage is a high performance operational amplifier with excellent slew rate, and the ability to drive high capacitance loads without instability. The switching element is a highly efficient bipolar transistor stage with extremely low leakage in the OFF condition. The output amplifier is a MOSFET input unity gain follower to achieve extremely low bias current.

MOSFET inputs are generally not used for D.C. amplifiers because their offset voltage drift is difficult to control. In this configuration, however, negative feedback is generally applied between the output and inputs of the entire device, and the effect of this offset drift at the inputs is divided by the open loop gain of the input amplifier stage.

The schematic of the HA-2420 is in Figure 2. During sampling (S/H control LOW) the signal path through the input amplifier stage starts at Q31-34, through Q45 and Q46, and then to the holding capacitor terminal through Q51-54. The output follower amplifier has its input at MOSFET Q60.

HA-2420/2425

Sample-and-Hold



OFFSET ADJ
R1 1020
R2 1020
V+
S H
PSC
CS
OUT
V-
IN+
IN-
R5
R3 1.8K
R6 10K
R7 10K
R8 10K
R9 30
R10 30
R11 144
R13 2.5K
R14 30
C1 5pF
C2 15 pF
C3 15pF
C4
C5
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
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Q38
Q39
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Q41
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Q62
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Q64
Q65
Q66
Q67
Q68
Q69
Q70
Q71
Q72
Q73
Q74
Q75
Q76
Q77
Q78
Q79
Q80
Q81
Q100
Q101
Q102
Q103
Q105
Q106

NOTE: 1. Unless otherwise specified resistance values are in OHMS, capacitance values are in picofarads.

Figure 2

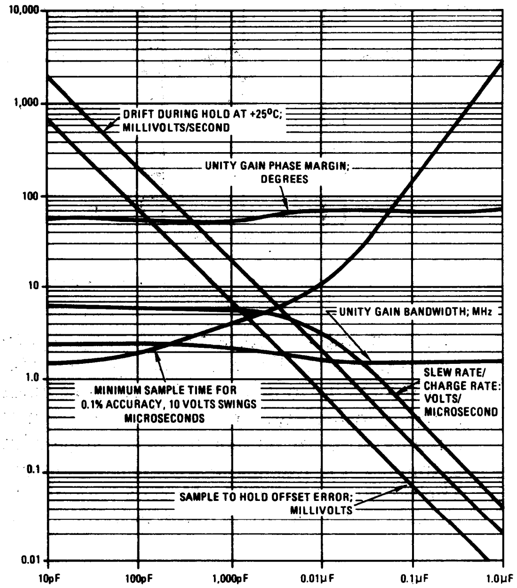


Figure 3 – Holding Capacitor, C_H

TYPICAL SAMPLE-AND-HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITANCE

In the "hold" mode, the S/H control is HIGH, so Q21 conducts, turning on Q27 which diverts the signal away from Q45 and Q46, and passes the signal to V - through Q57. Q57 also forces Q51-54 to ride up and down with the output signal, so there is virtually zero potential between these transistor bases and the voltage on C_H; completely eliminating leakage from C_H back into the input amplifier.

SAMPLE-AND-HOLD APPLICATIONS

A number of basic applications are shown on the following pages. The device is exceptionally versatile, since it can be wired into any of the hundreds of feedback configurations possible with any operational amplifier. In many applications the device will replace both an operational amplifier and a sample-and-hold module.

The larger the value of the timing capacitor, the longer time it will hold the signal without excessive drift; however, it will also reduce the charging rate/slew rate and the amplifier bandwidth during sampling. So the capacitance value must be optimized for each particular application. The graph in Figure 3 shows these tradeoffs. Drift during holding tends to double for every 10°C rise in ambient temperature. The holding capacitor should have extremely high insulation resistance and low dielectric absorption-polystyrene (below +85°C), Teflon, or mica types are recommended.

Guard Ring Layout (Bottom View)

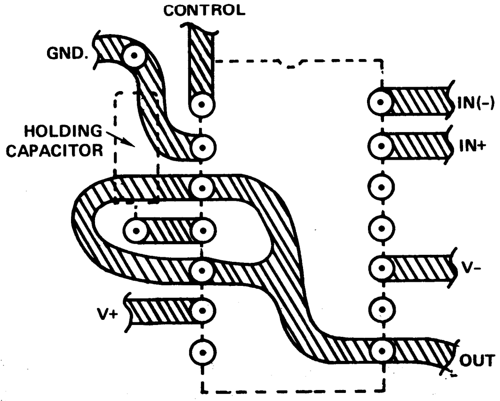


Figure 4

For least drift during holding, leakage paths on the P.C. board and on the device package surface must be minimized. Since the output voltage is nearly equal to the voltage on C_H, the output line may be used as a guard line surrounding the line to C_H. Then, since the potentials are nearly equal, very low leakage currents will flow. The two package pins surrounding the C_H pin are not internally connected, and may be used as guard pins to reduce leakage on the package surface. A suggested P.C. guard ring layout is shown in Figure 4.

GATED OPERATIONAL AMPLIFIER APPLICATIONS

An operational amplifier with a highly efficient analog switch in series with its output is a very useful building block for linear systems. The amplifier can be connected in any of the conventional op amp feedback configurations. With the switch closed, the circuit behaves as a conventional op amp with excellent bandwidth, slew rate, high output current capability, and is able to drive capacitive loads with good stability. With the switch open, the output node is an almost perfect open circuit.

The output buffer amplifier has extremely high input impedance and exceptionally low bias current, but is not particularly well suited for D.C. applications outside an overall feedback loop, since its offset voltage may be quite high.

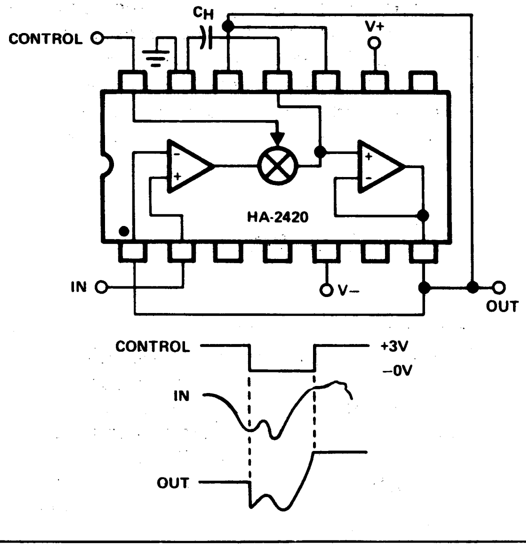
A number of possible gated amplifier applications are suggested in the following section.

APPLICATION NO. 1

Feedback is the same as a conventional op amp voltage follower which yields a unity gain, non-inverting output. This hookup also has a very high input impedance.

The only difference between a track-and-hold and a sample-and-hold is the time period during which the switch is closed. In track-and-hold operation, the switch is closed for a relatively long period during which the output signal may change appreciably; and the output will hold the level present at the instant the switch is opened. In sample-and-hold opera-

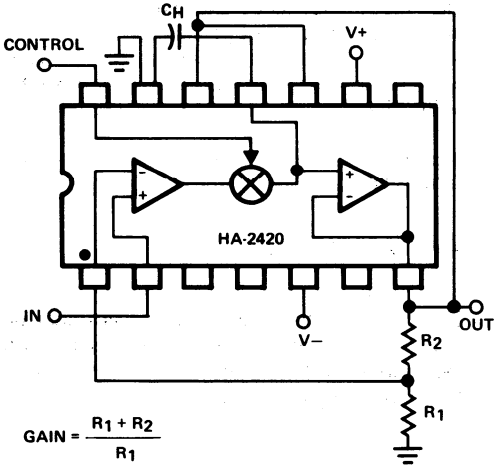
Basic Track-and-Hold/Sample-and-Hold



tion, the switch is closed only for the period of time necessary to fully charge the holding capacitor.

APPLICATION NO. 2

Sample-and-Hold With Gain



$$\text{GAIN} = \frac{R_1 + R_2}{R_1}$$

This is the standard non-inverting amplifier feedback circuit.

It illustrates one of the many ways in which the HA-2420 may be used to perform both op amp and sampling functions, eliminating the need for a separate scaling amplifier and sample-and-hold module.

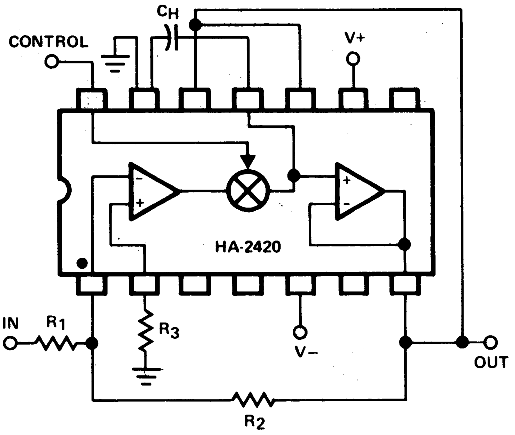
In general, it is usually best design practice to scale the gain such that the largest expected signal will give an output close to + or − 10 volts. Drift current is essentially independent of output level, and less percentage drift will occur in a given time for a larger output signal.

APPLICATION NO. 3

This illustrates another application in which the hookup versatility of the HA-2400 often eliminates the need for a separate operational amplifier and sample-and-hold module. This hookup will have somewhat higher input to output feedthrough during "hold," than the non-inverting connection, since output impedance is the open-loop value during "hold," and feedthrough will be:

$$\frac{V_{in} R_o}{R_1 + R_2 + R_o}$$

Inverting Sample-and-Hold



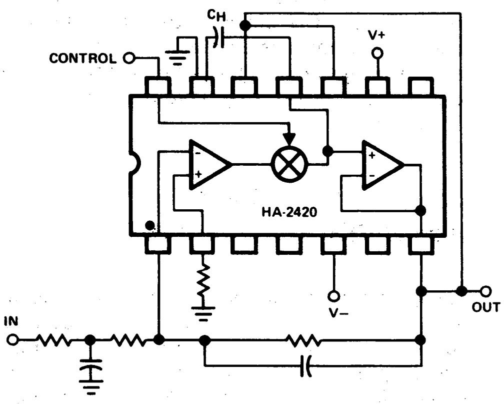
$$\text{GAIN} = -\frac{R_2}{R_1}$$

$$\text{MAKE} \quad R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

APPLICATION NO. 4

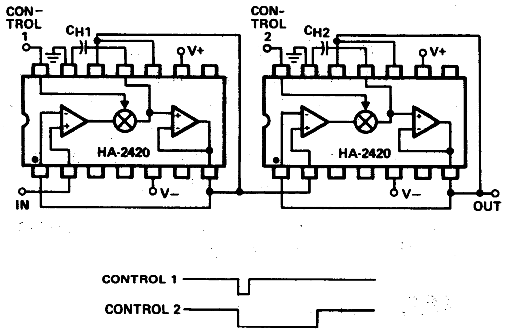
It is often required that a signal be filtered prior to sampling. This can be accomplished with only one device. Any of the inverting and non-inverting filters which can be built with op amps can be implemented. However, it is necessary that the sampling switch be closed for sufficient time for the filter to settle when active filter types are connected around the device.

Filtered Sample-and-Hold



APPLICATION NO. 5

Cascaded Sample-and-Hold

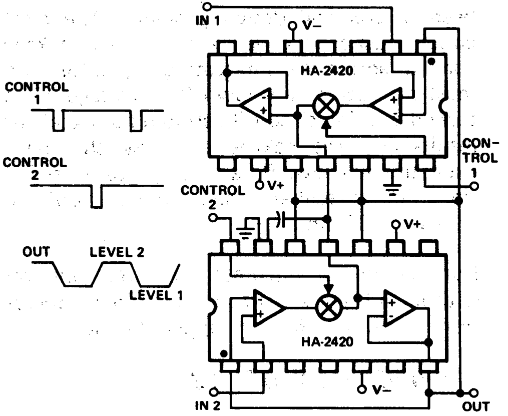

CON-
TROL
1
CH1
V+
HA-2420
V−
IN
CON-
TROL
2
CH2
V+
HA-2420
V−
OUT
CONTROL 1
CONTROL 2

Short sample times require a low value holding capacitor; while long, accurate hold times require a high value holding capacitor. So, achieving a very long hold with a short sample appears to be contradictory. However, it can be accomplished by cascading two S/H circuits, the first with a low value capacitor, the second with a high value. Then the second S/H can sample for as long a time as the first circuit can accurately hold the signal.

APPLICATION NO. 6

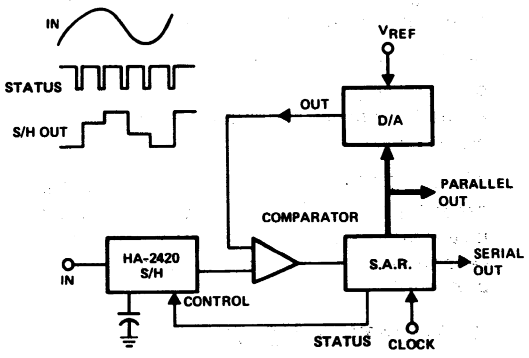
Two or more S/H circuits may share a common holding capacitor and output as shown. The only limit to the number of devices to be multiplexed is that the leakage currents of all devices add together, which increases drift during holding.

Multiplexed Sample-and-Hold


IN 1
V−
HA-2420
CON-
TROL
1
CONTROL
2
V+
V+
HA-2420
V−
IN 2
OUT
CONTROL
1
CONTROL
2
OUT
LEVEL 2
LEVEL 1

APPLICATION NO. 7

A/D Converter

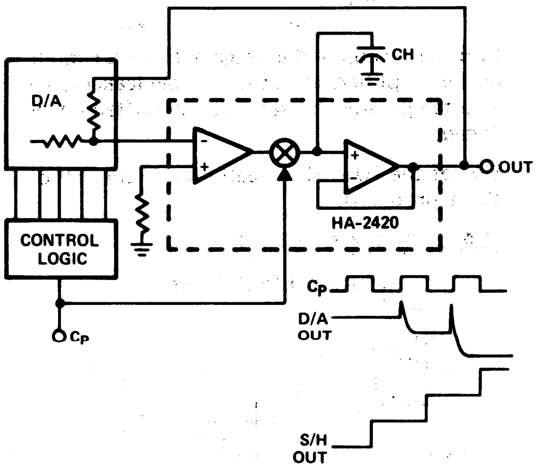

IN
STATUS
S/H OUT
VREF
OUT
D/A
PARALLEL
OUT
COMPARATOR
HA-2420
S/H
IN
CONTROL
S.A.R.
SERIAL
OUT
STATUS
CLOCK

Certain analog to digital converters such as the successive approximation type require that the input signal be a steady D.C. level during the conversion cycle. The HA-2420 is ideal for holding the signal steady during conversion; and also functions as a buffer amplifier for the input signal, adding gain, inversion, etc., if required.

The system illustrated is a complete 8 bit successive approximation converter requiring only four I.C. packages and capable of up to 40,000 conversions per second.

APPLICATION NO. 8

De-Glitcher


CH
D/A
OUT
HA-2420
CONTROL
LOGIC
Cp
D/A
OUT
S/H
OUT
Cp

The word "glitch" has been a universal slang expression among electronics people for an unwanted transient condition. In D to A converters, the word has achieved semi-official status for an output transient which momentarily goes in the wrong direction when the digital input address is changed.

In the illustration, the HA-2420 does double duty, serving as a buffer amplifier as well as a glitch remover, delaying the output by ½ clock cycle.

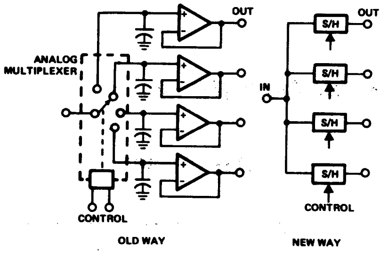
The HA-2420 may be used to remove many other types of "glitches" in a system. If a delayed sample pulse is required, this can be generated using a dual monostable multivibrator I.C.

APPLICATION NO. 9

This circuit reconstructs and separates analog signals which have been time division multiplexed.

The conventional method, shown on the left, has several restrictions, particularly when a short dwell time and a long, accurate hold time is required. The capacitors must charge from a low impedance source through the resistance and current limiting characteristics of the multiplexer. When holding, the high impedance lines are relatively long and subject to noise pickup and leakage. When FET input buffer amplifiers are used for low leakage, severe temperature offset errors are often introduced.

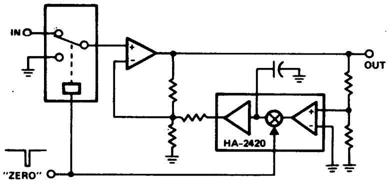
De-Multiplexer



Use of the HA-2420 greatly diminishes all of these problems.

APPLICATION NO. 10

Automatic Offset Zeroing



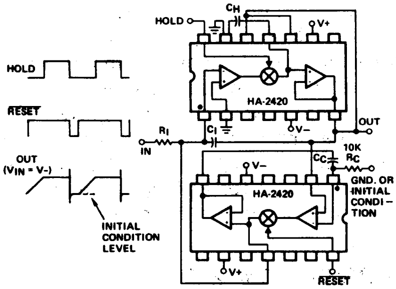
This basic circuit has widespread applications in instrumentation, A/D conversion, DVM's and DPM's to eliminate offset drift errors by periodically rezeroing the system. Basically, the input is periodically grounded, the output offset is then sampled and fed back to cancel the error.

The system illustrated automatically zeros a high gain amplifier. Care in the actual design is necessary to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

Many variations of this scheme are possible to suit the individual system.

APPLICATION NO.11

Integrate-Hold-Reset



This circuit accurately computes the functions,

$$V_O = \int_{T_1}^{T_2} V_{in}\, dt$$

and holds the answer for further processing.

Resetting circuits for integrators have always been a practical design problem. The reset circuit must produce an extremely low leakage current across the integrating capacitor, and must produce a very low offset voltage when turned on. The circuit illustrated has excellent results since the leakage at the switch node is exceptionally low. R_C and C_C prevent oscillations during reset and their product should be at least 0.02 times R_I X C_I.

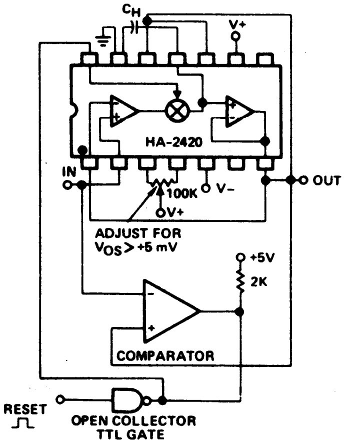
For the simpler integrate and reset function without a hold, substitute an ordinary operational amplifier for the upper device.

APPLICATION NO. 12

This accurate, low drift peak detector circuit combines the basic sample-and-hold connection with a comparator, and will detect 20V p-p signals up to 50kHz.

When the input signal level exceeds the voltage being stored in the S/H, the comparator trips, and a new sample of the input is taken. The S/H offset pot should be adjusted for a slight positive offset, so that the comparator will trip back when the new peak is acquired; otherwise the comparator would remain "on" and the S/H would follow the peak back down.

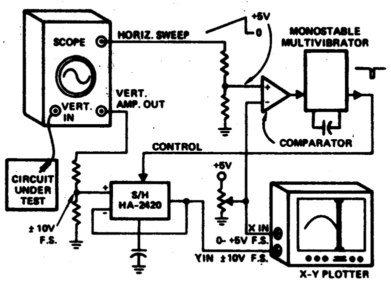
To make a negative peak detector, reverse the comparator inputs, and adjust the S/H for a negative offset.


C_H
V+
HA-2420
IN
100K
V−
V+
OUT
ADJUST FOR
V_{OS}>+5 mV
+5V
2K
COMPARATOR
RESET
OPEN COLLECTOR
TTL GATE

The reset function, which is difficult to achieve in other peak detector circuits, forces a new sample at the instantaneous input level.

APPLICATION NO. 13

Plot High Speed Waveforms With Sampling Techniques


SCOPE
HORIZ. SWEEP
+5V
0
MONOSTABLE MULTIVIBRATOR
VERT. AMP. OUT
VERT. IN
COMPARATOR
CONTROL
CIRCUIT UNDER TEST
±10V F.S.
+5V
S/H HA-2420
X IN
0- +5V F.S.
Y IN ±10V F.S.
X-Y PLOTTER

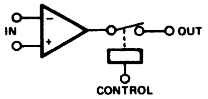
This useful application illustrates how fast repetitive waveforms can be slowed down using sampling techniques. The input signal is much too fast to be tracked directly by the X-Y recorder; but sampling allows the recorder to be driven as slow as necessary.

To operate, the waveform is first synched in on the scope. Then the potentiometer connected to the recorder X input is slowly advanced, and the waveform will be reproduced. The HA-2420 samples for a very short interval once each horizontal sweep of the scope. The sampling instant is determined by the potentiometer at the instant when the horizontal sweep waveform corresponds to the X position of the recorder.

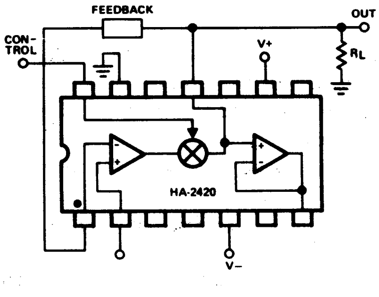
This principle can be applied to many systems for waveform analysis, etc.

APPLICATION NO. 14

Gated Operational Amplifier


IN
OUT
CONTROL

EQUIVALENT CIRCUIT


FEEDBACK
OUT
CON-TROL
V+
RL
HA-2420
V−

The following are a few of the many applications where an operational amplifier followed by a highly efficient analog switch could be used:

- Analog Multiplexer Element
- Gated Oscillator
- Precision Timing Circuit
- Chopper Type Modulator/Demodulator
- Crosspoint Switch Element
- Reset or Initial Conditions Switch
- Gated Comparator
- Automatic Calibration Switch
- Gated Voltage Regulator

APP NOTE

FOR YOUR INFORMATION

No. 519

Harris Analog

OPERATIONAL AMPLIFIER NOISE PREDICTION

By Richard Whitehead

INTRODUCTION

When working with op amp circuits an engineer is frequently required to predict the total RMS output noise in a given bandwidth for a certain feedback configuration. While op amp noise can be expressed in a number of ways, "spot noise" (RMS input voltage noise or current noise which would pass through 1Hz wide bandpass filters centered at various discrete frequencies), affords a universal method of predicting output noise in any op amp configuration.

THE NOISE MODEL

Figure 1 is a typical noise model depicting the noise voltage and noise current sources that are added together in the form of root mean square to give the total equivalent input voltage noise (RMS), therefore:

$$E_{ni} = \sqrt{e_{ni}^2 + I_{ni}^2 R_g^2 + 4KTR_g} \quad \text{where,}$$

E_{ni} is the total equivalent input voltage noise of the circuit.

e_{ni} is the equivalent input voltage noise of the amplifier.

$I_{ni}^2 R_g^2$ is the voltage noise generated by the current noise.

$4KTR_g$ expresses the thermal noise generated by the external resistors in the circuit where $K = 1.23 \times 10^{-23}$ joules/°K; $T = 300^\circ K$ (27°C) and $R_g = \left(\frac{R_1 R_3}{R_1 + R_3}\right) + R2$

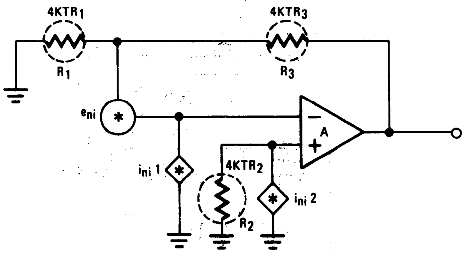


Figure 1

The total RMS output noise (E_{no}) of an amplifier stage with gain = G in the bandwidth between f_1 and f_2 is:

$$E_{no} = G\left(\int_{f1}^{f2} E_{ni}^2 df^{1/2}\right)$$

Note that in the amplifier stage shown, G is the non-inverting gain $\left(G = 1 + \frac{R2}{R1}\right)$ regardless of which input is normally driven.

PROCEDURE FOR COMPUTING TOTAL OUTPUT NOISE

1. Refer to the voltage noise curves for the amplifier to be used. If the R_g value in the application is close to the R_g value in one of the curves, skip directly to step 6, using that curve for values of E_{ni}^2. If not, go to step 2.
2. Enter values of e_{ni}^2 in line (a) of the table below from the curve labeled "$R_g = 0\,\Omega$".
3. From the current noise curves for the

amplifier, obtain the values of i_{ni}^2 for each of the frequencies in the table, and multiply each by R_g^2, entering the products in line (b) of the table.

4. Obtain the value of $4KTR_g$ from Figure 14, and enter it on line (c) of the table. This is constant for all frequencies. The $4KTR_g$ value must be adjusted for temperatures other than normal room temperature.

5. Total each column in the table on line (d). This total is E_{ni}^2.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2					
(b) $I_{ni}^2 R_g^2$					
(c) $4KTR_g$					
(d) E_{ni}^2					

6. On linear scale graph paper enter each of the values for E_{ni}^2 vs. frequency. In most cases, sufficient accuracy can be obtained simply by joining the points on the graph with straight line segments.

7. For the bandwidth of interest, calculate the area under the curve by adding the areas of trapezoidal segments. This procedure assumes a perfectly square bandpass condition; to allow for the more normal -6db/octave bandpass skirts, multiply the upper (-3db) frequency by 1.57 to obtain the effective bandwidth of the circuit, before computing the area. The total area obtained is equivalent to the square of the total input noise over the given bandwidth.

8. Take the square root of the area found above and multiply by the gain (G) of the circuit to find the total Output RMS noise.

A TYPICAL EXAMPLE

It is necessary to find the output noise of the circuit shown below between 1KHz and 24KHz.

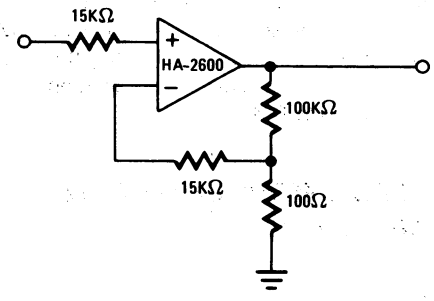
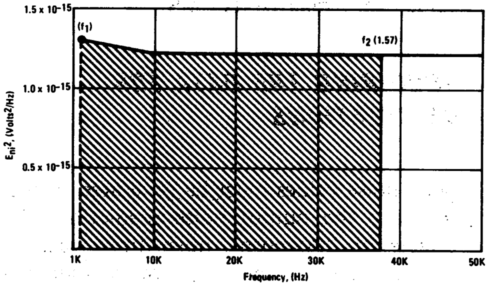


Figure 2
The HA-2600 In a Typical G = 1000 Circuit

Values are selected from Figures 5, 5a and 14 to fill in the table as shown below. An R_g of 30KΩ was selected.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2	3.6×10^{-15}	1.156×10^{-15}	7.84×10^{-16}	7.29×10^{-16}	7.29×10^{-16}
(b) $I_{ni}^2 R_g^2$	9.9×10^{-16}	1.89×10^{-16}	3.15×10^{-17}	7.2×10^{-18}	7.2×10^{-18}
(c) $4KTR_g$	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}
(d) E_{ni}^2	5.09×10^{-15}	1.86×10^{-15}	1.31×10^{-15}	1.23×10^{-15}	1.23×10^{-15}

The totals of the selected values for each frequency is in the form of E_{ni}^2. This should be plotted on linear graph paper as shown below:



HA-2600 Total Equivalent Input Noise Squared

Since a noise figure is needed for the frequency of 1KHz to 24KHz, it is necessary to calculate the effective bandwidth of the circuit. With AV = 60db the upper 3db point is approximately 24KHz. The product of 1.57 (24KHz) is 37.7KHz and is the effective bandwidth of the circuit.

The shaded area under the curve is approximately 45 x 10^{-12} Volts^2; the total equivalent input noise is $\sqrt{E_{ni}^2}$ or 6.7 microvolts, and the total output noise for the selected bandwidth is $\sqrt{E_{ni}^2}$ x (closed loop gain) or 6.7 millivolts RMS.

ACTUAL MEASUREMENTS FOR COMPARISON

The circuit shown below was used to actually measure the broadband noise of the HA-2600 for the selected bandwidth:

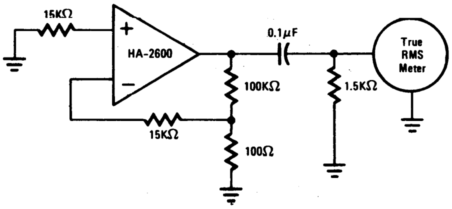


Figure 3
A Typical Test Circuit for Broadband Noise Measurements

The frequencies below the f_1 point of the bandwidth selected are filtered out by the RC network on the output of HA-2600. The measurement of the broadband noise is observed on the true RMS voltmeter. The measured output noise of the circuit is 4.7 microvolts RMS as compared to the calculated value of 6.7 microvolts RMS.

ACQUIRING THE DATA FOR CALCULATIONS

Spot noise values must be generated in order to make the output noise prediction. The effects of "Popcorn" noise have been excluded due to the type of measurement system.

The Quan-Tech Control Unit, model no. 2283 and Filter Unit, model no. 2181 were used to acquire spot noise voltage values expressed in $(V/\sqrt{Hz})$. The test system performs measurements from 10Hz by orders of magnitude to 100KHz with an effective bandwidth of 1Hz at each tested frequency.

Several source resistance (R_g) values were used in the measuring system to reveal the effects of R_g on each type of Harris' op amps and to obtain proper voltage noise values essential for current noise calculations.

A DISCUSSION ON "POPCORN" NOISE

"Popcorn" noise was first discovered in early 709 type op amps. Essentially it is an abrupt step-like shift in offset voltage (or current) lasting for several milliseconds and having amplitude from less than one microvolt to several hundred microvolts. Occurance of the "pops" is quite random — an amplifier may exhibit several "pops" per second during one observation period and then remain "popless" for several minutes. Worst case conditions are usually at low temperatures with high values of R_g. Some amplifier designs and some manufacturer's products are notoriously bad in this respect. Although theories of the popcorn mechanism differ, it is known that devices with surface contamination of the semiconductor chip will be particularly bad "poppers". Advertising claims notwithstanding, the authors have never seen any manufacturer's op amp that was completely free of "popcorn". Some peak detector circuits have been developed to screen devices for low amplitude "pops", but 100% assurance is impossible because an infinite test time would be required. Some studies have shown that spot noise measurements at 10Hz and 100Hz, discarding units that are much higher than typical, is an effective screen for potentially high "popcorn" units.

The vast majority of Harris op amps will exhibit less than 3 µV peak-to-peak "popcorn". Screening can be performed, but it should be noted that the confidence level of the screen could be as low as 60%.

REFERENCES

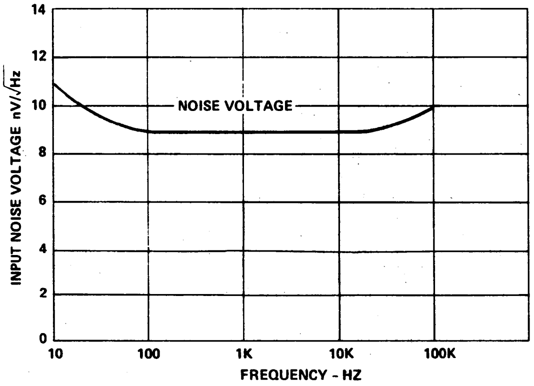
Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design. New York: John Wiley and Sons, 1973.

Instruction Manual, Model 2173C Transistor Noise Analyzer Control Unit. Quan-Tech, Division of KMS Industries. Whippany, New Jersey.

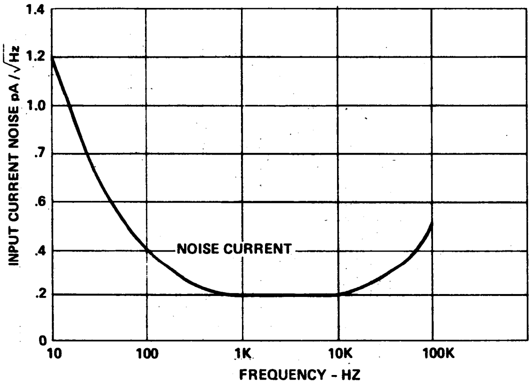
TYPICAL SPOT NOISE CURVES

Unless Otherwise Noted:
$V_S = \pm 15V \quad T_A = +25^{\circ}C$

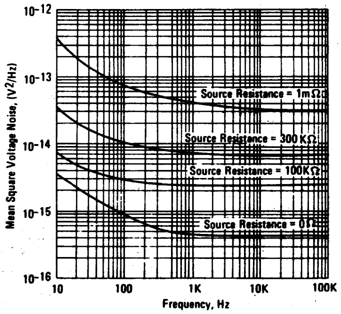
Curve 1
HA-5130/35 INPUT NOISE VOLTAGE



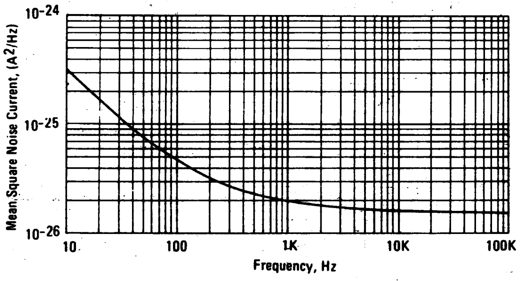
Curve 1A
HA-5130/35 INPUT NOISE CURRENT



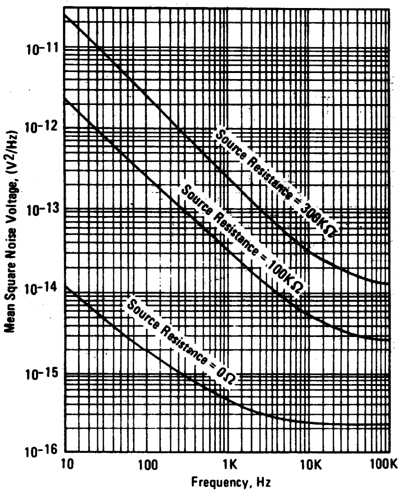
Curve 2
HA-2400 INPUT NOISE VOLTAGE



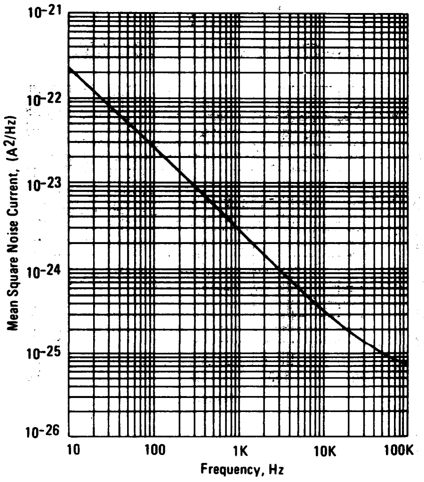
Curve 2A
HA-2400 INPUT NOISE CURRENT



Curve 3
HA-2500/2510/2520 INPUT NOISE VOLTAGE



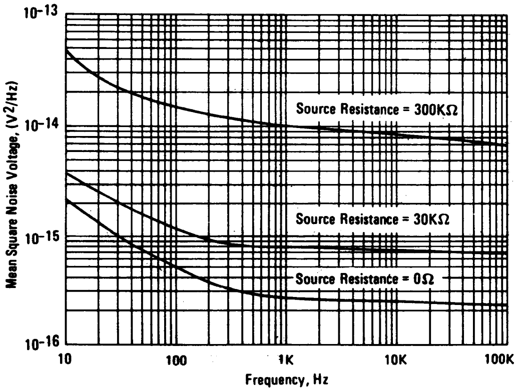
Curve 3A
HA-2500/2510/2520 INPUT NOISE CURRENT



TYPICAL SPOT NOISE CURVES (continued)

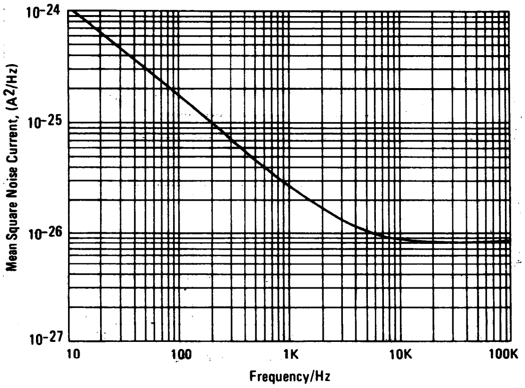
Curve 4

HA-2600/2620 INPUT NOISE VOLTAGE



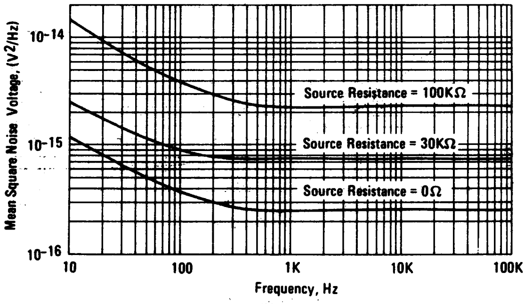
Curve 4A

HA-2600/2620 INPUT NOISE CURRENT



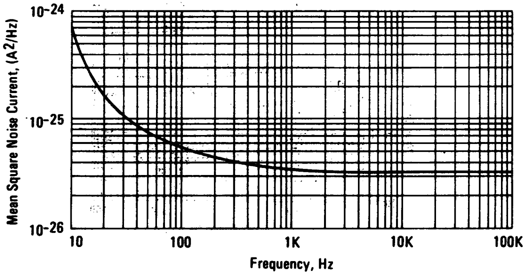
Curve 5

HA-2640/2645 INPUT VOLTAGE NOISE ($V_S = \pm 30V$)



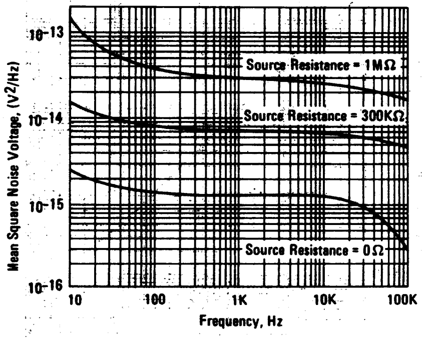
Curve 5A

HA-2640/45 INPUT NOISE CURRENT ($V_S = \pm 30V$)



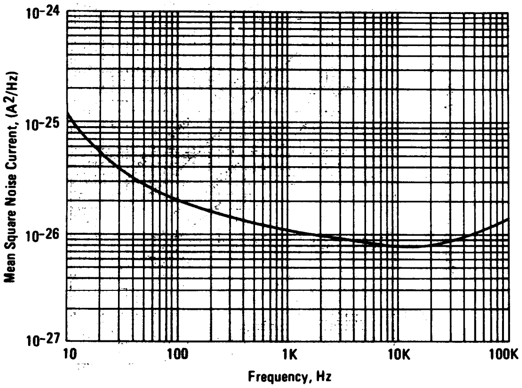
Curve 6

HA-2700 INPUT NOISE VOLTAGE



Curve 6A

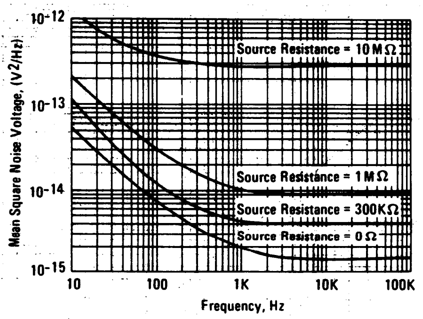
HA-2700 INPUT NOISE CURRENT



TYPICAL SPOT NOISE CURVES (continued)

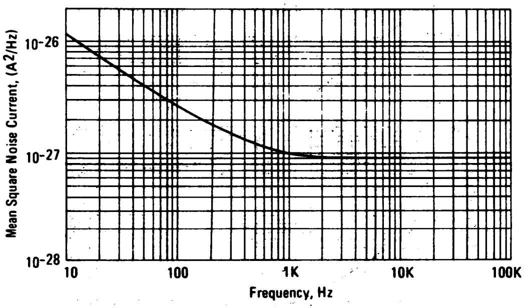
Curve 7

HA-2720/2730 INPUT NOISE VOLTAGE ($I_{SET} = 1\mu A$)



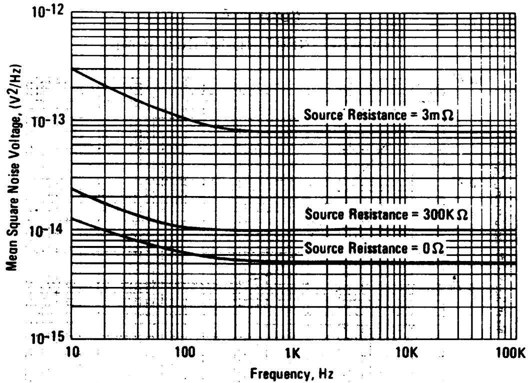
Curve 7A

HA-2720/2730 INPUT NOISE CURRENT ($I_{SET} = 1\mu A$)



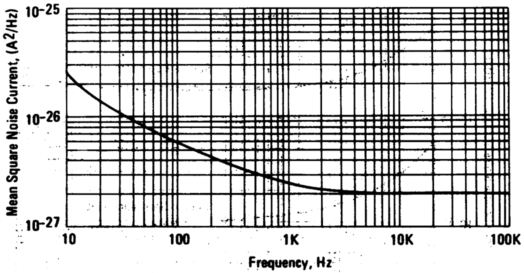
Curve 8

HA-2720/2730 INPUT NOISE VOLTAGE ($I_{SET} = 10\mu A$)



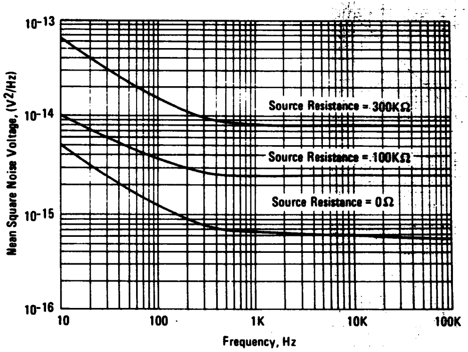
Curve 8A

HA-2720/2730 INPUT NOISE CURRENT ($I_{SET} = 10\mu A$)



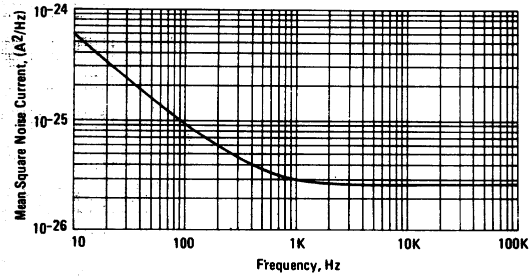
Curve 9

HA-2720/2730 INPUT NOISE VOLTAGE ($I_{SET} = 100\mu A$)



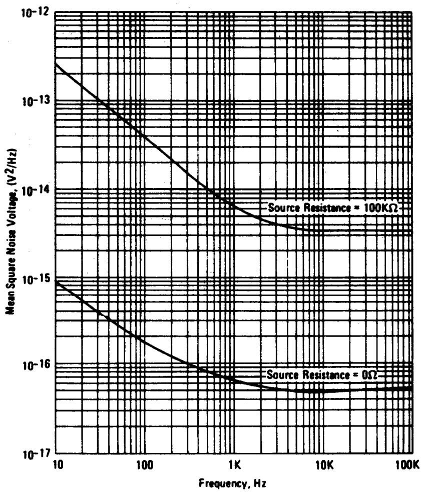
Curve 9A

HA-2720/2730 INPUT NOISE CURRENT ($I_{SET} = 100\mu A$)

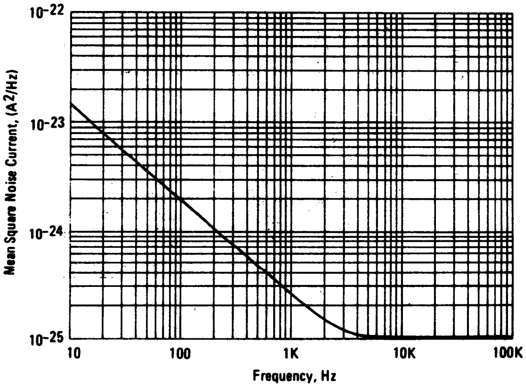


TYPICAL SPOT NOISE CURVES (continued)

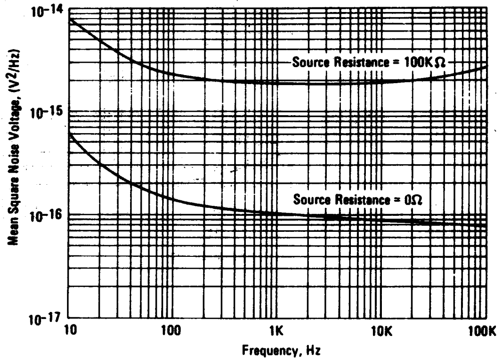
Curve 10
HA-4602/4605 INPUT NOISE VOLTAGE



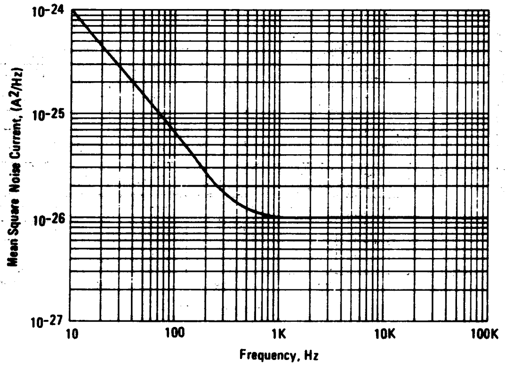
Curve 10A
HA-4602/4605 INPUT NOISE CURRENT



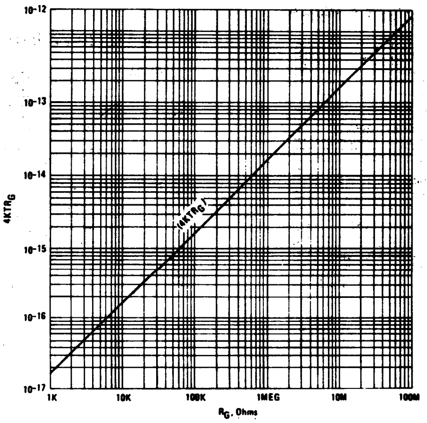
Curve 11
HA-4741 INPUT NOISE VOLTAGE



Curve 11A
HA-4741 INPUT NOISE CURRENT



Curve 12



APP NOTE

FOR YOUR INFORMATION

No. 520

Harris Analog

CMOS ANALOG MULTIPLEXERS AND SWITCHES; APPLICATIONS CONSIDERATIONS

Don Jones and Al Little

Introduction

This article describes several important considerations for the use of CMOS analog multiplexers and switches. It includes selection criteria, parameter definitions, handling and design precautions, interfacing, typical applications, and special topics such as overvoltage protection and R.F. switching. Some other devices which perform analog switching functions are discussed as well.

Application Note 521 is also recommended for the analog multiplexer and switch user. It details the different CMOS processes used by various manufacturers, showing the performance trade-offs and failure modes which may be encountered with each.

Choosing the Right Device

A. Multiplexers: Protected or Unprotected?

Analog input signals which originate externally to a system can be destructive to a multiplexer for several reasons:

1. Analog signals may be present while the MUX power supplies are off.
2. The signal lines may receive induced voltage spikes from nearby sources.
3. Static electricity may be introduced on the signal lines by personnel or equipment.
4. Grounding problems are frequent; A. C. power line voltages at high impedance can appear on the signal lines. Signal lines can be accidentally shorted to other voltage sources.

Each of these situations are common in data acquisition, telemetry, and process control systems. In each case, a voltage at the multiplexer input exceeds the rail voltage. Without current limiting, this voltage will degrade or destroy the device.

Any conventional CMOS multiplexer can be protected against overvoltage destruction by external resistor-diode networks which limit input current to a safe level. Such networks are expensive, however, both in cost and in circuit board space. Another drawback is the output signal corruption that accompanies an overvoltage - regardless of which input is selected. This occurs due to parasitic bipolar transistors within the multiplexer which turn on during overvoltage. (Application Note 521 explains this mechanism in detail).

A few multiplexers feature built-in overvoltage protection, designed to eliminate the external networks. The protection capability varies widely among these devices, however. Some offer very slight advantages over ordinary multiplexers while others withstand wide voltage extremes. Unfortunately, nearly all suffer from the same output signal corruption problem described above.

Harris overvoltage protected multiplexers, HI-506A/507A/508A/509A, are an exception to this rule. During overvoltage, active protection circuitry automatically shuts off the parasitic transistor, thereby preventing output signal contamination. These devices will withstand a continuous voltage on any one input of ±20 Volts greater than either supply (this limitation is due only to temperature rise considerations at maximum ambient) and have withstood simulated static discharge conditions of greater than 4,500 Volts.

It should be emphasized that only the HI-506A through 509A (and exact equivalents from authorized alternate suppliers) will have this kind of protection necessary for inputs from the outside world. Certain CMOS process improvements, such as "floating body" and "buried layer" do help minimize one failure mode (latchup) but will still fail under excess voltage or current conditions prevalent in this type application.

A simplified equivalent circuit of the Harris internal protection network is shown in Figure 1.

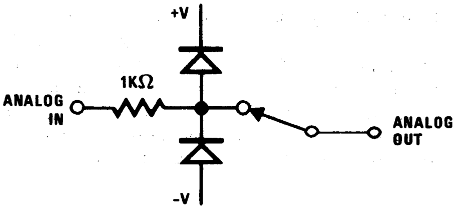


FIGURE 1.

This will help answer the question of what happens when the supplies are turned off, but input signals are present. If the supplies are shorted to ground, then the inputs will have about 1KΩ impedance to ground. If the supplies are open circuit, then the most positive and most negative inputs will act as supplies to the multiplexer.

In normal operating parameters, internally protected multiplexers have one difference from the unprotected versions-ON resistance is necessarily higher because of the added series current limiting resistor. However, to achieve the same degree of protection with conventional devices, the same resistance must be added externally, plus external diodes which would add to the effective leakage currents.

Conventional unprotected multiplexers are suitable for systems where the MUX inputs come from sources within the equipment, such as from op amps powered by the same ±15 volt supplies. The HI-506/507/1818A/1828A are intended for this type system. They are entirely free of any latch-up tendency, which have plagued some other types, even in these more benign applications. They are also free of the performance compromises which have accompanied some attempts to cure the latch-up problem.

B. Which Switch To Switch To?

Harris furnishes a complete line of CMOS analog switches, including replacements for most of the available CMOS and JFET switches. All types feature rugged no-latch-up construction, uniform characteristics over the analog signal range, and excellent high frequency characteristics.

The HI-200 and HI-201 replace the popular, low cost DG200 and DG201 types dual and quad switches.

The HI-1800A is low leakage dual DPST switch with a versatile addressing scheme, allowing use of a single type for many different switching functions.

The HI-5040 through HI-5051 are low resistance types, offering one to four switches in virtually all combinations. These replace the HI-5040 series with significantly better performance, and with both 75 ohm and 30 ohm switches available in all configurations. These are also plug-in replacements for many of the DG180 and DG190 series of FET hybrid switches, offering the advantage of monolithic construction, but with slightly longer switching times.

The analog switches do not contain overvoltage protection on the analog inputs, although they will withstand inputs 2 or 4 volts greater than the supplies. External current limiting should be provided if higher overvoltages are anticipated, such as a resistor in series with the analog input of value: $R(\text{ohms}) \geq (V_{IN} - V_{SUPPLY}) \times 50$ where VIN is the maximum expected input voltage. All digital inputs do have overvolgate/static charge protection.

Data Sheet Definitions

A. Absolute Maximum Ratings

As with all semiconductors, these are maximum conditions which may be applied to a device (one at a time) without resulting in permanent damage. The device may, or may not, operate satisfactorily under these conditions - conditions listed under "Electrical Characteristics" are the only ones guaranteed for satisfactory operation.

B. V_S, Analog Signal Range

The input analog signal range over which reasonable accurate switching will take place. For supply voltages lower than nominal, V_S will be equal to the voltage span between the supplies. Note that other parameters such as R_{ON} and leakage currents are guaranteed over a smaller input range, and would tend to degrade towards the V_S limits. All Harris devices can withstand $+V_S$ applied at an input while $-V_S$ is applied to the output (or vice-versa) without switch breakdown - this is not true for some other manufacturers' devices.

C. R_{ON}, On Resistance

The effective series on-switch resistance measured from input to output under specified conditions. Note that R_{ON} changes with temperature (highest at high temperature) and to a lesser degree with signal voltage and current.

D. I_S(OFF), I_D(OFF), I_D(ON): Leakage Currents

Currents measured under conditions illustrated on the data sheet. Harris prefers to guarantee only worstcase high temperature leakages, because room temperature picoampere levels are virtually impossible to measure repeatable on available automated test equipment. Even under laboratory conditions, fixture and test equipment stray leakages may frequently exceed the device leakage. Leakages tend to double every 10°C temperature rise, so it is reasonable to assume that the +25°C figure is about 0.001 times the +125°C measurement; however, in some cases there may be ohmic leakages, such as on the package surface, which would make the +25°C reading higher than calculated.

Each of these leakage figures is the algebraic sum of all currents at the point being measured: to each power supply, to ground, and through the switches; so the current direction cannot be predicted. In making an error analysis it should be assumed that all leakages are in the worst-case direction.

In most systems, I_D(ON) has the most effect, creating a voltage offset across the closed switch equal to $I_D(ON) \times R_{ON}$.

E. V_{AL}, V_{AH}; Input Thresholds

The lower and upper limits for the digital address input voltage at which the switching action takes place. All other parameters will be valid if all "0" addressd inputs are less than V_{AL} and all "1" inputs are greater than V_{AH}. Logic compatibility will be discussed in detail later in this paper.

F. I_A, Input Leakage Current

Current at a digital input, which may be in either direction. Digital inputs on Harris devices are similar to CMOS logic inputs; connection to MOS gates through resistor-diode protection networks. Unlike some other devices there is no DC negative resistance region which could create an oscillating condition.

G. T_A, T_{ON}, T_{OFF}; Access Time

The logic delay time plus output rise time to the 90% point of a full scale analog output swing. After this time the output will continue to rise, approaching the 100% point on an exponential curve determined by R_{ON} x C_D(OFF).

H. T_{OPEN}, Break-Before-Make Delay

The time delay between one switch turning OFF and another switch turning ON; both switches being commanded simultaneously. This prevents a momentary condition of both switches being ON, generally a very minor problem.

I. C_S(OFF), C_D(OFF), C_D(ON) Input/Output Capacitance

Capacitance with respect to ground measured at the analog input/output terminals. C_D(ON) is generally the sum of C_S(OFF) and C_D(OFF). C_D(OFF) is usually the most important term as rise time/settling characteristics are determined by R_{ON} x C_D(OFF), as well as the high frequency transmission characteristics.

J. C_{DS}(OFF), Drain to Source Capacitance

The equivalent capacitance shunting an open switch.

K. OFF Isolation

The proportion of a high frequency signal applied to an open switch input appearing at the output:

$$\text{off isolation} = 20 \log \frac{V_{IN}}{V_{OUT}}$$

This feedthrough is transmitted through C_{DS}(OFF) to a load composed of C_D(OFF) in parallel with the external load. The isolation generally decreases by 6dB/octave with increasing frequency.

L. C_A, Digital Input Capacitance

Capacitance to ground measured at digital input. This chiefly affects propagation delays when driven by CMOS logic.

M. P_D, Power Dissipation: I+, I-

Quiescent power dissipation, $P_D = (V+ \times I+) + (V- \times I-)$. This may be specified both operating and standby ("Enable" pin ON/OFF). Note that, as with all CMOS devices, dissipation increases with switching frequency; but that Harris devices exhibit much less of this effect.

Care And Feeding of Multiplexers And Switches

Dielectrically isolated CMOS ICs require no more care in handling and use than any other semiconductor - bipolar or otherwise. However, they are not indestructible, and reasonable common sense care should be taken.

In a laboratory breadboard, power should be shut off before inserting or removing any IC. It is especially important that supply lines have decoupling capacitors to ground permanently installed at the IC socket pins, as intermittent supply connections can create high voltage spikes through the inductance of a few feet of wire.

Because each of the major manufacturers of CMOS multiplexers and switches uses a radically different process, it is urged that units from all prospective suppliers be equally tested in breadboards and prototypes. It will be interesting to note which types survive best the hazards of a few weeks of breadboard testing.

Particular care of semiconductors during incoming inspection and installation is quite important, because the cost of reworking finished assemblies with even a small percentage of preventable failures can seriously erode profits. All equipment should be periodically inspected for proper grounding. With these devices, it is not usually necessary to shackle personnel to the nearest water pipe, if reasonable attention is paid to clothing and floor coverings; but be alert for periods of unusually high static electricity. If special lines are already set up for handling MOS devices, it wouldn't hurt to use them.

There are a few good rules for P.C. card layout:

1. Each card or removable subassembly should contain decoupling capacitors for each supply line to ground. This not only helps keep noise away from the analog lines, but gives good protection from static electricity damage when loose cards are handled.
2. When digital inputs come through a card connector, the pull-up resistor should be at the CMOS input. This forces current through the connector and prevents possible dry circuit conditions (see following discussion on digital interface).
3. All unused digital inputs must be tied to logic "0" (ground) or logic "1" (logic supply or device + supply) depending on truth table and action desired. Open inputs tend to oscillate between "0" and "1". It would also be best to ground any unused analog inputs/outputs and any uncommitted device pins.

Digital Interface

A. Reference Connection

HI-5040 thru HI-5051 and HI-1800A/1818A/1828A require a connection to the digital logic supply (+5V to +15V).

The HI-200/201/506A/507A have V_{REF} pins which are normally left open when driving from +5 volt logic (DTL or TTL), but may be connected to higher logic supplies (to +15V) to raise the threshold levels when driving from CMOS or HNIL. The HI-200/201 will have significantly lower power dissipation when V_{REF} is connected to a high level supply.

The HI-506/507/508A/509A do not have V_{REF} terminals, but will operate reliably with any logic supplied from +5 to +15 volts.

B. DTL/TTL Interface

One major difference found in comparisons of similar devices from different manufactures is the worst-case digital input high threshold (V_{AH} or V_{IH}). These range anywhere from +2V to +5V; and anything greater than +2.4V is obviously not compatible with worst-case TTL output levels. The fact is that no CMOS input is truly TTL compatible unless an external pull-up resistor is added. TTL output stages were not designed with CMOS loads in mind.

The experienced designer will always add a pull-up resistor from CMOS input to the +5 volt supply when driving from TTL/DTL:

1. Interchangeability: allows substitution of similar devices from several manufacturers.
2. Noise immunity: a TTL output in the "high" condition can be quite high impedance. Even when voltage noise immunity seems satisfactory, the line is quite susceptible to induced noise. The pull-up resistor will reduce the impedance while increasing voltage noise immunity.
3. Compatibility: one manufacturer does guarantee +2.0 volt minimum V_{AH}. However, this is accomplished with circuitry that is anything but TTL compatible: input current vs. voltage shows an abrupt positive then negative resistance region which is not the kind of load recommended for an emitter follower stage. A pull-up resistor will swamp out the negative resistance. Other CMOS inputs capacitively couple internal switching spikes to the input which could cause double-triggering without the pull-up resistor.
4. Reliability: it shouldn't happen with carefully processed ICs, but any possible long term degradation of CMOS devices usually involves threshold voltage shifts. The pull-up resistor will help maintain operation if input thresholds drift out of spec. On units without adequate input protection, the resistor will also help protect the device when a loose P.C. card is handled. Where the interface goes through a P.C. connector, the resistor will force current through the connector to break down any insulating film which otherwise might build up and cause erratic dry circuit operation.

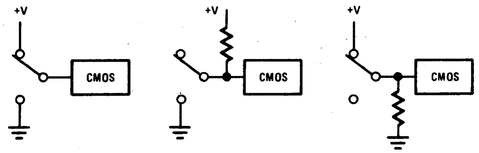
A 2K ohm resistor connected from the CMOS input to the +5 volt supply is adequate for any TTL type output. If power consumption is critical, open collector TTL/DTL should be used, allowing a higher value resistor - the voltage drop across the resistor is computed from the sum of specified "1" level leakage currents at the TTL output and CMOS input.

C. CMOS Interface

The digital input circuitry on all Harris devices is identical to series 4000 and 54C/74C logic inputs, and is compatible with CMOS logic with supplies between +5V and +15V without external pull-up resistors.

D. Electromechanical Interface

When driving inputs from mechanical switches or relays, either a pull-up or pull-down resistor must be connected at the CMOS input to clear the dry circuit and damp out any spikes, as illustrated in Figure 2, (b) and (c).



(a) POOR **(b) GOOD** **(c) GOOD**

FIGURE 2.

A Practical Multiplexer Application

Figure 3 illustrates a practical data acquisition system hookup using an analog multiplexer, a monolithic sample-and-hold and an A/D converter. The HA-2420/2425 sample-and-hold is a particularly good choice for this type application because it eliminates the need for a separate high impedance, high slew rate buffer amplifier. Its acquisition time is consistent with CMOS multiplexer settling times and most available A/D conversion times. Errors, after initial adjustment, are consistent with up to 12 bit absolute accuracy over a wide temperature range.

A. Accuracy

D.C. error sources include:

1. Multiplexer:
   a. input offset = R source x I_S(OFF)
   b. output offset = R(ON) x (I_D(ON) + I bias (S/H)
2. Sample-and-Hold
   a. input offset voltage
   b. charge injection; sample-to-hold offset
   c. gain error during "hold"
   d. drift during hold
3. A/D converter:
   a. linearity
   b. gain drift
   c. offset drift

Item 1(a) and (b), and 2(d) become significant only at very high temperatures. 2(a) and (b) are initially adjusted out with the offset adjustment pot on the S/H. 2(c) is usually adjusted out by A/D gain adjustment, but could also be removed by a voltage divider feedback on the S/H to give a slightly greater than unity gain during "sample". After initial adjustments, typical S/H errors are less than 0.5mV over 0°C to +75°C. Note that after adjustment, there may be an appreciable offset at the S/H output when switching from sample to hold. This is not a problem, since accuracy is required only during "hold", and the system is adjusted for this.

The largest system errors are usually 3(b) and (c), drifts with temperature and time. If two multiplexer channels can be dedicated for stable (+) and (-) reference voltage inputs, then the data processor can continuously calibrate the system, effectively removing all errors, except 1(a) and 3(a) which are usually negligible.

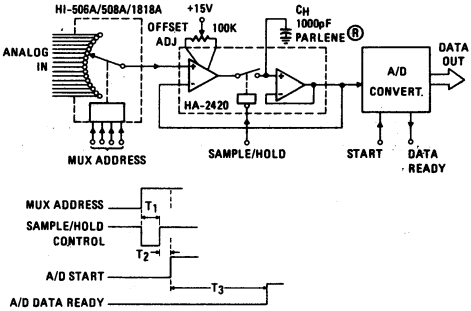


FIGURE 3.

B. Timing

The timing diagram in Figure 3 indicates the necessary system delays for each multiplexer address:

T_1 is the combined acquisition time for the multiplexer and S/H.
T_2 is the short interval required for the sample-to-hold transient to settle.
T_3 is the A/D conversion time.

The following table indicates minimum recommended timing for ±10 volt input range for acquisition/settling times to ½ LSB accuracy:

	T_1	T_2
10 bit:	6μs	1μs
12 bit:	12μs	2μs

The multiplexer, by itself, requires about 2μs and 9μs settling to 10 bit and 12 bit accuracy, respectively; but fortunately this can be concurrent with S/H acquisition time. This is longer than would be predicted by the R_{ON} C_D time constant; probably because of internal distributed capacitance, a rather long period is required to traverse the last few millivolts towards the final value.

It should be noted that impedance conditions at the multiplexer inputs can affect the necessary acquisition time. At the instant the multiplexer switches from one channel to a new one, there is appreciable current pulled through the new channel input in order to charge C_D from its old level to its new level. This can cause ringing on signal lines, or glitches at signal conditioning amplifier outputs which require longer periods to settle. It is best for signal conditioning amplifiers to be wide band types, such as HA-5170, so that their high frequency output impedance is low and recovery from load transients is fast; even though the signal to be measured is very low bandwidth.

The T_1 and T_2 times could be eliminated by alternating two S/H circuits, acquiring a new signal on the second while A/D conversion is taking place. The two S/H circuits would have inputs connected together, and outputs alternately connected to the A/D by an analog switch. Total time, then, would be T_3 plus the analog switch settling time.

If the MUX input channels are sequentially switched, each channel will be sampled at a rate of:

$$FS = \frac{1}{N(T_1 + T_2 + T_3)}$$

samples per second, where N is the number of channels. The frequency spectra of the input signals must then be no higher than $\frac{FS}{2}$.

In many systems, however, each channel carries a different maximum frequency of interest, and it may be desirable to depart from simple sequential scanning. Quickly varying signals, for example, could be addressed several times during a scanning period.

C. Adding Channels

For more than sixteen channels, several multiplexers may be tied together at the outputs, and addressed in parallel, but with only one "enabled" at a time. The MUX output offset will be increased, since I_D (OFF or ON) is additive. Also, output capacitance, C_D, is additive, creating increased access times.

These errors can be minimized in large systems by having several tiered levels of multiplexing; where the outputs of a number of MUXs are individually connected to the inputs of another MUX.

D. Differential Multiplexing

When low level analog signals must be conducted over a distance, it is generally better, from a noise pickup standpoint, to use a balanced transmission line carrying signals which are differential with respect to ground.

A dual multiplexer is used for this purpose, as shown in Figure 4. Two sample-and-hold circuits plus an op amp form a high impedance differential sample-and-hold with gain. At gains greater than 4, the minimum sampling time (T_1 in previous example) must be increased proportionately to gain to allow for overdamped settling characteristics.

When handling low level, or high impedance signals, consideration should be given to adding signal conditioning amplifiers at the signal sources, since this can often produce less troublesome, more accurate, lower cost systems.

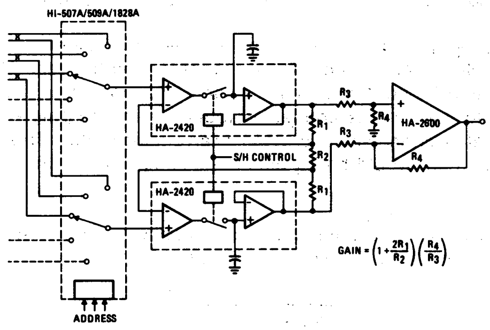


FIGURE 4.

E. Demultiplexing

Since the switches in a CMOS MUX conduct equally well in either direction, it is perfectly feasible to use it as a single input-selected multiple output switch. Figure 5 illustrates its use as a demultiplexer, with capacitors to hold the output signal between samples. When the address lines are synchronous with the address of the original multiplexer, the output lines will create the original inputs, except level changes will be in steps.

Overvoltage protection is not effective with signals injected at the normal MUX output, so an external network should be added, if necessary.

A more accurate demultiplexer could be constructed using the HA-2420/2425 sample-and-hold for each channel, connecting inputs together and sampling each channel sequentially.

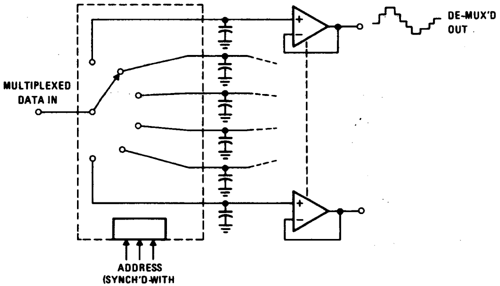


FIGURE 5.

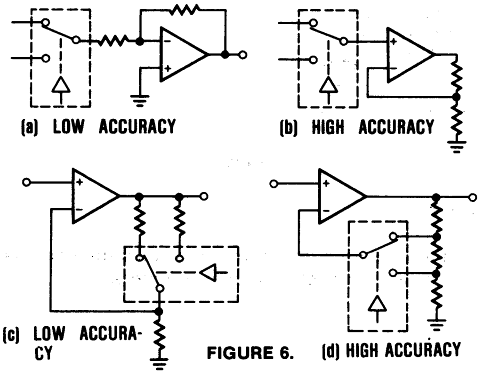
Analog Switch Applications

A. High Current Switching

Analog switches are sometimes required to conduct appreciable amounts of current, either continuous, or instantaneous - such as charging or discharging a capacitor. For best reliability, it is recommended that instantaneous current be limited to less than 80mA peak and that average power over any 100 millisecond period be limited to $I^2R_{ON} \leq$ (absolute maximum derated power-quiescent power). Note that R_{ON} increases at high current levels, which is characteristic of any FET switch. Switching elements may be connected in parallel to reduce R_{ON}.

B. Op Amp Switching Applications

When analog switches are used either to select an op amp input, or to change op amp gain, minor circuit rearrangements can frequently enhance accuracy. In Figure 6(a), R_{ON} of the input selector switch adds to R_1, reducing gain and allowing gain to change with temperature. By switching into a noninverting amplifier (b), gain change becomes negligible. Similarly, in a gain switching circuit, R_{ON} is part of the gain determining network in (c), but has negligible effect in (d).



(a) LOW ACCURACY (b) HIGH ACCURACY

(c) LOW ACCURACY (d) HIGH ACCURACY

FIGURE 6.

C. Switching Spikes And Charge Injection

Transient effects when turning a switch off or on are of concern in certain applications. Short duration spikes are generated (Figure 7(a)) as a result of capacitive coupling between digital signals and the analog output. These have the effect of creating an acquisition time interval during which the output level is invalid even when little or no steady state level change is involved. The total net energy (charge injection) coupled to the analog circuit is of concern when switching the voltage on a capacitor, since the injected charge will change the capacitor voltage at the instant the switch is opened (Figure 7(b)).

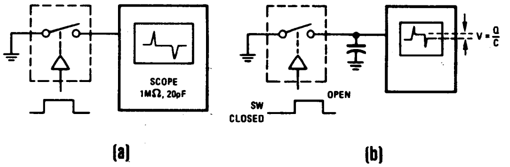


FIGURE 7.

Charge injection is measured in picocoulombs; the voltage transferred to the capacitor computed by

$$V = \frac{\text{Charge (pC)}}{\text{Capacitance (pF)}}$$

Both of these effects are, in general, considerably less for CMOS switches than for equivalent resistance JFET or PMOS devices, since the gate drive signals for the two switching transistors are of opposite polarity. However, complete cancellation is not possible, since the N and P channel switches do not receive gate signals quite simulaneously, and their geometrics are necessarily different to achieve the desired D.C. resistance match.

In applications where transients create a problem, it is frequently possible to minimize the effect by cancellation in a differential circuit, similar to Figure 8.

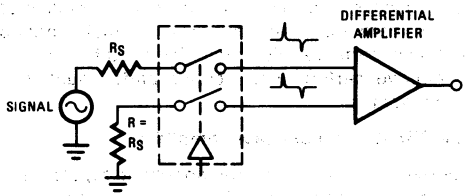


FIGURE 8.

Among the Harris analog switches, the HI-201 is the best from the transient standpoint, having turn-on spikes of about 100mV peak, 50ns width at the 50% point, and charge injection at turn-off of about 20 picocoulombs. Transients of the HI-5040 series are several times higher.

D. High Frequency Switching

When considering a switching element for R.F. or video type information, two factors must be watched: attenuation vs. frequency characteristics of an ON switch, and feedthrough vs. frequency characteristics of the OFF switch. Optimizing the first characteristic requires a low $R_{ON} \times C_D$ product, and the second a low value of C_{DS} (OFF).

One approach is to use the 30 ohm switch types of the HI-5040 series.

Figure 9 illustrates three circuit configurations; (a) is a simple series switch, (b) is a series-shunt configuration to reduce feedthrough, and (c) is a SPDT selector configuration with series-shunt elements. A 1K ohm load is illustrated, which might be the input impedance of a buffer amplifier; a lower load resistance would improve the response characteristics, but would create greater losses in the switch and would tend to distort high level signals.

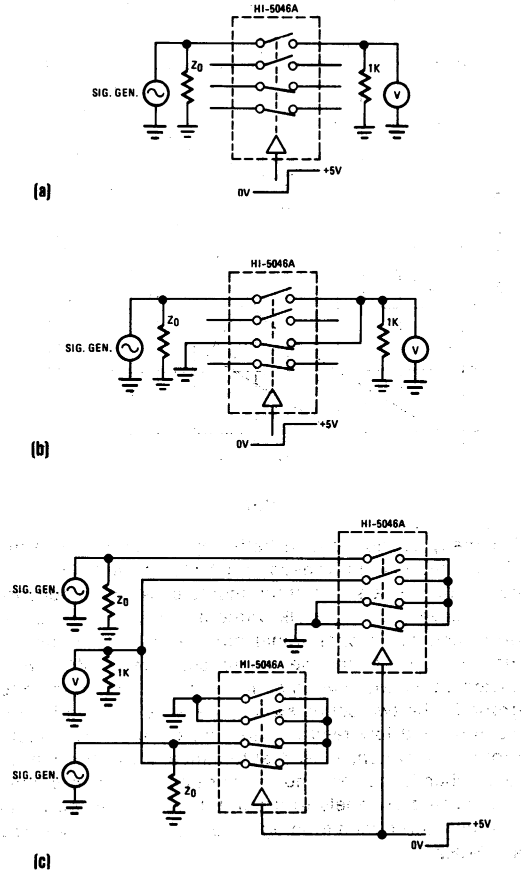


FIGURE 9.

Figure 10 shows ON and OFF frequency response for each of the above configurations. Arbitrarily, we will define useful frequency response as the region where ON losses are less than -3dB and OFF isolation is greater than -40dB.

The simple configuration (a) has excellent ON response, but OFF isolation limits the useful range to about 1MHz (the data sheet indicates -80dB isolation at 100kHz, but this is measured with 100 ohms load, which acounts for the 20dB difference).

The circuit in (b) shows a good improvement in isolation produced by the low impedance of the shunt switch. The useful range is about 10MHz; which could also be achieved in a simple SPDT 2-switch selector if source impedances are very low.

The selector switch in (c) has excellent characteristics, both ON and OFF curves indicating 40MHz useful response. Additional switches connected to the same point would reduce the ON response because of added shunt capacitance; but this could be eliminated by feeding separate summing amplifier inputs.

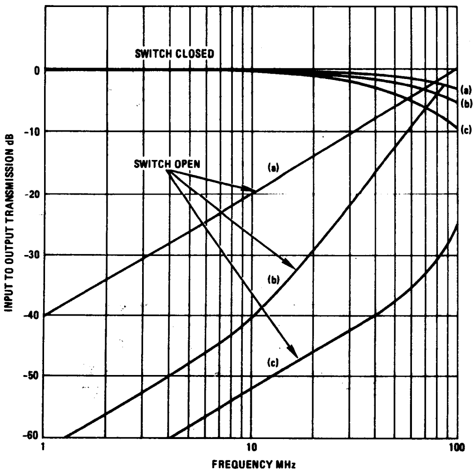


FIGURE 10.

For many applications, a better approach is to use the HI-524 monolithic wideband CMOS multiplexer. This device utilizes a series-shunt multiple switching network to achieve low crosstalk without sacrificing or compromising other operational parameters. As shown in Figure 11, each channel comprises three CMOS FET switch gates, with two in series and the third shunted to ground. The two series switches ensure both a high off isolation and low feed-through capacitance. The shunt grounding switch, closed automatically by the control logic when its corresponding series pair are open, shunts nonselected channels to ground, thus minimizing cross talk. With this circuit topology, crosstalk is typically -60dB at 10MHz.

A buffer amplifier is used with the HI-524 for high frequency applications, due to its higher ON resistance, and should offer sufficient bandwidth and slew rate to avoid degradation of the anticipated signals. For video switching, the HA-5033 and HA-2542 offer good performance plus ±100mA output current for driving coaxial cables. For general wideband applications, the HA-2541 offers the convenience of unity gain stability plus 90ns settling (to ±0.1%) and ±10V output swing. Also, the HI-524 includes a feedback resistance for use with the HA-2541. This resistance matches and tracks the channel ON resistance, to minimize offset voltage due to the buffer's bias currents.

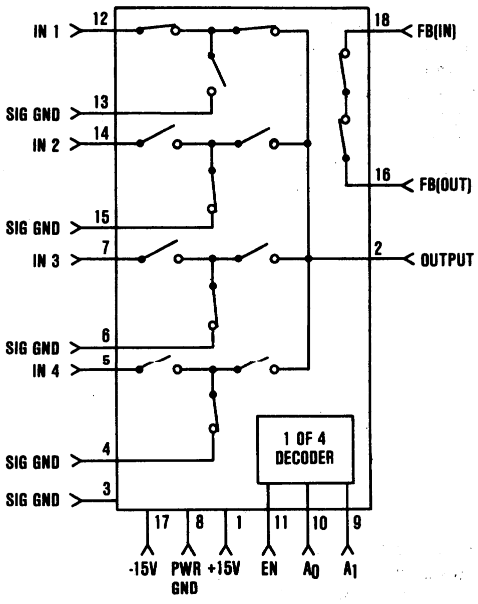


FIGURE 11.

Careful layout is, of course, important for high frequency switching applications to avoid feedthrough paths or excessive load capacitance.

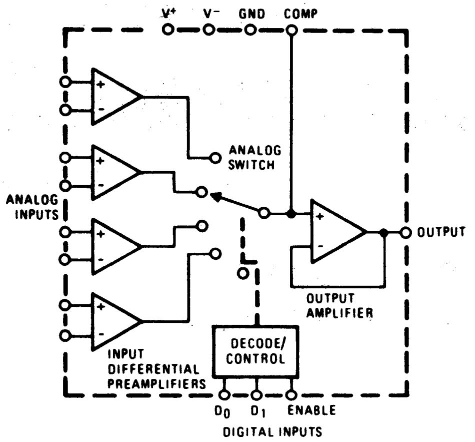
Alternatives to CMOS Switches and Multiplexers

CMOS devices are excellent in many applications. However, there are some other devices which merit consideration in certain analog switching circuits where they may improve performance, reduce parts count, or be more economical.

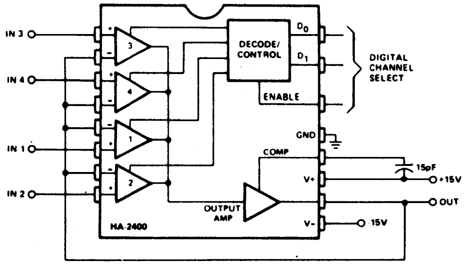
A. The PRAM, Programmable Amplifier

The HA-2400/2405 is a unique monolithic bipolar circuit which combines analog switching with high performance operational amplifiers. It basically consists of four op amp type input stages, any one of which is connected to a single output by bipolar switches controlled through a TTL compatible address decoder. In a single package, it contains the equivalent of 5 op amps plus a 4 channel multiplexer. It has literally hundreds of applications in signal selection and programmable signal conditioning.

Figure 12 illustrates a four channel multiplexer. Connections from the output to each input stage are always the same as a comparable op amp circuit; the +1 gain connection is illustrated.


V+
V-
GND
COMP
ANALOG SWITCH
ANALOG INPUTS
OUTPUT
OUTPUT AMPLIFIER
DECODE/ CONTROL
INPUT DIFFERENTIAL PREAMPLIFIERS
D0
D1
ENABLE
DIGITAL INPUTS

(a) FUNCTIONAL DIAGRAM


IN 3
IN 4
IN 1
IN 2
DECODE/ CONTROL
D0
D1
ENABLE
DIGITAL CHANNEL SELECT
GND
COMP
15pF
V+
+15V
OUT
OUTPUT AMP
HA-2400
V-
15V

(b) ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

FIGURE 12.

Advantages over a comparable CMOS multiplexer circuit areas follows:

1. High input impedance (10^{12} ohnms), low output impedance (<0.1 ohm) means than ON resistance and leakage currents are no longer of concern. There is negligible transient loading of input lines.
2. Gain filtering, etc. can easily be added with feedback networks.
3. Fast acquistion (1.5μs).
4. Wide bandwidth (8MHz).
5. Superior feedthrough characteristics (-110dB at 10kHz, -60dB at 1MHz).

Disadvantages include:

1. Less accuracy for low level D.C. signals; the offset voltages of each input stage do not necessarily match or track each other.
2. Cannot be used in reverse as a demultiplexer.
3. Disabling the device (enable pin low) does not open the output line, or drive the output to zero. Adding channels may be accomplished by tying compensation pins together.

Figure 13 illustrates the PRAM used as a programmable gain amplifier. Any connection possible with op amps can be wired 4 ways to make programmable active filters, oscillators, etc., etc. Harris Application Note 514 shows many possibilities.

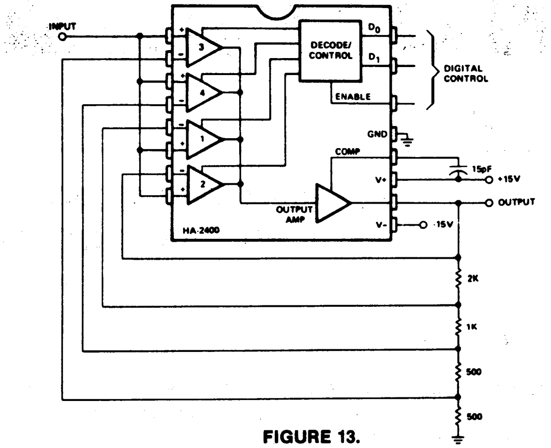

INPUT
DECODE/ CONTROL
D0
D1
DIGITAL CONTROL
ENABLE
GND
COMP
15pF
+15V
V+
OUTPUT
OUTPUT AMP
HA-2400
V-
-15V
2K
1K
500
500

FIGURE 13.
AMPLIFIER, NONINVERTING PROGRAMMABLE GAIN

B. Sample-And-Hold

The sample-and-hold function has often been accomplished with separate analog switches and op amps. These designs always involve performance tradeoffs between acquisition time, charge injection, and droop rate.

The HA-2420/2425 monolithic sample-and-hold, illustrated previously in Figure 3 has many times better tradeoffs, usually at a lower total cost than the other approaches. The switching element is a complementary bipolar circuit with feedback which allows high charging currents (30mA), low charge injection (10pC), and ultra low OFF leakage current (5pA); a combination not approached in any other electronic switch. These factors make it also superior as an integrator reset switch, or as a precision peak detector as shown in Figure 14. Harris Application Note 517 illustrates many other applications.

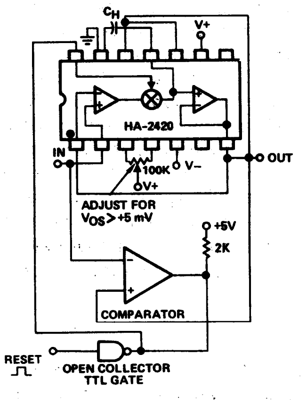

C_H
V+
HA-2420
IN
OUT
100K
V-
V+
ADJUST FOR V_{OS}>+5 mV
+5V
2K
COMPARATOR
RESET
OPEN COLLECTOR TTL GATE

FIGURE 14.

APP NOTE

FOR YOUR INFORMATION

No. 521

Harris Analog

GETTING THE MOST OUT OF CMOS DEVICES FOR ANALOG SWITCHING JOBS

By: Ernie Thibodeaux
and Al Little

Introduction

CMOS analog switches and multiplexers are now widely used for a broad range of applications. They offer low power consumption, low on-resistance, and will conduct a signal in either direction. In addition, CMOS switch structures exhibit no DC offset voltage and can usually handle signals up to the supply rails.

Not all CMOS analog switches are alike, however. Different technologies are employed by different manufacturers. Some types, handicapped by inherent process limitations, can create significant problems for the user. Switches built with older types of junction isolation, for example, can literally self-destruct when a latch-up condition occurs. To prevent destruction, costly external protective circuits are needed, but the devices can still latch up unless the power is turned on and off in a set sequence. Switch circuits can also be destroyed by electrostatic discharge, input overvoltage spikes and power supply transients.

Newer types of technologies include latch-proof junction isolation (JI), floating-body junction isolation, and dielectric isolation (DI). Both JI techniques are conventional processes that have been slightly modified to alleviate the old problem of latch-up. However, both of these JI technologies still require costly external protection circuits to guard against burn-out in such applications as analog-signal multiplexing that interface them with the outside world. That is why JI devices are best suited for internal-switching applications, where the electrical environment can be controlled. In contrast, the improved DI technology, by virtue of its construction, offers analog-switching devices suitable for many inside applications, as well as providing on-board analog protection for devices that interface with the other circuits. Happily, the smaller substrate area of the DI device delivers a better speed-power product than the JI technology.

The Basic CMOS Switch

The basic CMOS transistor (Figure 1) has parasitic junctions that are reverse-baised during normal operation. However, certain overvoltage conditions can forward-bias these junctions to cause high currents that could possibly destroy the devices.

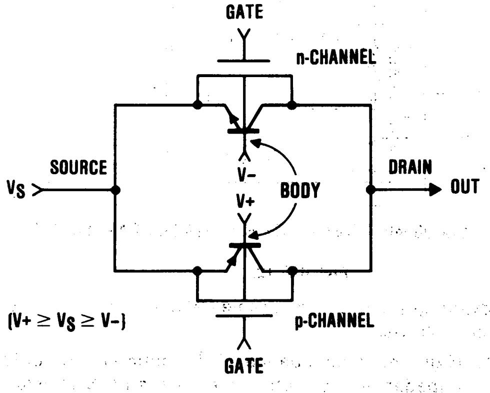


FIGURE 1. BAD

In the basic CMOS analog switch, the parasitic junctions are reversed-biased during normal operation. Large overvoltages, however, make them forward-biased and draw large currents.

The parasitic junctions are actually npn and pnp transistors that are normally reverse-biased by the applied body potentials. However, because many analog switches, and especially multiplexers, are connected to their analog sources through long lines, they are highly susceptible to externally induced voltage spikes. For example, these spikes, which can often exceed the p-channel body potential, V+, can inadvertently turn on a normally off switch through the parasitic pnp transistor (Figure 1).

The n-channel device is similarly affected when the parasitic npn transistor is turned on by a negative overvoltage. This action, commonly known as channel interaction, causes momentary channel-to-channel shorting, which introduces significant errors in the system. This intermittent condition is rarely isolated because it occurs only randomly.

One of the adverse effects of channel interaction is illustrated in Figure 2. Channel 1 of an analog multiplexer is selected when all other channels are off. Channel 16 receives an input-noise spike that momentarily exceeds the positive supply. The sequence causes channel 1 read-out to be +16V because of interaction with channel 16 just before initiating the hold command to the sample-and-hold device. To prevent this annoyance requires additional protective circuits that clamp each channel input to a voltage below the threshold of the parasitics to ensure that the channels remain inactive under any conditions.

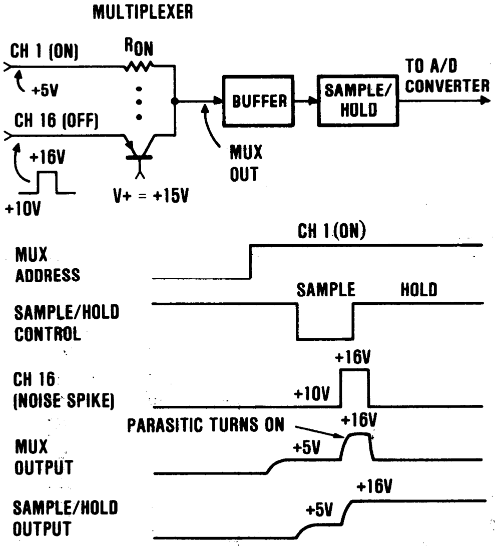


FIGURE 2. WORSE

With CMOS devices, noise spikes can cause channel interaction. In this multiplexer, although channel 1 is only one selected, noise spikes cause cross talk in channel 16, which affects reading.

A more serious condition exists when the substrates (p- or n-) lose their respective potentials to ground (Figure 3) -a condition that occurs when power to the device is turned off while the analog signals are still present. In this situation, the analog switch, which at that point represents a diode connected through the low impedance of the supply, draws high current from the analog source.

This current turns on the switch through its parasitics and shorts all channels to the output. These shorts can easily be catastrophic in multiplexer systems that have different power supplies for the analog source and the multiplexer switch. An error during troubleshooting or an inadvertent supply glitch can trigger this fault mode and destroy the whole system. Therefore, there is obviously much more to system reliability than having latch-proof CMOS devices.

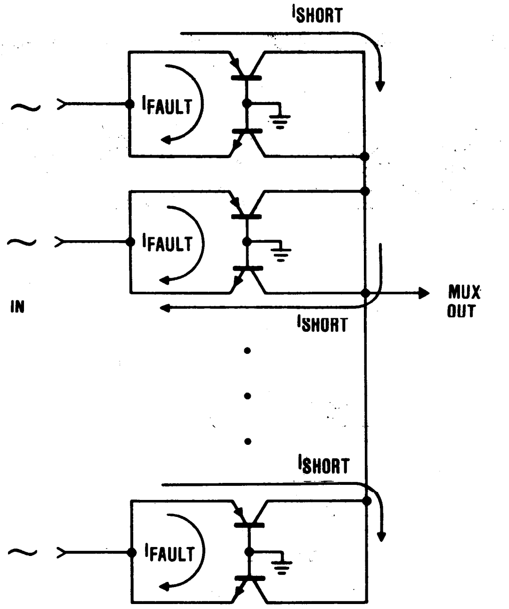


FIGURE 3. STILL WORSE

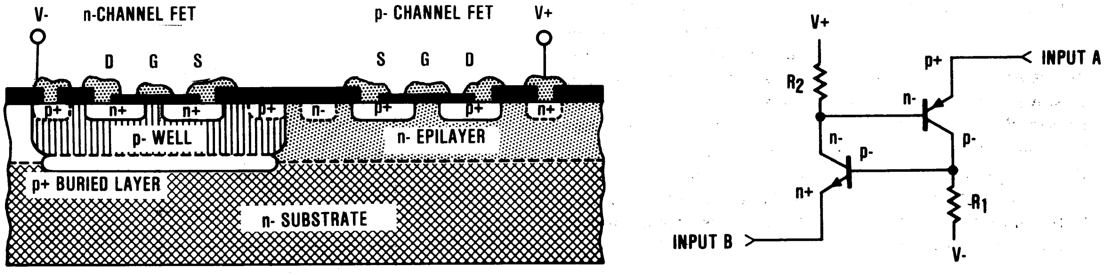
Most serious in CMOS swithes is losing substrate potential to ground. This condition, which happens when power is lost and the analog signal is present, causes very high currents.

Considering Latch-Proof JI Technology

The standard JI process has been modified by what is claimed to be latch-proof construction through control of the effective betas of the parasitic transistors. A cross section in Figure 4(a) shows the CMOS structure along with its parasitic transistors and the equivalent circuit in Figure 4(b) that gives rise to the silicon-controlled-rectifier latch-up problem.

Under any of the fault conditions previously mentioned, the npn and/or pnp can trigger this quasidual-gate SCR into a state of high conduction. If the transistor β product is 1 or greater, this configuration is sustained until either the device burns up or all sources of power are removed. By using a buried-layer configuration, as shown in the cross section, the β product is reduced to less than 1, eliminating the latch-up conditions.

Again, especially in multiplexer applications, the latch-free devices do not guarantee against destruction, and the JI multiplexer still requires costly discrete circuits around


V-
n-CHANNEL FET
D G S
p- CHANNEL FET
V+
S G D
p+
n+
n+
p+
n-
p+
p+
n+
p- WELL
n- EPILAYER
p+ BURIED LAYER
n- SUBSTRATE
V+
R2
p+
INPUT A
n-
n-
p-
p-
n+
R1
INPUT B
V-

(a) (b)

FIGURE 4. LATCH-PROOF.

Junction-Isolated devices are now made latch-proof with a buried-layer configuration (a), which keeps beta of parasitic transistor under unity. That kills chance for latch-up (b), which plagues devices built with older junction-isolation technology.

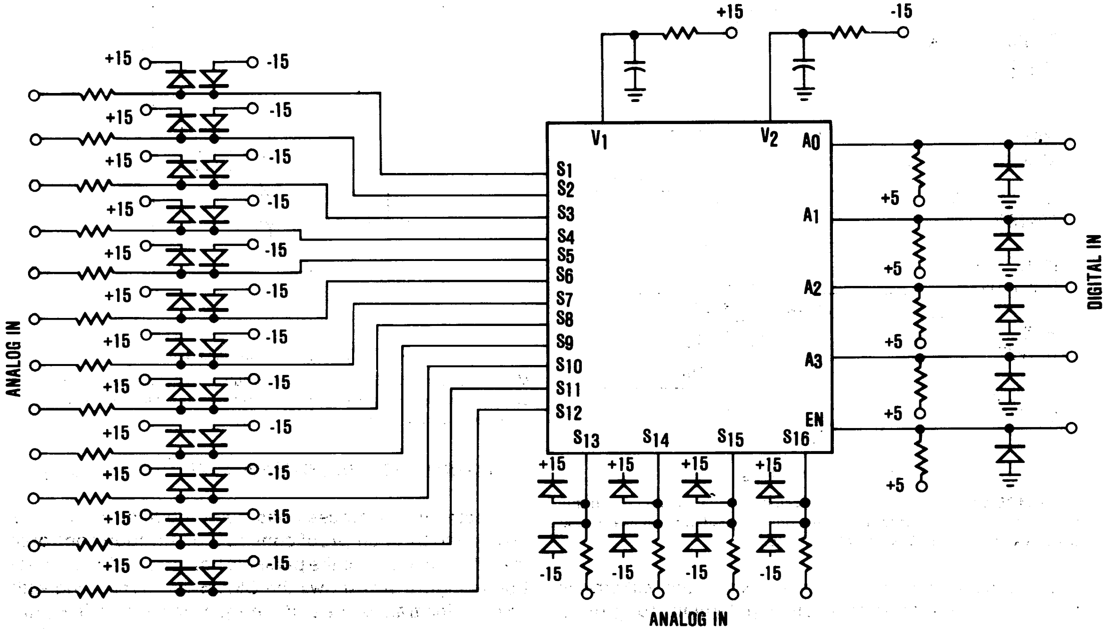

+15
-15
ANALOG IN
V1
V2
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
A0
A1
A2
A3
EN
+5
DIGITAL IN
ANALOG IN

FIGURE 5. PROTECTION STILL NEEDED.

Although new JI devices won't latch up, they still can be destroyed by large currents. That's why typical JI multiplexers, like the one shown here, still need to be surrounded by external protective components, which drive up system costs.

the device, as shown in Figure 5. If an overvoltage exists, the resistor/diode circuit at each analog input limits the input voltage to the supply-voltage range to prevent the parasitic transistor action.

The resistors limit the overvoltage currents through the diodes. The diodes must have a low threshold voltage-much lower than the 0.6V silicon-junction threshold of the internal parasitic diodes-to ensure that the parasitics do not turn on.

A germanium diode offers a low threshold voltage, but its high leakage current makes it impractical, especially in 0.1% systems. Therefore, in most applications, more expensive low-leakage diodes are used.

For example, Schottky diodes meet the requirements but they are expensive. The total cost per multiplexer, including parts and labor, for the discrete protection circuit may well be double the initial purchase price of the device. Even then, its reliability will never approach that of an IC that has this protection already built in.

The Floating-Body JI Technology

Standard JI technology allows another approach to latch-proof device construction: a portion of the SCR continuity is broken by floating the "body" or substrate of the n-channel switching device. A cross section of this process is similar to that in Figure 4(a), excluding the buried layer and the negative supply connection to the p- substrate, so that the dual-gate SCR is changed to a single-gate device that can only be triggered by the pnp parasitic. This, of course, reduces the latch-up probability by 50%.

To completely eliminate latch-up, as before, the β product of the transistors is reduced to less than 1. This accomplishment, certainly a significant improvement over the conventional process, offers greater reliability, but certain trade-offs must be made when the body of a MOSFET is floated.

Nominal source-to-drain breakdown voltages are reduced which limit the peak-to-peak signal range. Over-all breakdown is limited by the collector-emitter breakdown voltage, BV_{CEO}, of the non-parasitic transistor of the floating n-channel MOSFET. The breakdown voltage increases with the degree of reverse-bias potential applied to the substrate. With a floating body, BV_{CEO} is minimum, so particular care is necessasry when using these devices in configurations such as single-pole double-throw, dpst, and dpdt, where each side of the switch connects to opposite polarities. The peak-to-peak handling capability is specified at a minimum of 22V; therefore, 30V pk-pk cannot be switched with ±15V supplies, as it can with other CMOS devices.

What's more, the leakage currents of floating-body JI devices are higher than other types, simply because the ICEO of the floating base for the npn is much greater than ICBO of other devices having fixed reversed-biased body potentials. The increased leakage currents in spst switches may not be too significant.

However, in multiplexers that have the outputs of as many as 16 switches tied together in one IC, the total summation of currents can significantly affect system accuracy. For example, the specification for a worst-case 16-channel floating-body multiplexer is 10 microamperes, and the channel on resistance is 550 ohms. The DC offset error would be 5.5 millivolts, representing an accuracy to 0.055%.

Other 16-channel types specify worst-case parameters of 500 nanoamperes and channel resistance between 550 ohms and 2 kilohms. Their DC offset error is between 0.28mV and 1mV, respectively, allowing accuracy to 0.01% or better.

Finally, the effective off impedance of the floating-body switch is degraded by the floating-body technique. Off-isolation characteristics of a MOSFET are primarily determined by its source-to-drain capacitance. But with the base floating, the effective capacitance from emitter to collector is increased by the series combination of emitter-base and base-collector-junction capacitances (Figure 6a). This increase degrades the over-all off-isolation characteristics. For example, the off isolation for a typical floating-body channel at 1 megahertz that has R_L = 100 ohms is specified to be -54 decibels, which compares favorably with other types. However, at lower frequencies such as 1kHz, the isolation is only -62dB, compared to more than -110dB for improved devices. Capacitances C_1 and C_2 for them are shunted by the low AC impedance of the supply voltage (Figure 6b).

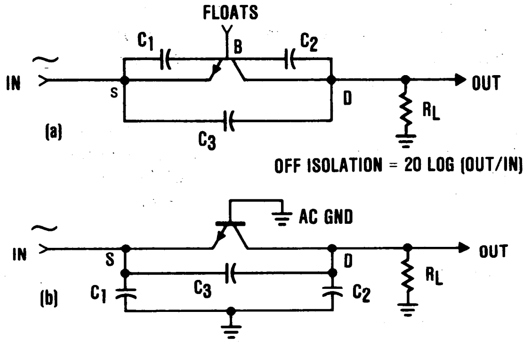


FIGURE 6. FLOATING BODIES.

Floating-body switches have degraded "off" impedance because total capacitance (a) combines two junction capacitances. In DI circuit (b), capacitances are shunted out.

The Linear Dielectric-Isolation Technology

The linear dielectric-isolation process requires no modifications to guard against latch-up. Its basic construciton ensures that the SCR configuration that causes latch-up can not exist. The functional cross section in Figure 7 reveals the silicon-dioxide isolation barrier fabricated between all parasitic transistors. This isolation allows each active element to be self-contained and independent with no interface junctions. At most, only three-layer structures are permitted for each tub, so that four-layer structures, or SCRs, are impossible. Also, since the DI technology requires no guard bands, junction capacitances, leakage currents, and size are minimized. The resulting increase in packing density per wafer, together with increased yields, enables these devices to be cost-competitive with other types.

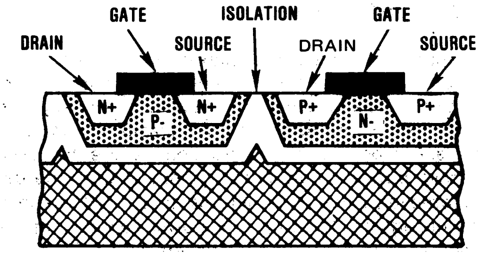


FIGURE 7. HOW DI DOES IT.

Dielectric isolation eliminates latch-up by a silicon-dioxide isolation barrier between devicees. This separates all active elements, eliminating interface junctions that cause parasitic SCRs.

In working with DI devices, the IC designer is not burdened with the fixed substrate potentials found in JI devices. He may let the substrate float, fix it to some potential, or even modulate it. Figure 8 depicts a typical DI analog switch circuit that minimizes the variation of on resistance with the analog signal. Ordinarily, in conventional circuits, the body or substrate potentials of the n and p-channel devices are fixed and the source-to-body bias potentials vary with the analog input voltage. This change in body bias causes a wide variation of on resistance within the analog signal range. However, the DI circuit, the bodies of P_1 and N_1 are connected together through N_3 during the on state. This change in body bias causes a wide variation of on resistance within the analog signal range. However, in the DI circuit, the bodies of P_1 and N_1 are connected together through N_3 during the on state. This allows the body to follow the input voltage providing a constant source-body bias and therefore a constant on resistance. During the offstate, the bodies of N_1 and P_1 are at their respective supply potentials through P_2 and N_2, thereby preserving high off isolation and low leakage currents.

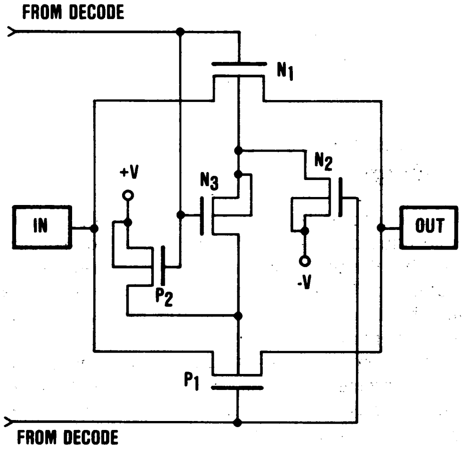


FIGURE 8. DI DOES IT.

In dielectrically isloated switches, on resistance modulation by the analog input is minimized by connecting N_1 and P_1 bodies together through N_3.

Designing a Foolproof CMOS Analog Multiplexer

In dielectrically isolated multiplexer circuits, protection can be provided on the chip primarily to eliminate channel interaction. This protection prevents normally off channels from being turned on by parasitics from other channels. And because this interaction is prevented, even worst-case power-supply faults cannot destroy the device. Moreover, since DI structures have no SCR effect, protection against latch-up and power-sequencing are not necessary. In short, DI multiplexers with built-in protection can withstand virtually any conceivable fault from the outside world.

The typical protected DI multiplexer (Figure 9) benefits from a combined bipolar/CMOS technology. The illustrated bipolar section is used to sense an analog over voltage condition and steer current away from the parasitic MOSFET junctions. Each of the switching devices, N_1 and P_1, has its own proteciton circuits. Devices P_3, D_6, D_7 and Q_6 protect P_1, while N_3, D_4, D_5 and Q_5 protect N_1. When the switch is off, the substrate of the p-channel FET, P_1, is connected to V+ through P_3 and diode D_7 for maximum isolation and low leakage currents in the off state. If the input voltage suddenly exceeds V+, the source-body junction, which would normally conduct, is instead clamped by transistor Q_6.

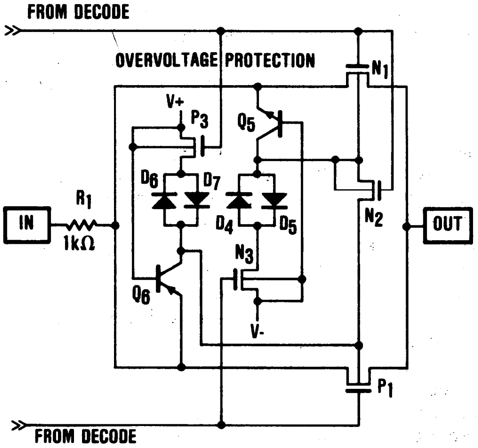


FIGURE 9. WINNING COMBINATION.

Combining bipolar and MOS technologies in the same multiplexer gives built-in protection. This circuit is typical for each channel in multiplexers HI-506A, HI-507A, HI-508A and HI-509A.

The base-emitter junction conducts to hold the source-body diode off with a saturation voltage VCE(SAT) of about 0.2V. Thus clamped, the switch is protected from the effects of overvoltage.

Clamp Q_6 always turns on before the forward-voltage drop of the source-body diode is exceeded because diode D6 requires an additional forward-voltage drop for conduction though the parasitic junciton. Moreover, resistor R_1 limits the current flowing through Q_6 when high overvoltages exist. Although R_1 adds to the total on-resistance of the channel, its associated error is insignificant, since most systems provide high-impedance buffering anyway. For negative overvoltages, N_1 is similarly protected. What's more, the protection circuit, rated at a continuous overvoltage of 35V, reveals a crosstalk current of only about 5nA (Figure 10).

When the switch is normally turned on, the substrates of N_1 and P_1 are connected together through N_2, which, as described before, results in a constant on resistance.

This condition represents an absolute error from channel interaction of only 6 microvolts ($R_{ON} \times 5nA$) - certainly negligible in most systems. In contrast, floating-body types have guarantees only that they won't be burned up by ±25V overvoltage. Their manufacturers do not make any claim against channel interaction. In fact, channel interaction occurs readily in these devices when the n- and p-channel thresholds are exceeded by an overvoltage.

For example, the n-channel device, although floating, would be inadvertently turned on if the analog input exceeded the negative supply by its gate-to-source threshold, which is typically 1.5V.

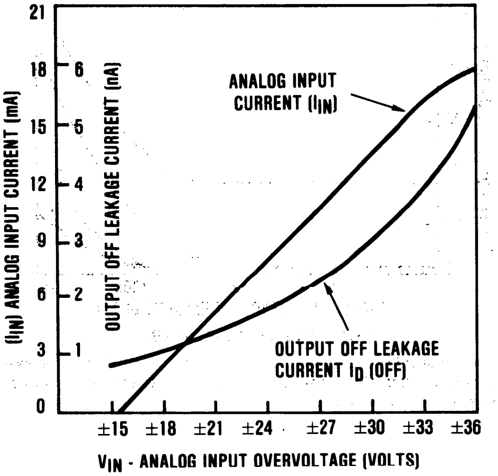


FIGURE 10. BLOCKING CROSS TALK.

DI switches have minimal cross-talk problems. An overvoltage of 33V produces a cross-talk current of only 5nA - an absolute error from channel interaction of only 6μV.

In addition to handling continuous input overvoltages, the HI-506A/507A/508A/509A multiplexers also survive very large transient conditions. These devices typically withstand repeated static discharges well beyond 4,000 volts at any analog input. In fact, even the unprotected HI-506/507/508/509 units can withstand discharges beyond 3,000 volts, though they do not compare to the steady state and signal protection offered by the "A" series.

Adding Benefits

Additional DI benefits are passed on to the user in the design of the digital input-protection circuit shown in Figure 11. The fabrication of all components as isolated silicon islands eliminates any possibility of latch-up. The diodes switch fast and quickly discharge any static charge that may appear at the digital MOS input gates. Tests have shown that the digital inputs can typically withstand repeated discharges at the 2,000 volt level.

The DI technology enables a wide variety of active elements to be integrated on the same chip to provide maximum versatility. For example, in the transistor-transistor-logic/CMOS reference circuit shown in Figure 12, the bipolar technology enables realization of a simple zener reference circuit, consisting of resistor R_2 and transistors Q_1, Q_2, and Q_3.

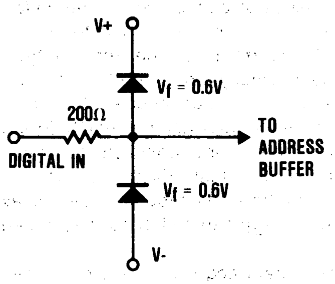


FIGURE 11. DIGITAL PROTECTION.

DI devices also protect digital inputs. For example, the diodes in this circuit quickly discharge any static charge that may appear on an MOS input gate.

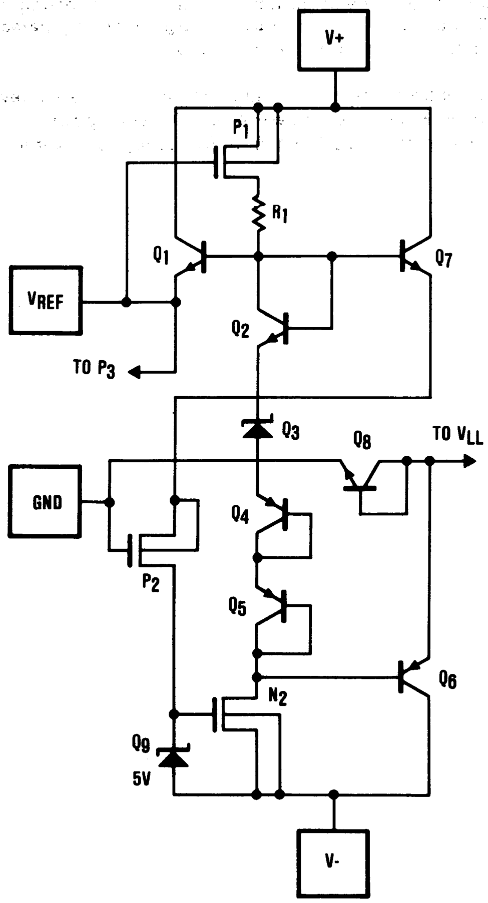


FIGURE 12. PACKING IT IN.

DI technology increases chip density of analog switch, allowing more circuit capability per package. For example, DI designs make possible this internal logic reference circuit in HI-200 and HI-201 switches.

The circuit develops a stable 5V reference for interfacing with TTL and eliminates the need for an additional 5V logic supply. Current for the zener (Q_3) is supplied through the normally on MOSFET, P_1, which can be easily turned off if not needed to minimize power consumption when interfacing with CMOS-logic circuits. P_1 turns off when V^+ or supply voltage V_{DD} is applied to the reference terminal V_{REF} to convert the ICs power consumption from bipolar to CMOS level. If power is not critical, V_{REF} can be left open to speed switching.

In high-speed data acquisition systems, the designer is concerned with both quiescent power and dynamic power consumption. If JI devices are used, the capacitance or leakage currents are so high they contribute a major portion of total power consumption. That situation is caused by the large-geometry parasitic junctions formed by the n- junction.

In contrast, the smaller substrate area of the DI device provides much less power drain. Dynamic-power consumption as a function of frequency for several 16-channel analog multiplexers ±15V supplies is shown in Figure 13. The DI device consumes only 100mW at 1MHz to yield the best speed-power product.

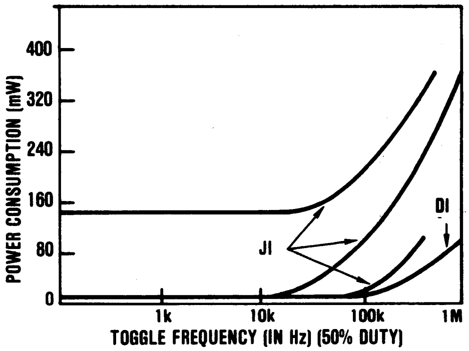


FIGURE 13. DI PERFORMS.

DI devices not only perform well, but do it with less power. Dynamic-power consumption data for commercial multiplexers shows DI device consuming only 100mW at 1MHz.

APP NOTE

FOR YOUR INFORMATION

No. 522

Harris Analog

DIGITAL TO ANALOG CONVERTER TERMINOLOGY

By Dick Ti Tung

INTRODUCTION

In recent years the development and rapid reduction in cost of digital integrated circuits have resulted in an explosion in the applications of digital processing systems in the area of data acquisition and automatic process control. The need for a building block, such as the digital-to-analog converter (DAC), which interfaces the digital system with the analog world, is evident.

The purpose of digital-to-analog conversion is to produce a unique but consistent analog quantity, voltage or current, for a given digital input code. The most commonly used input digital code to a DAC is the natural binary number. A natural binary number is represented as

$$N = A_n 2^n + A_{n-1} 2^{n-1} + \ldots + A_1 2^1 + A_0 2^0 + A_{-1} 2^{-1} + \ldots + A_{-n} 2^{-n}$$

where the coefficients A_i (for $n \geqslant i \geqslant -n$) assume the values of "0" or "1" and is called a "bit". The left half portion of the binary number N

$$A_n 2^n + A_{n-1} 2^{n-1} + \ldots + A_1 2^1 + A_0 2^0$$

constitutes the integer part of the number N, whereas the right portion

$$A_{-1} 2^{-1} + A_{-2} 2^{-2} + \ldots + A_{-n} 2^{-n}$$

constitutes the fractional part of the number N. The bit that carries the greatest weight (left most bit) is called the most significant bit, or MSB. Similarly, the bit with the smallest weight (right most bit) is called the least significant bit, or LSB.

The analog output of a n-bit binary DAC is related to its binary number in the following manner:

$$E_o = FS(A_{-1} 2^{-1} + A_{-2} 2^{-2} + \ldots + A_{-n} 2^{-n})$$

where the term FS is defined as the nominal Full-Scale output of the DAC and it is known as the unreachable Full-Scale. It is easy to see that the actual Full-Scale output of the DAC, E_{FS}, with all the input bits "1" is

$$E_{FS} = FS(2^{-1} + 2^{-2} + \ldots + 2^{-n}) = FS(1-2^{-n}).$$

The term $FS(1/2^n)$ is the smallest output level that the DAC can resolve and it is known as the 1 LSB output level change. It is universal practice that the input code of a DAC is written in the form of binary integer with the fractional nature of the corresponding number understood.

As an example, the transfer function of an ideal 3-bit binary DAC is plotted as shown in Figure 1. Since a 3-bit DAC has only 8 discrete input codes which correspond to 8 different output levels (ranging from zero to 7/8 FS), no other output levels can exist and it is plotted as a bar graph. The line that connects the Zero and FS is called the Gain Curve.

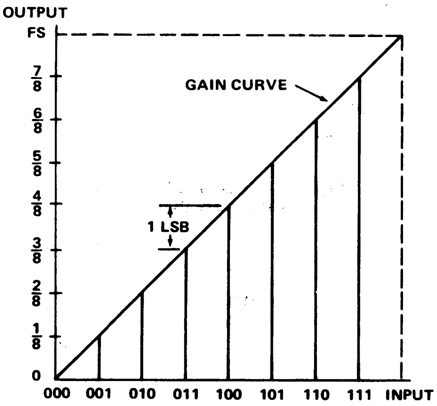


Figure 1 — Ideal Transfer Function Straight Binary (Unipolar)

There are two other input codings associated with binary DACs known as Bipolar codes, which are offset binary and two's complement binary codes. The offset binary code is obtained by offsetting the binary code such that the half-scale code, 10 . . . 0, becomes zero. And the two's complement code is achieved by inverting the MSB of the offset binary code such that it is mathematically consistent with computer arithmetic. The transfer functions for the 3-bit DAC with offset binary input code and two's complement input code are plotted as shown in Figure 2 and Figure 3, respectively. (The +FS and -FS limits are used for easy interpretation of Bipolar operations. They are not confined by the previous definition of FS.)

In practical DACs, the zero output level may not be exactly zero (offset error), the range from zero to FS may not be exactly as specified (gain error), the differences in output levels may not be changing uniformly (nonlinearity), and so on. In selecting a DAC for a given application, some characteristics may have to be weighted more than the others. An understanding of some of the terms and characteristics involved in D/A conversion is helpful in choosing the correct part.

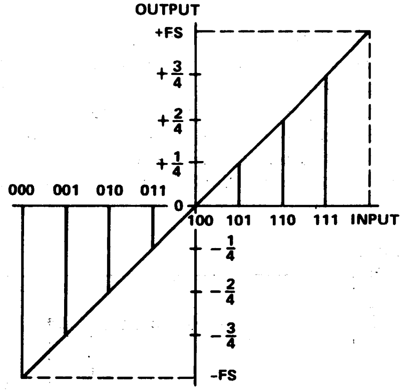


Figure 2 – Ideal Transfer Function Offset Binary (Bipolar)

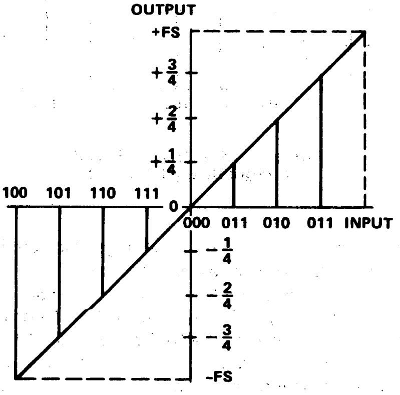


Figure 3 – Ideal Transfer Function Two's Complement (Bipolar)

TERMINOLOGY

Least Significant Bit (LSB) – The digital input bit carrying the lowest numerical weight ($1/2^n$); or the analog output level shift associated with this bit ($FSR/2^n$) which is the smallest possible analog output step.

Most Significant Bit (MSB) – The digital input bit carrying the highest numerical weight (1/2); or the analog output level shift associated with this bit. In a binary DAC the MSB creates a 1/2 FSR output level shift.

Resolution – An indication of the number of possible analog output levels a DAC will produce. Usually, it is expressed as the number of input bits. For example, a 12-bit binary DAC will have $2^{12} = 4096$ possible output levels (including zero) and it has a resolution of 12 bits.

Absolute Accuracy – A measure of the deviation of the analog output level from the ideal value under any input combination. Accuracy can be expressed as a percentage of full scale range, a number of bits (n bits accuracy means a magnitude of $1/2^n$ FSR possible error may exist), or a fraction of the LSB (if a DAC with n-bit resolution has 1/2 LSB accuracy the magnitude of the possible error is $1/2(1/2^n FSR)$). Accuracy may be of the same, higher, or lower order of magnitude as the resolution. Possible error in individual bit weight may be cumulative with combination of bits and may change due to temperature variations. Usually, the accuracy of a DAC is expressed in terms of nonlinearity, differential nonlinearity, and zero and gain drift due to temperature variations.

Nonlinearity (linearity error) – A measure of the deviation of the analog output level from an ideal straight line transfer curve drawn between zero and full scale (commonly referred as endpoint linearity).

Differential Nonlinearity – A measure of the deviation between the actual output level change from the ideal (1 LSB) output level change for a one bit change in input code. A differential nonlinearity of ±1 LSB or less guarantees monotonicity; that is the output always increases for an increasing input.

Gain Drift – A measure of the change in full scale analog output, with all bits 1's, over the specified temperature range expressed in parts per million of full scale range per °C (PPM of FSR/°C). It is measured with respect to +25°C at high (T_H) and low (T_L) temperature, and it is specified the larger of the two representing worst case drift.

Offset Drift (Unipolar or Bipolar) – A measure of the change in analog output, with all bits 0's, over the specified temperature range expressed in parts per million of full scale range per °C (PPM of FSR/°C). It is measured with respect to +25°C at high (T_H) and low (T_L) temperature, and it is specified the larger of the two representing worst case drift.

Settling Time – The total time measured from a digital input change to the time the analog output reaches its new value within a specified error band. Usually, the settling time is specified for a DAC to settle for a Full-Scale code change (00 . . . 0 to 11 . . . 1 or 11 . . . 1 to 00 . . .0) to within ±1/2 LSB of its final value.

Compliance – Compliance voltage is the maximum output voltage range that can be tolerated and still maintain the specified accuracy.

The effects of gain error, offset error, nonlinearity, and differential nonlinearity on the transfer functions are plotted, respectively, as shown in Figure 4, 5, 6, & 7. A conversion chart which shows the number of bits and its resolution is given in Table 1.

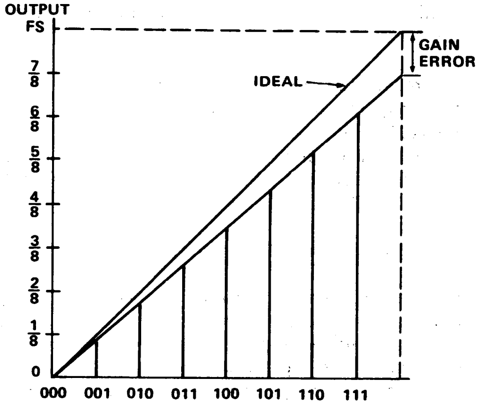


Figure 4 – Gain Error

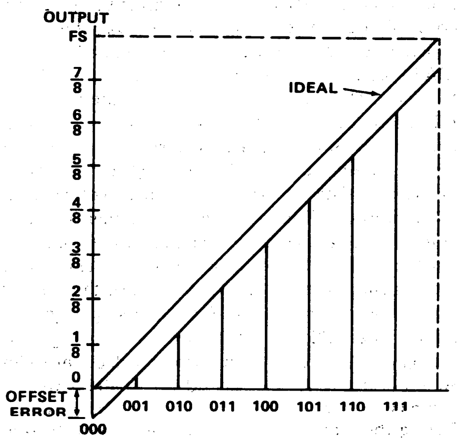


Figure 5 – Offset Error

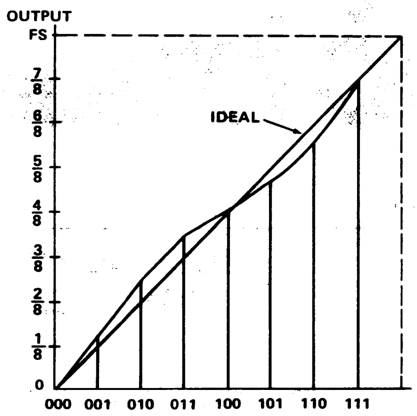


Figure 6 – Linearity Error

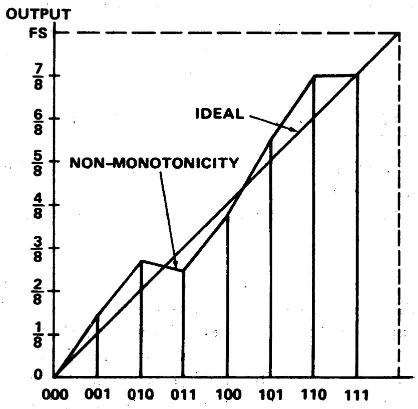


Figure 7 – Differential Linearity Error (Non-Monotonicity)

Table 1 – Conversion Chart

# OF BITS	LSB	RESOLUTION		TEMPCO PPM/°C – 1 LSB DRIFT OVER	
		%	PPM	0°C ≤ TA ≤ 75°C	-55°C ≤ TA ≤ 125°C
6	FS/64	1.5620	15,625	208.3	86.8
7	FS/128	0.7812	7.812	104.2	43.4
8	FS/256	0.3906	3,906	52.1	21.7
9	FS/512	0.1953	1,953	26.0	10.9
10	FS/1024	0.0977	977	13.0	5.4
11	FS/2048	0.0488	488	6.5	2.7
12	FS/4096	0.0244	244	3.3	1.4
13	FS/8192	0.0122	122	1.6	0.68
14	FS/16384	0.00610	61	0.8	0.34
15	FS/32768	0.00305	31	0.4	0.17
16	FS/65536	0.00153	15	0.2	0.08

APP NOTE

FOR YOUR INFORMATION

No. 524

Harris Analog

DIGITAL TO ANALOG CONVERTER HIGH SPEED ADC APPLICATIONS

By Dick Ti Tung and Tom Westenburg

ANALOG-TO-DIGITAL CONVERTER (ADC)

The uses of high speed DACs in CRT display, industrial process control, signal regeneration, etc., are well established. Perhaps one of the most important applications is to use the DAC in high speed ADC design. There are two types of ADC design where high speed and high resolution DACs are essential.

TRACKING ADC OR SERVO TYPE ADC

The tracking ADC is very efficient in monitoring one analog signal continuously, converting it into a sequence of digital codes representing the analog signal in real time.

Functionally, the analog input is compared with the output of a DAC, with the digital input of the DAC being driven by a counter. After the ADC is turned on, the counter increments until the DAC output crosses the analog input value. The counter will then, running up or down, drive the DAC 1 LSB at a time to track the input signal. The counter state represents the digital equivalent of the input signal.

In Figure 1, the analog input is fed into the span resistor of a DAC. The analog input voltage range is selectable in the same way as the output voltage range of the DAC. The net current flow through the ladder termination resistance, i.e.2kΩ for HI-562A, produces an error voltage at the DAC output. This error voltage is compared with 1/2 LSB by a comparator. When the error voltage is within ± 1/2 LSB range, the Q output of the comparators are both low, which stops the counter and gives a data ready signal to indicate that the digital output is correct. If the error exceeds the ±1/2 LSB range, the counter is enabled and driven in an up or down direction depending on the polarity of the error voltage.

Since the digital output changes state only when there is a significant change in the analog input, the data ready signal is then very useful in adaptive systems or computer systems for efficient data transfer. When monitoring a slowly varying input, it is necessary to read the digital output only after a change has taken place. The data ready signal could be used to trigger a flip-flop to indicate the condition and reset it after read-out.

The main disadvantage of the tracking ADC is that the time required to initially acquire a signal, for a 12 bit ADC, could be up to 4096 clock periods. The input signal usually must be filtered so that its rate of change does not exceed the tracking range of the ADC (1 LSB per clock period).

SUCCESSIVE-APPROXIMATION ADC

Perhaps the most widely used technique for a high speed analog-to-digital converter design is the successive approximation method. Ideal for interfacing with computers, this type is capable of both high speed and high resolution, and the conversion time is fixed and independent of the magnitude of the input voltage.

Figure 2 shows a block diagram of a successive-approximation ADC. When a negative going start conversion pulse is applied to the ADC, the internal registers of the successive approximation register (SAR) are set to low except for the MSB, which is set to high. This turns on the MSB of the DAC. The FS output current of the DAC is compared with the current fed through the span resistor by the analog input. The net current flow through the ladder termination resistance produces an error voltage at the DAC output. This error voltage is then compared with a fixed reference by a comparator to determine whether the analog input is greater or less than the present state of the DAC. The result of the comparison is clocked into the SAR at the rising edge of the clock. The MSB of the SAR will be set to high if the analog input is greater; otherwise, it will be set to low. At the same time, the second bit of the SAR is set to high with the remaining bits at their previous states. During the second clock period, the sum of the result of the first choice and the weight of the second bit is compared with the analog input. The second bit is set to high or low in the same manner as the MSB, and so on, until the LSB is updated.

During this conversion time, the output of a status flip-flop is set to high, indicating that a conversion is taking place. It will return to low at the end of conversion to signify that the output state of the SAR represents the digital equivalent of the input analog voltage.

It is easy to see that in any successive-approximation ADC application, the analog input should remain reasonably constant during the conversion to avoid erroneous results. This is usually accomplished by using a sample-and-hold circuit in the analog line.

However with the new digital error correction circuitry incorporated in the HI-774A the input can vary. During the first portion of the conversion the input can move up to +0.78%/-0.76% of FSR and remain 12-bits accurate. This error correction window allows the user to start a conversion before the input has completely settled.

DATA ACQUISITION SYSTEM

The typical data acquisition system is depicted in Figure 3. The HI-506 multiplexer is used as an analog input selector. Which is controlled by a binary counter to address the appropriate channel. The HA-5330 is a high speed sample and hold. Sample Hold Control is tied to the status (STS) output of the HI-774A, so that whenever a conversion is in process the S/H is in the hold mode. A conversion is initiated by the clock input going low, and when the clock goes high the mux address changes. The mux will be acquiring the next channel while the ADC is converting the present input, held by the S/H. The clock low time should be between 225ns and 6.5µs, with the period greater than 8.5µs. With this timing R/C will be high at the end of a conversion so the output data will be valid ~100ns before STS goes low. This allows STS to clock the data into the storage register. The register address will be offset by one, if this is a problem then a 4-bit latch can be added to the input of the storage register. With a 100KHz clock rate each channel will be read every 160µs.

This 16-channel data acquisition system is applicable to industrial process control, and multi-channel panel display. It can also interface with an intelligent terminal, such as a micro-computer system, to provide multi-channel data conversion function. The offset error and gain error of the data acquisition system over the operating temperature range can be easily compensated by proper programming.

By the same token, a 15-channel data acquisition system with offset correction could be easily incorporated as shown in Figure 4. Consider the case that one of the analog input channels is dedicated to sense the ground level, and its binary equivalent is stored in latch register B in its complementary form to establish a ground reference in real time. All the other analog input channels will then be converted and stored in register A, one at a time. The binary adder will perform the binary subtraction in less than 1µs for the given pair of A and B. This, in fact, eliminates the offset error of the ADC, offset error of the S/H circuit, and excess droop of the S/H due to temperature variation.

This circuit is easy to implement and is especially useful when an intelligent terminal is not available. To expand this concept one step further, the gain error of the system due to temperature variations could also be eliminated if a binary multiplier is used to correct the gain facter in real time.

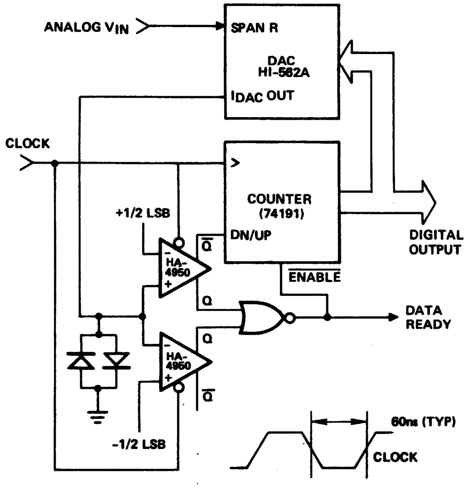


Figure 1. Tracking ADC

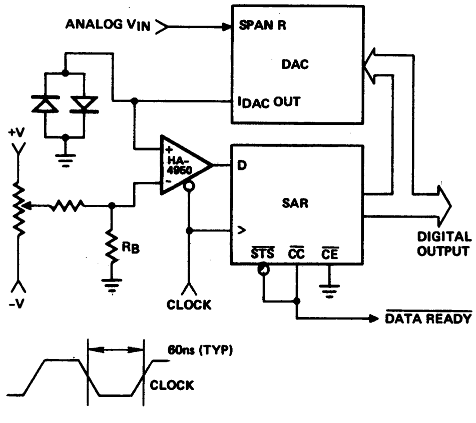


Figure 2. Successive-Approximation ADC

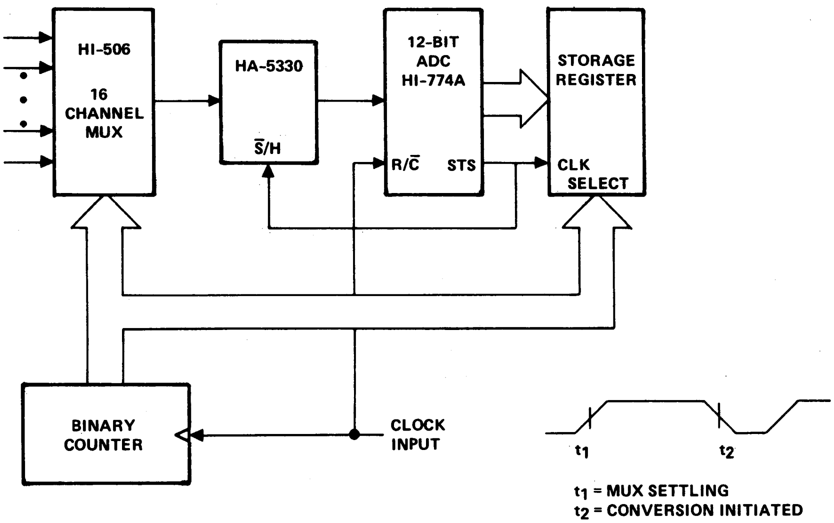

HI-506
16 CHANNEL MUX
HA-5330
S̄/H
12-BIT ADC HI-774A
R/C̄
STS
STORAGE REGISTER
CLK SELECT
BINARY COUNTER
CLOCK INPUT
t1
t2
t1 = MUX SETTLING
t2 = CONVERSION INITIATED

Figure 3. 16 Channel Data Acquisition System

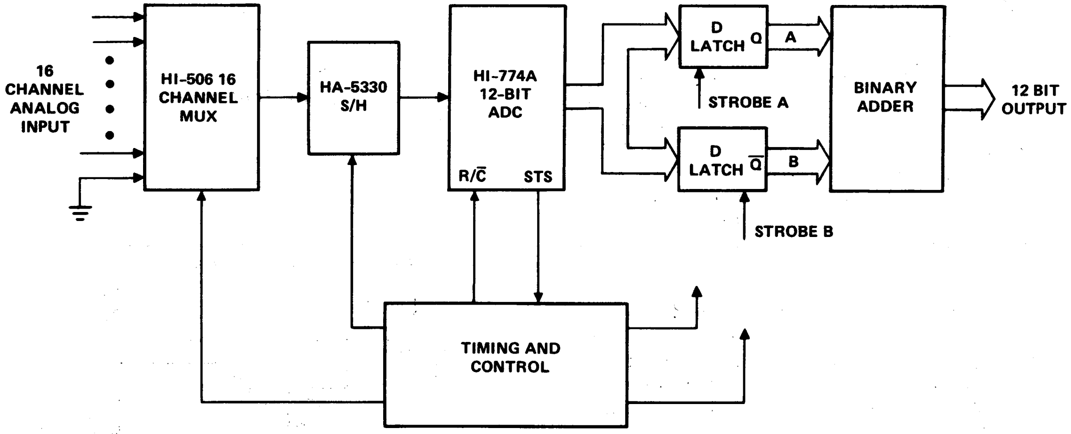

16 CHANNEL ANALOG INPUT
HI-506 16 CHANNEL MUX
HA-5330 S/H
HI-774A 12-BIT ADC
R/C̄
STS
D LATCH Q
A
STROBE A
D LATCH Q̄
B
STROBE B
BINARY ADDER
12 BIT OUTPUT
TIMING AND CONTROL

Figure 4. 15 Channel Data Acquisition System with Offset Correction

No. 525

Harris Analog

HA-5190/5195 FAST SETTLING OPERATIONAL AMPLIFIER

By G. Cotreau, D. Jones, R. Whitehead

INTRODUCTION

The military temperature range HA-5190 and its commercial temperature equivalent, HA-5195, are monolithic operational amplifiers featuring ±200V/μs slew rate, 150mHz gain-bandwidth-product, and 70ns settling time. Similar performance has previously been available only in more costly modular and hybrid amplifiers, which require much higher bandwidth and slew rate to achieve the same settling time as HA-5190/5195. Since it exhibits a classical -6dB/octave rolloff over most of its frequency range, remarkably smooth output wave forms are generated by HA-5190 when reasonable care is employed.

Applications for this op amp include pulse, RF, and video amplifiers, wave form generators, high speed data acquisition and instrumentation circuits.

INSIDE THE HA-5190/5195

Figure 1 shows the schematic of the HA-5190/5195 design. The schematic can be simplified to show the AC signal path as shown in Figure 2.

The input stage consists of two symmetrical differential transistor pairs. The signal path for positive going signals is Q_1, Q_2, and Q_3, while negative going signals pass through Q_4, Q_5, and Q_6. The signal then goes through the output stage (represented by the voltage follower symbol) consisting of one PNP and two NPN emitter followers.

In Figure 2, the compensation network is C_1, C_2, C_3, and R_{29}. This network makes the amplifier system appear as second-order critically damped. The scheme produces the dominant pole plus two zeros. The zeros are positioned to cancel the effects of undesired poles developed by the F_t of the transistors.

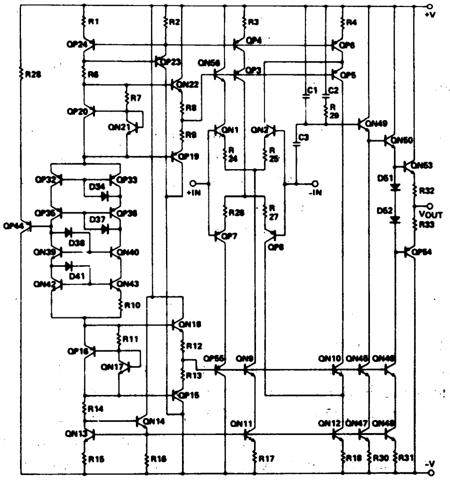

+V
R1
R2
R3
R4
QP4
QP6
QP24
QP23
QN58
QP3
QP5
R28
R6
QN22
C1
C2
R29
R7
R8
QP20
QN21
R9
QN1
QN2
C3
QN49
QN50
QP19
R24
R25
QN53
QP32
QP33
D34
+IN
-IN
D51
R32
QP35
QP36
D37
R26
R27
D52
VOUT
R33
QP44
D38
QP7
QP8
QN39
QN40
QP54
D41
QN42
QN43
R10
QN18
R11
R12
QP16
QP56
QN9
QN10
QN45
QN46
QN17
R13
QP15
R14
QN14
QN11
QN12
QN47
QN48
QN13
R15
R16
R17
R18
R30
R31
-V

Figure 1. HA-5190/5195 Schematic.

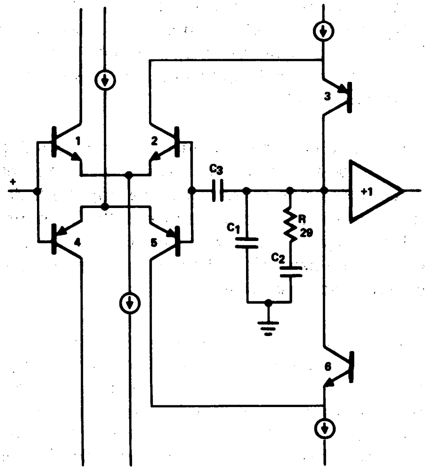

3
1
2
+
C3
+1
C1
R
29
C2
4
5
6

Figure 2. Simplified HA-5190 Schematic.

CONSIDERATIONS FOR PROTOTYPING

When using the HA-5190, high frequency layout techniques are recommended for bread-boarding. The device should be mounted through a ground plane. If an IC socket is to be used, Teflon types are recommended. Feedback components should be mounted between Teflon insulated standoffs located as close as possible to the device pins.

The input impedance characteristic of the HA-5190 is such that the closed loop performance (DC and AC) will depend on both the feedback component ratio and the actual impedance presented to each amplifier input. For best high frequency performance, resistor values for feedback networks should be limited to a maximum of 5K ohms (preferably less than 1K ohm). Film type resistors are recommended. Power supply decoupling with ceramic capacitors from the device supply pins to ground is essential.

It is recommended that optimum circuit values for a particular application be developed through experimentation using amplifiers from several production runs. The PC artwork in the vicinity of the HA-5190 should be prototyped early to determine any sensitivites to layout.

OPERATION AT ELEVATED TEMPERATURES

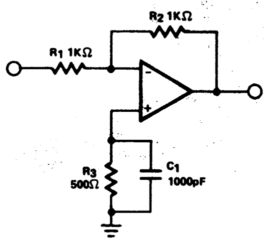
HA-5190/5195 may be used without a heat sink up to +75°C ambient. Above this temperature the power derating is 8.7mW/°C and a heat sink should be used. THERMALLOY model 6007 heat sink is recommended. For temperatures up to +125°C, the thermal resistance of the heat sink should be 30.6°C/W maximum.

FREQUENCY COMPENSATION

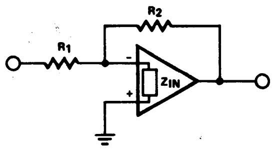
HA-5190/5195 is stable in standard DC amplifier configurations with closed loop gains exceeding +5 or -4. At these or higher gains, optimum AC performance can be achieved by keeping network resistor values as low as is practical.

Quite simple circuitry, as illustrated in Figure 3, gives excellent performance for lower closed loop gains. The compensation schemes use the amplifier's differential input impedance to reduce both the input and feedback signals thereby raising the effective noise gain approximately 14dB to a stable point on the frequency response curve.

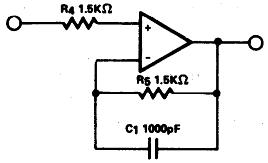
Inverting and non-inverting unity gain connections for HA-5190 are shown in Figure 3 (a) and (c). R_3 and R_5 serve only to balance DC voltage offsets due to input bias current, and may be replaced with a short for AC applications. C_1 is not neccessary for stability, but helps reduce overshoot and smooth the frequency response. Settling time or frequency response can be optimized (about 30mHz small signal bandwidth is practical) by fine tuning component values.



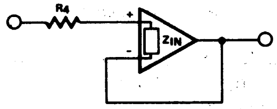
(a) Gain = -1



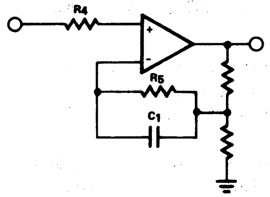
(b) Stabilization using Z_{IN}.



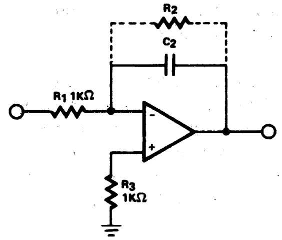
(c) Gain = +1



(d) Stabilization using Z_{IN}.



(e) Non-inverting gain stage.



(f) Integrator

Figure 3. Compensation recommended when $1 + \frac{R2}{R1} < 5$.

For closed loop gains between 1 and 5, reducing R_1 in Figure 3 (a) and (e) will raise the gain with minimum effect on bandwidth. However, in the inverting configuration, R_1 determines the input impedance, and it may be more practical to raise R_2 at the expense of bandwidth. In Figure 3 (e), R_4 and R_5 may be reduced as gain is increased and removed entirely at gains greater than +4.

For applications requiring 100% feedback at high frequencies, such as integrators and low pass filters, HA-5190/5195's compensation scheme should be thoroughly evaluated through experimentation. The circuit in Figure 3 (f) is quite stable, using the two 1K ohm resistors.

SUGGESTED METHODS FOR PERFORMANCE ENHANCEMENT

To avoid compromising AC performance, the HA-5190 design does not include provisions for internal offset adjustment.

The circuits in Figure 4 (a) and (b) show two possible schemes for offset voltage adjustment.

Figure 5 (a) and (b) uses the inherent qualities of the FET to reduce input bias currents by several orders of magnitude and raise input impedance to thousands of megohms. Both circuits are shown in the unity gain follower mode. Circuit gain can be implemented using normal feedback techniques. To optimize for speed, care should be taken in layout. Experimental results yielded slew rates of approximately 130V/μs.

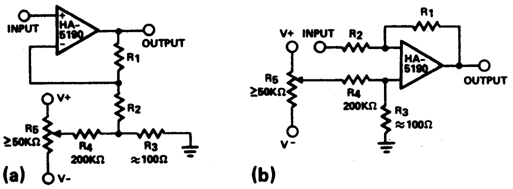
Figure 5 (c) illustrates a composite inverting amplifier which greatly reduces DC errors due to the HA-5190 input bias current and gain, while retaining superior settling time. The 0 dB frequency of the integrator section approximates the open loop low frequency pole (~2.5kHz) of the HA-5190. This circuit might also be connected as a current-to-voltage amplifier for use with a high accuracy, high speed DAC.

Figure 6 shows a composite amplifier scheme for boosting output current drive of the HA-5190/5195. The circuit gain (shown $A_V = 5$) can be adjusted using normal feedback systems. HA-5190 used in conjunction with HA-2630 can drive 50 ohm coaxial cable with 10 volt peak-to-peak signals at speeds up to 200V/μs.

APPLICATIONS

INTRODUCTION

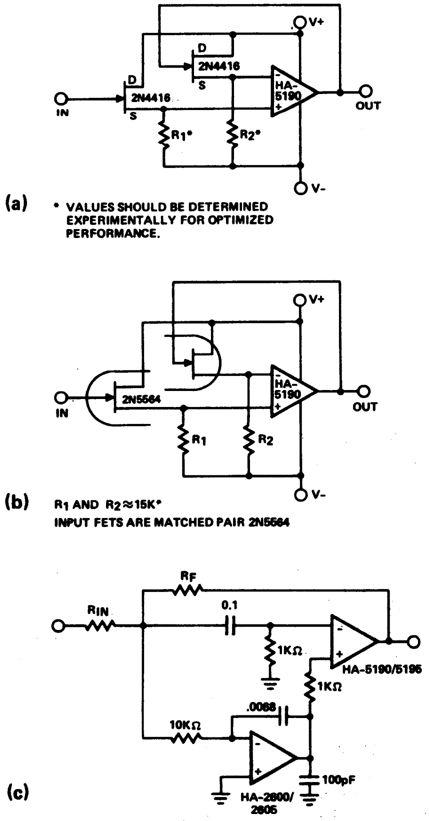
HA-5190/5195 represents an ideal building block for high speed, precision data acquisition systems and for video pulse amplification. Although this amplifier can be used in a wide variety of other applications, the ones to be discussed show where it can be used most advantageously.



RANGE OF ADJUSTMENT FOR BOTH NON-INVERTING (LEFT) AND INVERTING AMPLIFIERS (RIGHT) DETERMINED BY PRODUCT OF V_{SUPPLY} AND R_3/R_4 RATIO.

$$A_V = 1 + \frac{R_1}{R_2 + R_3}$$

Figure 4. Offset Nulling.



(a) * VALUES SHOULD BE DETERMINED EXPERIMENTALLY FOR OPTIMIZED PERFORMANCE.

(b) R_1 AND $R_2 \approx 15K$*
INPUT FETS ARE MATCHED PAIR 2N5564

Figure 5. Reducing Input Bias Currents.

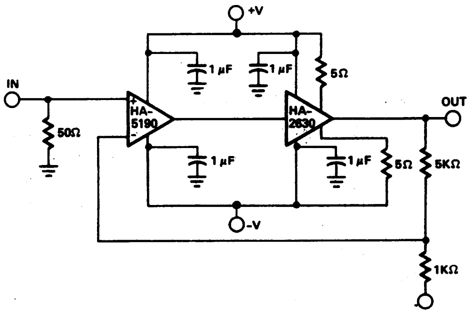


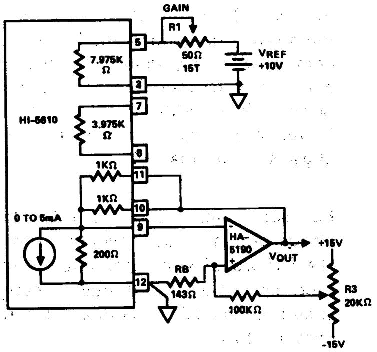
Figure 6. Boosting Output Current.

Application 1 Fast DAC Output Buffer

The circuit at right illustrates the HA-5190's usefulness as a high speed DAC buffer.

The amplifier operates as a current-to-voltage converter/output buffer to the HI-5610 which is a precision 10 bit DAC with output current settling time less than 100ns. The voltage divider on the non-inverting input serves to null any DC errors introduced into the system. The amplifier maximizes speed of the system since its dynamic performance exceeds that of the DAC.

Application 1


GAIN
R1
50Ω
15T
VREF
+10V
7.975K Ω
3.975K Ω
HI-5610
1KΩ
1KΩ
0 TO 5mA
200Ω
5
3
7
8
11
10
9
12
RB
143Ω
HA-5190
VOUT
+15V
100KΩ
R3
20KΩ
-15V

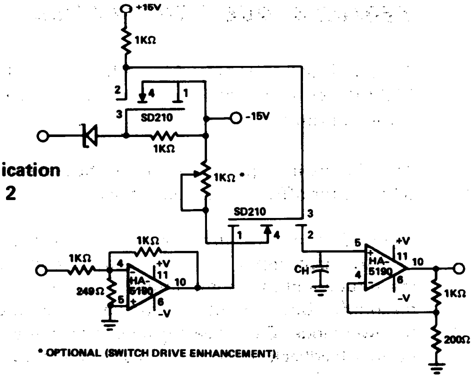
Application 2 High Speed Sample/Hold

Sample/Hold circuits are used in many areas of data acquisition systems such as de-glitchers for D/A converters and input stages for successive approximation A/D converters.

The circuit at right uses the speed and drive capability of the HA-5190 coupled with two high speed DMOS FET switches.

The input amplifier is allowed to operate at a gain of -5 although the overall circuit gain is unity. Acquisition times of less than 100ns to 0.1% of a 1 volt input step are possible. Drift current can be appreciably reduced by using FET input buffers on the output stage of the Sample/Hold.

Application 2


+15V
1KΩ
SD210
-15V
1KΩ
1KΩ *
SD210
1KΩ
1KΩ
249Ω
HA-5190
+V
-V
CH
HA-5190
+V
-V
1KΩ
200Ω
1
2
3
4
5
6
10
11

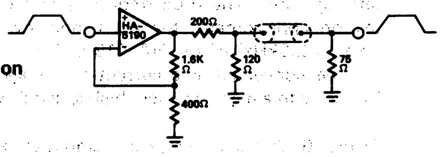
* OPTIONAL (SWITCH DRIVE ENHANCEMENT)

Application 3 Video Pulse Amplifier/75 ohm Coaxial Driver

HA-5190/5195 is also well suited for video pulse applications. The circuit at right could be found in various types of video broadcasting equipment where 75 ohm systems are commonly employed.

HA-5190 can drive the 75 ohm coaxial cable with signals up to 2.5 volts peak-to-peak without the need for current boosting. In this circuit the overall gain of the circuit is approximately unity because of the impedance matching network.

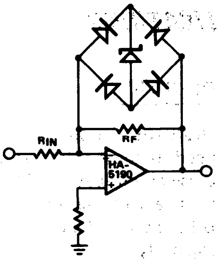
Application 3


HA-5190
200Ω
1.6K Ω
400Ω
120 Ω
75 Ω

Application 4 Output Limiter

HA-5190 is rated for ± 5 volt output swing, and saturates at ± 7 volts. As with most op amps, recovery from output saturation is slow compared to the amplifier's normal response time; so some form of limiting, either of the input signal or in the feedback path, is desirable if saturation might occur. The circuit above illustrates a feedback limiter, where gain is reduced if the output exceeds ± (Vz + 2Vf). A 5 volt zener with a sharp knee characteristic is recommended.

Application 4


RIN
RF
HA-5190

APP NOTE

FOR YOUR INFORMATION

No. 526

Harris Analog

VIDEO APPLICATIONS
HA-5190/5195

By L. E. Garner

INTRODUCTION

Offering superior performance in video and RF circuits, the HA-5190/5195 family can be used effectively in the design of television broadcast studio equipment, test instruments, and monitoring or surveillance TV systems. A very high 200V/μs slew rate, a full power bandwidth of 6.5MHz, and a fast settling time of only 70ns (typ) are but three of the unique characteristics which make these devices ideal for critical wideband video and RF applications. Other features include true differential operation, excellent stability with gains ≥ 5, and complete freedom from latch up, the latter a result of the exclusive HARRIS dielectric isolation process combined with optimized chip design and layout.

The op amp family can be used, typically, as studio tape head, test instrument, and video camera preamplifiers, as buffers, as broadcast relay link repeaters, as coaxial line drivers, and as cable or industrial system video repeater and bridging amplifiers. Extremely versatile, the devices can be operated effectively in AGC and dc gain controlled configurations as well as in fixed gain designs, and are fully capable of driving low impedance loads.

When used in standard video amplifier configurations, the HA-5190/5195 devices easily meet or exceed the performance tolerance specifications of applicable current FCC (NTSC) composite TV signal standards as well as the requirements of EIA Tentative Standard RS-170A.

VIDEO PERFORMANCE

The overall color video performance of the HA 5190/5195 family was confirmed by checking a number of standard devices. Tests were made to determine both video response and signal/noise ratio under typical operating conditions. The basic video amplifier circuit illustrated in Figure 1 was used for the tests, with the actual procedures abstracted from those described in EIA Standard RS-250-B. The general test setup is shown in Figure 2.

VIDEO RESPONSE TESTS

Referring to Figure 1, the test video amplifier comprised an HA5190/5195 op amp, BNC coaxial input jack J1, input level control R1 shunted by impedance matching resistor R2, input series stabilization resistor R3, gain control network R4-Rgain, series output limiting resistor Rs, and BNC coaxial output jack J2. Operational power was supplied by a well regulated and filtered dual line operated power supply.

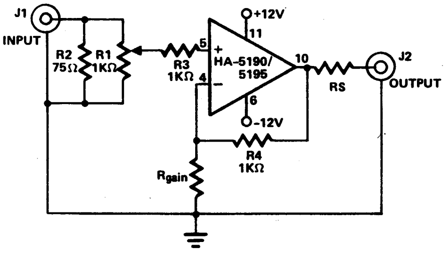


Figure 1–Test Video Amplifier

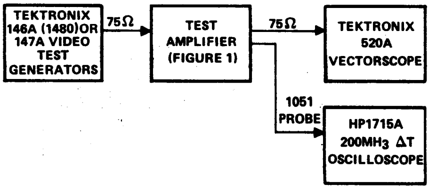


Figure 2–Video Response Test Setup

Initially, standard NTSC and EIA ramp and timing test signals were applied using the Tektronix Models 146A (1480) and 147A video test generators. Amplifier performance was observed and measured at various levels with a Tektronix 520A Vectorscope and HP Model 1715A 200MHz delta time Oscilloscope. Three of the RS-250-B specified test waveforms used are illustrated in Figure 3, including the (a) ramp linearity, (b) 12.5T and 2T sine-squared pulse and bar, and (c) multiburst signals. With the test signal level maintained at 1.0V p-p, level control R1 was adjusted as needed to establish a 1.0V p-p output signal (at J2) for each gain value. The Vectorscope was used to measure color differential phase and gain, with the Oscilloscope used to check for distortion of the 2T, 12.5T, multiburst and color bar signals. The average test results are summarized in Table A. All measured values were well within applicable specifications.

Table A - Summary of Test Results

NOMINAL GAIN	R_{gain}	R_s	DIFF ϕ	DIFF GAIN	2T	12.5T	MULTI	COLOR BARS
1	∞	0	-0.2°	-0.5%	UNM*	UNM*	FLAT	UNM*
2	1k	75Ω	-0.15°	≈0	UNM*	UNM*	FLAT	UNM*
5	251Ω	200Ω	-0.2°	≈0	UNM*	UNM*	FLAT	UNM*
10	110Ω	200Ω	-0.4°	-0.5%	UNM*	UNM*	FLAT	UNM*

*UNM : UNMEASURABLE DISTORTION

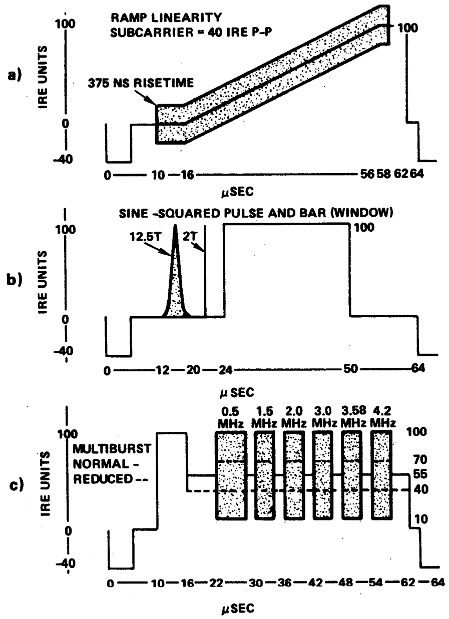


Figure 3—Video Test Signal Waveforms

S/N RATIO

Signal/noise (S/N) ratio measurements were made using the same basic amplifier configuration, but with Rgain fixed at 251Ω, ±1%, and Rs at 200Ω ±5%. The dc power supply terminals were bypassed with a 100 μ F tantalum capacitor. A Tektronix 147A NTSC Test Signal Generator was used as a signal source, with output measurements made using a Rhode & Schwartz Video Noise Meter, as diagrammed in Figure 4. The Tektronix 147A was set to deliver a flat field signal at 50 IRE units, with the R&S Video Noise Meter adjusted as follows: (a) 10kHz High pass, (b) Video Bandpass, (c) Subcarrier Trap OFF, (d) Internal Sync, (e) Tilt & Sag Comp OFF.

Under the specified conditions and with level control R1 adjusted to deliver a 1.0V p-p signal at J2, the measured p-p signal/RMS noise ratio averaged 68dB, or well over the minimum value required by applicable standards.

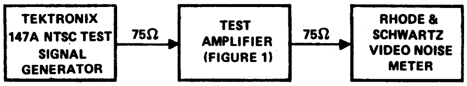

TEKTRONIX 147A NTSC TEST SIGNAL GENERATOR
75Ω
TEST AMPLIFIER (FIGURE 1)
75Ω
RHODE & SCHWARTZ VIDEO NOISE METER

Figure 4—S/N Ratio Test Setup

GENERAL CONSIDERATIONS

Since the HA-5190/5195 devices do not require special treatment, optimum video performance can be achieved by observing standard high frequency design and wiring practices. However, the following suggestions, abstracted in part from HARRIS Application Note 525, should prove helpful when developing practical designs.

POWER SUPPLY REQUIREMENTS

A well-regulated, well-filtered dual dc power source is required for best operation, for the op amps draw moderate currents during normal operation. Although not essential in all applications, it is recommended that the power supply lines be decoupled using 0.01 μ F ceramic capacitors to circuit ground, with the capacitors located as near to the amplifier terminals as possible to minimize lead inductances. For optimum performance and operation at specified parameters, the dc power supply should furnish not less than ±10V dc, with higher source voltages (±15V, typically) preferred.

TEMPERATURE CONSIDERATIONS

The HA-5190/5195 devices can be used without heat sinks at ambient temperatures up to 75°C. Under these conditions, the internally generated heat stabilizes device operation and ensures relative immunity to external temperature variations. At ambients above 75°C, however, the devices should be derated at 8.7mW/°C, with a suitable heat sink, such as a THERMALLOY Model 6007, used to provide adequate heat dissipation. At temperatures up to +125°C, the thermal resistance of the heat sink should be no greater than 30.6°C/W.

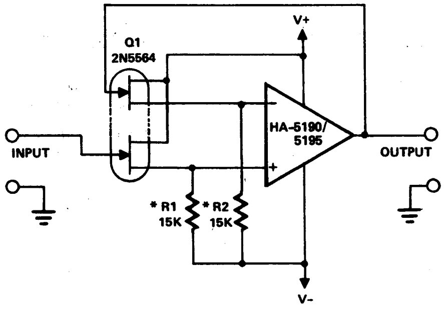
Under some conditions, the internally generated heat can affect other components. Therefore, avoid mounting temperature sensitive devices or components near or directly adjacent to the op amps.

DESIGN HINTS

Except for their exceptional performance specifications, the HA-5190/5195 devices are essentially standard op amps and may be treated as such by the video equipment or system designer. Thus, conventional design techniques may be used when developing specific circuit configurations, as long as maximum ratings are observed and adequate compensation is made for device operational characteristics. For example, the closed loop performance (dc and ac) at gains≥5 depends on both the feedback component ratio and the actual impedance at each amplifier input. Since the devices offer a comparatively low input impedance, feedback network resistor values should be 5k or less (preferably, less than 1k) for optimum high frequency performance.

If the intended video application requires a high input impedance, a FETpreamp stage may be added ahead of the HA-5190/5195 op amp, as shown in Figure 5. Full details and an additional FET input circuit are provided in HARRIS Semiconductor Application Note 525.

Where used, a FET preamp not only raises the effective input impedance from (approximately) 10k to thousands of megohms, but also reduces the input bias current requirement by several orders of magnitude. There is, of course, a trade-off in frequency response, with a FET input stage reducing the effective overall slew rate from 200V/µs to 130V/µs (typically). However, the full power bandwidth with a FET input is more than adequate for all low to mid level video applications.



*Approximate Values

Figure 5– FET Input Circuit

Some video applications may require output currents which exceed the maximum capabilities of the HA-5190/5195 devices. In these cases, the HA-5190/5195 op amps can be teamed with high performance current boosters such as, for example, the HA-2630/2635 devices. A typical cascaded op amp/booster circuit is illustrated in Figure 6. Since the current booster, a unity gain device, has a typical slew rate and bandwidth (Slew rate 500V/µs, BW 8.0MHz) far greater than that of the op amp, the overall frequency performance of the composite amplifier is essentially that of the op amp alone.

To compensate for manufacturing tolerances and ensure optimum performance, the fixed component values used in specific designs should be finalized empirically, using active devices from several production runs.

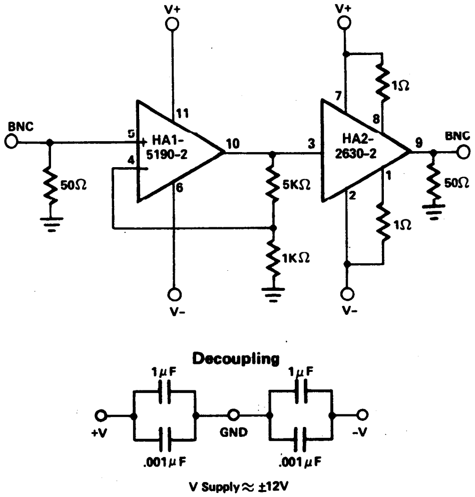


Figure 6—Boosting Output Current

PROTOTYPING TIPS

In accordance with standard engineering practice, new circuit designs should be breadboarded to verify overall operation. Afterwards, a number of preproduction prototypes identical to the planned production design should be assembled and tested using active devices from several production runs. These prototype tests permit optimization of component values and determination of circuit sensitivities to layout and component positioning. Preliminary environmental tests, if required, also may be made using the prototypes.

If IC sockets are used, Teflon types are preferred to minimize distributed capacitances. For the same reason, feedback components should be mounted between Teflon insulated standoffs located as close as practicable to the device pins or socket terminals. For maximum stability, film type resistors are recommended for the feedback networks.

Signal carrying leads should be kept short and direct, of course, to minimize both lead inductances and distributed capacitances. The devices should be mounted through a ground plane cr, if this is impracticable, single point grounding should be used to avoid ground loops.

TYPICAL APPLICATIONS

The test circuit given in Figure 1 may be used as a general purpose video amplifier, although minor changes in component values may be needed to optimize operation for specific requirements. Additional practical circuits are illustrated in Figures 7 and 8.

RF AGC AMPLIFIER

Designed and checked as a buffer for the head pre-amp of a studio video tape recorder, the circuit shown in Figure 7 functions as a wide band adjustable AGC amplifier. With an effective bandwidth of approximately 10 MHz, it is capable of handling RF input signal frequencies from 3.2 to 10MHz at levels ranging from 40mV up to 3V p-p.

AGC action is achieved by using opto coupler/isolator OCI as part of the gain control feedback loop. In operation, the positive peaks of the amplified output signal drive the OCI LED into a conducting state. Since the resistance of the OCI photosensitive element is inversely proportional to light intensity, the higher the signal level, the lower the feedback resistance to the op amp inverting input and hence the greater the negative feedback, thereby lowering stage gain. Any changes in gain occur smoothly because the inherent memory characteristic of the photoresistor acts to integrate the peak signal inputs. In practice, the stage gain is adjusted automatically to a point where the output signal positive peaks are approximately one diode drop above ground.

GAIN SET control R5 applies a fixed dc bias to the op amp non-inverting input, thus establishing the steady-state zero input signal current through the OCI LED and determining the signal level at which AGC action begins. In experimental tests under large signal conditions (i.e., E_{IN} = 3V p-p), a GAIN SET value of -0.26V provided unity gain, while a value of -1.55V yielded on A_V of 2.7 , with a flat response to 5.0MHz at both levels. Under small signal conditions (i.e., E_{IN} = 40mV), gains from 8 to 50 could be achieved as the GAIN SET value was adjusted from 0.65V to -80mV. At A_V = 8, the frequency response was flat to 5MHz, while at A_V = 80, the response was limited to that of the HA-5190/5195.

The effective AGC range depends on a number of factors, including individual device characteristics, the nature of the RF drive signal, the initial setting for R5, et al. Theoretically, however, the AGC range can be as high as 4000:1 for a perfect op amp, for the OCI photoresistor can vary in value from 1 Megohm with the LED dark to 250Ω with the LED full on.

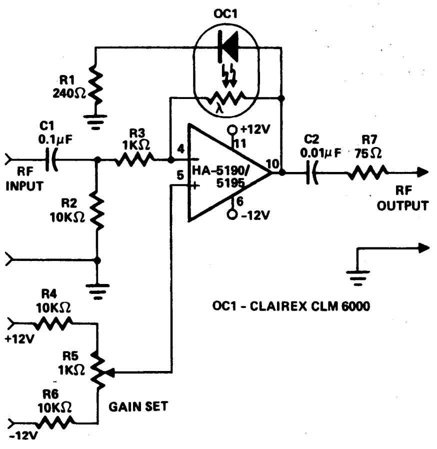
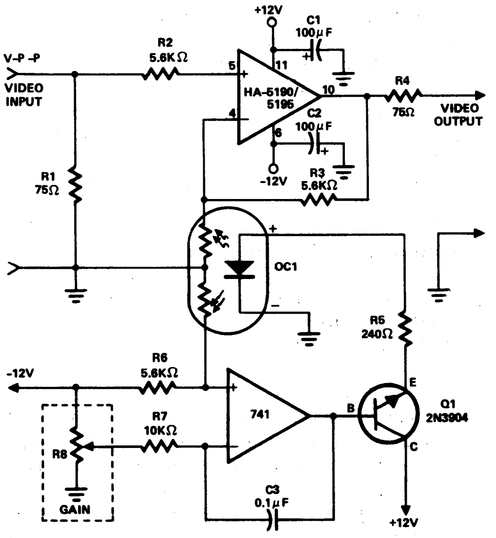


Figure 7–RF AGC Amplifier



OC1-CLAIREX CLM 8500/2
C1, C2 - TANTALUM TYPES

Figure 8– DC Gain Controlled Video Amplifier (Analog Multiplier)

DC GAIN CONTROLLED VIDEO AMPLIFIER

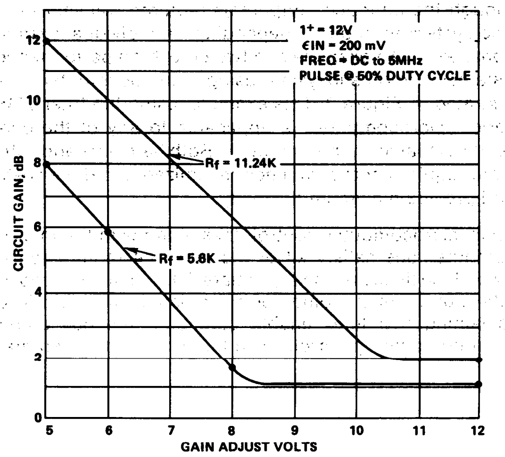
Suitable for use in virtually any application requiring a variable gain wideband or video amplifier, the circuit illustrated in Figure 8 employs a cascaded op amp integrator and transistor buffer (Q1) to drive the amplifier gain control element. Except for a simple modification, the HA-5190/5195 stage is connected as a conventional non-inverting operational amplifier, and includes input and output impedance matching resistors R1 and R4, respectively, series stabilization resistor R2, and power supply bypass capacitors C1 and C2. The circuit differs from standard designs in that the gain control network includes a photoresistor, part of OCI.

Referring to the schematic diagram, opto coupler/isolator OCI contains two matched photoresistors, both activated by a common LED. The effective resistances offered by these devices is inversely proportional to the light emitted by the LED. The greater the current through the LED, then, the more intense its light emission, and the lower the effective values of the photoresistors. One photoresistor is part (with R3) of the HA-5190/5195 gain network, while the other forms a voltage-divider with R6 to control the bias applied to the integrator non-inverting terminal.

In operation, the dc voltage supplied by GAIN control R8 is applied to the integrator inverting input terminal through input resistor R7. Depending on the relative magnitude of the control voltage, the integrator output will either charge or discharge C3. This change in output, amplified by Q1, controls the current supplied to the OCI LED through series limiting resistor R5. This action continues until the voltage applied to the integrator non-inverting input by the R6-photoresistor voltage divider matches the control voltage applied by R8 to the inverting input. At the same time, of course, the ratio of the R3-photoresistor gain network is changing, adjusting the op amp stage gain. As the control (R8) voltage is readjusted, the OCI photo-resistances track these changes, automatically readjusting the op amp gain in accordances with the new control voltage setting.

In experimental tests with typical devices, the amplifier gain could be varied from 12dB to 2dB as the dc control voltage was changed from 5.0 to 10.5Volts. Typical plots of stage gain (A_V) versus control voltage (V) are shown in Figure 9.

Since all temperature sensitive components are inside the integrator feedback loop, the circuit is quite stable with respect to changes in the ambient temperature.



ACKNOWLEDGEMENTS

A. J. Carl Cooper of HARRIS CVS (Consolidated Video Systems), 1255 E. Arques Ave., Sunnyvale, CA. 94086, developed the basic circuits described herein and, in addition, devised and executed the initial evaluation and performance tests.

B. Richard Whitehead and Robert Junkins of HARRIS SEMICONDUCTOR, P.O. Box 883, Melbourne, Fla. 32901, carried out additional confirmation tests of circuit performance and made other significant contributions to this publication.

REFERENCES

1. HA-5190/5195 Wideband, Fast Settling Operational Amplifiers (Harris data brochure)

2. Application Note 525 - HA-5190/5195 Fast Settling Operational Amplifier. May 1979.

3. EIA STANDARD RS-170A - Color Television Studio Picture Line Amplifier Output.

4. EIA STANDARD RS5-250-B - Electrical Performance Standards for Television Relay Facilities.

APP NOTE

FOR YOUR INFORMATION

No. 529

Harris Analog

MICROPROCESSOR INTERFACE METHODS FOR HIGH-SPEED DATA ACQUISITION SYSTEMS

By L. E. Enriquez, J. E. Sullivan, D. T. Tung, T. Westenburg

Since their introduction in the early 1970's microprocessors have dramatically displaced random logic for system design. This explosive growth of microprocessor applications has greatly influenced the increased use of peripheral interface integrated circuits (IC's). These special IC's were developed to support CRT's, printers, floppy disks and other peripheral devices, but virtually none were offered for analog input signal conditioning and conversion. Typical systems using a single microprocessor board and multiple analog interface boards became commonplace due to the lack of suitable analog interface IC's. Today, new units are available which provide microprocessor compatibility with analog input signal conditioning and processing within a compact package. These new products permit the assembly of a complete analog interface and microprocessor system on a single board no larger than those used in the past for the microprocessor alone. The HY-9590 and the HY-9591 analog signal processors and the HI-574A family of Analog to Digital Converters (ADC) are state-of-the-art devices.

A typical analog to microprocessor interface (data acquisition subsystem) consists of five functional blocks. (See Figure 1). Multiple input signals are accepted and selected by the input multiplexer, with the programmable gain instrumentation amplifier providing both common mode signal rejection and signal amplification. Additional signal processing is required between the output of the instrumentation amplifier and the ADC, for the latter connot convert a continuously changing analog signal into digital form. The additional processing is provided by the track-and-hold stage, which samples the instantaneous value of the analog signal on command and holds this level as a steady input to the ADC until the conversion cycle is completed. The ADC supplies a series of digital output words, which correspond to the individually sampled analog levels. Finally, digital logic circuitry is required to interface the function control signals from the microprocessor to the individual circuit elements.

As shown by the dotted lines in Figure 1, two devices, the HY-9590 (or the HY-9591), and the HI-574A contain all of the necessary analog and digital building blocks needed, for a complete two package, multi-channel data acquisition subsystem. The HY-9590 includes an eight-channel differential input multiplexer, a precision gain programmable instrumentation amplifier and a unity gain track-and-hold stage. Designed for 16-channel pseudo-differential or single-ended applications, the HY-9591 features a 16-channel multiplexer, a precision gain programmable instrumentation amplifier and a unity gain track-and-hold amplifier. All input control lines are microprocessor compatible and well suited for NMOS, CMOS, and TTL logic.

The HI-574A, 674A and 774A are a high speed, 12 bit ADC family which features a microprocessor compatible three-state output bus and software programmable output format permitting its application in 8, 12, and 16-bit systems. Accepting either unipolar or bipolar inputs, the device incorporates input latches on all digital control lines, assuring full compatibility with TTL, CMOS, and NMOS logic. The unit also features an on-board, overridable, precision +10 volt reference with sufficient output current capability for external applications.

When used in combination, the HY-9590 (or 9591) and the HI-774A form a high performance, extremely acccurate two-package data acquisition subsystem with a 100KHz throughput rate with optimized timing. The system is compatible with all standard microprocessor systems although the interface peripherals required will vary from one system to another, depending on individual system complexity. An example of a two chip, high performance data acquisition subsystem using a microcomputer is illustrated in Figure 2. This example, using the Intel 8748 series microcomputer, is applicable to any of the currently available microcomputers. Both hardware and software requirements have been minimized to reduce costs and provide maximum flexibility.

Four microcomputer control lines along with the microcomputer bus satisfy all of the interface requirements. Two of the lines are used to initiate data conversion and to interrupt the microcomputer when data is available. The remaining two lines enable data onto the bus under microcomputer control. The bus is structured so that channel selection, amplifier gain and ADC modes of operation are controlled by simply outputting data to the bus. Input data is in the form of two bytes: the first byte contains the most significant eight bits with the second byte continuing the least significant four bits, and four trailing zeroes.

The complete DAS operates under software control for maximum flexibility. A microcomputer internal software timing loop establishes the necessary hardware timing signals. The software flowchart in Figure 3 illustrates typical system operation.

The system depicted in Figure 2 operates at a 50KHz throughput rate, but can be optimized for 100KHz throughput by implementing overlapped timing (see Figure 3). Similar high performance DAS's systems can be implemented for a variety of applications and offering compatibility with most microcomputers.

Interfacing a DAS to a microprocessor system bus is similar to interfacing any other perhipheral device. Figure 4 illustrates an interface for an Intel 8085A microprocessor system and is similar to most popular microprocessors.

As with any peripheral device an address selection technique must be used to select specific devices. In small systems a simple bit flag and latch can be implemented, but in larger systems an address decoder or PIA is better suited. The circuit in Figure 4 uses two separate addresses, one for the Signal Processor and one for the ADC. This allows the use of overlapped timing for higher throughput rates. When a conversion is initiated status (STS) will go high, this places the track & hold into the hold mode. The MSB decision is approximately 600ns after STS goes high which leaves a safe margin for the track & hold to settle (hold mode settling = 250ns max).

While the conversion is underway the signal processor can be set up for the next conversion. By selecting the next channel and gain now, the input to the track & hold will have time to settle before the next conversion is initiated. When STS goes low the processor is interrupted and directed to a read routine, simultaneously the track and hold goes into track and acquires the new input voltage. As soon as the read cycle is complete, another conversion can be initiated.

This system could be further enhanced by using a 16-bit processor, which eliminates the two byte read operation. It actually eliminates both the second byte read and a move (MOV) command used for storing the first byte. Another method would be to add latches on the output of the HI-774A, this reduces the inactive time for the converter. If latches are implemented they can be clocked by the falling edge of STS, if R/C is high at least 650ns before the end of conversion.

Further enhancement of system performance can be achieved with Direct Memory Access (DMA), FIFO's and other circuits to alleviate the high speed data handling requirements that a 100kHz throughput DAS places on the microprocessor.

In conclusion, a single board microprocessor DAS can now be easily implemented using newly available analog interface devices. These devices not only support the requirements of microprocessor system buses but provide superior performance compared to discrete designs, while using far less printed circuit (PC) board real estate. The versatile HY-9590, HY-9591, and the HI-574A family offer ideal solutions for these and other applications requiring high performance, and cost-effective microprocessor interface capability.

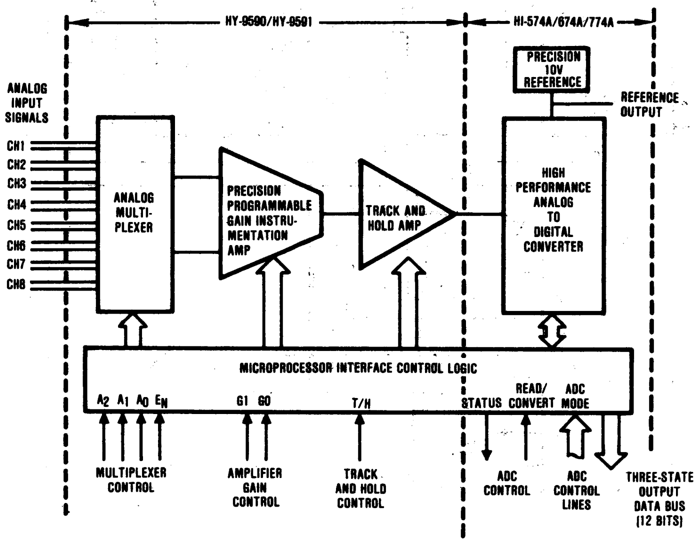

HY-9590/HY-9591
HI-574A/674A/774A
ANALOG INPUT SIGNALS
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
ANALOG MULTI-PLEXER
PRECISION PROGRAMMABLE GAIN INSTRU-MENTATION AMP
TRACK AND HOLD AMP
PRECISION 10V REFERENCE
REFERENCE OUTPUT
HIGH PERFORMANCE ANALOG TO DIGITAL CONVERTER
MICROPROCESSOR INTERFACE CONTROL LOGIC
A2 A1 A0 EN
G1 G0
T/H
STATUS
READ/ CONVERT
ADC MODE
MULTIPLEXER CONTROL
AMPLIFIER GAIN CONTROL
TRACK AND HOLD CONTROL
ADC CONTROL
ADC CONTROL LINES
THREE-STATE OUTPUT DATA BUS (12 BITS)

FIGURE 1. DATA ACQUISITION SUBSYSTEM

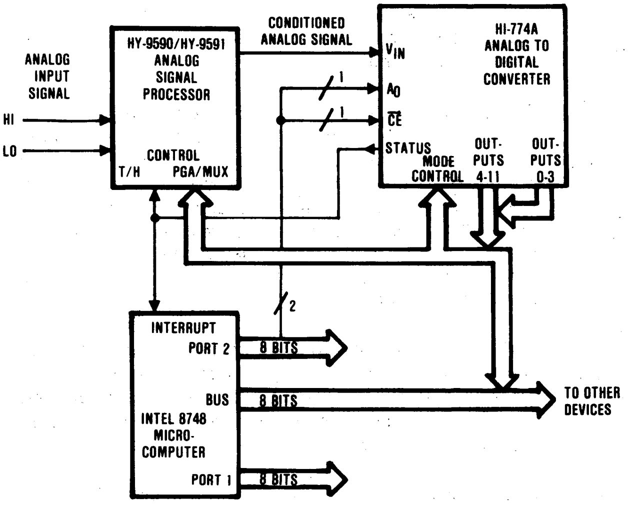

ANALOG INPUT SIGNAL
HI
LO
HY-9590/HY-9591 ANALOG SIGNAL PROCESSOR
CONTROL
T/H
PGA/MUX
CONDITIONED ANALOG SIGNAL
HI-774A ANALOG TO DIGITAL CONVERTER
V_{IN}
A_0
$\overline{CE}$
STATUS
MODE CONTROL
OUT-PUTS 4-11
OUT-PUTS 0-3
1
1
2
INTERRUPT
PORT 2
8 BITS
BUS
8 BITS
INTEL 8748 MICRO-COMPUTER
PORT 1
8 BITS
TO OTHER DEVICES

FIGURE 2. MICROCOMPUTER WITH HIGH PERFORMANCE DATA ACQUISITION SUBSYSTEM

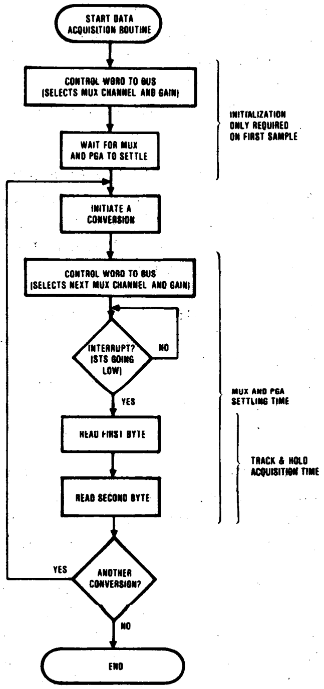

START DATA ACQUISITION ROUTINE
CONTROL WORD TO BUS (SELECTS MUX CHANNEL AND GAIN)
WAIT FOR MUX AND PGA TO SETTLE
INITIALIZATION ONLY REQUIRED ON FIRST SAMPLE
INITIATE A CONVERSION
CONTROL WORD TO BUS (SELECTS NEXT MUX CHANNEL AND GAIN)
INTERRUPT? (STS GOING LOW)
NO
YES
MUX AND PGA SETTLING TIME
READ FIRST BYTE
TRACK & HOLD ACQUISITION TIME
READ SECOND BYTE
ANOTHER CONVERSION?
YES
NO
END

FIGURE 3. SOFTWARE FLOW CHART

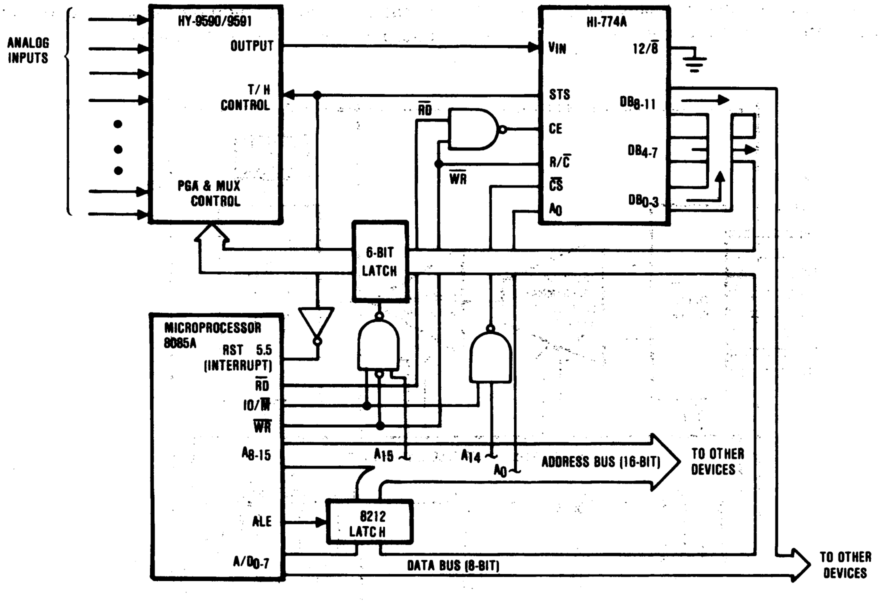

ANALOG INPUTS
HY-9590/9591
OUTPUT
T/H CONTROL
PGA & MUX CONTROL
HI-774A
V_{IN}
$12/\overline{8}$
STS
DB_{8-11}
CE
$R/\overline{C}$
DB_{4-7}
$\overline{CS}$
A_0
DB_{0-3}
$\overline{RD}$
$\overline{WR}$
6-BIT LATCH
MICROPROCESSOR 8085A
RST 5.5 (INTERRUPT)
$\overline{RD}$
$IO/\overline{M}$
$\overline{WR}$
A_{8-15}
ALE
A/D_{0-7}
A_{15}
A_{14}
A_0
ADDRESS BUS (16-BIT)
TO OTHER DEVICES
8212 LATCH
DATA BUS (8-BIT)
TO OTHER DEVICES

FIGURE 4.

No. 530
Harris Analog

A DATA ACQUISITION AND CONVERSION SYSTEM WITH LESS THAN ±1 LSB OFFSET ERROR

By John E. Sullivan

The continuing pressure for higher resolution and higher accuracy Data Acquisition Systems requires smaller overall system offset errors. Historically, with eight-bit systems, offsets of up to 30 or 40 millivolts were acceptable, and the use of trimpots or fixed resistors for adjustment was more than adequate. State-of-the-art systems with 12 to 16-bit resolution, however, require total system offset over temperature to be less than 5 millivolts. Offset voltages of this magnitude are difficult to achieve using trimpots, and extremely difficult to stabilize in uncontrolled thermal environments.

Ideally, a DAS system should have less than ±1 LSB of offset error regardless of the number of bits incorporated in the system. This goal is extremely difficult to achieve using linear design techniques. Digital design techniques, however, can be used to null offsets, typically to ±1/2 LSB over the complete temperature operating range.

A typical Data Acquisition System is illustrated in Figure 1. System offset correction can be accomplished at any stage even though each stage contributes to the overall offset. The first step to offset correction is to have the analog to digital converter (A/D) calculate the digital code representing total system offset when the input is grounded. This code, when converted back to analog form, inverted and added to the input circuitry at a convenient point, will null all offsets.

Figure 2 shows a simple digital offset correction scheme. The additional digital to analog converter (D/A) U3 and op amp U2 convert the calculated digital offset code back to analog form. Op amp U1 inverts this signal and adds it to the input differential amplifier. The inverted signal is scaled by resistors RA and RB such that a 1LSB step of the A/D is equal but opposite in sign to a 1LSB step of the D/A at TP1. This scaling can be calculated by Equation 1.

Equation 1

$$\frac{VP_1}{2^{n_1}} = \frac{RA}{RB} \cdot \frac{VP_2}{2^{n_2}}$$

Where:
VP_1 = Dynamic range of Linear A/D in volts
n_1 = Number of Bits of A/D
VP_2 = Dynamic Range of Linear D/A in volts
n_2 = Number of Bits of D/A
RA = Feedback Resistor
RB = Input Resistor

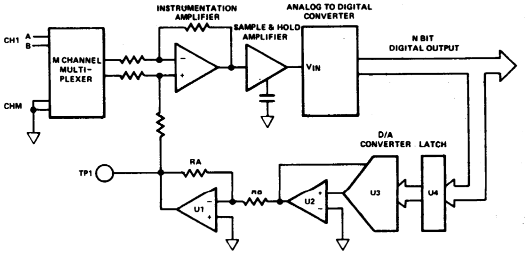

INSTRUMENTATION AMPLIFIER
ANALOG TO DIGITAL CONVERTER
SAMPLE & HOLD AMPLIFIER
N BIT DIGITAL OUTPUT
CH1
A
B
M CHANNEL MULTI-PLEXER
CHM
V_{IN}
D/A CONVERTER
LATCH
TP1
RA
RB
U1
U2
U3
U4

Figure 1 — Typical Data Acquisition Block Diagram

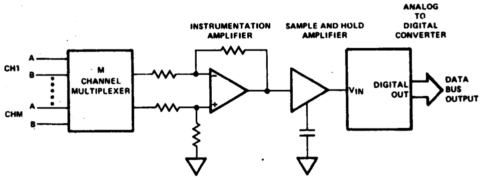

INSTRUMENTATION AMPLIFIER
SAMPLE AND HOLD AMPLIFIER
ANALOG TO DIGITAL CONVERTER
CH1
A
B
A
CHM
B
M CHANNEL MULTIPLEXER
V_{IN}
DIGITAL OUT
DATA BUS OUTPUT

Figure 2 - Digital Error Correction Block Diagram

Measurement of the system offset is made with all digital input bits to the D/A set at logic 0. Further, the D/A is configured for bipolar operation so that a digital input bits to the D/A set at logic 0. Further, the D/A is configured for bipolar operation so that a digital zero input results in a positive half full scale output voltage at TP1. This ensures that the A/D need only measure positive offset voltages and not negative voltages, allowing for systems operating both in uinpolar and bipolar modes.

The size of the D/A converter is determined by the maximum amount of offset that must be corrected by the system:

Equation 2

$$\text{D/A Size (Bits)} \geq \frac{\dfrac{\ln\ (\text{Max offset} \quad 2^{n1})}{VP_1}}{\ln(2)}$$

In operation, a spare input channel is grounded and the input to the D/A is forced to digital zero. The resulting compound offset, Voffset, is then equal to the voltage at TP1 plus all component offsets. The A/D then calculates a digital code representing V_{offset} which is latched into the D/A. Due to the inversion and scaling of the Op Amp U2, this is equivalent to subtracting Voffset from the half full scale output of the D/A. Obviously the result is the nulling of V_{offset}.

The most critical parameter in this circuit is the ratio of the resistors RA and RB. This ratio will determine the overall accuracy of the correction, and 1% resistors are sufficiently accurate to null all offsets. Normally for 12 and 14-bit systems, a 6-bit DAC will correct all possible offsets.

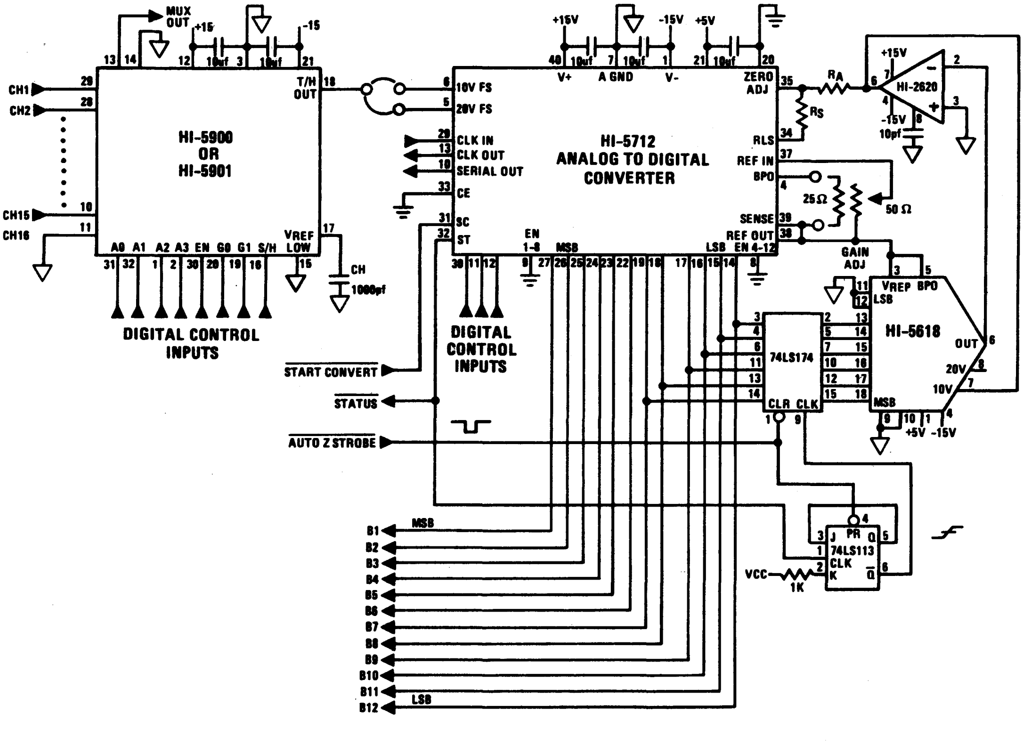

MUX OUT
+15
-15
10uf
10uf
CH1
CH2
CH15
CH16
HI-5900 OR HI-5901
T/H OUT
VREF LOW
A0 A1 A2 A3 EN G0 G1 S/H
CH 1000pf
DIGITAL CONTROL INPUTS
+15V
-15V
+5V
V+
A GND
V-
10V FS
20V FS
CLK IN
CLK OUT
SERIAL OUT
CE
SC
ST
HI-5712 ANALOG TO DIGITAL CONVERTER
ZERO ADJ
RLS
REF IN
BPO
SENSE
REF OUT
EN 1-8
MSB
LSB
EN 4-12
DIGITAL CONTROL INPUTS
START CONVERT
STATUS
AUTO Z STROBE
RA
RS
HI-2620
10pf
25Ω
50 Ω
GAIN ADJ
74LS174
CLR CLK
HI-5618
VREF BPO
LSB
MSB
OUT
20V
10V
+5V -15V
J PR Q
74LS113
CLK
K Q̄
VCC
1K
B1 MSB
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12 LSB

Figure 3 – Auto-Zero Analog to Digital Converter

Various configurations can be employed to minimize parts count. Fully automatic offset correction is added to the HI-5900/HI-5712 DAS component set using only four additional I.C.'s as shown in Figure 3. External digital logic or a microprocessor selects a spare input channel which has been previously grounded. Receipt of the Auto-Z strobe initializes the auto-zero function by clearing the latch to all zeroes, resulting in a D/A output of 32 LSB's of positive offset. The microprocessor then initiates an analog to digital conversion sequence. The Conversion Complete status line of the A/D causes the latch to strobe and store the digital offset correction term to the D/A converter. The analog correction term is then injected into the zero adjust pin of the A/D converter. Care must be taken when injecting the correction term to this point on the A/D since the ratio of RA/RB is affected by the impedance of the summing junction.

Table 1 lists the accuracy of correction for various full scale input ranges. The offset after correction listed in the Table is the maximum observed offset when 10 different 5900's and 5712's were tested at all temperature ranges between -55°C, and +125°C ambient. In no case did the offset after correction ever exceed 1LSB of the analog to digital converter.

HI-5712 INPUT CONFIGURATION	R_S	R_A	OFFSET AFTER CORRECTION
0 TO +10V	681Ω	147kΩ	0.5mV
0 TO +20V	825Ω	147kΩ	1.0mV
-5V TO +5V	580Ω	147kΩ	1.0mV
-10V TO +10V	681Ω	147kΩ	2.0mV

Table 1 — Offset Correction Accuracy

Along with the straight forward benefit of greatly improved offset performance, this correction technique eliminates the requirement for any offset adjustments, either initially or during the operating life of the DAS. In practice, the auto-zero function need only to be used after system power is applied or after a significant change in ambient temperature. Therefore, high performance microprocessor-based DAS systems requiring maximum performance can employ this technique to improve accuracy with minimal impact on throughput rate.

APP NOTE

FOR YOUR INFORMATION

No. 531

Harris Analog

ANALOG SWITCH APPLICATIONS IN A/D DATA CONVERSION SYSTEMS

By Richard Whitehead

INTRODUCTION

A choice of three approaches is available when implementing a data conversion system: 1). "build-from-scratch", 2) buy sub-systems and configure a system, or 3) purchase a pre-engineered system which meets the requirements. Also, as a matter of economics, the users of sensor-based data acquisition systems make it common practice to ensure a maximum number of elements are shared in the system. An invaluable tool used in this process is the analog switch or multiplexer. The purpose of this article is to focus attention on those parts of the system which require analog switches and to emphasize the importance of relative operating parameters.

BASIC SYSTEM CONFIGURATIONS

A/D data conversion systems can be categorized into two general groups: 1) low level signal conversion (analog signals below 1 volt) and 2) high level signal conversion (analog signals above 1 volt). Within these categories, four basic data conversion configurations are illustrated to point out the advantages of using analog switches.

Conditioning the analog signals prior to multiplexing (Figure 1A) is the most popular system arrangement and is both efficient and capable of high performance This configuration, which shares the level signals. Figure 1B represents a more austere approach resulting in lower cost and decreased performance. This type is useful in less demanding applications such as processing high level signals. To process multichannel, single event information such as wind tunnel or seismographic measurements the arrangement shown in Figure 1C is most likely to be used. This configuration represents a more expensive, less efficient approach due to the decreased number of shared elements. Figure 1D shows the elimination of the analog multiplexer and sample and hold circuits. By moving the multiplexing task to the digital domain, slower and lower cost A/D converters can be used.

TYPES OF ANALOG SWITCHES

The most commonly used types of analog switches found in today's data conversion systems are: reed relay, JFET, and CMOS. Reed relays offer low ON and high OFF resistance and are capable of handling very high voltages, but have slow speeds. JFET switches have lower OFF leakage current and are capable of very high speeds. CMOS switches, which are the most popular and widely used in multiplexer applications, have low OFF leakage currents, good speed, and stable ON resistance under varying input signal conditions.

SELECTING THE PROPER CMOS ANALOG SWITCH

The data conversion system error budget should be used to narrow the field of CMOS analog switches suitable for the application. Primarily, the speed of the switch must be consistent with the systems's sample rate requirements without introducing unacceptable transfer error. Significant dynamic errors inherent to CMOS analog switches are OFF channel leakage current and a settling time value dictated by the device's ON resistance and its inherent capacitance. Figure 2 shows the equivalent of a CMOS analog switch giving all of the inherent and distributed properties which may become the source of unwanted system errors.

Other system restrictions may further narrow the field of candidates suitable to performing the switching task. These restrictions could include, low power budget, hostile environment, cost, alternate sourcing, and package density. It's possible that all of these restrictions could occur, and this situation mat influence the user to seek a compromise solution to his problem.

Fortunately, CMOS analog switches consume very little power and only the most demanding power budget would feel the strain of their power requirements. If the poerating environment of the device includes high voltage spikes, excessive noise pickup, and/or power supply interruptions, the selection should be narrowed to the internally protected analog multiplexers such as the HARRES HI-506A/507A or the HI-546/547. These multiplexers come with guaranteed overvoltage specifications which engance the reliability of the data conversion system. They also insure output signal integrity while an overvoltage condition occurs on an unselected channel. It should also be ensured that the CMOS analog switch selected does not exhibit any inherent latch-up tendencies. The Harris dielectrically isolated CMOS analog switches offer latch free operation.

To some users the proper CMOS analog switch selection may become complicated leading to possible alternate solutions. An example of such a situation could be in high speed data conversion system where the settling time constraint placed on the multiplexer results in an unacceptable time penalty (Figure 3A). Figure 3B shows an alternate and practical solution to this problem. The two tiered multiplexing scheme may reduce the errors caused by leakage currents and settling time by an order of magnitude. Another practical solution would be to select an analog signal processor such as the HARRIS HY-9590/9591 shown in Figures 4A and 4B. These devices facilitate user application and reduce engineering time thereby reducing overall cost.

OTHER USES FOR CMOS ANALOG SWITCHES

Attention has been focused on the selection of CMOS analog multiplexers used to increase efficiency of data conversion systems through shared elements. But the versatile CMOS switch is not limited to only that function. Obviously they can be used in sample and hold circuits, with important parameters being switching speed, OFF leakage current, and charge transfer. Analog switches such as the HARRIS HI-200/201 and HI-300 series may be used in sample and hold circuits and also in auto-zeroing circuits for integrating type data converters (Figure 5).

Figure 6 shows the CMOS analog switch used to program the gain of an instrumentation amplifier.

HIGHLIGHTS

In A/D data conversion systems analog switches are mainly used as multi-channel multiplexers to increase system efficiency through shared elements.

CMOS analog switches are the most widely used in data conversion systems.

When selecting the proper CMOS analog switch, look for low OFF leakage current, good settling time, latch free operation, and stable ON resistance under varying analog signal input conditions.

If the environment is histile, select from the internally protedted CMOS analog multiplexers.

Where an alternate solution is required, attempt to ensure your solution is the most practical with respect to your error budget.

References:

Garrett, Patrick H. Analog Systems for Microprocessors and Minicomputers. Virginia: Reston Publishing Company, Inc., 1978.

Kaufman, Milton and Seidman, Arthur H. Handbook of Electronic Calculations. New York: McGraw-Hill Book Company, 1979.

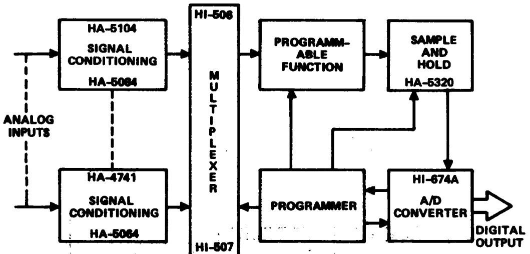


Figure 1A – Multiplexed. Signal Conditioning for Low Level Inputs

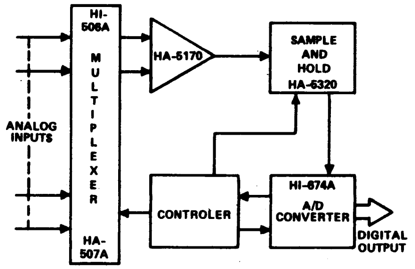

HI-506A
MULTIPLEXER
HA-507A
ANALOG INPUTS
HA-5170
SAMPLE AND HOLD HA-5320
CONTROLER
HI-674A A/D CONVERTER
DIGITAL OUTPUT

Figure 1B — Multiplexed. High Level Inputs

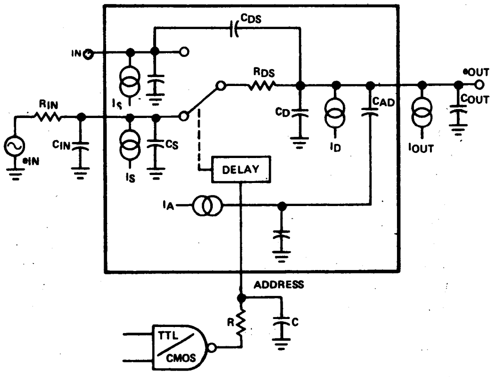

CDS
IN
RDS
OUT
RIN
IS
CD
ID
CAD
IOUT
COUT
CIN
eIN
CS
IS
DELAY
IA
ADDRESS
R
C
TTL
CMOS

Figure 2 — Equivalent CMOS ANALOG SWITCH
DC Offset Error = $R_{DS} \times I_D$
Setting Time Determined by $R_{DS} \times C_D$

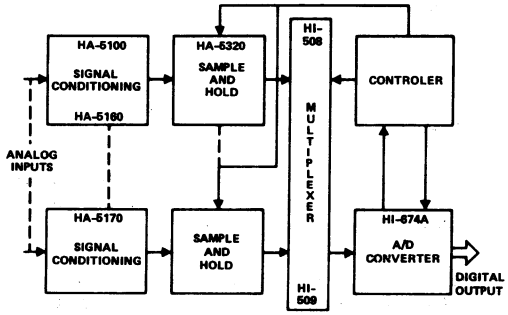

HA-5100
SIGNAL CONDITIONING
HA-5160
HA-5320
SAMPLE AND HOLD
HI-508
MULTIPLEXER
HI-509
CONTROLER
ANALOG INPUTS
HA-5170
SIGNAL CONDITIONING
SAMPLE AND HOLD
HI-674A
A/D CONVERTER
DIGITAL OUTPUT

Figure 1C — Multiplexed. Sample / Hold Outputs

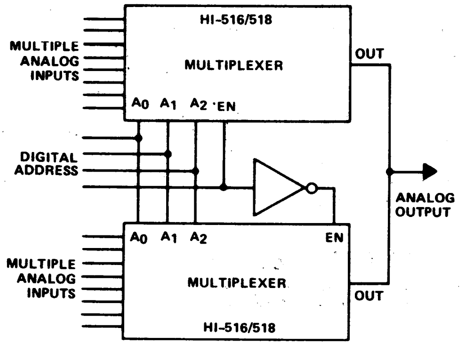

HI-516/518
MULTIPLEXER
MULTIPLE ANALOG INPUTS
A0 A1 A2 EN
OUT
DIGITAL ADDRESS
ANALOG OUTPUT
A0 A1 A2
EN
MULTIPLE ANALOG INPUTS
MULTIPLEXER
OUT
HI-516/518

Figure 3A — Cascaded Multiplexers: Output Leakage Currents and Output Capacitance Increase Errors

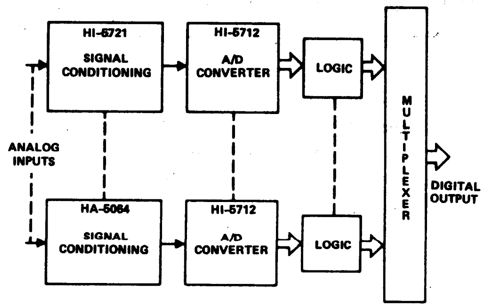

HI-5721
SIGNAL CONDITIONING
HI-5712
A/D CONVERTER
LOGIC
MULTIPLEXER
ANALOG INPUTS
DIGITAL OUTPUT
HA-5064
SIGNAL CONDITIONING
HI-5712
A/D CONVERTER
LOGIC

Figure 1D - Digitally Multiplexed A/D Outputs

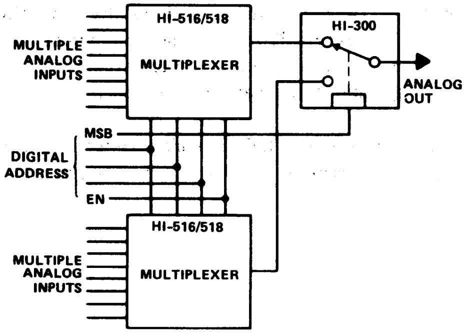

HI-516/518
MULTIPLEXER
MULTIPLE ANALOG INPUTS
HI-300
ANALOG OUT
MSB
DIGITAL ADDRESS
EN
HI-516/518
MULTIPLE ANALOG INPUTS
MULTIPLEXER

Figure 3B — Cascaded Multiplexers Two - Tiered Method: Errors Reduced Through Shared Switch

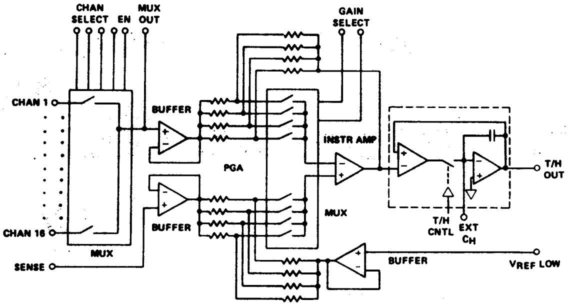

CHAN SELECT
EN
MUX OUT
GAIN SELECT
CHAN 1
CHAN 16
SENSE
MUX
BUFFER
BUFFER
PGA
INSTR AMP
MUX
T/H CNTL
EXT CH
T/H OUT
BUFFER
VREF LOW

Figure 4B - HI- 9591 Analog Signal Processor

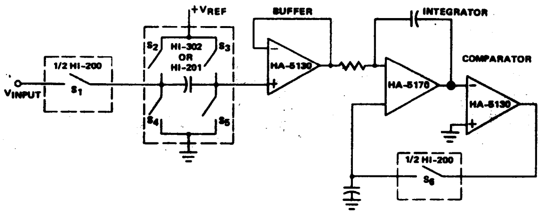

+VREF
BUFFER
INTEGRATOR
1/2 HI-200
S1
VINPUT
S2
HI-302 OR HI-201
S3
S4
S5
HA-5130
HA-5170
COMPARATOR
HA-5130
1/2 HI-200
S6

Figure 5. This autozero integrating converter uses six analog switches – S_1 through S_6. Zero correction occurs when S_3, S_4 and S_6 are "on". Integration occurs with S_1 closed. Integrate-reference takes place when S_2 or S_5 is "on".

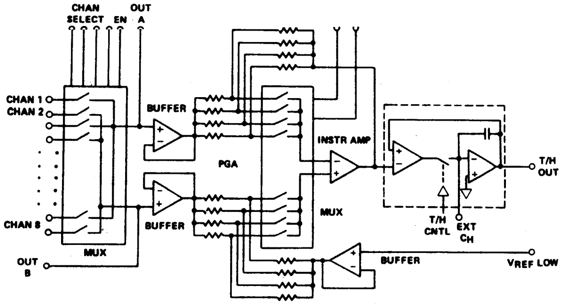

CHAN SELECT
EN
OUT A
CHAN 1
CHAN 2
CHAN 8
MUX
OUT B
BUFFER
BUFFER
PGA
INSTR AMP
MUX
T/H CNTL
EXT CH
T/H OUT
BUFFER
VREF LOW

Figure 4A - HY-9590 Analog Signal Pricessor

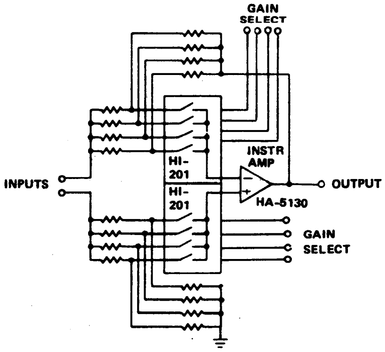

GAIN SELECT
INPUTS
HI-201
HI-201
INSTR AMP
HA-5130
OUTPUT
GAIN SELECT

Figure 6 – Programmable Gain Instrumentation Amplifier

APP NOTE

FOR YOUR INFORMATION

No. 532

Harris Analog

COMMON QUESTIONS CONCERNING CMOS ANALOG SWITCHES

By Carl Wolfe

INTRODUCTION

The following information is a direct result of a significant amount of time spent in response to questions from users of HARRIS analog switches. Among the variety of questions are a few which seem to be asked more frequently than others. Over the next few pages, these questions are discussed with the hope that the answers will be helpful to the users and potential users of HARRIS analog switches. Some questions are technical in nature while others are simply questions on interpretation of the HARRIS Analog Data Book.

POWER SUPPLY CONSIDERATIONS

The first two questions are similar questions and the explanation will apply to both:

QUESTION #1: If the power supplies are off, will the switch be open? (Present a high impedance to the input signal)

QUESTION #2: If the power supplies are off, can an input signal be applied?

Both of these questions refer to an overvoltage condition when the supplies are off and an input signal is applied. A common misunderstanding is that the switch will be open and block the signal when actually the opposite occurs.

What is meant by the power supplies being off? Does it refer to the supplies being shorted to ground or does it imply they are open circuited?

If the power supplies go to ground, the input signal will pass through the switch and appear at the output. The explanation for this can be seen in Figure 1, which is a simplified CMOS switch cell. This switch cell consists of two enhancement type field effect transistors, one N-channel and one P-channel. An enhancement type of device is a FET which is normally off without some potential (gate voltage) to turn it on. A P-channel FET requires a negative potential (gate to source voltage) to turn it on and an N-channel FET requires a positive potential (gate to source). Contained in the physical structure of the FETS are parasitic transitors which are shown in Figure 1 as diodes from the source and drain to the body potentials of the devices. These diodes or parasitic junctions are normally reversed biased. If those junctions are forward biased, a fault condition exists where the signal is passed through the parasitic transitor. This is what occurs if the power supplies go to ground. Depending on the polarity of the input signal, either the N or P channel FET parasitics will be forward biased and the signal passed through the switch.

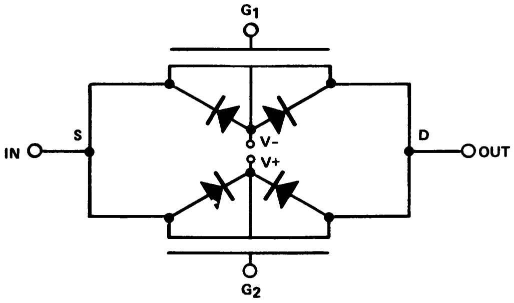


Figure 1. Basic CMOS Transmission Gate

Having the signal pass through the switch may be acceptable in some applications, but most likely it is not. An example would be user who was switching various voltages (transducers) as shown in Figure 2. If the supplies go to ground and these signals pass through the switch, the input voltage sources could easily be shorted.

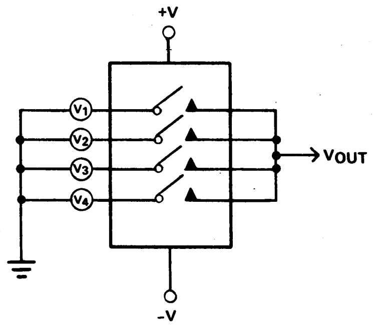


Figure 2. Switching Multiple Inputs

Another situation occurs if the power supplies are open circuited where the most positive and negative input signals will provide power to the switch. In this case, the signals being used for power will be passed to the output, but the remaining switches with inputs less than those used for supply will operate properly.

INPUT OVERVOLTAGE PROTECTION

There is a possibilty the switch will be damaged if exposed to excessive current levels during an overvoltage condition. A second overvoltage condition is the case where the input signals exceed the existing power supply levels. Neither of these situations are recommended and the following questions are similar to those frequently asked.

QUESTION #3: Can an input greater than the supplies be applied?

QUESTION #4: In my application, there is a possibility that the switch will lose power and the input signal will still be applied. Is there a way to protect the switch if this situation occurs?

Referring to Figure 1 once again, if the input signal exceeds the supply by an amount greater than the breakdown voltage of the parasitic junction, the normally reversed biased junction will come forward biased. These forward biased junctions will pass the input signals to the output and possibly short out the input voltage sources.

The most common form of protection circuit for these types of overvoltage conditions is the resistor-diode network at the input of the switch as shown in Figure 3.

This circuit protects the device if the supplies go to ground or if the input exceeds the supply. If either of these situations occur the diodes will be forward biased and current path to ground will exist. This will protect the switch from excessive current levels. The primary purpose of the resistor is to limit the current through the diode.

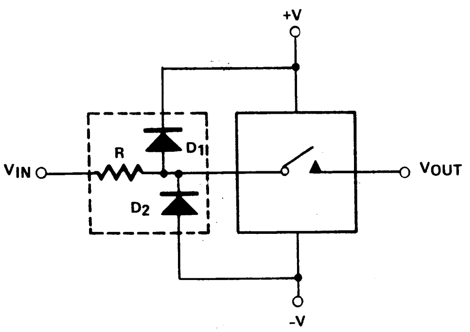


Figure 3. Protection for Each Analog Input

Another advantage of using diode protection is that it prevents the input signal from passing to the output. This is a result of the input being clamped to the breakdown voltage of the protection diodes. If this breakdown voltage is less than the threshold voltage (turn on voltage) of the parasitic diodes, the parasitic transistor will remain reverse biased and the signal will not pass through the switch.

There are some disadvantages to the user with this type of protection. One would be the economics involved with using external protection for each analog input. This could present a cost problem if a large number of channels were involved. Another concern would be the current limiting resistors which adds to the on resistance of the switch contributing to the overall system error. A further possible source of error is current leakage in the diodes. It is recommended that low leakage diodes, such as schottkey diodes be used.

The protection circuit just discussed is not used to protect the switch from latch up. The HARRIS switches are constructed using the dielectric isolation process and the four layer SCR found in JI technology does not exist. This circuit is intended to protect the device from high current levels which result from the forward biasing of the parasitic transistors which are inherent in all FET structures.

If for some reason the resistor-diode protection circuit cannot be used there are other possibilities. The following method may help to avoid the extra cost of protecting each input. In this method, since the supplies are open circuited, the most positive and most negative signal will power-up the chip and any input with signals less than those being used for power will operate properly. However, this method can only be used if the outputs are not common and a user can afford to have at least two signals pass to the output.

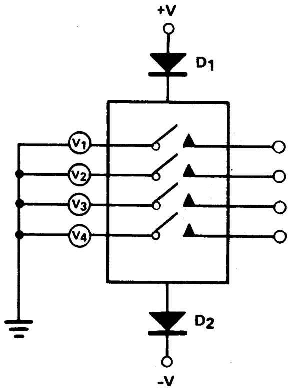


Figure 4. Powering the Switch With the Input Signals

Another alternative does not involve protection circuitry, but instead takes advantage of CMOS technology. An example would be a user who has ±15V supplies and needs to switch a +18V signal as shown in Figure 5. This appears to be an overvoltage condition since the input exceeds the supply. But rather than protect the device, the user can shift the supplies to +20V, -10V. Now the input signal is within the supply level and the switch should work properly. In certain applications the supply voltages can be adjusted in order to pass a larger range of input signals.

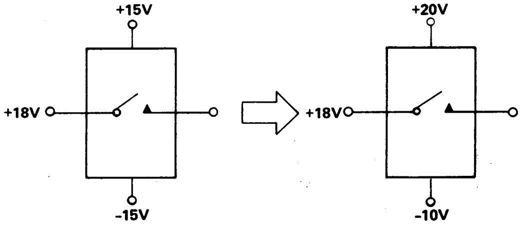


Figure 5. Varying the Supplies to Meet the $V_{IN} <$ V Supply Requirements

SINGLE SUPPLY OPERATION

Single supply operation is a topic which is discussed frequently and the following are examples of typical questions.

QUESTION #5: Can the switch be operated at a single power supply?

QUESTION #6: What is the minimum power supply possible?

Usually engineers with critical power requirements request single supply operation. An example would be battery operated applications such as portable equipment. In these cases the designer is limited to single supply, low supply or both.

Trade-offs exist with single supply operation that should be pointed out to the user. An example is the HI-300 series of switches which has the capability of operating with a single +5 volt supply. The performance of the switch will vary, however, as the supply voltage varies. So, for the HI-300 series, as supply voltage decreases, the on resistance and the switching times increase. A 300 series switch with a single +5 volt supply will have higher on resistance and slower switching speeds than the same device at ±15 volts or even a single +15 volt supply. This represents a change in both DC and AC performance. Even though the switch may now meet the users power requirements at single supply, the question is whether it will still meet the performance requirements.

The explanation for these variations can be found in the FET devices composing the switch cell itself. The variation in on resistance is due to the fact that the channel impedance of FET is dependent on the gate - source bias. Since the gate voltage is determined by the supply voltage, it can be concluded that the on resistance is a function of the supply voltage.

The fact that the on resistance varies with supply voltage directly relates to the slower switching times, since the higher on resistance will reduce the available current needed to charge the internal capacitance of the switch. Lower changing current relates directly to slower switching times.

QUESTIONS ABOUT HARRIS SWITCHES

Many of the questions asked about switches could apply to any CMOS switch manufacturer's products. But some questions are unique to both the Harris product line and data catalog. The following are examples of some of the more common questions concerning the Harris Analog Data Catalog.

QUESTION #7: What is the difference between the VL and VR pins on the HI-5043 and V_{REF} pins on the HI-201 ?

The device pins mentioned above have their own individual functions even though they are all associated wth the logic reference circuits of their respective designs. For the HI-201, the V_{REF} pin is the terminal which establishes the logic threshold levels for which the switch will change state. Although it is normally left open when driving from +5V logic (DTL or TTL), it can be connected to a higher supply in order to raise the switching threshold levels when driving from CMOS Logic greater than 5 volts. The V_{REF} pin enables the user to change from TTL to CMOS Logic.

The reference circuit of the HI-50XX series of switches is different from the HI-201, which accounts for the V_R and V_L pins. Even though the V_R terminal is brought out on the package, it is recommended that this pin be grounded. This terminal establishes the ground for the internal reference circuit. The V_L pin performs a similar function to the V_{REF} pin on the HI-201. It is normally connected to 5 volts for TTL logic but can be tied to a higher supply for CMOS levels. This effectively raises the switching thresholds to accomodate the higher CMOS level.

The next question is easily the most frequently asked question about HARRIS HI-50XX series of switches.

QUESTION #8: Are the switch functions shown on the data sheet a result of the logic address being HIGH or LOW ?

Actually, the answer to the question is printed at the top of the data sheet page,depicting switch functions "switch states are for a logic 1 input". Therefore, the address is in the HIGH state for the switch functions shown on that page.

Some other areas which are often questioned on the data sheets are the maximum ratings and performance between channels of the switches. The following questions are typical:

QUESTION #9: Will the switch operate at the absolute maximum ratings?

The topic of absolute maximum ratings does create some confusion. Basically, the contents of the Electrical characteristic table are the guaranteed parameters. The switch may operate with conditions other than those recommended, but are not guaranteed parameters. Anything above absolute maximum ratings may permanently damage the device.

Problems sometime arise when a customer tests some parts at conditions other than those which are guaranteed. If the parts work, the user may go ahead and design around these conditions. But there is a good possibility the next batch of switches may not perform in the same manner. The user must be aware that anything outside the guaranteed limits is a user's risk and susceptable to variations in manufacturing.

QUESTION #10: What is the variation in "on" resistance between channels on the switch?

There are two causes for these variation. One cause is process variation which is due to variables in manufacturing. This can create variation between channels on the same unit. The second reason is lot variation which can cause differences in performance from unit to unit. After all variations are taken into account, a good "rule of thumb" is ±10% tolerance on typical parameter values. So if a device has a typical on resistance of 50Ω , a user could expect a $\pm 5\Omega$ variation.

APP NOTE

FOR YOUR INFORMATION

No. 534

Harris Analog

ADDITIONAL INFORMATION ON THE HI-300 SERIES SWITCH

By Carl Wolfe

INTRODUCTION

The introduction of the HI-300 series of CMOS analog switches is the latest addition to the HARRIS switch family and gives the designer a viable second source to the Siliconix DG 300 series analog switch.

This family of monolithic, dielectrically isolated, CMOS analog switches consists of twelve products, the HI-300 thru HI-307 and the HI-381 thru HI-390 are designed for TTL level compatibility (logic "0" = .8V, logic "1" = 4.0V). The HI-304 thru HI-307 are CMOS compatible (logic "0" = 3.5V, logic "1" =11V).

The HI-300 series features low and nearly constant on resistance over analog signal range, low leakage and minimal power dissipation.

IMPROVED PERFORMANCE

An understanding of what a designer would consider important in an analog switch is useful in order to illustrate the advantage of the HI-300 series. Although any parameter could be considered important for a particular application, there are certain parameters considered to be most critical for the majority of applications. These parameters are:

"on" Resistance (Ron)
leakage current (I_{SOFF}, I_{DOFF}, I_{DON})
switching speed (ton, toff)
power supply current (I+, I-)

These parameters are important because the majority of designs require either high accuracy, speed, or low power dissipation.

ON RESISTANCE

In high accuracy systems, such as data acquisition systems, the designer would be concerned with minimizing errors caused by "on" resistance and leakage currents. An inverting programmable gain amplifier shown in Figure 1 will help illustrate the need for low on resistance and leakage current in high accuracy systems.

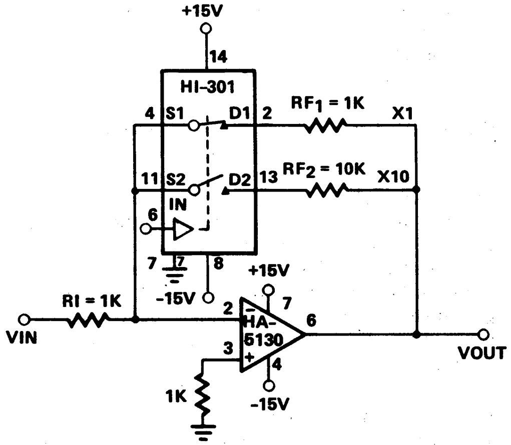


Figure 1 — Inverting Programmable Gain Amplifier

Ideally, the voltage gain of this inverting amplifier would be, $A_V = -(R_F/R_I)$. But when using a switch to program the gain, its characteristics must be taken into account and the amplifier gain equation must be modified to $A_V = -(R_F + R_{ON}/R_I)$. The higher the on resistance of the switch, the greater the gain error. Variations in the on resistance of the switch will also effect the gain error.

LEAKAGE CURRENT

Another source of error occurs in the switch "off" state, where leakage current causes offset voltage errors. In Figure 1, leakage current flowing through the feedback resistor creates an output voltage error equivalent to the expression, $V_o = R_F \times I_{DOFF}$.

SWITCHING SPEED

A designer concerned with switching times would obviously be sensitive to the ton and toff specifications. A low value of "on" resistance is also important, since this resistance increases the RC time constants and can slow the circuits overall performance.

POWER SUPPLY REQUIREMENTS

The last critical parameter would be power consumption. There are certain applications where power supply currents are the primary concern of the designer. Examples would be portable or battery operated equipment.

The majority of switch applications require critical performance in one or more of the areas just discussed. The HI-300 series offers improved performance in each of these areas. The following tables compare the HI-300 series with existing HARRIS switches. Table 1 contains maximum specifications for T = 125°C and Table 2 consists of typical values at T = 25°C.

+125°C Maximum Specifications

SWITCH TYPE	RON	I LEAKAGE	I SUPPLY	tON	tOFF
HI-200	125Ω	500nA	2mA	500ns	500ns
HI-5040	75Ω	500nA	.3mA	1000ns	500ns
HI-300	75Ω	100nA	.1mA	300ns	250ns

Table 1 – Switch Comparisons at T=125°C

+25°C Typical Specifications

SWITCH TYPE	RON	I LEAKAGE	I SUPPLY	tON	tOFF
HI-200	55Ω	1nA	.5mA	240ns	330ns
HI-5040	25Ω	.8nA	.3mA	370ns	280ns
HI-300	30Ω	.1nA	.23μA	210ns	160ns

Table 2 – Switch Comparisons at T=25°C

From these tables it should be clear that the HI-300 series offers improved performance to the designer.

INSIDE THE HI-300

Figure 2 shows the schematic of the digital input and driver stages of the HI-300. The purpose of this stage is to take the logic level signals and condition them to drive the gates of the FET switch cells.

The HI-300 series has a digital input protection circuit consisting of a 200Ω series resistor and clamping diodes, D1 and D2, to the supplies.

These diodes will quickly discharge any static charge which might appear at the digital inputs.

The F. E. T. Devices N1 thru N5 and P1 thru P5 form the input buffer and level shifter which establishes the proper voltages to drive the switch cell. N6, N7, P6, and P7 form the output buffers which isolate the level shifter from the capacitive load of the switch cell.

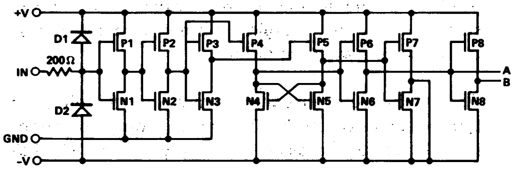


Figure 2 – Partial Schematic

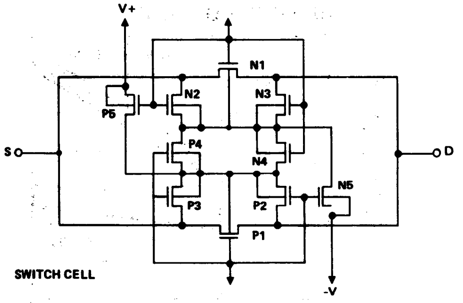


Figure 3 – Schematic

The switch cell shown in Figure 3 is based on the FET devices N1 and P1. The remaining devices, N2 thru P5 serve various functions, such as reducing leakage current, minimizing on resistance variations and minimizing charge injection.

ADDITIONAL PERFORMANCE CHARACTERISTICS

(A) SINGLE SUPPLY OPERATION

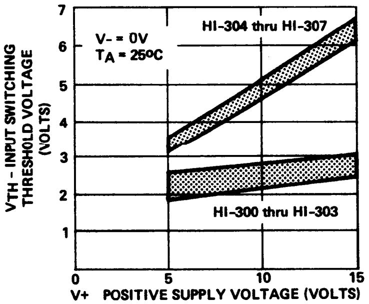
The HI-300 series has the capability of single supply operation. These switches can operate to a minimum supply of +5 volts, although designers must be aware of the trade off which exists at these levels. The trade off is the performance of the switch will vary as the supply level varies. Examples of these performance variations are increased on resistance and slower switching times. So, a HI-300 series switch with a single five volt supply will have higher on resistance and slower switching speeds then the same device at ±15 volts or even a single +15 volt supply.

The explanation for these variations can be found in the F.E.T. devices composing the switch cell itself. The variation in on resistance is due to the fact that the channel impedance of the FET is dependent on the gate-source bias. Since the gate voltage is determined by the supply voltage, it can be concluded that the on resistance is a function of the supply voltage.

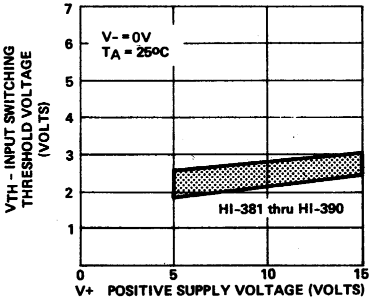
The fact that the on resistance varies with supply voltage directly relates to the slower switching times. The higher resistance reduces the available current needed to charge the internal capacitances of the switch. Lower charging current directly relates to the slower switching times.

The explanations, just given, along with the following typical curves of the HI-300 single supply operation, should aid the designer in applying the HI-300 series in single supply applications.

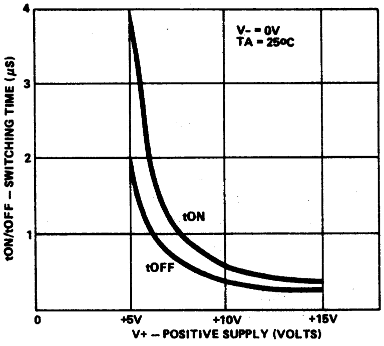
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE
HI-300 THRU HI-307



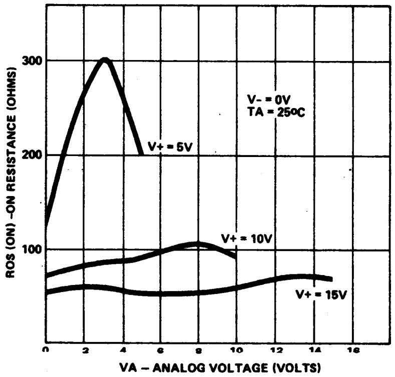
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE
HI-381 THRU HI-390



SWITCHING TIME VS. V+ - POSITIVE SUPPLY VOLTAGE



RDS(ON) VS. ANALOG AND POSITIVE SUPPLY VOLTAGE WITH V- = 0V



B) CHARGE INJECTION

The charge injection of a switch is a critical parameter for certain applications, such as small signal switching or sample and hold circuits.

For the case of small signal switching, unwanted switching spikes result from this transferred charge causing system errors. These spikes are created when the transitions of the gate voltage are capacitively coupled to the output through the gate to source and gate to drain capacitances, as shown in Figure 4. The magnitude of these switching spikes will depend on the values of the load and source impedances, the value of the gate voltage and the size of the internal capacitances of the switch.

For the sample and hold circuit, shown in Figure 5, a common problem is sample to hold offset error. It is caused by the same mechanisms discussed for the small signal application, but in this case the charge is transferred to the hold capacitor and an offset voltage is created. The voltage is determined by the following relationship. V = Q/CH.

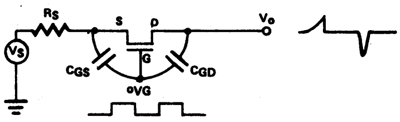


Figure 4 — Charge Transfer

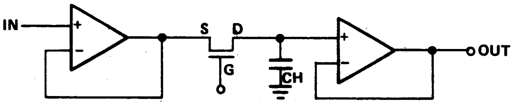


Figure 5 — Sample and Hold

Charge injection can create problems in the type of applications just described. A typical curve of the HI-300 series charge injection performance is shown in Figure 6 as an aid to designing in these type of circuits.

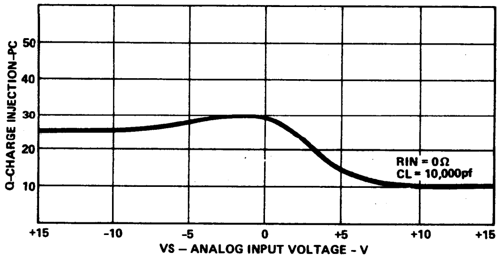


Figure 6 — Charge Injection vs. Input Voltage

APPLICATION HINTS

A. POWER SUPPLY CONSIDERATIONS

The HI-300 series analog inputs do not feature overvoltage protection. External protection circuitry would be necessary if the switches were subjected to possibly destructive situations.

An example could be an overvoltage condition where the power supplies to the switch go down while an analog input signal is still present. A common misunderstanding is that the switch will be open and block the input signal, when actually the opposite occurs.

If the power supplies go to ground, the input signal will pass through the switch and appear at the output. The explanation for this can be seen in Figure 7, which is a simplified CMOS switch cell. This switch cell consists of two enhancement type field effect transistors, one N-channel and one P-channel. An enhancement type of device is a FET which is normally off without some potential (gate voltage) to turn it on. A P-channel FET requires a negative potential (gate to source voltage) to turn it on an N-channel FET requires a positive potential (gate to source). Contained in the physical structure of the FETS are parasitic transistors which are shown in Figure 7 as diodes from the source and drain to the body potentials of the devices. These diodes or parasitic junctions are normally reversed biased. If those junctions are forward biased, a fault condition exists where the signal is passed through the parasitic transistor. This is what occurs if the power supplies go to ground. Depending on the polarity of the input signal, either the N or P channel FET parasitics will be forward biased and the signal passed through the switch.

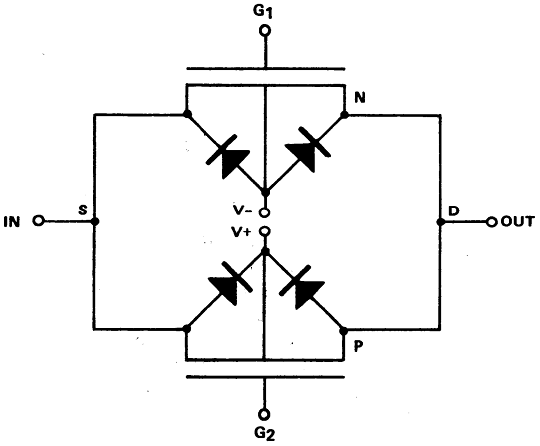


Figure 7 — Basic CMOS Transmission Gate

Another situation occurs if the power supplies are open circuited, the most positive and negative input signals will provide power to the switch. In this case, the signals being used for power will be passed to the output, but the remaining switches with input signals less than those used for supply will operate properly.

A second overvoltage condition is the case where the input signals exceed the existing power supply levels. Referring to Figure 7, if the input signal exceeds the supply by an amount greater than the breakdown voltage of the parasitic junction, the normally reversed biased junction will become forward biased. These forward biased junctions will pass the input signals to the output and possibly short out the input voltage sources.

The most common form of protection circuit for these types of overvoltage conditions is the resistor-diode network at the input of the switch as shown in Figure 8. This circuit protects the device if the supplies go to ground or if the input exceeds the supply. If either of these situations occur, the diodes will be forward biased and a current path to ground will exist. This protects the switch from excessive current levels. The primary purpose of the resistor is to limit the current through the diodes.

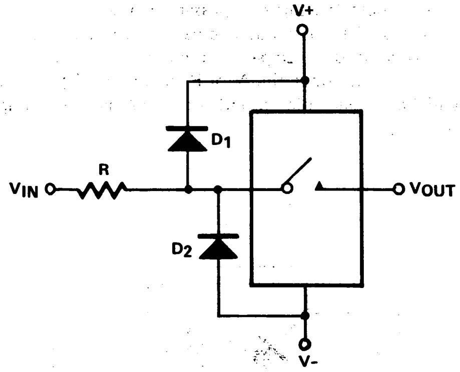


Figure 8 — Protection for Each Analog Input

Another advantage of using diode protection is that it prevents the signal from passing to the output. This is a result of the input being clamped to the breakdown voltage of the protection diodes. If this breakdown voltage is less than the threshold voltage (turn on voltage) of the parasitic diodes, the parasitic transistor will remain reversed biased and the signal will not pass through the switch.

The protection network may introduce unwanted error into the circuit in the form of leakage current and increased on resistance. It is recommended that low leakage diodes be used, such as Schottkey diodes. If the switch is looking into a high impedance, such as the input operational amplifier, the error introduces by the increased on resistance will be negligible.

The protection circuit just discussed is not used to prevent the switch from latch up. The HI-300 series switch is constructed using the HARRIS dielectric isolation process and the four layer SCR found in JI technology does not exist. This circuit is intended to protect the device from high current levels which result from the forward biasing of the parasitic transistors which are inherent in all FETS.

An alternative to protection circuits takes advantage of CMOS technology. Assume an overvoltage condition exists where the input exceeds supply. Rather than use external components to protect the device, it may be possible to shift the supplies in order to accomodate the input signal. An example would be an application with ±15 volt supplies, but attempting to switch a +18 volt input signal. A possible solution would be to shift the supplies to V+ = +20V and V- = -10V and now the input signal is within the existing supplies. In some applications the supply voltage can be adjusted in order to pass larger input signals.

ACKNOWLEDGEMENT

A. Engineering staff of Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901, particularly Frank Cooper, whose useful comments contributed to this publication.

REFERENCES

(1) Eugene L. Zuch, "Keep track of a sample - hold from mode to mode to locate errors", Electronic Design, Dec 6, 1978.

(2) Don Jones, "CMOS Analog Multiplexers and Switches' Applications Considerations" Harris Application Note 520.

(3) Ernie Thibodeax, "Getting the most out of C-MOS devices for analog switching jobs", Harris Application Note 521.

(4) Hunter, Bill, CMOS DATA BOOK: Tab Books, 1978.

APP NOTE
FOR YOUR INFORMATION
No. 535
Harris Analog

DESIGN CONSIDERATIONS FOR A DATA ACQUISITION SYSTEM (DAS)

By Tarlton Fleming

INTRODUCTION

This is a collection of guidelines for the design of a data acquisition system. Its purpose is to supplement the more methodical block-by-block discussions available in numerous other papers and application notes. Emphasis in this note is on the less easily quantifiable happenings "between the blocks", rather than a description of the block components and their error contributions. This latter information may be found in the Bibilography under "General".

A data acquisition system is defined to include all the components needed to generate the electrical analogs of various physical variables, transmit these signals to a central location and digitize the information for entry into a digital computer. Among these components are transducers, amplifiers, filters, multiplexers, sample/holds and analog-to-digital converters. The system also includes all signal paths tying these functions together.

Several system architectures will be considered, followed by a general discussion aimed at the designer who must choose hardware for a given application. Topics include:

- Data Acquisition System Architecture
- Signal Conditioning
- Transducers
- Single-Ended vs. Differential Signal Paths
- Low-Level Signals
- Filters
- Programmable Gain Amplifier
- Sampling Rate
- Computer Interface

DATA ACQUISITION SYSTEM ARCHITECTURE

At present the most widely used DAS configuration is that shown in Fig. 1. It handles a moderate number of analog channels, feeding into a common multiplexer, programmable gain amplifier (if required), track/hold amplifier and A-D converter.

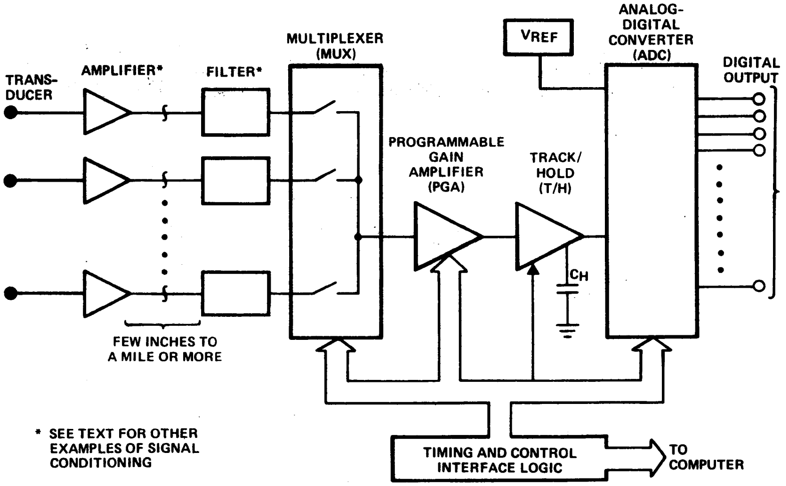
A more specialized and expensive variation is to place a Track/Hold in each channel as shown in Fig. 2. Switching all channels to HOLD simultaneously produces a "snapshot" view which preserves the phase relation of signals in all channels. This information is important in seismic studies and vibration analyses.

The DAS system of Fig. 3 offers many advantages, but is not yet practical except for slowly changing channel data. Low frequency signals allow dedication of a slow but accurate integrating type A-D converter for each channel. The channel filters often included to reduce aliasing errors and noise are not necessary, since aliasing is not a problem with low bandwidth signals. The integrating converter suppresses wideband noise by averaging it about the instantaneous signal level. Also, the converter's integration period may be chosen to provide almost complete rejection of a specific interference frequency such as 60 Hz. Digital outputs from the converters are then digitally multiplexed.

The system shown in Fig. 3 has an inherent advantage over the other two systems, having eliminated both the track/hold and the analog multiplexer with their many error contributions. The disadvantage, of course, is cost. Fig. 3 would become the system of choice in many more applications, if a significant reduction should occur in the price of successive - approximation A-D converters.

A small RAM may be added at the converter's output in any of these systems, to buffer the computer and offload its involvement with individual conversions. Timing and control may be arranged to scan all channels repeatedly, and continuously update a RAM location for each channel. The computer is then free to look at a recent reading for any channel, at any time.

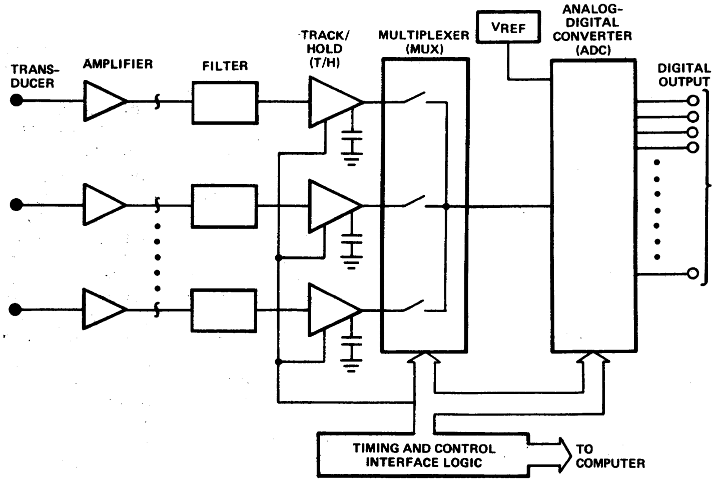
Further discussion will center on Fig. 1, both in the single-ended version shown, and in the differential version.



TRANS-
DUCER
AMPLIFIER*
FILTER*
MULTIPLEXER
(MUX)
VREF
ANALOG-
DIGITAL
CONVERTER
(ADC)
DIGITAL
OUTPUT
PROGRAMMABLE
GAIN
AMPLIFIER
(PGA)
TRACK/
HOLD
(T/H)
CH
FEW INCHES TO
A MILE OR MORE
TIMING AND CONTROL
INTERFACE LOGIC
TO
COMPUTER

* SEE TEXT FOR OTHER EXAMPLES OF SIGNAL CONDITIONING

FIGURE 1. Typical Data Acquisition System



TRANS-
DUCER
AMPLIFIER
FILTER
TRACK/
HOLD
(T/H)
MULTIPLEXER
(MUX)
VREF
ANALOG-
DIGITAL
CONVERTER
(ADC)
DIGITAL
OUTPUT
TIMING AND CONTROL
INTERFACE LOGIC
TO
COMPUTER

FIGURE 2. DAS System For Simultaneous Sampling Of All Channels

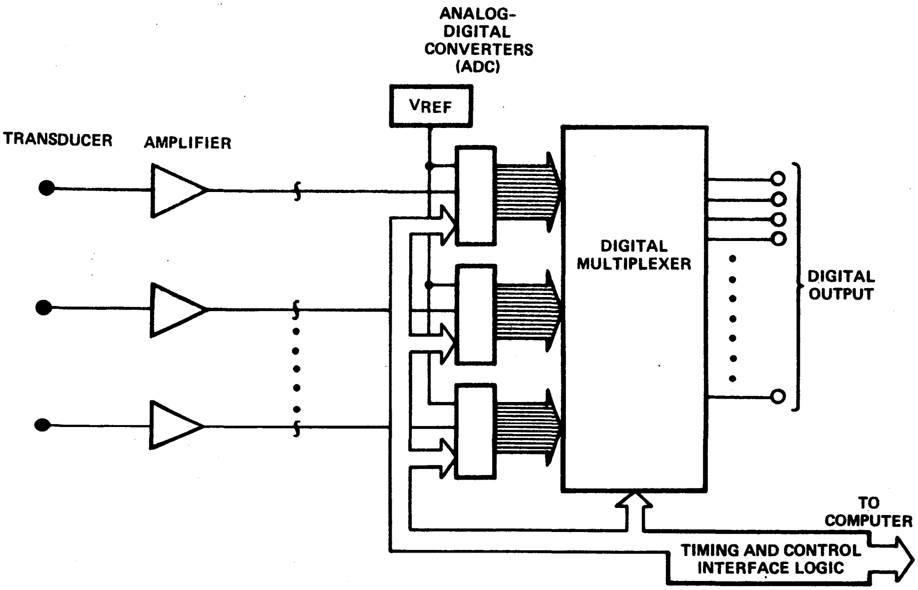


FIGURE 3. High Accuracy, Multi-Converter DAS System

SIGNAL CONDITIONING

Signal conditioning refers to all the operations performed on a transducer signal up to (and including) digitization by the A-D converter. Standard among these operations are multiplexing, programmable gain, and Track/Hold. Others may be added as required:

- Transducer excitation
- Amplification
- Filtering
- Calibration
- Linearization
- Voltage to current conversion (4 to 20 mA; 10 to 50 mA)
- rms to dc conversion
- Logarithmic signal compression
- Common mode rejection

For highest signal-to-noise ratio all signal conditioning should be performed near the transducer, with the exception of common mode rejection and filtering. Filters should be located near the multiplexer input. Besides minimizing alias errors originating in the high end of the transducer's output spectrum, filters suppress wideband noise picked up on signal lines to the transducer.

TRANSDUCERS

The first item in the signal path of a DAS is the transducer. This device usually transforms energy from one form to another, producing an electrical analog of the physical variables to be monitored or measured. Transducers are based on a variety of physical principles but most produce a voltage as output. Some yield an intermediate variable such as resistance or capacitance, which is transformed to voltage by an applied electrical excitation (carrier frequency, dc voltage, current source).

Often, several types of transducers are available to sense a given quantity. When selecting a voltage output transducer, remember that a low source resistance is desirable, both to minimize noise and to reduce loading by the next "block" in the signal path. Provision on the transducer for a convenient method of signal calibration will be welcome, once a system is in operation. Also, a center tap on the transducer allows better interface to a balanced line if low level signals are to be transmitted.

Several questions arise at this point:

- Should the signal path be single-ended or differential?
- Should the signal be transmitted at low level (100 mV) or high level?
- What type of conductor should be used for signal transmission?

Answers to these and other questions are covered in the following Sections.

SINGLE-ENDED VS. DIFFERENTIAL SIGNAL PATHS

Consider the transducer output. A high level signal (100 mV to 10 V) is easier to handle than low level. Is a common mode signal present? If not, is it likely to be acquired as "pickup" during transmission? This is likely if the cable is routed near fluorescent lights, motors or other electrical machinery. If common mode voltage is not expected, then an economical single-ended connection is possible, with a single wire per channel and a common return. (see Fig. 4). High level signals, short distance and controlled conditions will ensure good performance with this arrangement.

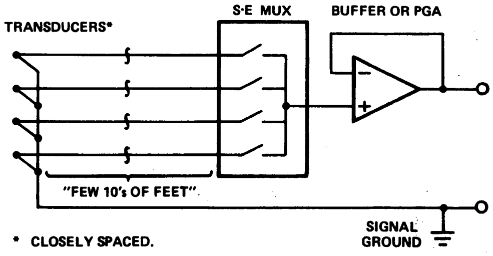


FIGURE 4. Single-ended Data Paths

Low level signals require special treatment. Whether high or low level, the presence of common mode voltage calls for a differential signal path. The most widely used solution is an unshielded, twisted pair of wires, good for 1000 feet or so with a bandwidth of 100 KHz. As a minimum then, two wires per channel feed into a differential amplifier or multiplexer, buffered by a full or pseudo-differential amplifier to reject the unwanted common mode voltage (see Fig. 5).

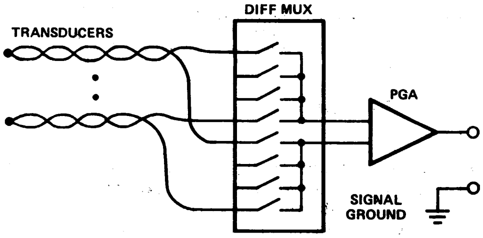


FIGURE 5. Differential Data Paths

For the case in which the transducer output is a low level voltage, the choice is whether to transmit it as is, or to boost the level by adding an amplifier. The amplifier will provide low source impedance as well as gain; two valuable forms of signal conditioning. However, providing power to a remote amplifier can be difficult. Even if a supply is available at the remote site, the voltage between two widely separated commons presents a problem. If the sum of signal plus common mode voltage does not exceed the input range of either the multiplexer or buffer amplifier, Fig. 5 can be used.

A more expensive approach is required for higher common mode voltages. One reliable technique is the "flying capacitor" multiplexer of Fig. 6, using reed relay switches. This works well for thermocouples bonded to machinery and riding on hundreds of volts relative to DAS ground, but in some applications the reed relay's 1 ms response time can be a limitation.

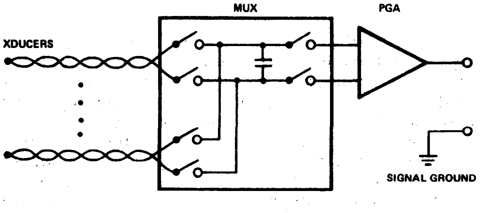


FIGURE 6. "Flying Capacitor" multiplexer using reed relay switches for high CMV signals.

Isolation amplifiers can handle higher voltages and higher bandwidths than the system of Fig. 6. For example, magnetically isolated amplifiers are rated at 2KV and up with a small signal bandwidth of approximately 2 KHz. One of these per channel is expensive, but in addition to common mode rejection it can solve the problem of supplying power at the remote transducer. Isolation amplifier models are available which include ± 15V terminals, referenced to the floating front-end of the amplifier. This power can provide transducer excitation and supply an amplifier or other signal conditioning circuitry.

For higher bandwidth data, optically isolated isolation amplifiers are available with $f_{-3dB} = 15KHz$ and 2KV isolation. These amplifiers do not provide the external supply terminals to power transducer circuitry.

LOW LEVEL SIGNALS

The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded, differential signal path is essential for transmitting these signals, especially to maintain a noise level below 50μV rms.

Most transducer outputs are low level and low bandwidth as well. Since shielding precautions to be described are intended to produce an acceptable signal to noise ratio, filters may not be necessary. Otherwise, active filters with their relatively large dc errors should not be used for low level signals. Passive filters on the other hand, are restricted to two or three poles as a practical limit, which in turn restricts the allowable signal bandwidth for a given accuracy (see the Section titled Filters).

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area, to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only one tenth as much leakage capacitance to ground per foot.

A key requirement for the transmission cable is that it present a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled inphase to both conductors and rejected as common mode voltage. Again, any such noise will be directly proportional to the source impedance driving the line. An isolation or instrumentation amplifier may be used to terminate the line, providing high input impedance, common-mode rejection, conversion from a differential-to single-ended signal path, and a buffer for the ON resistance of the following multiplexer.

Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12-bits or more.

The table of Fig. 7 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values for inductance.)

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 OZ. Cu.)	DC RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				AT 60Hz	AT 10KHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.38μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

FIGURE 7. Impedance of Electrical Connections, +20° C

As an example, suppose the ADC in Fig. 1 has 12-bit resolution, and the system accuracy is to be ± ½ LSB (± 1.2mV). The interface logic might draw 100 mA from the +5V supply. Flowing through six inches of #24 wire, this current produces a drop of 1.28mV; more than the entire error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

FILTERS

The presampling or anti-aliasing filters shown in Fig. 1 are normally required with high-level signals of significant bandwidth, especially if the signal is to be reconstructed by a digital-to-analog converter after processing. If low level signals require a passive filter, the differential configuration of Fig. 8 preserves some degree of impedance balance on the line.

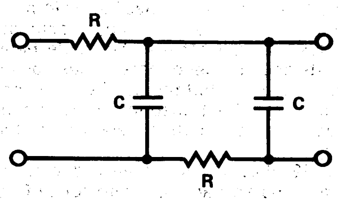
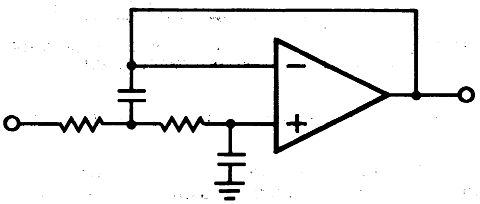


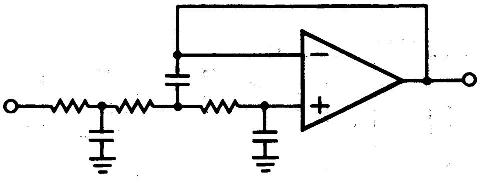
FIGURE 8. A Passive, Two Pole, Low Pass, Differential Input Filter

A low-pass Butterworth response is best for the channel bandlimiting filter in most data acquisition systems. The Butterworth filter output decreases monotonically with frequency, though this attenuation is very slight within the passband. Other filter types produce ripple in the passband, whose amplitude degrades accuracy unless expensive, high tolerance components are used.

Butterworth is not the most linear phase response, and if signal group delay is critical an elliptic (Bessel) filter should be chosen. Again, however, Butterworth fits most applications. A given number of poles may be had by cascading the two and three pole sections shown in Fig. 9. Either reference under "Filters" in the Bibliography gives a systematic procedure for calculating R and C values in terms of a given cutoff frequency. See the Section on "Sampling Rate" for the poles vs. accuracy requirement.



a. TWO POLE SECTION



b. THREE POLE SECTION

FIGURE 9. Butterworth Low-Pass Filters

PROGRAMMABLE GAIN AMPLIFIER (PGA)

Unless the ratio of highest to lowest signals anticipated on any channel is ≤ 2, some form of programmable gain amplification is desirable between the multiplexer and A-D converter. Without this variable gain block, the MSB's are idled one after another as input level decreases. Although the resolution of an n-bit converter remains a constant $FS/2^n$ by definition, resolution referred to the input level is decreasing (FS = Full Scale).

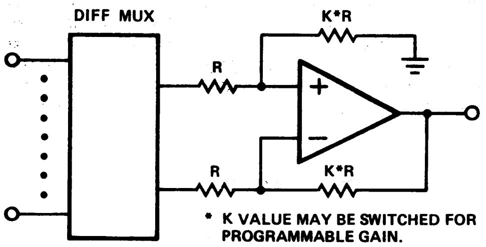
Considering resolution as referred to the input level, a 12-bit converter digitizes an input of .06FS to only 8 bits. The full 12-bit resolution applies only for $V_{IN} \geq FS/2$. Therefore to fully utilize the converter, gain should be added as necessary before each conversion, to meet the condition $FS/2 \leq V_{IN} \leq FS$. Then the amount of gain introduced by the PGA is noted by the computer to keep track of the actual input value.

Three other services are performed by the PGA:

1. Buffering: Prevents a loading effect due to the multiplexer's ON resistance.

2. Differential to Single-Ended Conversion: Necessary for the majority of Track (or Sample) /Holds and A-D converters.

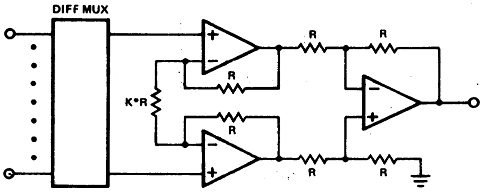
3. Common Mode Rejection (CMR). When connected to the output of a differential multiplexer, the PGA's differential input rejects the common mode voltage accumulated by a signal transmission cable. Fig. 10 shows a subtractor or "pseudo-differential" PGA suitable for wideband signals with low common mode content. In this circuit, CMR is limited by precision of the "K" ratio and variations in the channel source impedance.



* K VALUE MAY BE SWITCHED FOR PROGRAMMABLE GAIN.

FIGURE 10. Subtractor or Pseudo-Differential PGA

Fig. 11 is the full differential PGA, necessary for low-level, high common mode signals. This version offers the highest gain accuracy and for high gain, the best CMR.



* VARY K TO CHANGE THE GAIN.

FIGURE 11. Full Differential PGA

The PGA normally precedes the Track/Hold, since the PGA would amplify any error introduced by that device. This order must be reversed to implement an auto-range capability, because the signal voltage must be held at the PGA input for the duration of an auto-range subroutine by the computer. Such an algorithm consists of:

- Set PGA gain
- Trigger a conversion
- Note RESULT
- Iterate until (FS/2 ≤ RESULT ≤ FS)

SAMPLING RATE

Throughput rate for a DAS may be defined as the maximum number of digital samples per second that it can produce without exceeding its specified limit for accuracy. The system may run at a lower speed to avoid generating redundant and useless data; but if a waveform of significant bandwidth is to be reconstructed from the digital samples, then "the higher the better" is generally the rule for sampling rate.

The required rate is often higher than one would suppose. For example, using the criteria of data bandwidth alone, a very low sample rate is required for the slowly changing voltage outputs from a solar panel. Once per minute for each channel might be enough. With 60 channels though, the rate required is once per second. In addition, one might require a maximum of one second for notice of failure on any channel, boosting the required sample rate to 60 samples per second. In this manner low bandwidth channels may require a high speed DAS, according to the relationship:

System Sample Rate = (Highest Channel Rate) X (Number of Channels)

Also, a very high sample rate is required to preserve the high frequency content of a transient event on a single channel. The most commonly encountered requirement though, is a multichannel DAS (see Fig. 1) with a modest bandwidth on each channel. For example, each data source might be an accelerometer with an output ranging through several hundred Hertz.

Notice that the low and high bandwidth signals just described cannot be handled efficiently with the same system. A sample rate high enough for the highest bandwidth channel will oversample the lower bandwidth channels, generating unnecessary data. High and low bandwidth data are best handled by separate multiplexer/converter systems.

Presampling filters are essential to ensure accuracy in the sequence of digital samples representing a given channel. Since the multiplexer is a sampler (as is the Sample/Hold and A-D Converter) this means a separate filter dedicated to each channel preceding the multiplexer. A single filter following the multiplexer would do the job, but its modest response time would form a bottleneck restricting the sample rate. Guidelines are needed then, to relate a given level of accuracy to data bandwidth, filter cutoff frequency, and number of filter poles.

As mentioned earlier, a filter limits the error due to alias frequencies by restricting the bandwidth of both signal and noise. Either acting alone or in concert may cause error, since alias frequencies arise in several ways:

1. Overlap of the signal spectrum and the lower sideband associated with the sampling frequency f_S.

2. Overlap of the upper and lower sidebands associated with any two consecutive harmonics of f_S.

3. Overlap of any sideband with wideband noise from the data channel.

A band-reject filter would control case 1, but a low-pass type is needed to handle cases 2 and 3 as well. Again, the Butterworth response is preferred in most applications, but it does offer increasing phase shift and gain error for frequencies approaching the cutoff (-3dB) frequency. This cutoff should be set no higher than necessary for acceptable gain error in the highest signal components. A higher cutoff will only include unnecessary noise bandwidth.

Finally, for a given accuracy specification such as ± ½ LSB, a tradeoff may be made between the sample rate and number of poles. These poles usually come from the filter, but the number may include any pole(s) inherent in the transducer, provided they occur at an acceptable location relative to the cutoff frequency.

Fig. 12 shows aliasing error due to the signal spectrum alone vs sampling rate for different numbers of poles. The horizontal axis is normalized to Sampling Frequency/Cutoff Frequency. Notice that a 2-pole filter requires a sampling frequency 30 times the filter cutoff frequency, just to obtain 1% accuracy. For ± ½ LSB error in a 12-bit system (±.01%), a 5-pole filter requires sampling at 11 times the cutoff frequency. Remember, Fig. 12 applies only to the signal spectrum. Noise will cause some additional aliasing error.

Clearly, Nyquist's Sampling Theorem is not a practical guide for sampling rate in real applications. Actual (as opposed to hypothetical) filters cannot bandlimit a signal sufficiently to permit the theoretical minimum of two samples per cycle of highest signal frequency.

APP NOTE

FOR YOUR INFORMATION

No. 538

Harris Analog

MONOLITHIC SAMPLE/HOLD COMBINES SPEED AND PRECISION

By Tarlton Fleming

INTRODUCTION

A new Sample-Hold amplifier from Harris Semiconductor offers the best combination of speed and accuracy available in a monolithic device. It was developed for moderate to high speed applications-and particularly as an input for successive-approximation A/D converters which perform a precise conversion in 30 microseconds or less. This second-generation design includes a 100pF MOS hold capacitor, and offers a 1.0 microsecond acquisition time along with high accuracy over the commercial and military temperature ranges.

This new product, the HA-5320, can track a signal indefinitely (like an op amp) while in the sample mode. At the instant a digital HOLD command is applied the corresponding signal level is held and maintained at the output. The ratio of sample (track) to hold time is set by the user, according to the duty cycle of his digital control signal.

COMPARISON WITH EARLIER DESIGN

The HA-5320 retains the versatility of its predecessor, the popular HA-2420. That is, both have the uncommitted differential inputs of an op amp, allowing their Sample-Hold function to be combined with many conventional op amp circuits. Their circuit designs are different, though, producing significant differences in performance. These are best illustrated by describing the new device in contrast with older HA-2420. Table 1 summarizes the electrical characteristics of each, based on a 100pF hold capacitor.

Both IC's are packaged in a 14 pin DIP and operate on ±15V supplies. The hold capacitor connections differ as shown in Figure 1. Otherwise, the pinouts are compatible to this extent: Either device will operate in an existing HA-2420 socket if pin 6 is grounded, preferably to the system signal ground.

The HA-5320 delivers optimum performance when used as intended – relying on the internal 100pF hold capacitor alone. At +75°C this capacitor allows only 19μV of droop in 15μs. The Droop Rate is proportional to Drift Current, which increases with temperature (Figure 3). Droop may be reduced by adding external cpacitance C_H as shown in Figure 1B. This extra capacitance will reduce the bandwidth (Figure 5) and affect other parameters as shown in Figure 4. Also, a capacitor of value $0.1C_H$ should be added at pin 8 to reduce output noise in the Hold mode. Whether operating with additional hold capacitance or not, an HA-5320 offers a considerable improvement in accuracy over the HA-2420. Particularly welcome is the elimination of variation in "pedestal" error with input voltage. Further, the residual pedestal error may be nulled to zero, yielding great accuracy at a given temperature.

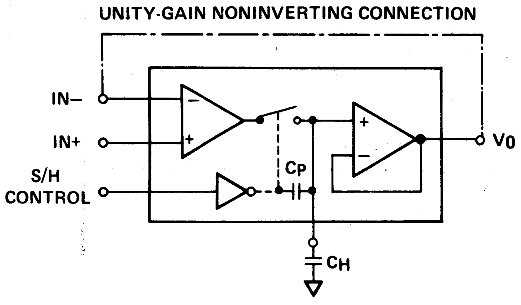


Figure 1A. HA-2420 Diagram

Test Conditions: $V_{PS} = \pm 15V$; $V_{AL} = 0.8V$ (Sample);
$V_{AL} = 2.0V$ (Hold); $C_H = 100pF$

(Room Temp R = +25°C; Full Temp. F is -55°C to +125°C)

PARAMETERS	TEMP.	HA-5320			HA-2420			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Characteristics								
Offset Voltage	R		0.2	0.5		2		mV
	F			2.0			6	mV
Bias Current	R		70	200		40		nA
	F			200			400	nA
Offset Current	R		30	100		10		nA
	F			100			100	nA
Common Mode Range	F	±10			±10			V
CMRR	R	-80	-90		-80	-90		dB
Transfer Characteristics								
Large Signal Voltage Gain	R	1×10^6	2×10^6			50K		V/V
Feedthrough Attentuation, 100KHz	F	76	80			76		dB
Gain Bandwidth Product	R		2.0			2.8		MHz
Output Characteristics								
Voltage	F	±10			±10			V
Current	R	±10			±15			mA
Full Power Bandwidth	R		600			100		KHz
Transient Response								
Rise Time	R		100			50	75	nS
Overshoot	R		15			25	40	%
Slew Rate	R		45		5	7		V/S
Digital Input Characteristics								
Voltage High (V_{AH})	F	2.0			2.0			V
Voltage Low (V_{AL})	F			0.8			0.8	V
Current ($V_{AL} = 0V$)	F			-4			-800	µA
Current ($V_{AH} = 5V$)	F			100			20K	nA
Sample/Hold Characteristics								
Acquisition Time, to ±0.1% FS	R		0.8			2.5		µS
±0.01% FS	R		1.0			3		µS
Aperture Time	R		25			30		ns
Effective Aperture Delay Time	R		-25			30		ns
Aperture Uncertainty	R		0.25			5		ns
Drift Current	R		8			5	50	pA
	F		1.7			0.5	4.0	nA
Pedestal Error	R		1.0			9		mV
Power Supply Characteristics								
Positive Voltage	F	14.5	15	16		15		V
Negative Voltage	F	-14.5	-15	-16		-15		V
Positive Current	R		11	13		8.5	12.5	mA
Negative Current	R		-11	-13		-8.5	-12.5	mA
PSRR	F	-65	-75		-80	-90		dB

Table 1. Electrical Characteristics HA-5320 vs. HA-2420.

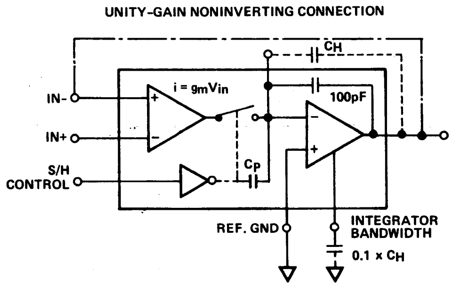


Figure 1B. HA-5320 Diagram

UNDERSTANDING PEDESTAL ERROR

When a S/H amplifier is switched from Sample to Hold, its output voltage rarely matches the ideal value one would expect from a perfect device. Instead, it differs by a small ΔV of a few millivolts, even with a DC input applied. Called "Sample to hold offset" or "pedestal", this error has a predictable polarity and magnitude for given conditions.

In general, this error is affected by magnitude of the input voltage, magnitude of the digital control level V_{AH}, rise time of the logic transition, size of the hold capacitor and temperature. Most troublesome of these is the variation of pedestal with input voltage, and this effect has been completely eliminated in the HA-5320.

Pedestal error is caused by the injection of charge onto the hold capacitor from a digital input, through small values of parasitic capacitance. Injection can come directly from the S/H control input or from the internal switch action. In Figure 1A and 1B, the capacitance of a base-collector junction in the switching circuit is represented as Cp, which varies with base-collector voltage for the transistor. That voltage is constant for the HA-5320, since Cp connects to a virtual ground. Therefore, charge injection and the resulting pedestal error are not affected by changes in V_{IN}. (For the HA-2420 in Figure 1A, Cp varies with V_{IN} and produces a varying pedestal.)

Another source of injected charge is the S/H control signal. This coupling is virtually zero within the HA-5320 chip, but a packaged unit exhibits about one millivolt change in pedestal per volt change in TTL level. However, compensation in the chip has been adjusted for zero pedestal at the nominal TTL level of 3.5V.

NULL THE PEDESTAL

This may be accomplished by introducing an equal and opposite voltage at the output, using the Offset Adjust terminals as shown in Figure 2. Since pedestal error does not change with V_{IN}, it may be treated as a simple offset. Use of the Offset Adjust shifts the pedestal error to the Sample Mode though, which may cause problems in a few applications.

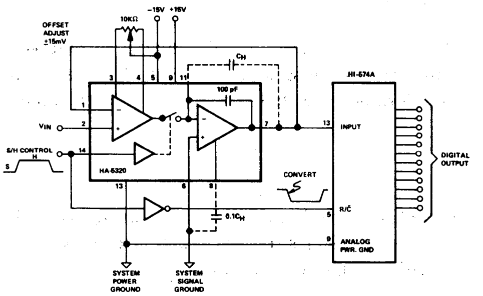
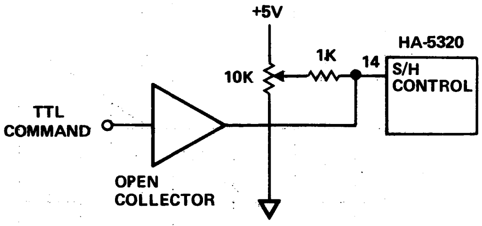


Figure 2. Signal Processing System

For these, one may make use of the relation between pedestal magnitude and the digital input level.

As mentioned earlier, the pedestal changes about one mV per volt of change in the digital "1" level, or V_{AH}. For small systems simply adjust V_{AH} until the pedestal is eliminated. In larger systems, the same adjustment may be made locally:



UNDERSTANDING DROOP ERROR

"Droop" is a change in output voltage vs. time while in the hold mode, caused by a flow of leakage current from the hold capacitor. For the HA-5320, this change is quite linear with time. The leakage current includes "off" leakage from the bipolar switch and bias current into the inverting input of the output integrator. The switch output consists of the joined collectors of two "off" transistors, NPN and PNP. These are tied to a JFET gate at the integrator input, so the hold capacitor looks at three leakage components, each of which doubles every 10°C. Ideally, these sum to zero and maintain a net zero leakage into the hold capacitor with changes in temperature. Effort has been made to achieve this. The JFET also produces less output noise than does the MOSFET used in the HA-2420.

An externally-supplied hold capacitor may provide other avenues for leakage current, but of course the HA-5320 does not require an external capacitor. Its 100pF internal hold capacitor is a guaranteed and factory-tested component. This eliminates the uncertainty associated with a user supplied component, and also eliminates the selection, purchase, stocking, test and assembly of high quality hold capacitors.

The typical leakage (called "drift") current varies with temperature as shown in Figure 3. Then, droop error is directly related to drift current by the relation

$$V_{DROOP} = \frac{I_{DRIFT}\,\Delta t_H}{C_H}$$

where t_H is time in the hold mode. Using C_H=100pF and Δt_H = 25μs, typical droop error may be calculated for a given temperature:

$$V_{DROOP} = \begin{matrix} 1.25\,\mu V\ @ +25^{o}C \\ 23.0\ \ \mu V\ @ +75^{o}C \\ 425.0\ \ \mu V\ @ +125^{o}C \end{matrix}$$

This shows a typical droop error of less than 1/5 LSB in 12 bits at +125oC, for one of the major applications targeted for this device (input to a successive-approximation A/D converter with 25μs conversion time.)

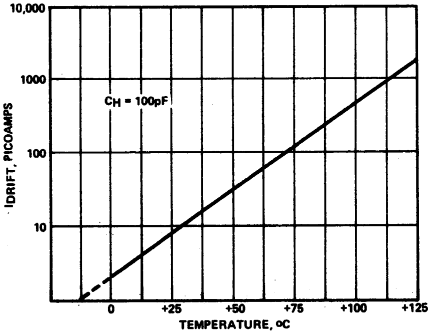


Figure 3. Hold Mode Drift Current v.s. Temperature

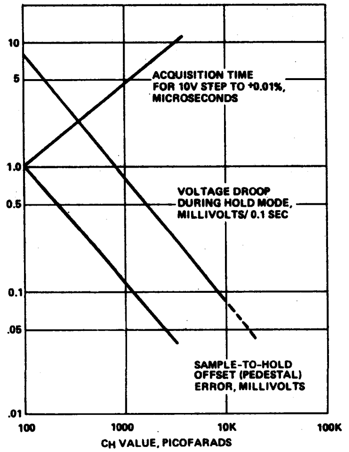


Figure 4. Typical Sample-and-Hold Performance v.s. Hold Capacitance

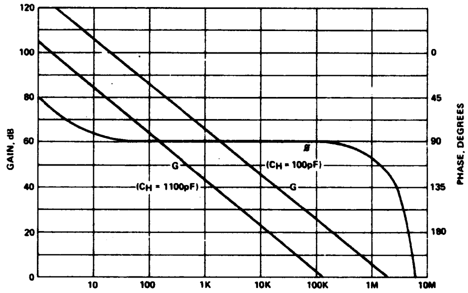


Figure 5. Open Loop Gain and Phase Response

OUTPUT CURRENT

Up to ±20mA may flow without damage, but the guaranteed limit for normal operation is ±10mA. The design does not include short circuit protection; consequently output impedance remains low with increasing frequency. This is an advantage in Figure 2, where the S/H output sees step changes in load current as a conversion proceeds. The HA-5320 is able to absorb these current changes with only a small and brief (5mV, 100nS) perturbation in its output voltage. A higher output impedance would extend this transient toward the moment of decision by the converter's comparator, producing a degradation in digital output accuracy.

With power applied, avoid a momentary short of the HA-5320 output to any fixed potential such as ground or either supply.

SIGNAL PROCESSING CONSIDERATIONS

An analog signal may be digitized by a Sample/Hold-AD converter system such as the one shown in Figure 2. If required, the analog signal may then be reconstructed from that sequence of digital samples, using a D/A converter. One might ask, how does the sample/hold alone constrain this sampling process? That is, how high a frequency can be digitized to a given level of accuracy?

The HA-5320 imposes three types of limit on the highest signal frequency applied at its input. First, the analog channel in the Sample mode has a 2MHz small signal BW, and a 600KHz Full Power BW (20 Vpp input). Next, Aperture Uncertainty Time contributes a trade-off between accuracy and frequency. Finally, Acquisition Time places a ceiling on the maximum sample rate obtainable with a given A/D converter, according to:

$$\text{MAX SR} = \frac{1}{t_{ACQ} + t_{CONV}}$$

where t_{CONV} is the A/D converter's conversion time. (Input frequency must not exceed one half the Sample rate, unless the application is tolerant of "alias" errors).

For example, the typical HA-5320 Acquisition Time for a 10V step is:

Temp	Acquisition Time, t_{ACQ} ±0.1%	±0.01%
+25°C	0.8μs	1.0μs
+125°C	0.9μs	1.1μs

Thus a 25μs converter could generate approximately $(1\mu s + 25\mu s)^{-1} = 38{,}460$ samples per second, allowing input frequencies as high as 19.23 KHz under ideal conditions (a low noise signal source with abrupt bandlimiting).

In most applications though, a low pass "antialiasing" filter is required to bandlimit the HA-5320 input. This filter controls "alias" error by reducing the amplitude of all signals and noise at andabove the Nyquist frequency (SR/2). A given accuracy requirement translates to a minimum attenuation at the Nyquist frequency, which is accomplished by increasing the sample rate and/or the filter complexity(# poles). Twelve bit (±1/2 LSB) accuracy for example, calls for a 5 pole filter and sampling at 11X the highest signal frequency of interest. Using 38.46KHz for Sample Rate, this limits the input frequency to 3500Hz (SR/11). If this seems low, bear in mind that 12 bits ±1/2LSB is a tight specification.

The HA-5320's Aperture Uncertainty Time also imposes a limit on input frequency, independent of that due to filter poles and sample rate. The relation is

$$f_{max} = \frac{1}{2^{n+1} \pi t_{AU}}$$

where t_{AU} is the aperture uncertainty and f_{max} is the highest frequency that can be sampled to ±1/2 LSB accuracy at n-bit resolution. Typical t_{AU} is 270ps for the HA-5320, leading to 143.9 KHz for f_{max} at 12 bits. That makes the HA-5320 compatible with some of the fastest 12 bit converters available today. Also, since f_{max} increases for lower resolution, the frequency limit based on aliasing will be encountered first in nearly all applications.

Another parameter of concern is feedthrough. After sampling a signal and holding it, how much of that signal will couple to the output and appear superimposed on the DC level there? At 100KHz, the answer is 1mVpp at the output, due to 10Vpp at the input. At 10KHz, the feedthrough is still -80dB indicating the coupling path is resistive over this range.

At lower frequencies, the feedthrough is less (better) than this, since the HA-5320 is designed for relatively short hold periods. For example, the 3500Hz limit mentioned above for a 12 bit, 25μs converter requires 285μs to complete one cycle. The HA-5320 will see only a small fraction of this input cycle during each hold period.

OP AMP PROPERTIES

Both the HA-5320 and HA-2420 behave like op amps in the sample mode, and may be treated as such–that is, external feedback may be connected to form filters, integrators, inverting and non-inverting amplifiers with gain, etc. This versatility is in contrast to many other designs in which the inverting input is internally connected, committing the device to the noninverting unity gain configuration.

Referring to Figure 1, it may be noted that the HA-5320 is even more like an op amp that the HA-2420. Where the HA-2420 input stage is a voltage amplifier (actually an op amp by itself), the HA-5320 input stage is a transconductance amplifier, producing an output current $g_m V_{IN}$. Also, the HA-5320 output stage is an integrator, analogous to the 2nd stage of a classical op amp. The hold capacitor corresponds to the op amp's compensation capacitor, through here the analogy falters. Like the op amp though, closed loop gain-bandwidth product for the HA-5320 may be predicted from the expression g_m/C_H.

Fabrication of the HA-5320 features the Harris high frequency dielectric isolation (DI) process, with front-diffused collectors and P-channel JFET's. This approach has yielded DC input characteristics which compare well with those of premium monolithic op amps. Typical Offset Voltage is 200μV at +25°C and only 2mV at +125°. Offset Current is guaranteed less than 100nA at +125°C, or half the value of Bias Current at that temperature. Common Mode Rejection is guaranteed 80dB minimum over the ±10V range, with 90dB typical.

The HA-5320 is very stable in the noninverting unity gain connection. Typical phase margin is 60° at an open loop unity gain frequency of about 2MHz.

As mentioned earlier, the addition of external hold capacitance has a direct affect on bandwidth. For example, adding 1000pF increases C_H from 100pF to 1100pF. As a result, the 2MHz unity gain bandwidth shrinks to (100/1100) 2MHz = 182KHz. This means more time must be allowed for acquisition for a new sample, but not in the same ratio: Acquisition Time to .01% increases from 1.0μs to only 8.7μs.

Figure 6 shows the response to a 10 volt step in the sample mode. The asymmetry from rise to fall time for slew rate and overshoot is common to all units.

Figure 7 shows some Sample/Hold characteristics for a small signal (10mVpp) input. The Sample to Hold settling time is less than 200ns–higher gain and sweep speed resolve this to about 160ns. Notice the final overshoot is less than .01% (one millivolt). This response is the same for any signal level. Also, slew rate is proportional to the magnitude of an input step, yielding a fairly constant value for slewing time, regardless of the distance slewed. This produces about one microsecond of acquisition time for any step change exceeding small signal conditions. For the small signal input of Figure 7, however, acquistion time is about 400ns (no slewing).

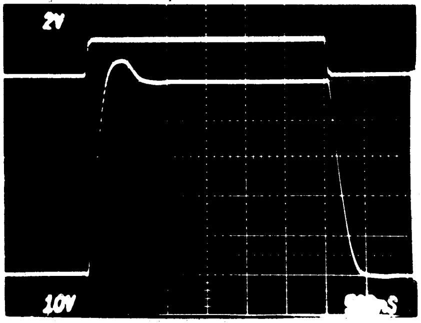


Figure 6. Step Response

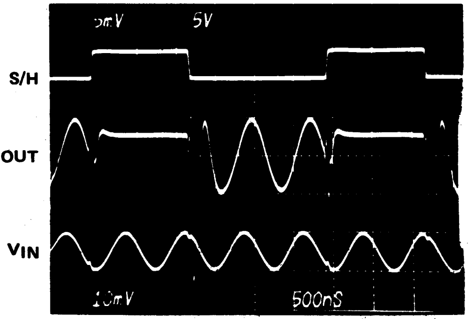


Figure 7. Small Signal Transient Response

APPLICATIONS

A/D CONVERTER INPUT

An important application has been presented in Figure 2, in which the HA-5320 serves to reduce the aperture time of an A/D converter. More directly, the Sample/Hold "freezes" an instantaneous value of V_{IN} and holds it constant during the analog to digital conversion. In Table 2, f_{max} without a Sample/Hold is relatively low, since aperture time equals the HI-5712 conversion time. Adding the HA-5320 substitues a much smaller aperture, which could allow an input frequency over 100KHz, but a lower limit is imposed by alias error effects. This limit depends on various conditions in the application, so the values listed for f_{max} (using the HA-5320) are only representative.

REQUIRED	HI-5712 CONVERSION TIME, MAX.	f_{MAX} (Vin) WITHOUT SAMPLE/HOLD	USING THE HA-5320		
			MAXIMUM SAMPLING RATE	f_{MAX} (Vin)	Min.#POLES, ANTI-ALIASING FILTER
8 BITS ±1/2LSB	7μS	88.8Hz	111KHz	24.8KHz	8
10 BITS ±1/2LSB	8.5μS	18.3Hz	95KHz	6.2KHz	3
12 BITS ±1/2LSB	10μS	3.9Hz	83KHz	1.5KHz	3

Table 2. Accuracy v.s. Maximum Input Frequency f_{max}

AUTO-ZERO CIRCUIT

A Sample/Hold may be used to form a simple but effective auto-zero loop. In Figure 8, an HA-5320 is used to maintain zero calibration for 7 channels of data.

The HI-5900 is a DAS subsystem which includes an 8 channel differential multiplexer, programmable gain amplifier and output sample/hold (the HA-2420). By dedicating channel 8 as the ground reference, a zero correction is accomplished whenever channel 8 is addressed. This must be done often enough to avoid the affects of droop error, and also following each change of PGA gain. The 10K/10Ω divider reduces the percentage effect of droop error by causing the Sample/Hold to store 1000X the actual correction value.

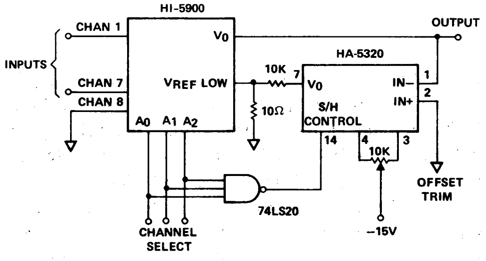


Figure 8. Auto-Zero Circuit

PEAK DETECTOR

An analog signal requires about 100ns to propagate through the HA-5320. For time varying signals, this assures a voltage difference between input and output. Also, the voltage changes polarity when the signal slope changes polarity (passes a peak). This behavior makes possible a Sample-Hold peak detector, by adding a comparator to detect the polarity changes.

In Figure 9 the exclusive NOR gate allows a reset function which forces the HA-5320 to the sample

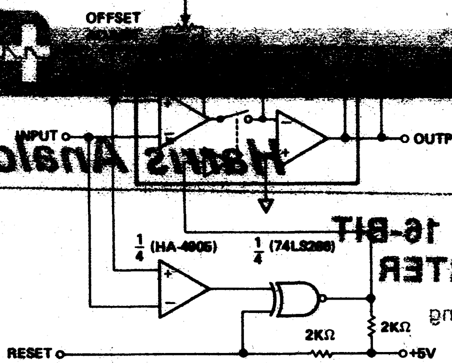

OFFSET
INPUT
OUTPUT
¼ (HA-4905)
¼ (74LS266)
2KΩ
2KΩ
RESET
+5V

Figure 9. Positive Peak Detector

mode. The connections shown detect positive peaks; the comparator inputs may be reversed to detect [illegible]

This circuit works well from below 100Hz up to the frequency at which slew rate limiting occurs. It captures the amplitude of voltage pulses, provided the pulse duration is sufficient for slewing to the [illegible]

The author wishes to thank design engineer Paul Hernandez and senior technician Roger O'Brien for their technical support.

APP NOTE

FOR YOUR INFORMATION

No. 539

Harris Analog

A MONOLITHIC 16-BIT D/A CONVERTER

By Tarlton Fleming

INTRODUCTION

Close attention to second order error sources has produced a 16 bit monolithic current-output DAC whose performance over temperature surpasses all similar products available at this time. The HI-DAC 16B is a dielectrically-isolated, bipolar device offering typical differential and integral nonlinearities of +1/2LSB, +3/4LSB respectively at room temperature, increasing to double those limits (maximum) at +75°C. Current mode settling time is 1μ s to ±.003% FSR. It carries forward a tradition among monolithic electronic components, in performing a function both at lower cost and with smaller size than most of its predecessors.

The prospect of an emerging market for digital audio equipment is driving the development of high-resolution converters within many semiconductor companies. All are anticipating a need for D/A converters in high volume, whose technical requirements are already well established (14 bit resolution and accuracy, monotonic from 0° to 70°, 1-2 μs settling time). Also, the aggressively low selling price of audio playback units dictates a monolithic IC component as the most promising solution.

HARRIS offering in this area was first announced at the 1982 International Solid State Circuits Conference in San Francisco. Called the HI-DAC16, its architecture is an extension of the earlier 12 bit HI-562, but with several significant innovations in circuit design and layout topology. The current result is solid performance at 15 bits. A sixteen bit accurate device is also under development. Since this performance exceeds the present requirements for playback of digital audio, the HI-DAC16 has targeted the markets for high resolution process control and precision instrumentation. It also promises a lower cost alternative for industrial weighing systems, automatic test equipment and high performance vector graphics, as well as digital audio. Performance is specified in Table 1 for the B and C grade units, which were introduced in March.

PARAMETER	MODEL	
	HI-DAC16B	HI-DAC16C
Resolution	16 Bits	•
Unipolar Offset @ 25°C	±.002% FSR	•
0° =75°C	±.5ppm of FSR/°C	•
Integral Nonlinearity @ 25°C	±.0023% FSR	±.0045% FSR
0° -75°C	±.0045% FSR, Max	±.009% FSR, Max
Differential Nonlinearity	± .0015% FSR	±.003% FSR
0° - 75°C	±.003% FSR, Max	±.006% FSR, Max
Reference Input		
Voltage	10V	•
Resistance	10KΩ	•
Output		
Resistance	2.5KΩ	•
Capacitance	10pf	•
Settling Time (Full Scale Transition) Current Settling to +.003%	1μsec	•
Noise at Output		
RMS +1 0.1Hz to 5MHz	1/5 LSB	•
		•
		•
Power Supply Sensitivities		
Gain	85db or .8ppm/%	•
Differential Nonlinearity	95db or .3ppm/%	•
Power Dissipation	465mW	•

Table 1

To appreciate the challenge posed by a 16 bit converter, consider that an LSB is only 153μV, based on a 10V full scale voltage output. Similarly for current outputs, the nominal 2mA full scale sets an LSB at only 30.5 nanoamps. One must be very careful in handling these small increments of signal to avoid losing them among the offsets, noise and bias currents normally present in a system application.

For example, the analog ground connection to a conventional switched current source DAC contains code-dependent currents varying from zero to 2mA or more. Flowing through 6 inches of a typical 40 mil wide printed circuit trace, these currents produce an IR drop of 66 micro volts – nearly 1/2 LSB in a 16 bit system.

The HI-DAC16 eliminates this problem by supplying the ground current from within the chip. This allows its analog ground terminal to sense the system ground at any reasonable distance, without an IR drop.

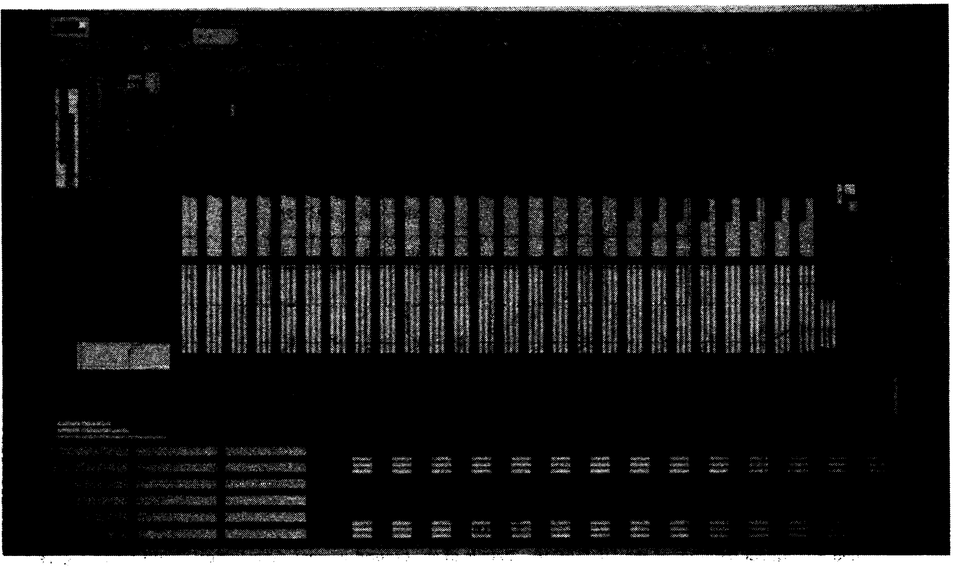


Figure 1.

Photomicrograph of the HI-DAC16. Digital-to-Analog Converter circuit combines dielectrically isolated bipolar technology with nichrome thinfilm resistors.

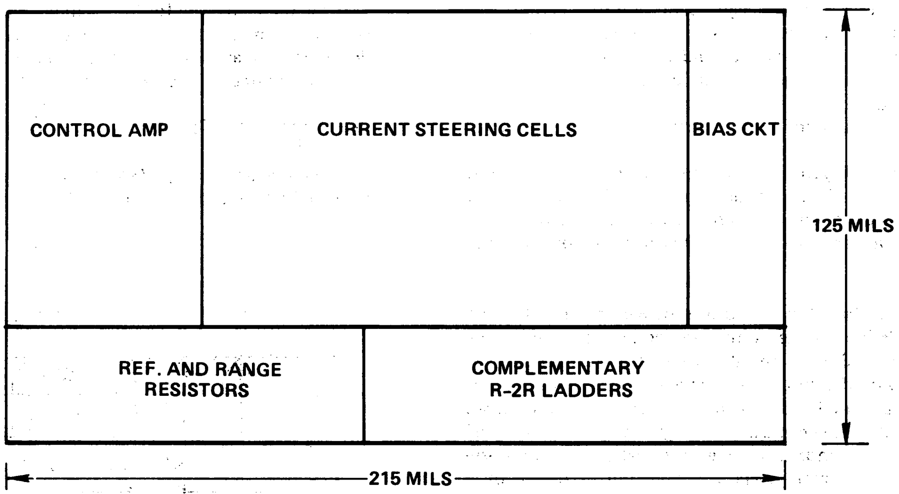


Figure 2.
Chip Diagram

BASIC FACTS

The HI-DAC16 operates on ±15V, with 456mW typical power dissipation. Package is a 40 pin side braze DIP. The 16 digital inputs accept a TTL compatible Straight Binary code word, and the nominal full scale current output is 2mA. An external +10V reference must be supplied. See Figures 1 and 2 for the chip layout and location of functions.

As shown in Figure 3, an onboard thin-film resistor provides a one-half scale offset for the bipolar ranges. Two more span resistors provide feedback around an external op amp to establish any of the standard ranges of output voltage: +5V, +10V, ±2.5V, ±5V and ±10V.

To minimize offset error due to the op amp's input bias currents, each amplifier input should see the same source resistance. An additional onboard resistor network may be connected to the amplifier's noninverting input to provide this matching for three of the five output ranges.

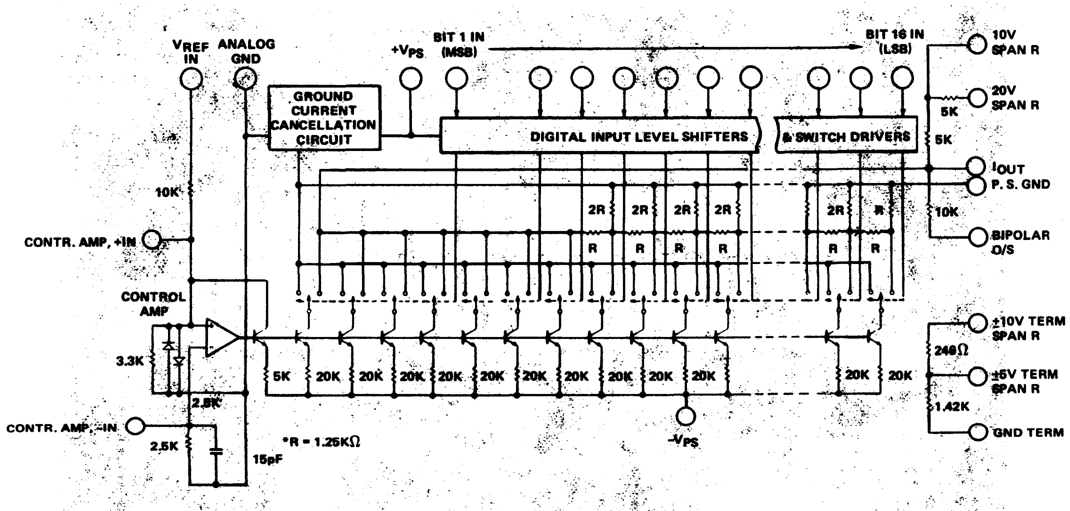

VREF IN
ANALOG GND
GROUND CURRENT CANCELLATION CIRCUIT
+VPS
BIT 1 IN (MSB)
BIT 16 IN (LSB)
10V SPAN R
20V SPAN R
5K
5K
DIGITAL INPUT LEVEL SHIFTERS
& SWITCH DRIVERS
IOUT
P. S. GND
10K
BIPOLAR O/S
10K
CONTR. AMP. +IN
2R
R
*R
CONTROL AMP
±10V TERM SPAN R
240Ω
3.3K
5K
20K
±5V TERM SPAN R
2.5K
1.42K
CONTR. AMP. -IN
2.5K
15pF
*R = 1.25KΩ
-VPS
GND TERM

Figure 3.

Simplified Functional Diagram of the HI-DAC16. Details of the ground current cancellation circuit are in Figure 4.

A LOOK AT DESIGN DETAILS

Internal cancellation of ground current is one of the HI-DAC16's most significant improvements. It simplifies application of the device by reducing current in the analog ground terminal nearly to zero. DC offset voltage between the package and system ground is eliminated, and dynamic code-dependent current variations are contained within the chip.

Refer to Figure 4. The chip includes two identical thin film R-2R ladders, deposited with physical symmetry about a common analog ground bus. The main ladder generates output current I_O for the lower 13 bits.

The auxiliary ladder is driven by a complement of the DAC's input code, so the two ladders together draw a constant 3mA from the internal analog ground regardless of input code. (The auxiliary ladder generates a complementary current $\overline{I_O}$ which is dumped into the non-critical power ground.) The nominal three milliamps is supplied internally from the positive power supply, via a current mirror driven by a 0.5mA current source. Net current through the external analog ground is zero. Further, this null condition is maintained with variations in temperature and reference voltage, since the current source is driven by the control amplifier.

To accomplish binary weighting of the sixteen bit currents, identical current cells are employed, each with a 250μA sink and a differential transistor pair used as a two position bipolar switch. For the three MSB's, cell currents are switched either to I_O or power ground. For the remaining 13 bits, binary currents are obtained from an R-2R ladder.

Four cells are switched in tandem for the MSB; two for bit 2 and one for bit 3. In all, 20 cells mirror current from a set of four reference cells, with all 24 driven by an onboard control amplifier and the reference voltage. The resulting transfer function is:

$$I_O = \frac{V_{REF}}{4R_{REF}}\left(4B_1 + 2B_2 + B_3 + \frac{B_4}{2} + \frac{B_5}{4} + \frac{B_6}{8} + \dots\dots + \frac{B_{16}}{2^{13}}\right)$$

. . . . where B_1 through B_{16} are logical values for the sixteen digital inputs, ie. either "1" or "0".

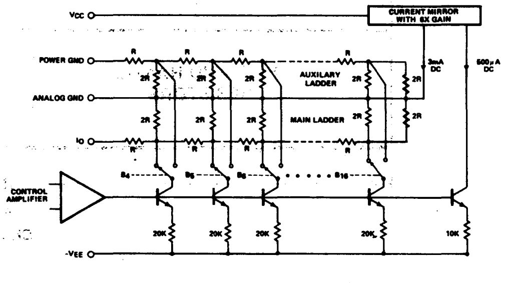

VCC
CURRENT MIRROR WITH 6X GAIN
POWER GND
R
2R
AUXILARY LADDER
3mA DC
500μA DC
ANALOG GND
MAIN LADDER
IO
B4
B5
B6
B16
CONTROL AMPLIFIER
20K
10K
-VEE

Figure 4.

Ground Current Cancellation. The auxiliary ladder adds complementary current to Analog Ground, to eliminate variations due to input code changes. The resulting DC current is then supplied internally from V_{CC}.

Several measures have been taken to counteract the linearity errors produced by any slight mismatch in cell currents or non-ideal tracking of the composite reference cell. First, the four reference calls are physically positioned among the cells of the first three MSB's in a pattern which minimizes tracking errors. Although close matching is assured by the control of process parameters and the careful matching of resistor and transistor geometries, small errors arise due to thermal gradients and IR drops in the negative supply bus. This bus is configured as a tree rather than a single wide conductor, to minimize the impact of IR drops and their change with temperature. Further, cell matching is enhanced by operation of all cells at the same current, which establishes a uniform power dissipation across the cell array.

"Superposition error" is another aberration in the transfer function of D/A converters, in which the voltage output for a given code does not exactly agree with the sum of those bits if they are turned on one at a time. Small IR drops in the ground line can cause this; as can a slight change in value of the onboard span resistor. Small changes are produced by self heating due to the flow of feedback current from the op amp. This effect is nonlinear with current and may be calibrated to zero at full scale, yielding a maximum error for outputs near 0.6 of full scale.

In the HI-DAC16, however, superposition error is hardly measureable. Ground current has been cancelled, eliminating that error component. To minimize the effect of self heating, the reference resistor is located between the two span resistors to provide a tight thermal coupling among the three. The ratio of reference to span value is only 2:1, using identical geometries, so a temperature change in either span quickly produces a similar effect in the reference resistor. However, a change in the reference produces an opposite effect on the output. The net effect is a first order cancellation of superposition error.

SETTLING TIME - A CHALLENGING MEASUREMENT

This measurement is routine at 8 bit resolution and challenging at 12 bits, but at 14 bits it pushes the limit of currently available techniques. As mentioned earlier, typical full scale settling for the HI-DAC16's current output is one microsecond (to ±0.003% of full scale which is ±1/2 LSB at 14 bits). Although the time interval is only moderately fast, it is difficult to measure the ±1/2LSB window at high resolution.

The method in use at Harris Analog Division simulates the conditions seen by a DAC when used in a successive approximation A/D converter. A strobed comparator (The HA-4950) is used to sense the DAC output with respect to a ±1/2LSB window about the final settled value. At 14 bits, the comparator operates reliably (HI-DAC16 provides 203μV for the LSB in this setup) but at higher resolution the smaller LSB doesn't provide enough overdrive. These measurements will require either a better comparator or a different test method.

For the voltage output case, the LSB is large enough at a given resolution to ease the problem. Also, the settling time is longer. If the amplifier settles in t_a, the DAC in t_d and the measured value for the combination is t_m, then $t_d = \sqrt{t_m^2, - t_a^2}$, provided the amplifier has a single pole response.

VOLTAGE OUTPUT - ANY OLD OP AMP WON'T DO

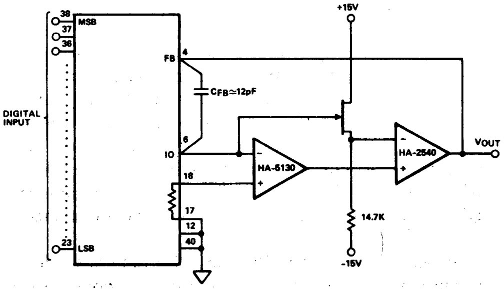


Figure 5.

Composite amplifier provides fast, accurate conversion of output current to voltage.

The HI-DAC16 imposes strenuous demands on its output current-to-voltage amplifier. Amplifier offset voltage adds error to its voltage output; input bias current adds error to the DAC output current; and finite open loop gain introduces gain error. These errors can be compensated by the calibration of offset and gain, but some error will reappear as temperature varies. A precision op amp like the HA-5130 contributes so little DC error that no calibration is required in most cases. It's not fast enough though, for high rates of update at the DAC input. HA-5130 settling time is rated 11μs, just to settle within ±0.1% (for a 10V step, slewing at 0.8V/μs).

Other op amps with different compromises in speed and accuracy may be chosen, but no single monolithic op amp can meet all these requirements:

Input Bias Current	3nA
Input Offset Voltage	15μV
Large Signal Voltage Gain	10^6
Settling Time to ±0.003%	2μs
Unity Gain Stable	

However, a composite based on two monolithic op amps can offer that performance at reasonable cost. The basic connections are shown in Figure 5.

In this arrangement the HA-5130 contributes low input bias current, low offset voltage and high open loop gain, while the HA-2540 contributes high slew rate, wide bandwidth and fast settling. The JFET buffers the HA-2540's input bias current, and C_{FB} may be selected to optimize settling time.

DATA BUS INTERFACE

In general, a D/A converter is more readily connected to a digital data bus than its counterpart, the A/D converter. The interface is especially straightforward if the DAC input and data bus have the same width (in number of bits).

Figure 6 for example, shows the HI-DAC16 providing an analog output from the 16 bit data bus of an 8086 system. The DAC is updated with every coincidence of the M/$\overline{\text{IO}}$ and $\overline{\text{WR}}$ signals and a proper address. Low Power Schottky TTL latches are recommended for minimal time skew in the arrival of individual bit signals. This in turn, minimizes glitch energy in the DAC output during code changes.

Interfacing the HI-DAC16 to an 8 bit data bus simply requires the microprocessor to write two consecutive bytes to the DAC input. Unless some form of double buffering is employed, however, the DAC output will assume an unwanted intermediate state during the interval between application of the first byte and arrival of the second. This problem is eliminated in Figure 7 with a few additional ICs.

In Figure 7, the HI-DAC16 is connected to a generalized 8 bit system. The Address Decode Logic produces exclusive low states on Q_1, then on Q_2, for two consecutive addresses. These two decoded address signals are gated with "Address Valid" and "Write" from the microprocessor to produce clock inputs for the latches. As a result, the first (and least significant) byte is latched into FF1, then both bytes are fed to the DAC input simultaneously via FF2 and FF3.

The programmable interface devices available in most microprocessor component families are not "double-buffered" and so offer little advantage for interface to the HI-DAC16. The circuits of Figures 6 and 7 are more direct and less expensive. Also, digital feedthrough to the DAC's analog output can be a problem when interface circuitry is included on the DAC chip. For the HI-DAC16, external gates and latches provide a barrier to shut out this digital noise from the microprocessor.

The author wishes to thank design engineer, Tom Guy, for technical advice in support of this article.

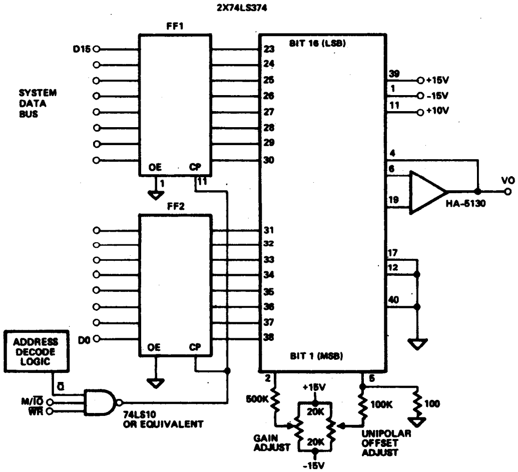

2X74LS374
FF1
FF2
D15
D0
SYSTEM DATA BUS
OE
CP
1
11
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
BIT 16 (LSB)
BIT 1 (MSB)
39
1
11
+15V
-15V
+10V
4
6
19
HA-5130
VO
17
12
40
ADDRESS DECODE LOGIC
Q̄
M/IO
WR
74LS10 OR EQUIVALENT
2
5
500K
+15V
20K
20K
-15V
100K
100
GAIN ADJUST
UNIPOLAR OFFSET ADJUST

Figure 6.

Interface for a 16 bit DAC and 16 bit data bus (8086 system, minimum mode): New data is latched to the DAC input following a simultaneous low on each input to the NAND gate. The latches are strobed when $\overline{\text{WR}}$ returns high.

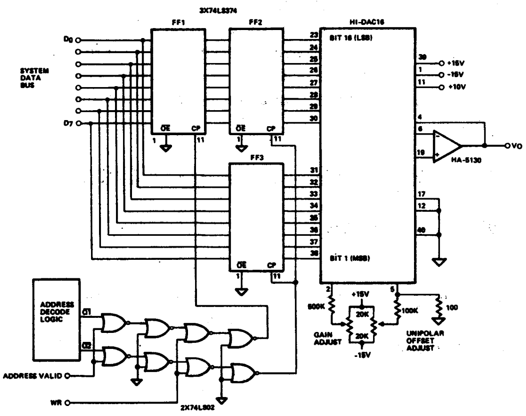

3X74LS374
FF1
FF2
FF3
HI-DAC16
D0
D7
SYSTEM DATA BUS
ŌE
CP
1
11
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
BIT 16 (LSB)
BIT 1 (MSB)
39
1
11
+15V
-15V
+10V
4
6
19
HA-5130
VO
17
12
40
ADDRESS DECODE LOGIC
Q̄1
Q̄2
ADDRESS VALID
WR
2X74LS02
2
5
500K
+15V
20K
20K
-15V
100K
100
GAIN ADJUST
UNIPOLAR OFFSET ADJUST

Figure 7.

An 8 bit data bus feeds a 16 bit DAC through this simple interface. The address for the least significant byte produces Q_1. Coincidence of Q_1, ADDRESS VALID and WR Clocks this first byte into FF1. Similarly, the second byte produces Q_2 which results in a strobe to FF2 and FF3, applying both bytes to the DAC input simultaneously.

APP NOTE

FOR YOUR INFORMATION

No. 540

Harris Analog

HA-5170 PRECISION LOW NOISE JFET INPUT OPERATIONAL AMPLIFIER

By J. S. Prentice and R. W. Leath

INTRODUCTION

The HA-5170 is a precision, JFET input, operational amplifier which features low noise ($12\,\mu V/\sqrt{Hz}$ at 1KHz), low offset voltage ($100\,\mu V$), low offset voltage drift ($3\,\mu V/^\circ C$), and low bias currents (20pA). Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An $8V/\mu s$ slew rate, 5MHz bandwidth and fast settling times less than $1.5\,\mu s$ (settling to 0.01%) make the HA-5170 well suited for fast, precision A/D OR D/A converter designs, precision sample and holds, precision integrators, or transducer signal amplifier designs.

INSIDE THE HA-5170

The Harris technology has two important advantages. First, a unique ion implant process produces JFET's with excellent matching and low 1/f noise. Second, the JFET's are in their own dielectrically isolated islands which completely eliminates the largest gate current component — the island to substrate leakage.

The HA-5170 has two voltage gain stages. The first consists of a differential JFET pair with resistor loads which develops a gain of 10. The second is a complete bipolar op amp with a gain of 30K. The absence of active loads in the first stage insures that the offset voltage, offset voltage drift and noise voltage result exclusively from the input JFET pair.

When it comes to JFET noise, bigger is better. The JFET input noise voltage, both the 1/f and white components, is inversely proportional to the square root of the gate area. Likewise, the input noise voltage due to the drain load resistors is inversely proportional to the square root of the resistance value. The JFET's "weigh in" at a whopping 110 mil^2 gate area with the resistors at $14K\Omega$. This results in typical noise voltages of 12nV/Hz at 1K Hz, 25nV/Hz at 10Hz and $1\mu V$ p-p over the 0.1 to 10Hz frequency band.

Trimming the offset voltage of a JFET op amp usually degrades the offset voltage temperature coefficient, so a trim scheme that simultaneously nulls both the offset voltage and offset voltage temperature drift was developed. The dominant JFET mismatches arise from mismatches in the channel height and doping profiles, not photolithography errors. It is not surprising that the V_P mismatches correlate with the I_{DSS} mismatches.

The amplifier offset voltage is given by

$$V_{OS} = \Delta V_P \left(1 - \sqrt{\frac{I_{DS}}{I_{DSS}}}\right) + \frac{V_P}{2}\sqrt{\frac{I_{DS}}{I_{DSS}}}\left(\frac{\Delta I_{DSS}}{I_{DSS}} - \frac{\Delta I_{DS}}{I_{DS}}\right)$$

In this circuit, the mismatch of the drain load resistor sets the JFET drain current mismatch.

$$\frac{\Delta I_{DS}}{I_{DS}} = -\frac{\Delta R}{R}$$

Thus, the offset voltage can be zeroed by trimming the load resistors. Since V_P has a large positive temperature coefficient, the offset voltage drift is normally degraded. By making the loads from composite resistors, thin film resistors in series with diffused resistors, the temperature coefficient of the $\Delta R/R$ ratio can be set to cancel both the trimming induced drift and also the JFET mismatch induce drift. This makes the HA-5170 the first JFET op amp in which trimming the offset voltage simultaneously trims the offset temperature drift. Furthermore, the offset voltage drift is reduced to even lower values when the offset voltage is nulled externally with an offset adjustment pot. The 5170 has a typical offset voltage of $100\,\mu V$, offset drift of $3\,\mu V/^\circ C$ (without external offset nulling), and warm-up drift of only $20\mu V$.

The excellent dc performance of the HA-5170 is complemented with dynamic ac performance never before available from precision operational amplifiers. The $8V/\mu$ slew rate and 5MHz bandwidth allow the designer to extend precision instrumentation applications in bolth speed and bandwidth. The fast settling time of the HA-5170 (typically less than

1.5μs, settling to 0.01%) also makes it well suited for fast precision A/D and D/A converter designs.

APPLICATIONS

Several applications which utilize the design features and excellent performance of the HA-5170 are described below.

Single Op Amp Instumentation Amplifier

The HA-5170 may be used as a single op amp instrumentation amplifier because of a unique design feature which places the offset adjust terminals at the juncture of two differential gain stages. The instrumentation amplifier, as shown in Fig. 1, is very simple and provides good performance features such as low noise, low offset voltage, low offset voltage drift and high input impedance at low cost.

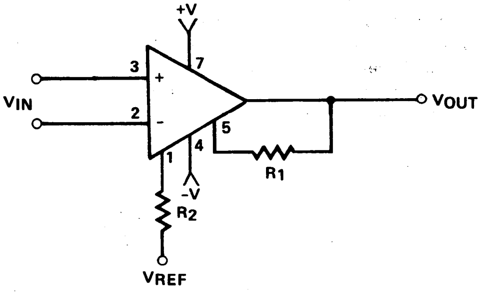


Figure 1. Single Op Amp Instrumentation Amplifier

The gain of the first differential stage is internally fixed at a gain approximately equal to 12. A feedback resistor R_1 connected between the output (Pin 6) and the balance pin (Pin 5) will close the loop around the second differential stage and set its gain. The closed loop gain of the instrumentation amplifier varies directly with the value of R_1 and is approximately

$$A_{VCL} = 12.5\ V/V/K\Omega$$

The minimum gain which can be applied is about 125 ($R_1 = R_2 = 10K\Omega$) because the current into pins 1 or 5 must be limited to 4mA.

The second resistor (R_2, which is connected between Pin 1 and a reference voltage) is used to establish a reference voltage level for the output. This reference voltage may be placed at ground potential or may be variable for use as offset adjustment. The resistor R_2 should also be matched with R_1 in order to maintain high common mode and power supply rejection ratios. Standard 1% tolerance resistors will typically provide 90dB rejection ratios.

The two inputs of the HA-5170, pins 2 and 3, may now be used as high impedance, true differential inputs with a common mode range of $-V_{supply}+3V$ to $+V_{supply}+0.1V$. If resistor values $R_1 = R_2 = 16K\Omega$ are used, for example, this circuit will provide a closed loop gain of 200 with a 3dB bandwidth of 20kHz and a THD $< 0.5\%$ ($V_{out} = 2V_{p-p}$). The gain linearity is typically better than 0.2%. However, the gain also changes about 0.2%/V with both common mode and power supply voltages. The gain T.C. is around 450ppm/°C but this can be reduced to less than 200ppm/°C just by using carbon film resistors which normally have negative T.C.'s (approximately 260ppm/°C for 16KΩ resistors). Of course using resistors which have negative T.C.'s near 450ppm/°C will cancel gain T.C.'s altogether. If a variable gain is desired, a trim pot (in addition to R_1 and R_2) may be placed between the offset adjust pins. Resistors R_1 and R_2 and the maximum value of the trim pot will set the minimum gain. As the resistance of the trim pot is decreased, the gain will increase proportionally to the inverse of the trim pot resistance. This relationship of gain and trim pot resistance is shown in Fig. 2.

This circuit also maintains all to the HA-5170's excellent as and dc characteristics such as low offset voltage, low offset voltage drift, low noise, and high gain.

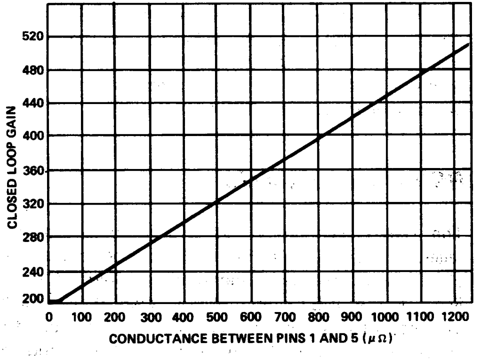


Figure 2. Closed Loop Gain Vs. Conductance Of Trimpot

SINE WAVE OSCILLATOR

The instrumentation amplifier circuit described above can be easily modified to produce a low distortion sine wave oscillator with voltage controlled amplitude as shown in Fig. 3. The small changes in gain of the instrumentation amplifier that occur with changes in common mode voltage has been exploited here to provide oscillator amplitude control with a voltage source. Another unique feature of this circuit is that is does not require any of the nonlinear components that most other sine wave oscillators require.

The phase lead network, which consist of R_3, R_4, and C_1, cancel the phase lag through the amplifier and oscillation occurs at the frequency where the product of amplifier gain and voltage feedback exactly equals one. The amplifier gain is expressed as

$$A_V = \frac{A}{(1 + j\,\omega/\omega_o)}$$

where A is the dc gain (about 125 for $R_1 = R_2 = 10k\Omega$), ω_o is the bandwidth (about 200K rad/s) and ω is the frequency of oscillation. The voltage feedback is expressed as

$$\frac{j\,\omega C_1 R_4}{[1 + j\,\omega C_1 (R_3 + R_4)]}$$

For their product to be equal to one, both of the following must be true:

$$\omega = \frac{\omega_o}{[C_1 (R_3 + R_4)]}$$

$$AC_1R_4 = C_1 (R_3 + R_4) + \frac{1}{\omega_o}$$

The oscillation amplitude is stabilized at the point where the loop gain is equal to one by the small gain nonlinearity of the instrumentation amplifier.

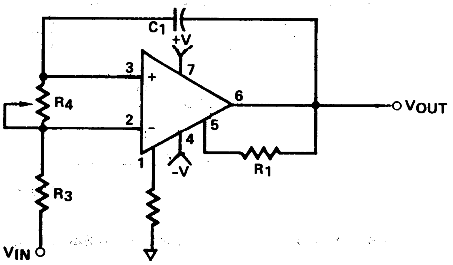


Figure 3. Sine Wave Oscillator With Voltage Controlled Amplititude

This operating point and initial amplitude is set by the resistor divider network of R_3 and trim pot R_4 ($R_4 \ll R_3$). The amplitude can then be varied by applying a common mode voltage (V_{IN}) through R_3. Positive common mode voltages increase amplitude by decreasing gain non-linearity while negative common mode voltages decrease amplitude. A typical curve of amplitude versus common mode voltage is shown in Figure 4. The gain non-linearity of the instrumentation amplifier is small, however, and distortion less than 0.5% can be obtained over a 100Hz to 100kHz range.

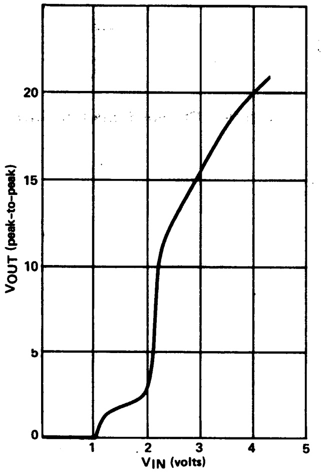


Figure 4. Oscillation Amplitude Vs. V_{IN}

Frequencies down to 10Hz can be achieved by lowering ω_o with a capacitor in parallel with R_1.

HIGH IMPEDANCE TRANSDUCERS

The HA-5170 is well suited as a preamplifier for high impedance transducers, such as photo diodes and hydrophones, because of its high input impedance and low current noise. Fig. 5 shows a photo diode preamplifier circuit whose output voltage is approximately the photo diode current times the value of R_1. When no light is present, the output of the HA-5170 is

$$V_O = I_{ND} R_1 + I_N R_1 + V_{NR} + V_N$$

where I_{ND} = Shot noise of diode
I_N = Noise current of Op Amp
V_{NR} = Noise voltage of resistor
V_N – Noise voltage of Op Amp

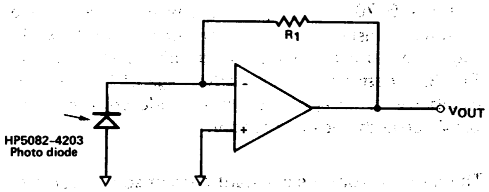


Figure 5. Photodiode Preamplifier

The signal to noise ratio is maximized when the rms sum of op amp and resistor noise current sources is equal to or lower than the noise current of the photo diode. Noise voltage sources are converted to noise current sources by dividing by R_1. The noise current of the photo diode may be approximated by the shot noise formula $2qI_d$, where I_d is the dark current, and is in the range of 10^{-13} to 10^{-14} $A/\sqrt{Hz}$, depending upon the choice of photo diodes. The rms sum of the three sources is approximately 4×10^{-14} $A/\sqrt{Hz}$ at 1kHz, assuming $R_1 = 20M\Omega$. This rms summation is approximately the same magnitude as the noise current of the photo diode with the dominant noise source being the resistor noise (about 2.9×10^{-14} $A/\sqrt{Hz}$). If a bipolar op amp were used instead of the HA-5170, the noise current (typ. 4×10^{-13} $A/\sqrt{Hz}$) would be much higher than the noise current of the photo diode. The response time of the photo diode can be improved by applying 5 to 20 volts of reverse bias but the increased speed is achieved at the expense of higher shot noise.

A resistor equal to the feedback resistor could be inserted between the non-inverting input and ground to reduce offset voltage. This is usually not necessary since the output offset voltage would only be 600μV for a 20MΩ resistor.

Fig. 6 shows a hydrophone preamplifier with a 100Hz to 100kHz bandwith and a gain of 100. Since hydrophone impedance is capacitive, it should be bypassed with a large bleeder resistor to shunt the bias currents to ground.

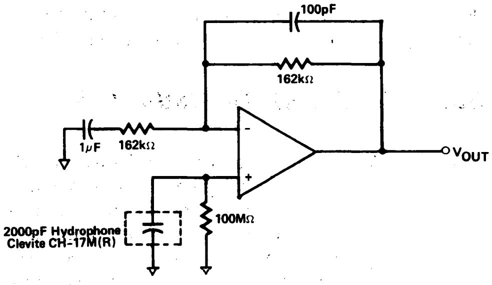


Figure 6. Hydrophone Preamplifier

CURRENT SOURCE/SINK AND CURRENT SENSE CIRCUITS

The HA-5170 can be used as a well regulated, two terminal, constant current source or sink, as shown in Fig. 7, or as a current sense amplifier, as shown in Fig. 8. These circuits take advantage of FET inputs' capability to accept a common mode voltage up to 0.1V above the positive supply.

The current from the constant current source consists of amplifier supply current and load current through R_2, both of which pass through the sense resistor R_1. The amplifier output will sink just enough current to cause the IR drop across R_1 to equal the amplifier offset voltage. This offset voltage may be adjusted by the trim pot R_3 and typically has a minimum adjustment range of 6mV. Smaller offset voltages give better power supply rejection ratios and usually give better results. The amplifier supply current, typ. 1.8mA, sets the minimum constant current while the amplifier short circuit protection limits the maximum to 15mA. Current regulation better than 0.08%/V and temperature variations better than 0.08%/°C can be achieved with this design.

Two operating constraints should be observed for best results. The resistor R_1 should be selected so that the amplifier output voltage remains at least 1.3V from either supply pin and the total voltage across pins 4 and 7 should be at least 12V but not over 40V.

The HA-5170 may also be used as a simple current sense amplifier in power supply applications. In this circuit, the power supply current develops a small voltage drop across the sense resisitor (R_S in Fig. 8) and the ammeter will display a current which is equal to $I_s \times \frac{R_s}{R_1}$. Of course the HA-5170 could also be placed in an open loop (comparator) configuration in which case the output would "trip" when the IR drop across R_s exceeds the offset voltage. This "trip" point can be controlled by an offset adjust trim pot connected as shown. The low noise, low offset voltage, and low bias current characteristics of the HA-5170 provide accurate measurement of supply current with very few components and can operate over a supply range of 7 to 40V.

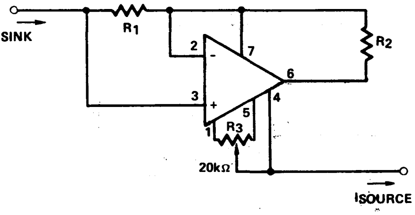


Figure 7. Two Terminal Constant Current Source/Sink

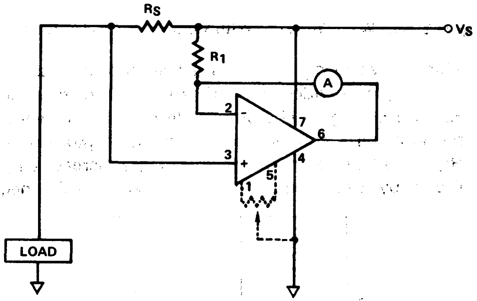


Figure 8. Current Sense Amplifier

APP NOTE

FOR YOUR INFORMATION

No. 541

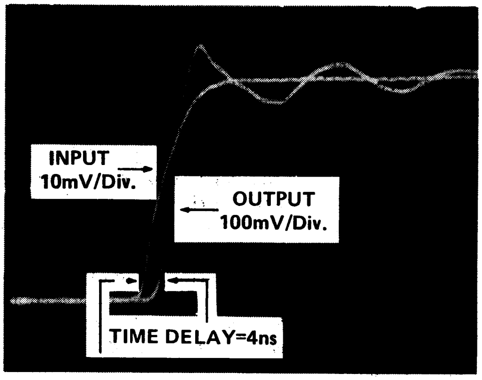
Harris Analog

USING HA-2539 VERY HIGH SLEW RATE WIDEBAND OPERATIONAL AMPLIFIERS

By Richard Whitehead

Introduction

With the superior dynamic performance available from HA-2539, a wide variety of applications can be "idealized". From high fidelity audio to television broadcast and receiving equipment these operational amplifiers can be used to provide increased system capabilities. Employing the Harris high frequency dielectric isolation process these true differential input devices offer 600V/μs slew rate coupled with 600MHz gain bandwidth product. These parameters in conjunction with an excellent time delay of 4ns (see photo), standardize HA-2539 in critical wideband video and RF applications.



HA-2539 Transient Response Waveforms

Protyping With HA-2539

Being a "true" operational amplifier, HA-2539 may be "designed in" using conventional high frequency amplifier techniques. Quality I.C. sockets may be used, but for maximized dynamic performance it is suggested these devices be mounted through a ground plane. External components should have minimal lead lengths and preferably connected directly to the device pins. Metal film or metal oxide resistors are recommended for feedback components. If direct connection is not possible, Teflon insulated standoffs should be used with locations as close as possible to device pins. Power supply decoupling with .001μF ceramic ca-

is essential. Alternatively, filter connectors such as Erie 1201-052 are suggested for optimum decoupling.

HA-2539 may be used without heat sinks up to +75°C ambient. Power derating above this temperature is 8.7mW/°C and heat sinking is recommended. Thermalloy model 6007 or Unitrack CPU 1017 heat sinks are suggested for temperatures up to +125°C ambient.

General Operating Considerations

Dynamic performance of HA-2539 was maximized through the exclusion of output short circuit protection and internal offset voltage adjustment circuitry.

Although these amplifiers can withstand momentary short circuits to ground, it is recommended that some output current limiting network be used, if the operating environment is hostile. Figure 1 shows a suggested method for output terminal protection.

Offset voltage adjustment may be accomplished by the suggested methods shown in Figure 2 (a) and (b).

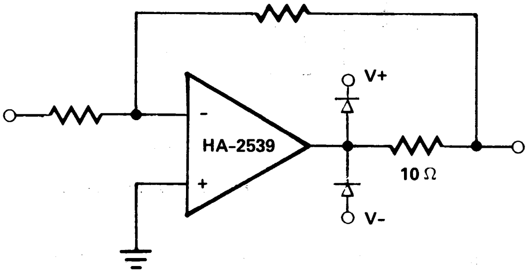
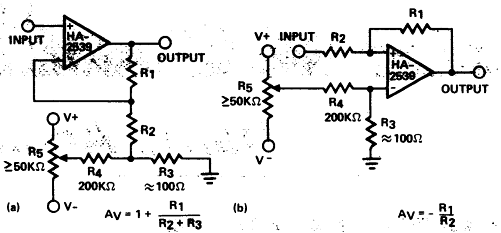


Figure 1. OUTPUT PROTECTION FROM FAULT CONDITIONS



RANGE OF ADJUSTMENT FOR BOTH NON-INVERTING (LEFT) AND INVERTING AMPLIFIERS (RIGHT) DETERMINED BY PRODUCT OF V_{SUPPLY} AND R_3/R_4 RATIO.

Figure 2. OFFSET NULLING

As with many wideband, high speed devices, recovery from output saturation can be in the order of microseconds. HA-2539's saturation recovery from its positive rail is of the classical variety where voltage charges on the "body" capacitances of output devices must discharge before normal operation can be resumed. Recovery from the negative rail is similar to the positive rail recovery except during saturation small signal oscillation may occur. This oscillation is due mainly to a regenerative signal coupled back to the input during saturation.

General Applications

FREQUENCY COMPENSATION

HA-2539 is stable in standard operational amplifier circuits with closed loop gains exceeding +10 or -9. Keeping the network resistor values as low as practical in these configurations should optimize the dynamic performance.

Circuit configurations shown in Figure 3 may be used to stabilize HA-2539 at closed loop gains less than specified. Figure 3 (a) employs capacitance to over damp HA-2539's response. Stable operation to gains of 5 are practical. Figure 3 (b) utilizes the amplifier's differential input impedance to reduce input and feedback signals thereby raising noise gain to a stable point on the response curve. Gains of -3 are practical.

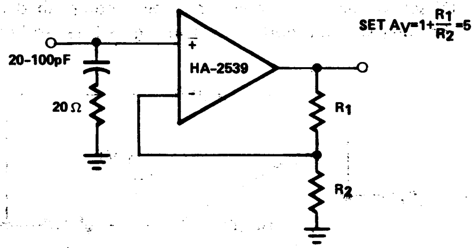


Figure 3. a. COMPENSATION BY OVERDAMPING

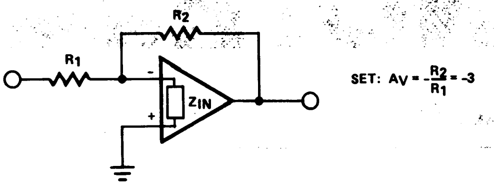


Figure 3. b. STABILIZATION USING Z_{IN}

Reducing DC Errors

A composite amplifier scheme may be used to reduce errors due to offset voltage and bias current. Figure 4 shows HA-2539 and HA-5170 in a composite configuration which greatly reduces DC errors without compromising the high speed, wideband characteristics of HA-2539.

The HA-2539 amplifies signals above 40KHz which are fed forward via C_2 and R_2. Resistors R_4 and R_5 set the voltage gain at -10. The slew rate of this circuit was measured at 350V/μs. Settling time to a 0.1% level for a 10V output step is under 150ns and the gain bandwidth product is 300MHz.

The HA-5170 amplifies signals below 40KHz, as set by C_1 and R_1, and controls the dc input characteristics such as offset voltage, drift, and bias currents of the composite amplifier. Therefore, it has an offset voltage of 100μV, drift of 2μV/°C and bias currents in the 20pA range. The offset voltage may be externally nulled by connecting a 20K pot to pins 1 and 5 with the wiper tied to the negative supply. The dc gains of the HA-5170 and HA-2539 are cascaded which means that the dc gain of the composite amplifier is well over 160dB.

The excellent AC and DC performance of this composite amplifier is complemented by its low noise performance, 0.5μV rms from 0.1Hz 100Hz, and makes it very useful in high speed data acquisition systems.

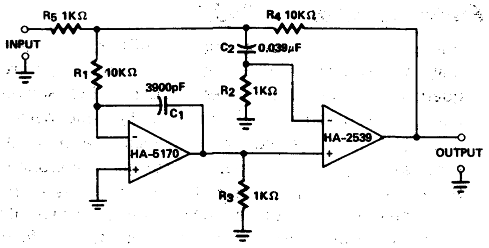
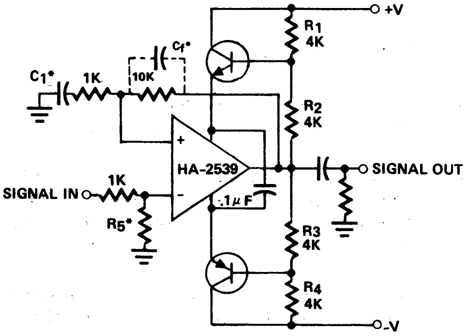


Figure 4. COMPOSITE AMPLIFIER

Boosting Output Power And Increasing Output Signal Swing

Figure 5 shows a cost effective method for increasing output voltage swing or boosting power of HA-2539 while adapting the device to supply rails which exceed the absolute maximum ratings. The supply rail values are limited only by the breakdown voltages of the transistors used, provided R_1 through R_4, are set to limit the voltage at the device supply pins to nominal supply values (±15V). Transistor selection should be limited to high f_T (greater than 60MHz) types such as MPS-A06 and MPS-A56. Physical layout properties may necessitate the use of phase lead compensation, in which case C_F may be added. It has unmeasurable distortion and very low noise within the audio band.



*NOTES

1) Used for experimental pourposed. $C_f \approx 3pF$.

2) C_1 is optional (.001μF~.01μF ceramic)

3) R_5 is optional as can be utilized to reduce input signal amplitude and/or balance input conditions $R_5 = 500\Omega$ to $1K\Omega$.

Figure 5. BOOTSTRAPPING FOR MORE OUTPUT POWER AND VOLTAGE SWING

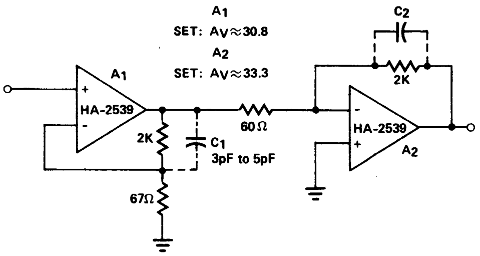
Applications

INTRODUCTION

HA-2539 may be utilized in a wide variety of applications ranging from active filters to video pulse amplification. However, the applications to follow were selected to show where this can be used most advantageously.

APPLICATION 1: CASCADED AMPLIFIER

Cascaded amplifier sections are used to extend bandwidth and increase gain. Using two HA-2539 devices, this circuit is capable of 60db gain at 20MHz.



APPLICATION 1 CASCADED AMPLIFIER SECTION

APPLICATION 2: VIDEO GAIN BLOCK

Video drivers and gain blocks used in color video systems are most always required to have outstanding differential phase and differential gain specifications. These requirements historically have eliminated the use of operational amplifiers and favor large discrete amplifiers which can be tailored to minimize system errors.

This configuration utilizes the wide bandwidth and speed of HA-2539 plus the output drive capability of HA-2630. Stabilization circuitry is avoided by operating HA-2539 at a closed loop gain of 10 while maintaining an overall block gain of unity. However, gain of the block may be varied using the equation:

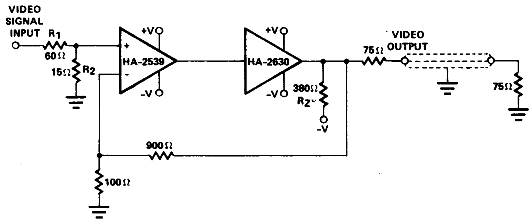
$$\frac{V_{OUT}}{V_{IN}} = 5 \frac{R_2}{(R_1+R_2)}$$

where $R_1 + R_2 = 75$ ohms

A maximum block gain of 3 is recommended to prevent signal distortion.

The output stage of HA-2630 is biased to a higher current level through resistor R_Z. Maintaining this biased "on" condition reduces signal distortion and virtually eliminates errors due to differential phase by decreasing the percent change in the output stage operating point.

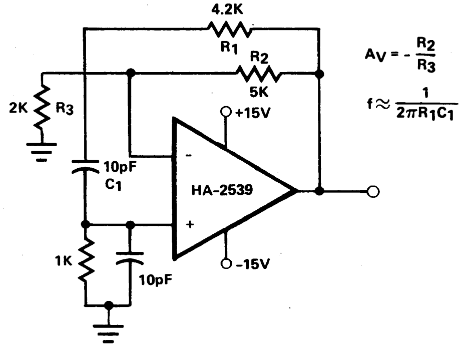
The circuit in Figure 1 was tested for differential phase and differential gain using a Tektronix 520A vector scope and a Tektronix 146 video signal generator. Both differential phase and differential gain were too small to be measured.


VIDEO SIGNAL INPUT
R1
60Ω
15Ω
R2
+V
-V
HA-2539
HA-2630
380Ω
Rz
-V
75Ω
VIDEO OUTPUT
75Ω
900Ω
100Ω

APPLICATION 2 VIDEO GAIN BLOCK

APPLICATION 3: HIGH FREQUENCY OSCILLATOR

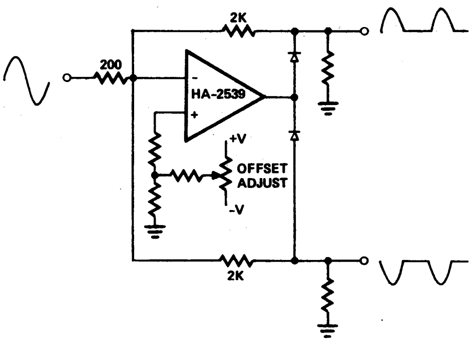
Intended primarily as a building block for a QRP transmitter, this 20MHz oscillator delivered a "clean" 6Vp-p signal into a 100 ohm load.


4.2K
R1
R2
5K
2K
R3
+15V
-15V
10pF
C1
HA-2539
1K
10pF
$A_V = -\frac{R_2}{R_3}$
$f \approx \frac{1}{2\pi R_1 C_1}$

APPLICATION 3 20MHz OSCILLATOR

APPLICATION 4: WIDEBAND SIGNAL SPLITTER

With one HA-2539 and two low capacitance switching diodes, signals exceeding 10MHz can be seperated This circuit is most useful for full wave rectification, AM detectors or sync generation.


2K
200
HA-2539
+V
OFFSET ADJUST
-V
2K

APPLICATION 4 WIDEBAND SIGNAL SPLITTER

Acknowledgments

A. Terry D. Hass of Solitron, Inc., Stuart, Fl. developed and tested video gain block.

B. Ron Jasinski of Sound Studio Services, 3208 Cahuenga Blvd. West, Los Angeles, CA. 90068 Developed and tested bootstrapped output scheme.

C. Russ W. Leath of Harris Semiconductor developed and tested composite amplifier circuit.

References

Application Note 525 - HA-5190/5195 Fast Settling Operational Amplifier May 1979.

Tobey, Braeme, and Huelsman. Operational Amplifiers Design and Applications. New York: McGraw-Hill Book Company, 1971.

APP NOTE

FOR YOUR INFORMATION

No. 542

Harris Analog

USING THE HV-1000 INDUCTION MOTOR ENERGY SAVER

By P. W. Shackle and R. S. Pospisil

WHAT'S IN A NAME?

The HV-1000 is an integrated circuit intended to reduce onto one chip, most of the circuitry of the single phase, induction motor, energy saver circuits first described by Frank Nola of the NASA Marshall Space Flight Center in U.S. Pat. 4052648. The original name given to such motor controller circuits was "power factor controller", or more precisely "power factor sensing controller". The origin of this name lay in the fact that induction motors draw almost a constant current regardless of load, as long as the motor is turning. The motor responds to loading by producing a more resistive power factor, thus drawing more power from the line. The load on the motor can be sensed by measuring the power factor, and so this can be used as the basis of a control algorithm. The original controllers adjusted the firing time of a TRIAC in series with the motor in such a way that the time delay between the voltage zero crossing and the current zero crossing was reduced and held constant. To the extent that this time interval represents the power factor for a non-sinusoidal waveform, the power factor was indeed being improved and kept constant. However, if one adopts the utility company definition of power factor as

$$\frac{\text{Watts}}{\text{Volt Amperes}}$$

then, because both the Amperes and the Watts are reduced roughly proportionately, the power factor, by this definition, is almost unchanged. To avoid confusion, Harris has chosen not to refer to power factor control, using instead the acronym "IMES" (Induction Motor Energy Saver).

APPLICATIONS

Generalities on when to use an IMES:

The induction motor energy saver performs its function by taking advantage of the fact that an AC induction motor runs at almost a constant speed regardless of the voltage applied, its speed being determined by the frequency of the AC supply. When the motor is lightly loaded the voltage applied to the motor can be reduced so that it consumes less current and power, as long as a sufficient voltage remains to drive whatever load is present. All that the IMES does is to sense the load on the motor (through the power factor), and then turn down the voltage by a predetermined amount. To a first approximation, the usefulness of applying an IMES in a given situation can be gauged by driving the motor with a variable transformer and using a power meter to measure the power consumed. If there are circumstances where reducing the voltage reduces the power consumed, then probably the IMES can save some energy. Remember when you do this that the IMES can turn the voltage up and down much faster than you can to follow rapid variations in loading.

Some obvious circumstances where a motor is very lightly loaded part of the time include a radial arm saw (or any saw), a bench grinder or a drill press. In each case it is easy to see that until the machine is actually cutting something, little work is being done and usually the power consumed can be reduced by having the IMES reduce the voltage in between the actual work periods. Less obvious circumstances are the commercial washing machine and the office typewriter. The key to these applications is that in each case, the motors in question must be capable of briefly delivering very high torque, so that for much of the rest of the time, the motor is relatively lightly loaded. The would-be energy saver engineer must keep firmly in mind the fact that for energy savings to be possible, the motor must be relatively lightly loaded compared to its real capability. To make the point more strongly, if you reduce the voltage applied to a one horsepower motor when it is driving a one horsepower load, most likely it will use more power, not less. For example, many of the pump designs used for irrigation sprinklers, pool pumps and well pumps are relatively inefficient hydraulically and load their motors to about the same degree regardless of the volume of water being pumped. Furthermore, the motor supplied is likely to be very well matched to this nearly constant load so that any attempt to reduce the voltage with an IMES will cause more, not less power to be used.

Sometimes the manufacturer of say, a belt sander or a sump pump will have designed the equipment with the idea in mind that the usage will only be very intermittent. In this case, when the motor is actually working, it might be outputting twice its rated power. If this condition were prolonged, the motor might be burned out very rapidly. Clearly no power savings are to be had when the machine is loaded. In the case of the sump pump, no savings are to be had at all since the motor is off when it is not pumping. In the case of belt sanders, the authors have once seen a belt sander in which the motor was running almost at full load when the machine was not doing any work at all. Again, no energy savings are possible in these circumstances by reducing the voltage. This should not be taken as an implication that the IMES cannot be used on any belt sander – merely that some such machines can have much under-powered motors.

One application that is less obvious is the reverse cycle air conditioner or heat pump. It frequently happens that the motor in these machines is much less heavily loaded during the heating cycle than it is during the cooling cycle. In this case, application of the IMES can result in useful energy savings. An industrial clutched compressor, where the motor runs continuously and the compressor is clutched in intermittently, is another useful application.

Three specific tests to identify an IMES application:

From the foregoing discussion and examples, we can now proceed to develop a set of test criteria which allow the identification of good applications for the IMES. The first question is – is the motor in question a single phase induction motor? Vacuum cleaners and portable drills, for instance, frequently have so called universal motors, a totally different kind of motor to which the IMES is not applicable. The IMES principle can be applied to big industrial three phase motors, but such controllers are typically complex and expensive systems. The prime candidates for application are single phase, 120 or 240V induction motors of more than ¼ HP. The HV-1000 can be applied to capacitor-start motors and to capacitor-start, capacitor-run or two value capacitor motors. It would not normally be useful to apply it to a permanent split capacitor motor, since these are usually applied to equipment with steady, non varying loads.

The second question is – does the motor in question experience strongly varying loads, with a large part of the time being lightly loaded? For instance, most ventilation fans have very steady loads and could not be expected to show any power savings. On the other hand, industrial sewing machines have such strongly varying loads that large flywheels are often incorporated to try and smooth the variations. These are an excellent area of application for the IMES.

The third question to be asked is whether the motor operates a sufficient number of hours per year, for the power savings that result, to pay for the cost of the IMES over the lifetime of the equipment, or in the case of an after-market add on, over the desired financial payback period. Sometimes surprising results are obtained – for instance, consider a typewriter which uses 60W when plugged in. If it runs eight hours a day, five days a week for a year, the motor is switched on for 2080 hours per year. With the IMES attached, the power consumed may go down to only 30W, a savings of 30W or 62.4 kilowatt hours per year. In an area such as New York City, where electricity costs about $.10 per KW hour at time of writing, the savings are $6.24 per year or $18.72 over a three year payback period. This number is surprisingly large considering the low power consumption of the typewriter, but the result is inflated by the 50% savings which are possible. In the case of say, a domestic washing machine, energy savings of 60 W-hours are possible over a complete cycle. So that with ten cycles per week, the potential savings are 31.2 KW hours per year. At an average power cost of $.07 per KW hour, the savings are $2.18 per year or $13.10 over a six year lifetime. In a launderette context where 100 cycles per week are possible, the savings would be $21.84 per year. A profile of a typical application of an IMES might be a light industrial carpentry shop where a circular saw operated by a ¾ HP motor was operated for six hours per day. For 50% of the time, the saw is spinning idly as the planks are loaded in to be cut or cleared away. When idling, the motor normally draws 200W – this is reduced to 100W by the IMES. Thus the savings are .1KW x 6 x 50% x 260 days = 78 KW hours per year. At an average price of $.07 per KW hour, the payback is $5.46 per year of $27.30 over a five year lifetime for the machine. Finally, in computing savings, the hard to quantify fact should not be forgotten that most motors run quieter and cooler with an IMES.

PRECISELY, WHAT DOES THE HV-1000 IMES DO AND WHY DOES IT HAVE TO BE THAT WAY?

In this section we describe the functional capabilities of the HV-1000 and their significance for the user.

The characteristics of a TRIAC controlled motor:

The earliest IMES circuits simply placed a TRIAC in series with the motor and gated the TRIAC on at such a point in each half cycle, that the time delay between the current zero crossing and the voltage zero crossing was kept constant (Figure 1). The trouble with this method of control is that in order for the motor to respond in a stable fashion, the phase sense signal had to be averaged over many cycles otherwise the slightest jerk, vibration, or electrical noise would produce an undesirable large response from the motor. This then gave another problem – that a genuinely fast changing load was not catered to – e.g. when feeding the wood into a circular saw, the motor would stall before the controller turned the voltage up in response to the load. For this reason, it is necessary for an IMES to have a load anticipator or panic button. When a rapid increase in load is sensed, the HV-1000 IMES instantaneously produces full voltage, preventing a stall.

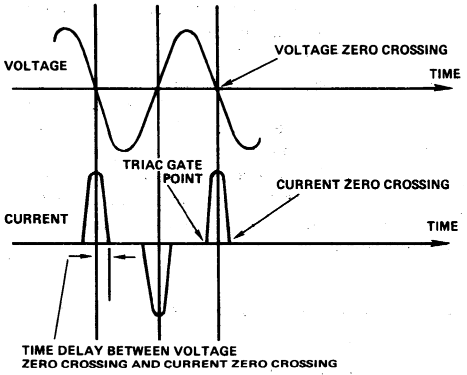


Figure 1.

In determining the best characteristics for an IMES, it is clearly necessary that when the motor is fully loaded, the TRIAC should be fired at the current zero crossing. In other words, the TRIAC should be on continuously, so that full voltage is applied to the motor. This also defines the desired point in the cycle for the current zero crossing. The diagram at the top of Figure 2 illustrates the voltage waveform as a function of time across the terminals of a TRIAC controlled motor. θ_C is the current zero crossing and θ_t is the TRIAC trigger point. At full load these should coincide. If a motor is controlled in such a way that θ_C is kept constant, then as the state of the motor is moved from full load to no load, θ_t will be observed to gradually move to the right, resulting in a throttling back of the voltage applied to the motor. At no load, θ_t will have been delayed by the maximum amount consistent with maintaining θ_C constant. If, by virtue of forced control of the system, θ_t is now moved even further to the right, θ_C will move to the left, but most motors will keep running. In other words, this experiment demonstrates that simply maintaining θ_C constant is not the optimum algorithm for getting the best savings — more power savings can be obtained by an algorithm which moves θ_C to the left by a few hundred microseconds as the load on the motor decreases.

To quantitatively represent this more optimum algorithm, the graphical presentation in the lower half of Figure 2 is helpful. θ_C is plotted against θ_t, and the resulting plots can be used to characterize both the motor and the controller. To characterize the motor, consider first the circumstance where full voltage is applied to the motor. In this case, $\theta_C = \theta_t$ and the full voltage condition may be represented by the line AC along all points of which $\theta_C = \theta_t$. The operating point will move up and down AC as the motor load is varied. Now, suppose that for a given value of θ_t, the load on the motor is increased, decreasing θ_C, until the motor stalls. Recording the value of θ_C at which this happens produces the line DB, the locus of θ_C values at which the motor stalls. It is apparent that for a given point on AC, i.e. a given load, θ_t can be increased (the motor throttled back) at constant load. θ_C will decrease in response, and the operating point of the motor will trace out a line, such as CB, until the motor finally stalls. In this way, the family of curves CB, AD, etc. is traced out. These curves represent the characteristics of a TRIAC controlled motor.

The HV-1000 algorithm:

In the experiment described above, θ_C was kept constant starting from point A, the fully loaded motor with full voltage. It can now be seen that the classic "constant power factor" type of controller has a characteristic which is a horizontal line of constant θ_C across to the no load characteristic from point A. Clearly point B, the condition where the motor is throttled back as much as possible, will never be achieved unless the controller has a characteristic which allows θ_C to vary with θ_t. The HV-1000 IMES is programmed with such a characteristic, shown by the controller line of Figure 2. The HV-1000 IMES does not keep θ_C constant, but instead allows it to vary in such a way that the voltage is throttled back as much as possible for lightly loaded motors. The curves of Figure 2 were plotted for a General Electric ⅓ HP general purpose motor. Different families of curves will be obtained for other motors. The controller line corresponds to the HV-1000 without an external potentiometer (pins 4, 5, 6 shorted together).

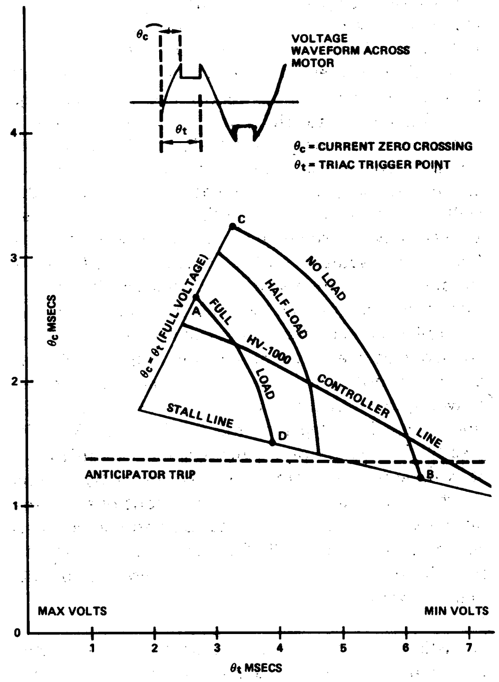


Figure 2.

The load anticipator:

Figure 2 illustrates several interesting properties of the HV-1000/motor combination. Note that the controller line does not hit the full voltage line until above full load; in other words, the voltage is still throttled back slightly even at full load. For this particular motor this produces close to optimum power savings. For a small number of motors the controller line may have to be moved up or down (see next section) with an external potentiometer to get optimum power savings. When the HV-1000 is fitted with a relatively small (e.g. 0.10 microfarad) time constant capacitor, the operating point of the motor will be observed to stay usually within 100 microseconds of the controller line. However, with a relatively large (5 microfarad) time constant capacitor the response time of the system will be several seconds. In this case when a sudden shock load is applied, θ_t will at first stay constant, and the operating point will drop vertically downwards as θ_c diminishes. Because of angular momentum stored in the rotor and pulleys, the operating point may actually drop a few hundred microseconds below the stall line before the motor stops. As mentioned above, the HV-1000 has built into it a load anticipator designed expressly to prevent such a stall. Its operation can be represented by the "anticipator trip" line shown in Figure 2. Whenever θ_c drops below this line, the HV-1000 connects an "on" SCR and a resistor across the time constant capacitor and discharges it, after at most a hundred milliseconds, depending on the size of the capacitor. The HV-1000 thus is forced to produce full output voltage almost instantaneously. It will be observed, that since the controller characteristic slopes, the anticipator trip line is much closer to the controller line at no load than it is at full load. At no load, only a small disturbance is required to trigger the anticipator, whereas at half load, a much larger shock (and corresponding change in θ_c) is needed to trigger the anticipator. The trip line shown represents the HV-1000 without an external potentiometer. It is interesting to observe that above half load, the trip line actually lies below the stall line. This means that in this region the anticipator can only be tripped by a very large, sudden shock load, which actually pushes θ_c momentarily below the stall line. In theory, there exists a certain size and rate of change of shock, which is fast enough that the controller cannot respond normally, and yet slow enough that the anticipator is not tripped. For this particular motor, there was no problem in practice; however, there are motors with a relatively higher stall line, where it is apparent that adding the HV-1000 clearly does cause premature stalling. In this case, it is necessary to increase the sensitivity by moving up the anticipator trip line. This is controlled by the absolute value of the external potentiometer when added on pin 4, 5 and 6. 5k ohms raises the trip line by 100 microseconds, 10k ohms raises it to 200 microseconds.

Adjusting the set point of the potentiometer allows the controller line to be moved vertically up and down on the θ_c axis. For small absolute values (e.g. 1k) the motion is essentially upwards only, and depending on the motor, may not be sufficient to apply full voltage to an unloaded motor. A 10k potentiometer will allow up to 500 microseconds of downward movement and will permit even an unloaded motor to have full voltage applied. When the controller line is slewed up and down with an external potentiometer, the anticipator trip line is automatically moved by the same amount in the same direction so that the relationship between the two lines is unchanged. This relationship can only be changed by modulating the absolute value (not the ratio) of the potentiometer. As a starting point where a potentiometer has to be added to optimise the control line for a given motor, a 2k potentiometer is recommended. Smaller absolute values give a lesser range of control, while larger values tend to make the anticipator too sensitive and the potentiometer setting too critical.

The HV-1000 self-adapts to different motors:

It is illuminating to reflect that, different motors have their no load, half load, etc. curves differently placed on Figure 2, while the contoller line is fixed. Then, when the HV-1000 is applied to different motors, entirely different values of θ_c and θ_t will result at say, no load or half load. This in sharp contrast with the earlier generation of IMES devices which simply forced every motor to a constant θ_c. It can be seen that because of the sloping characteristic of the controller line, the HV-1000 can apply different values of θ_c and θ_t at no load to each motor according to its need. In other words, the HV-1000 has a degree of self-adaptability. It can accomodate a surprisingly wide range of motors using its internal settings without an external potentiometer. The HV-1000, without a potentiometer, will control a majority of fractional horsepower American induction motors. However, when sufficiently common requirements are identified, HV-1005 and HV-1010 are planned, which will have the controller line set at different points on the θ_c axis.

NON STANDARD BEHAVIORS OF THE HV-1000

As stated previously, the HV-1000, with no potentiometer, will do a fairly good job of driving most U.S., fractional horsepower, induction motors most of the time. In this section, we describe a number of circumstances in which undesirable effects can manifest themselves. Most of these are relatively rare, and most represent oversights in the design of the application circuit.

Instability:

The symptom here is the motor shaft drives the load in short, erratic, violent bursts. An erratic banging noise may be heard. This problem is worse with relatively big (above 1 HP) motors for which the ratio of the torque available to the rotor inertia is more extreme. A special kind of application circuit is needed to control the motor in this circumstance, as described in the next section. Motors from different manufacturers vary greatly in their behavior with respect to this problem.

Anticipator banging:

The symptoms of the problem are that the controller rhythmically applies full voltage with a bang, then slowly throttles back until full voltage is again applied with a bang. The periodicity is fixed by the external time constant capacitor. This problem is easily fixed, but very disconcerting when first observed. Refer to Figure 2. It can be seen that inside the no load – full load range of the motor, the anticipator trip line does not intersect the controller line. This is not always the case – suppose, for instance, that the anticipator trip line had been deliberately shifted up with an external potentiometer, when it might intersect the controller line inside the operating area, or possibly a different motor might have characteristics shifted relatively to the right in Figure 2. Again, the intersection of the controller line and the anticipator trip line could come inside the motors operating area (although in practice this has never yet been observed without an external potentiometer). Suppose the system of motor and IMES had just had a heavy load removed. The operating point will relax along the "no load" line CB with a speed fixed by the time constant capacitor. If the anticipator trip line has been moved upwards sufficiently, the operating point will encounter the anticipator trip point before the controller line. The anticipator will then fire, transferring the operating point abruptly to point C. The operating point will then start off along CB again. The cure is to either place a slight load on the motor or to reduce the absolute value of the potentiometer, shifting down the anticipator trip line. If a resistor is being used in series with pin 5, its value should be reduced.

Latch up:

In this circumstance the HV-1000 simply does not throttle back after reacting to a full load. This is normal, expected behavior associated with too high a value of external potentiometer. It normally starts at about 10K ohms, but is somewhat motor dependent. The cure is to reduce the absolute value of the potentiometer or the resistor in series with pin 5.

Gross rectification:

Here the controller applies half rectified AC to the motor, causing it to vibrate loudly and not turn. Switch off at once. It is caused by too small a time constant capacitor. It cannot happen with a time constant capacitor above 0.1µF.

Glitching:

With this effect, the symptom is that the motor intermittently gets a higher voltage applied to it. The effect is infrequent and non-periodic. The most likely cause is voltage spikes on the AC line breaking over the input protection crowbars. When this happens, the output SCRs are usually turned on delivering full power to the motor. The input protection crowbars fire at ±500V. This symptom can sometimes be helped with a capacitor (high voltage!) between pins 1 and 16. Sometimes also electrical noise, even from the firing of the TRIAC, can cause the anticipator to fire prematurely. Placing 0.01µF (5V) between Pins 1 and 12 usually stops such problems, since such noise normally comes in on the phase sense lead, Pin 12. Since A.C. power lines are often full of spikes, infrequent glitches are regarded as normal HV-1000 behavior. They do not detract from power savings and are the means by which HV-1000 protects itself.

DESIGNING THE APPLICATION CIRCUIT FOR HV-1000

A general purpose application circuit for the HV-1000 is shown in Figure 3. This is the simplest application circuit possible, and will satisfactorily drive a large percentage of U.S., fractional horsepower, induction motors. The TRIAC must be capable of handling the locked rotor condition of the motor for as long as this condition may exist. This is often as much as three times or more the normal running current of the motor – as high as 30A for a typical 115V, ½ HP motor. Normally the TRIAC will require some kind of heat sink – eight or ten watts power dissipation in not, uncommonly encountered. The snubber shown is primarily for illustration. Its purpose is to minimize radio frequency interference, prevent high frequencies being sent down the AC line, and to attenuate the inductive voltage kickback, which appears at the zero crossing of the current through the motor, from accidentally triggering the output stage of HV-1000 or the TRIAC. In some circumstances, the snubber capacitor and resistor can be eliminated completely, and the system will still run normally, although generating a lot of radio frequency noise. Different sizes of capacitors will also work.

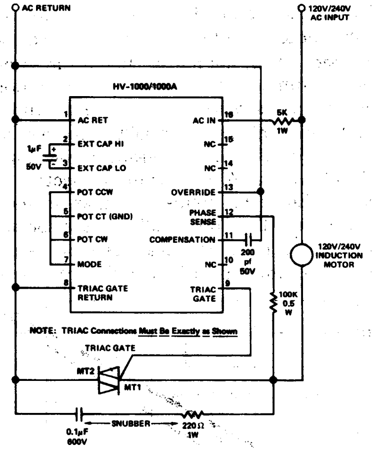


Figure 3. Basic Application Circuit For HV-1000

The 5K ohm resistor shown is for surge protection – in the event of an overvoltage surge, internal protection clamps between pins 1 and 16 breakover and latch down to 1.5V, momentarily dropping all the voltage across this resistor. This voltage can be many kilovolts for a few microseconds, and even though the power dissipation is low, the physically large size of a 1W resistor is needed to stop arcing from taking place between the terminals and to absorb the energy of the surge. The 1μF capacitor sets the response time constant for the system. Figure 4 shows the relationship between capacitor size and response time of the system. It must be kept in mind that this is basically the time in which the IMES throttles back the voltage after removing a heavy load. The load anticipator will always stop the motor from stalling when the load increases sharply. The sensitivity of the load anticipator can be enhanced by adding an external potentiometer. Even with the potentiometer shorted, the HV-1000 will still produce full power in response to extremely sharp load shocks. The greater the absolute value of the potentiometer, the more sensitive is the load anticipator.

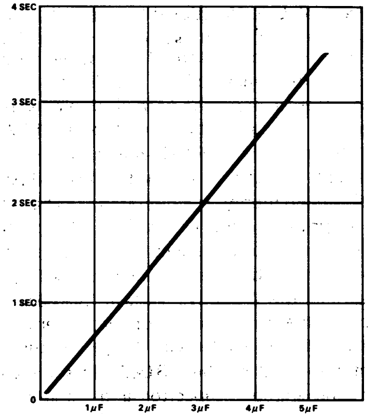


Figure 4.
HV-1000 Response Time as a Function of Capacitor Size

The criteria for satisfactory operation of the HV-1000 IMES circuit are that full line voltage should be applied to the motor when it is close to full load, and that the motor should not stall when exposed to a shock load. Also, the motor should run smoothly at all times without any juddering or vibration. The energy savings should normally be around 50% at no load, diminishing to essentially nothing at full load. A typical plot of Power In against Power Out for the HV-1000 with a ½ HP, Century, electric motor is shown in Figure 5. Remember that in many kinds of equipment, the "no load" losses associated with driving pulley belts and bearings may be sufficient to load the motor by 50 or 100 watts, so the true no load savings of the motor may not be seen.

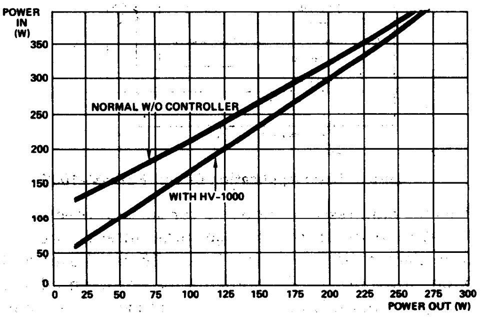


Figure 5.
Power Savings of the HV-1000 on a ½ HP Motor

If the motor stalls more easily with the HV-1000 IMES than it did before, this means that the anticipator trip line is probably too low for the motor and needs raising as described previously. The anticipator sensitivity can be increased with the use of an external potentiometer as shown in Figure 6. A 5 kilohm potentiometer will commonly give a sufficient increase in sensitivity. Ten kilohms gives an extreme increase. If the absolute value of the potentiometer is too high, the motor will observed to give a bump or bang as it gets full power in response to the slightest disturbance. In the extreme case, the rhythmic anticipator banging described in the previous section will be seen. The angular setting of the potentiometer has to be set so that the motor is given full voltage at full load, or produces optimum power savings in the application at hand. (Some motors exist which give optimum power savings when full voltage is only applied at twice full load.) If a piece of equipment is being manufactured containing the HV-1000, then once the potentiometer settings are established, the potentiometer can be replaced by two resistors having the same values. If many hundreds of thousands of such parts are needed, the equivalent resistor settings can be incorporated inside the HV-1000 by arrangement with the factory.

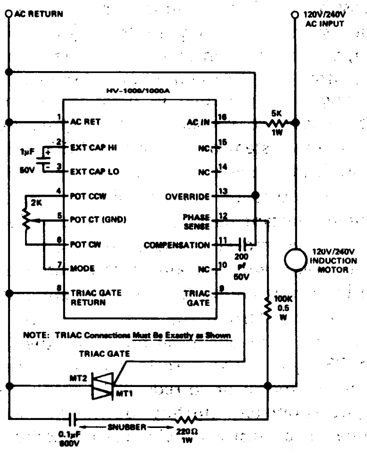


Figure 6.
Application Circuit for the HV-1000 with Potentiometer to get Increased Anticipator Sensitivity and Adjustable Phase Setting.

If difficulties with the stability of the motor being controlled are encountered, as descibed previously, special precautions are needed. The nature of the instability is that the controller may over-correct the voltage in response to a small disturbance in the motor's load. Thus the instability comes about as a result of the relationship between the response times of the motor and controller — for disturbances of a certain frequency, the controller's response may be lagging that of the motor by half a cycle, so the controller is actually increasing the voltage at a point in time when it should be decreasing it. Frequently, the inertia of the motor's normal load slows down the motor's response sufficiently to produce stability. Failing this, capacitor values as large as 10μF or as small as 0.1μF can be tried between pins 2 and 3. If all these simple expedients are not effective, the remedy is to tailor the frequency response of the controller with a circuit like that shown in Figure 7. This circuit is shown for example only, it was found to be optimal for a 1.5 HP Emerson motor. For other motors, slightly different values of the compensation network components connected to pins 2 and 3 may be needed. The purpose of the diode across the 50K resistor is to permit the load anticipator to discharge the 3μF capacitor rapidly, when necessary. At the time of writing no motor has yet been found which could not be stabilized by a compensation network of the general type shown between pins 2 and 3 in Figure 7.

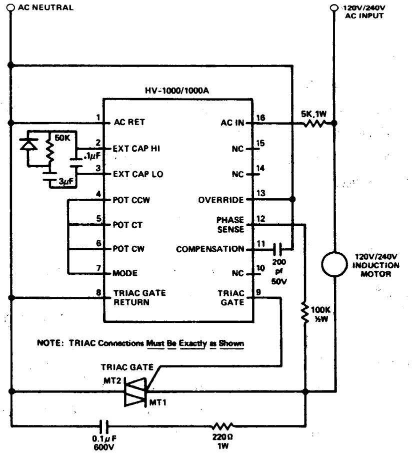

AC NEUTRAL
120V/240V AC INPUT
HV-1000/1000A
1 AC RET
2 EXT CAP HI
3 EXT CAP LO
4 POT CCW
5 POT CT
6 POT CW
7 MODE
8 TRIAC GATE RETURN
16 AC IN
15 NC
14 NC
13 OVERRIDE
12 PHASE SENSE
11 COMPENSATION
10 NC
9 TRIAC GATE
50K
.1µF
3µF
5K,1W
200 pf 50V
120V/240V INDUCTION MOTOR
100K ½W
NOTE: TRIAC Connections Must Be Exactly as Shown
TRIAC GATE
MT2
MT1
0.1µF 600V
220Ω 1W

Figure 7.
Application Circuit for a 1½ HP Motor Which Showed Instability with the Basic Application Circuit.

SPECIALIZED APPLICATION FEATURES OF HV-1000

Tailoring the response curve:

Referring to Figure 2, the reader will remember that the HV-1000 controller line is a line sloping down to the right, by contrast with earlier generations of IMES, which had a horizonal (constant θ_C) characteristic. For specialized purposes, typically involving stability, the HV-1000 controller line can be made into a horizontal line if desired. This is done simply by not contacting Pin 7, the Mode pin. A consequence of this is that the load anticipator sensitivity then becomes independent of load. For historical reasons, this is called "single slope" operation. Operation with pins 7 and 5 strapped together is called "dual slope". In single slope operation, the controller loses its self-adaptive property.

Moving back the phase setting without increasing the anticipator sensitivity:

So far the only method of moving down the controller line (reducing θ_C) described has involved the use of a potentiometer which has the side effect of increasing the anticipator sensitivity. To reduce θ_C without affecting the anticipator, try placing a low voltage (5V) capacitor between pins 1 and 12. 0.05μF reduces θ_C about 0.5 msecs and shifts the anticipator trip point by the same amount in the same direction.

Over riding the control function:

There are certain circumstances in which it may be necessary or desirable to disable the control function completely, and simply feed the straight line voltage to the motor. This can be done using pin 13, which is a TTL logic input. It is activated by the application of +2.4V with respect to pin 1 and a current of 0.1mA. Doing this triggers the load anticipator. Figure 8 shows this feature being used with the 0.1mA being derived from the AC Input, Pin 16. This figure also shows pin 7 open to produce single slope operation. The diode shown between pins 13 and 1 is to prevent negative polarity voltages being applied to the TTL input, pin 13. (Not using this diode would result in degraded long term reliability.) In this illustration the positive voltage to trigger the logic input each cycle is being derived from the AC input power.

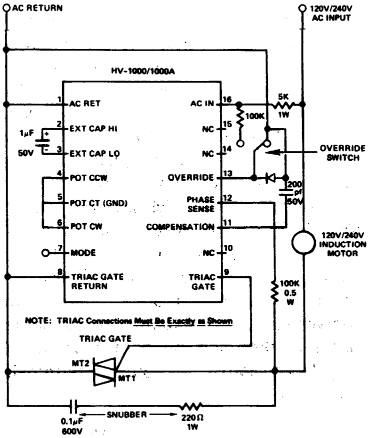

AC RETURN
120V/240V AC INPUT
HV-1000/1000A
1 AC RET
2 EXT CAP HI
3 EXT CAP LO
4 POT CCW
5 POT CT (GND)
6 POT CW
7 MODE
8 TRIAC GATE RETURN
16 AC IN
15 NC
14 NC
13 OVERRIDE
12 PHASE SENSE
11 COMPENSATION
10 NC
9 TRIAC GATE
1µF 50V
100K
5K 1W
OVERRIDE SWITCH
200 pf 50V
120V/240V INDUCTION MOTOR
100K 0.5 W
NOTE: TRIAC Connections Must Be Exactly as Shown
TRIAC GATE
MT2
MT1
0.1µF 600V
SNUBBER
220Ω 1W

Figure 8.
Application Circuit for the HV-1000 Illustrating Single Slope Operation and Electronic Override.

Circumstances in which the overide might be needed include when equipment other than the motor are connected to the motor and need momentary full voltage. Also it sometimes happens that TRIACs fail by turning into a diode in one direction. In this case, circuitry could detect the imbalance and apply a voltage to pin 13, turning the IMES full on most of the time, and preventing essentially direct current from being applied to an AC motor.

Full power starting:

As a generalization, the HV-1000 will start the motor with full power. When the system has been previously inactive, the time constant capacitor will be discharged corresponding to full power. Also for most motors, the transients associated with starting will usually trigger the load anticiapator, again producing a full power start. However, there are certain special circumstances where HV-1000 may not produce a full power start.

a) If a motor is driving a light load, so the time constant capacitor is fully charged, and switched off momentarily while a full load is applied; then, when the motor is switched on again, the HV-1000 may "soft start" for a fraction of a second. This tendency can be minimized by using a larger time constant capacitor and by increasing the load anticipator sensitivity with an external potentiometer or resistor. If the behavior is frequent and totally unacceptable, a complete fix is to use the application circuit for electronic override shown in Figure 9. Here the 100kohm resistor which sends the line voltage to pin 13 is replaced by 0.01μF to the start capacitor of the motor. Thus all the time the starter winding is operating, the HV-1000 is commanded to full voltage, guaranteeing a full power start. Since the start capacitor terminals may be inside the motor, this circuit is best suited for motor manufacturers.

b) In some installations the presence of a switch between the HV-1000 and the motor may be unavoidable. When the switch is opened, the HV-1000 will slew to minimum output voltage. In most cases the transient associated with switch closure will trigger the load anticipator, but this can not be guaranteed. Sometimes a "soft start" may then occur. A fix for this circumstance is to place a 0.01μF linepower voltage capacitor across the motor and its switch. This "closes the loop" on the HV-1000 control system even when the switch is open. The result is that the HV-1000 will slew to full voltage, not minimum voltage, when the switch is open, guaranteeing a full power start. For example, in the context of an after-market add on controller, the 0.01μF is placed across the output terminals of the controller.

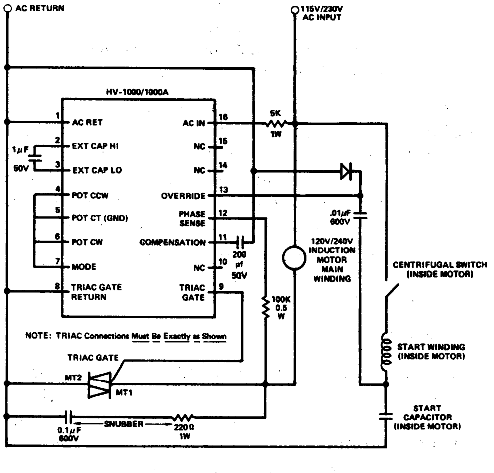

AC RETURN
115V/230V AC INPUT
HV-1000/1000A
1 AC RET
2 EXT CAP HI
3 EXT CAP LO
4 POT CCW
5 POT CT (GND)
6 POT CW
7 MODE
8 TRIAC GATE RETURN
16 AC IN
15 NC
14 NC
13 OVERRIDE
12 PHASE SENSE
11 COMPENSATION
10 NC
9 TRIAC GATE
1µF 50V
5K 1W
.01µF 600V
200 pf 50V
100K 0.5 W
120V/240V INDUCTION MOTOR MAIN WINDING
CENTRIFUGAL SWITCH (INSIDE MOTOR)
START WINDING (INSIDE MOTOR)
START CAPACITOR (INSIDE MOTOR)
NOTE: TRIAC Connections Must Be Exactly as Shown
TRIAC GATE
MT2
MT1
SNUBBER
0.1µF 600V
220Ω 1W

Figure 9.
Application Circuit Which Ensures Full Power Starting Under All Conditions.

MEASURING POWER SAVINGS

A relatively simple and inexpensive power meter can be obtained from the Robinaire Manufacturing Company of Montpelier, Ohio. For many times the price a sophisticated watt-volt-amp meter (Model 259 V.A.W. meter) is sold by Clarke Hess Communications Research Corporation of New York City. Used utility company kilowatt hour meters, rebuilt and recalibrated, can be obtained from the Hialeah Meter Company of Hialeah, Florida.

All of the above will give slightly differing results for power savings, because of the different ways in which they react to the high frequency components in a TRIAC chopped current.

SAFETY

The HV-1000 application circuits shown in the previous figures contain linepower voltages which can be lethal under certain conditions. In assembling and testing such circuits all precautions relevant to the safe handling of 120V and 240V AC should be observed.

In some instances, TRIACs have been known to fail through overheating in such a manner that they resemble a diode in one direction. If no other precautions are taken, an HV-1000 IMES circuit under this circumstance will end up supplying a large component of direct current to the motor, which will not be limited by the inductance of the windings. The motor may overheat, unless it is thermally protected, as are most motors made today. Alternatively, a sense circuit can be devised to detect the rectification and trigger the HV-1000 via the Override, Pin 13.

If the TRIAC fails in the off or open circuit state, the HV-1000 will be destroyed immediately, since it is not designed to carry significant amounts of line current.

HANDLING PRECAUTIONS AND RELIABILITY

Although the HV-1000 can survive multi-kilovolt surges in its application circuit, the chip by itself is sensitive to electrostatic discharge, and precautions should be taked, and handling, to prevent accidental "zapping" of the dual in-line package.

If the HV-1000 is inadvertently inserted backwards into its socket, the chip is not damaged. Usually, the motor will be observed to run without any control. Normal operation will resume when the package is rotated.

Because of the relatively high voltages (including multi kilovolt lightning surges) to be found on the HV-1000 circuit, it is recommended for best reliability, that if a printed circuit board is used, the conductors having large potential differences should be widely spaced. Coating the whole assembly with resin or varnish will usually improve the reliability achieved.

ACKNOWLEDGEMENTS

The authors wish to acknowledge several helpful conversations with Frank J. Nola of the NASA Marshall Space Flight Center. The development of the HV-1000 was aided by the donation of a motor collection by Reliance Electric, Leeson Electric, Gould Electric, Bodine Motors and Emerson Electric. Illuminating comments from the engineering staff of Doerr Electric and the G.E. General Purpose Motor Division were invaluable.

BIBLIOGRAPHY

The following selected readings may be of interest to those wishing to further pursue the study of single phase induction motor energy savers.

1. NASA Technical Brief MFS 23280. Summer 1977. "Save Power in AC Induction Motors".
2. U.S. Patent 4052648. "Power Factor Control System for AC Induction Motors". F.J. Nola.
3. NASA Technical Brief MFS 23988. Spring 1979. "Fast Response Power Saver for Induction Motors".
4. NASA Technical Brief MFS 25323. Summer 1980. "Improved Power Factor Controller".
5. "Circuit Saves Power in AC Induction Motors". F.J. Nola, EDN, P185, September 5, 1979.
6. "Improvement in Energy Efficiency of Induction Motors by Means of Voltage Control". N. Mohan. IEEE Trans. on Power Apparatus and Systems. Vol PAS-99, No. 4, July/Aug 1980. P1466.
7. "Energy Efficiency of Electric Motors". A Report Prepared for the U.S. Department of Energy. Report No. HCP/M50217-01 reprinted April 1978.
8. "Load Responsive Motor Controller". NASA Tech Briefs. Spring 1981. Vol. 6, No. 1, MFS-25560.
9. "The Case for the Power Factor Sensing Motor Controller". M.L. Cohen. Proceedings of the Second International MOTORCON Conference, March 29, 1982. P 621. Published by Intertec Communications, Oxnard, California.
10. "Energy-Efficient Electric Motors". A book by J.C. Andreas, Published by Marcel Dekler Inc., of New York, 1982.

APP NOTE

FOR YOUR INFORMATION

No. 543

Harris Analog

NEW HIGH SPEED SWITCH OFFERS SUB-50ns SWITCHING TIMES

By Carl Wolfe

INTRODUCTION

An ideal CMOS analog switch would exhibit such characteristics as zero resistance when turned on, infinite resistance when turned off, zero power consumption, and zero switching time. Unfortunately, such a device is usually found as an example in a college textbook. The real world offers tradeoffs and imperfections which prevent the realization of the ideal. The integrated circuit designer works within these limits and attempts to optimize device performance by utilizing new technologies and improving circuit design. The development of a new high speed analog switch required the use of both of these techniques to achieve its performance. (See Appendix I: "Inside the HI-201HS").

The HARRIS HI-201HS is the industry's first sub-50ns monolithic analog switch and along with fast switching speed, offers improved performance and pin compatibility with industry standard 201's (Fig. 1). This article will discuss the technology, performance, and applications for this product.

IMPROVE THOSE EXISTING DESIGNS

The application circuits which follow are examples of typical applications and illustrate how the HI-201HS can improve existing applications where standard 201's are presently being used.

The first example is a high speed multiplexer shown in Fig. 2. The analog multiplexer is a circuit which switches a number of analog inputs to a single output and is used heavily in data conversion and avionic applications. This function can be easily achieved with the HI-201HS by tieing the outputs together and selecting the appropriate analog input. The HI-201HS is an excellent choice for this application since its low on resistance and leakage current will reduce system error, and its high speed is unmatched by any other monolithic analog switch. Since the output capacitance is additive, the RC time constant of the load will increase when the outputs are made common.

The next application is a high speed sample and hold which takes advantage of the improved performance of the HI-201HS and the precision F.E.T. input of the HA-5160 high slew rate amplifier. A sample and hold circuit or track and hold as it is sometimes called, has two operating modes. In one mode the switch is closed and the capacitor charges to the input voltage. The second mode occurs when the switch is opened and the capacitor holds this charge for a specified period of time.

The speed of a sample and hold circuit is directly related to the switching device used and the output amplifier. This characteristic of a sample and hold circuit is called the acquisition time. It is defined as the time required following a "sample" command, for the output to reach its final value. The acquisition time includes the switch delay time, the time constant of the switch on resistance and hold capacitor ($T = R_{ON} C_{HOLD}$), and the slew and settling times of the output amplifier.

The photographs shown in Fig. 3 illustrate the improvement in the acquisition time possible by using the HI-201HS. The first photograph represents the sample/hold circuit using a standard 201 switch and an HA-5100 operational amplifier. The first waveform is the "Sample" voltage (V_A). The second waveform is the voltage on the hold capacitor (V_1). And the third waveform is the output of the amplifier (V_2).

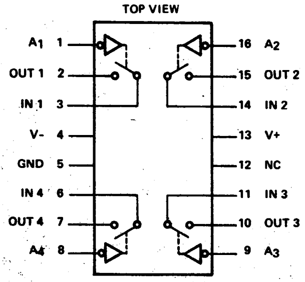
The second photograph is the same circuit with a HI-201HS and on HA-5160 op amp. Comparison of the photographs shows the HI-201HS has significantly reduced the switch delay time and the high slew rate of the 5160 amplifier has also contributed to the reduced acquisition time.

A source of error in this circuit is a d. c. offset which is called sample to hold offset error. This error is primarily due to the charge injection (Q) of the switch and is related to the hold capacitance by the following expression,

$$\text{offset error } (V_O) = \frac{\text{charge transfer } (Q).}{C_H}$$

The reduced charge injection of the HI-201HS (typically 10 pc) will result in immediate reduction of this error.

Using analog switches with operational amplifiers is common in circuit design. An example is shown in Figure 4 which is an integrator with start/reset capability.

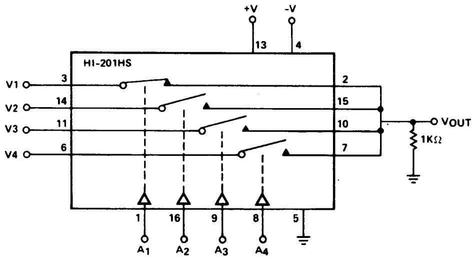

TOP VIEW
A1 1
OUT 1 2
IN 1 3
V- 4
GND 5
IN 4 6
OUT 4 7
A4 8
16 A2
15 OUT 2
14 IN 2
13 V+
12 NC
11 IN 3
10 OUT 3
9 A3

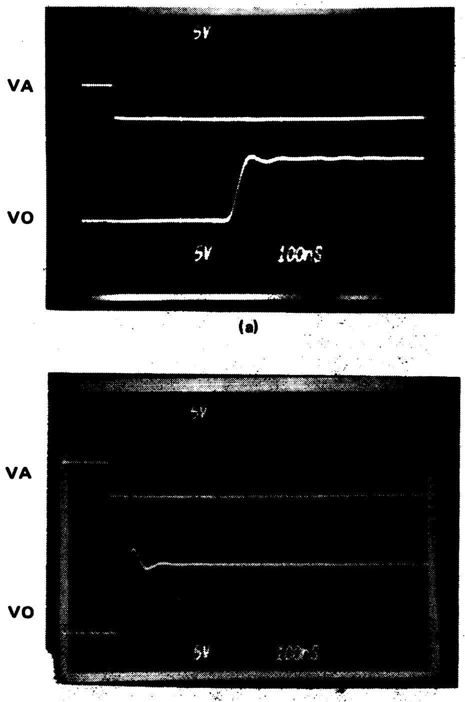
LOGIC	SWITCH
0 - $V_{AL} \leq .8V$	ON
1 - $V_{AH} \geq 2.4V$	OFF

TYPICAL SPECIFICATIONS (±15V Supply)

Analog Signal Range	±15V
On Resistance	30Ω
Off Leakage	.3nA
Switch On Time	30ns
Power Dissipation	120mW

Figure 1. Typical Pinout and Specifications – The HI-201HS is pin compatible with standard 201's and offers improved performance. Specifications given are typical values at T_A = 25°C.


+V
-V
13
4
HI-201HS
V1
3
V2
14
V3
11
V4
6
2
15
10
7
VOUT
1KΩ
1
16
9
8
5
A1
A2
A3
A4



(a)

(b)

Figure 2. High Speed Analog Multiplexer: (a) circuit response using the standard 201 (T_{access} = 400ns) (b) circuit response using HI-201HS (t_{access} = 50ns). The access time is defined as total time required to activate an "off" switch to the "on" state. Access time is normally measured from the initiation of the digital input pulse (V_A) to the 90% point of the output transition.

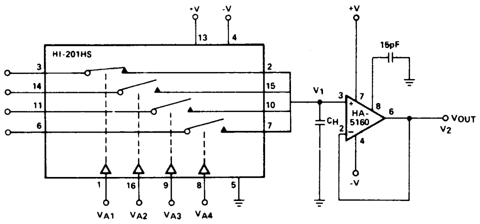

+V
-V
13
4
HI-201HS
3
14
11
6
2
15
10
7
1
16
9
8
5
VA1
VA2
VA3
VA4
+V
V1
CH
15pF
HA-5160
VOUT
V2
-V

Figure 3A. High Speed Sample and Hold: The basic sample and hold samples the input voltage when the switch is closed and the capacitor holds the voltage when the switch is open. The speed of the switching element affects the speed of the sample and hold.

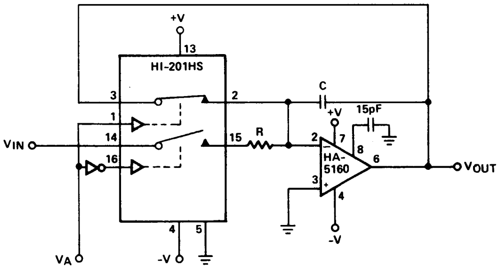

+V
13
HI-201HS
3
2
1
14
15
16
4
5
C
+V
15pF
R
HA-5160
7
8
6
VIN
VOUT
VA
-V
-V

Figure 4A. Integrator with Start/Reset: A low logic input pulse disconnects the integrator from the analog input and discharges the capacitor. When the logic input changes to a high state, integrator is activated.

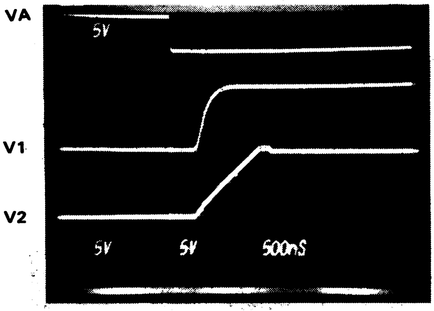


Figure 3B. Circuit response to a "Sample" command using a standard 201 and an HA-5100 operational amplifier (Acquisition time = 1.5μs)

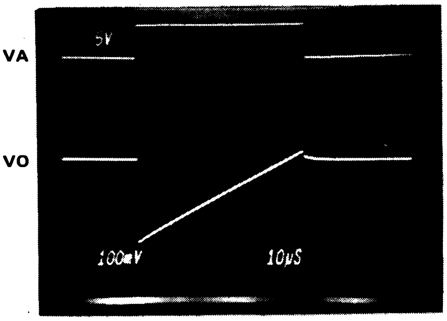


Figure 4B. Low Level Integration— Circuit response using standard 201 switch.

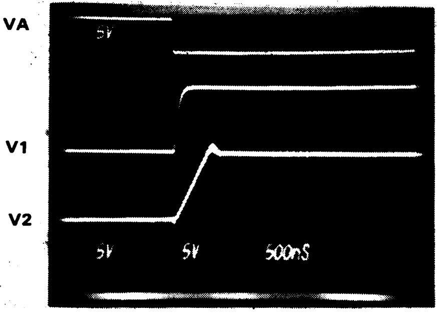


Figure 3C. Circuit response using an HI-201HS and HA-5160: HI-201HS significantly reduces switch delay time. (Acquisition time = 500ns)

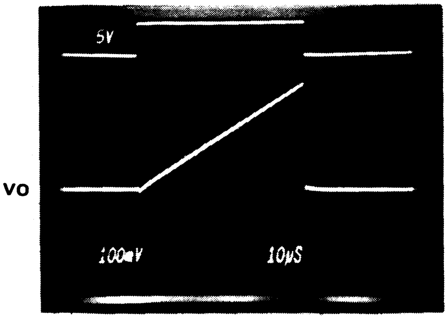


Figure 4C. Low level integration—Circuit response illustrates improved charge injection of the HI-201HS.

The switch is used to apply the input signal and to reset the integrator. Applying a low logic level removes the input signal and the capacitor is discharged. When a logic level high is present, the input signal is integrated with a rate of change equal to

$$dv_o/dt = \frac{i_f}{C_f} = \frac{-V_i}{R_1C_f}$$

The reduced on resistance, leakage current, and charge injection of the HI-201HS will improve the performance of this circuit and an example of this improved peformance can be seen in the photographs in Figure 4. These photographs illustrate the reduced charge injection which the 201HS offers. The component values are R_1 = 1MΩ , C = 150pF and V_{IN} = -1V. With these values, the amplifier will integrate the input signal with a slope of 6.6mv/μ s. For a 50 μs time period, the amplifier will integrate to a magnitude of ≈ 300mV. The photographs of the test results indicate this to be true, but it should be apparent that the two photographs are quite different. The first photograph represents the amplifier output using a standard 201 as the reset switch. The second photograph is the same circuit with a 201HS.

The offset error in the first photograph is due to the charge injection of the switch. Using the expression Q = V x C and knowing the standard 201 has a typical charge transfer of 30pc, this offset can be calculated. V = Q/C = 30pc/150pf=200mV.

Other examples of combining switches and amplifiers are shown in figures 5 and 6. In both these applications the switch is used to tailor the amplifiers performance. Figure 5 is a low pass filter with a selectable break frequency.

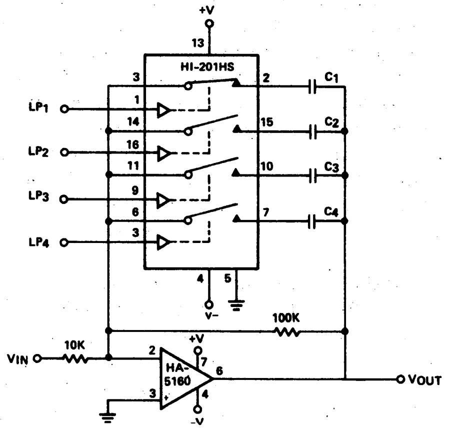


Figure 5. Low Pass Filter with Selectable Break Frequency— Switch selection places various values of capacitance in parallel with the feedback resistor. The value of the capacitor determines the break frequency. The break frequency is that frequency at which the signal begins attenuation.

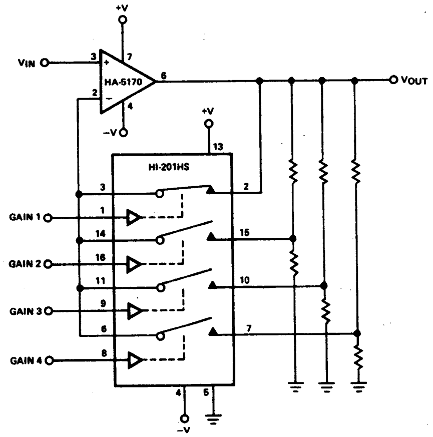


Figure 6. Amplifier with Programmable Gain— Switch selection activates a new voltage gain which is determined by the resistive feedback.

Depending on which switch is selected, a particular cutoff frequency is introduced by the expression,

$$F_C = \frac{1}{2\pi R\, C_X}$$

A programmable gain amplifier is shown in Figure 6. Similar in function to the filter application, the gain of the amplifier is determined by selection of a switch.

When using switches with other components it is important that a switch be selected which introduces a minimal amount of error to the circuit. Operational amplifier gain error due to high on resistance or offset voltages due to excessive leakage current and charge injection are examples of potential error created by the switch. The previous applications have demonstrated that the 201HS offers improved performance by minimizing circuit error and increasing system speed.

ON THE DRAWING BOARD

Since the introduction of the HI-201HS switch, many engineers have expressed an interest in using this new product. Although much of their work is in a preliminary stage and they do not want to divulge exact details on their designs, the following information is intended to give you an idea of how other engineers are considering using the HI-201HS.

The majority of the engineers are interested in taking advantage of the products fast switching speed. One particular engineering group is investigating replacement of DMOS (double-diffused MOS) transistors with the HI-201HS.

The DMOS transistor is capable of extremely fast switching speeds (1ns) and until now, switches fabricated using CMOS technology have not been fast enough to be considered. But the HI-201HS is attractive since it offers unprecedented switching speed along with the established benefits of CMOS technology. Such benefits include a wider analog signal range capability and lower operating power requirements.

A common application for analog switches is time division multiplexing, where many signals are processed on a single channel. High speed switching allows higher information capacity on the channel, since the switching speeds of an analog switch are directly related to the maximum switch activation frequency. The faster a switch can turn on and off, the higher the possible switching frequency. An example of this relationship is shown in Figure 7. If a switch is activated at a frequency of 1MHz, it must turn on and off within a 500ns time period. Since the HI-201HS has a maximum on and off times of 50ns, and can turn on and off within a 100ns time period, it theoretically possible that it can be activated at a 5MHz frequency rate. This improved capability is making the HI-201HS an attractive component to design engineers requiring high frequency data processing. Conversations with engineers indicates that possible applications are computer graphics and visual display circuit designs.

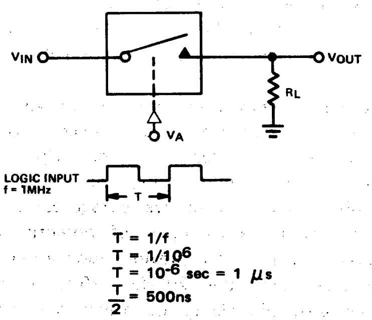


Figure 7. High Frequency Switching – HI-201HS fast switching times allow it to transfer data at a higher rate of frequency.

Another area where the HI-201HS is generating interest is in the area of medical electronics. This is a growing field and improvements are continously being made as products become available much of the medical equipment being designed requires both high speed and accuracy.

Medical test equipment is primarily used to transmit or receive information from the patient. An example where both these functions are used is in the area of ultrasound. Ultrasound testing requires that a signal be transmitted to the patient and the return signal is then amplified and displayed or recorded. The 201HS is being considered for the use in such an application and would be used to control the transmission and reception of these signals.

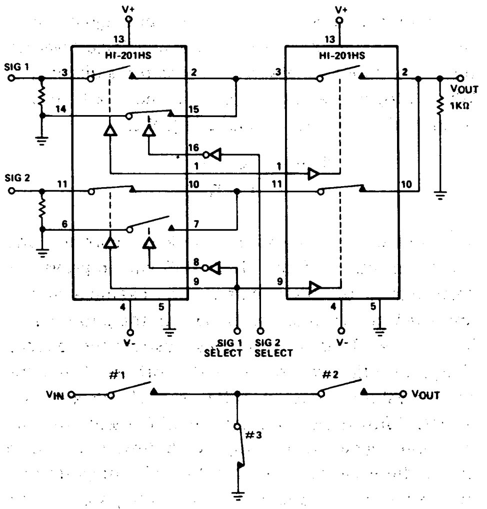


Figure 8. Video Switching with Improved Isolation—Improved high frequency off state performance is obtained by using a T-Switch configuration. When two series switches are off, the third switch is shorted to ground.

The designers are not only interested in fast switching speed, but also in low on resistance. This is an important aspect of the switch since many of the electrical signals in medical electronics are of a small magnitude. An example is patient monitoring equipment which converts physiological parameters into electrical signals. If these low level electrical signals require switching before amplification, a low on resistance switch is essential to minimize the voltage drop across the switch itself. The low on resistance of the HI-201HS enables it to be used in applications using signals of smaller magnitude.

Video circuit design involves the control of high frequency signals. Applications which require the switching of these high frequency signals are usually limited by the off isolation and crosstalk performance of the switch. Off isolation is defined as the amount of feedthrough of an applied signal through an off switch. Crosstalk is the amount of cross coupling of an "off" channel to the output of an "on" channel. Both of these switch characteristics will degrade as the frequency of the input signal increases.

The HI-201HS has some improvement over the standard 201 in these areas but the configuration shown in Figure 8 is being used by designers to improve the isolation capabilities of CMOS analog switches. This configuration is known as "T" switching since the three switches used for passing the signal could be thought of in the shape of the letter T. The simplified figure shows that when switches # 1 and # 2 are off, switch # 3 is tied to ground. When switches # 1 and # 2 are on, # 3 is off. This improves isolation by having two channels in series off and any feedthrough is fed to ground.

CONCLUSION

The HARRIS HI-201HS is the fastest monolithic CMOS analog switch available. It offers improved performance for existing designs and should be considered for use in any application where switching speed is an important criteria.

ACKNOWLEDGEMENTS

The author would like to thank Gary Maulding, Frank Cooper, and Bob Junkins for their technical assistance, Ken Timko and Dick Whitehead for their editorial comments, and the dynamic duo of Lilly Andrews and Kathy Glines for their secretarial skills and patience in the preparation of this paper.

REFERENCES

1. D. F. Stout, "Handbook of Operational Amplifier Circuit Design". New York: McGraw-Hill, 1976.
2. J. G. Graeme, G.E. Tobey, and L. P. Huelsman, "Operational Amplifiers: Design and Applications". New York: McGraw Hill, 1971.
3. J. A. Connelly, "Analog Integrated Circuits" New York: John Wiley & Sons, 1975.
4. HA-2420/2425 Fast Sample and Hold data sheet, Harris Semiconductor.

APPENDIX I - INSIDE THE HI-201HS

The HI-201 is a TTL compatible quad CMOS analog switch which features switching times under 50ns and a typical "on" resistance of 35Ω. The fast switching times are achieved through a combination of process and circuit design techniques. The HI-201HS is fabricated using a dielectric isolation process with complementary PNP and NPN bipolar transistors and polysilicon-gate CMOS. The use of bi-technology process enabled a unique circuit called a D. C. Static Level Shifter to be designed.

The typical CMOS analog switch consists of a switch cell which is driven by a level shifter. The level shifter converts a single logic input into two complementary outputs which drive the gates of the CMOS switch cell (Fig. A). The switch cell represents a capacitive load to the level shifter, so fast switching times require large drive currents to charge these capacitances quickly. The D. C. Static level shifter circuit (Fig. B) provides large drive currents only when switching and dissipates little power in a quiescent condition.

The D. C. static level shifter achieves high switching speeds through the use of a unique bipolar input stage and a network of switching and holding MOS transistors. Devices MN5, MP5, MN9 MP9 are the switching transistors and MN6, MP6, MN10, MP10 are the holding transistors. The major advantage of the bipolar input transistors is that its transconductance (g_m) is much higher than that possible with F. E. T. transistors.

To understand the level shifter operation, consider a change of logic input from low state to high. Initially V_A is low, $Q = Q_1 = Q' = -15V$ and $\bar{Q} = \bar{Q}_1 = \bar{Q}' = 15V$. VB is at ground and QN2, QP2 are off. When V_A goes high, QN2, QP2 turn on, which slew the gates of switching devices MN5, MP5 with a current $I = (V_A - 2V_{BE})/R$. The switching devices overcome the holding devices, MN10, MP10 and switch the internal nodes Q_1, and $\bar{Q}_1$. CMOS buffers I_{11}, I_{13} provide large drive currents to the switch cell, while inverters I_{12}, I_{14} provide delayed feedback signals. The feedback signals turn off holding devices MN10, MP10 while turning on holding devices MN6, MP6. The feedback also turns on QN2, QP2 by means of MN1, MP1. These feedback signals have returned the level shifter to a static condition by turning the bipolar input stage and MOS switching transistors off.

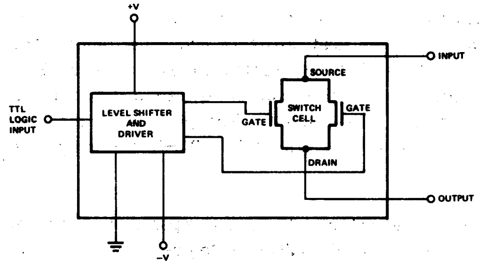


Figure A. Simplified I. C. Analog Switch Operation— Level Shifter converts logic input into drive signal for CMOS switch cell.

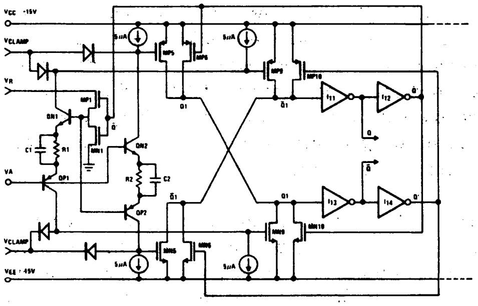


Figure B. Simplified D. C. Static Level Shifter – The level shifter consists of a unique bipolar input stage and a network of switching and holding devices.

Similar operation occurs when V_A goes from high to low, bipolar transistors QN1, QP1 turn on MN9, MP9. The feedback resets the holding devices and turns off the bipolar input stage.

APPENDIX II HI-201HS VS. STANDARD 201

The use of a dual technology process and a creative design improves the performance of this analog switch. The following table illustrates the results of this combination by comparing the specification of the HI-201HS with the standard 201.

It should be apparent from Table 1 the substantial improvement in switching speeds offered by the HI-201HS. But since the switch "off" time of the high speed switch is measured differently from the standard 201, a brief discussion of test methods will avoid any confusion.

Figure A is a typical switching time test circuit for an analog switch. The "on" time is measured from the logic input to the 90% point of the output.

The "off" time can be measured from the logic input to either the 90% or 10% point of the output. This variation in the "off" time test point is due to the dependence of the measurement on the load. The dominant component of the switch "off" time is an exponential RC time constant determined by the values of the load resistance and capacitance. The "off" time of the HI-201HS is measured to the 90% point. The RC time constant due to load is excluded from this measurement. The photograph included in Figure A is a typical HI-201HS switching time response.

The remainder of table one compares other critical specifications of CMOS analog switches. The HI-201HS is not only a high speed switch but also offers improved performance in other areas. The parameters of "on" resistance, leakage current, and charge injection can all contribute unwanted errors to system level applications. With the improvements shown in these areas, the HI-201HS offers potential improvement in system accuracy for a wide variety of applications. and since the HI-201HS is pin compatible with existing 201's, the high speed version can be plugged into existing designs for immediate improvement in performance.

The HI-201HS is an improvement over the standard 201 in many areas, but some trade-offs still exist. One such trade-off was the power dissipation of the product. In order to meet the high speed criteria, larger internal currents are needed which in turn demand increased supply current. But this apparent shortcoming is more than offset by the products performance.

Parameter	Temperature	HARRIS HI-201HS	HARRIS HI-201
Switching Speed			
t_{ON}	25°	50ns	500ns
t_{OFF}	25°	50ns	500ns
ON Resistance	125°	75Ω	125Ω
Leakage Current			
I_{SOFF}	125°	100nA	500nA
I_{DOFF}	125°	100nA	500nA
Charge Injection Q	25°	10pc (typ)	30pc (typ)
Power Dissipation Pd	125°	240mw	60mw

Table 1. Specification Comparison: Improved performance of HI-201HS over standard 201's (all values are maximums unless stated otherwise).

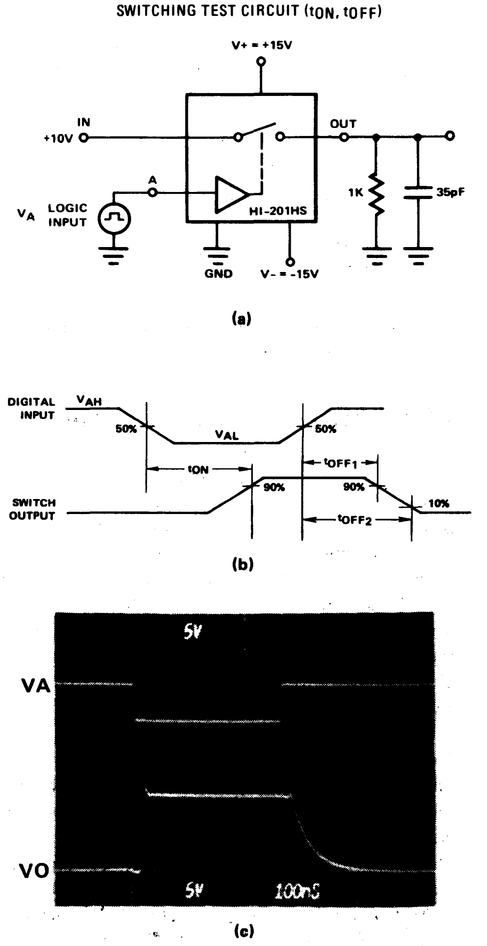


Figure A. **Switching Time Test Circuit: (a) Switching test circuit, (b) Switching waveforms, (c) Typical HI-201HS response.**

APP NOTE

FOR YOUR INFORMATION

No. 544

Harris Analog

MICROPOWER OP AMP FAMILY

Russell Leath and Richard Whitehead

Introduction

Offering the best speed power product of any low power operational amplifier available, the HA-5141/42/44 can be effectively utilized in a wide variety of portable system applications. The features available from this family of devices can be easily incorporated into dictation equipment, medical monitoring systems, remote electronic sensors and other system designs.

Low or Micropower?

Actually, the HA-5141/42/44 operational amplifiers are micropower devices. That is, they consume microwatts of power (250µW typ.) as opposed to low power devices which consume 1 to 10mW. This exceptionally low power consumption however does not compromise the speed and flexibility of this family of amplifiers. Table 1 lists the speed/power relationships of the HA-5141 and other amplifiers in its class. The industry standard 741 was listed to show that HA-5141 has more speed for a fraction of the power consumed. A brief discussion concerning how the HA-5141/42/44 achieves this unique relationship can be found in the inset below.

Part Number	Power Dissipation	Slew Rate	Full Power Bandwidth	Gain Bandwidth
HA-5141	250µW	1.5V/µs	60KHz	400KHz
RC4132	250µW	.13V/µs	5.5KHz	150KHz
OP-20	275µW,	.02V/µs	.9KHz	100KHz
LM1OC	2000µW	.11V/µs	5.5KHz	80KHz
LM741	8000µW	.7/Vµs	20KHz	1500KHz

TABLE 1. SPEED/POWER RELATIONSHIPS

For highest speed for power consumed, HA-5141 is a factor of 10 better than the nearest device.

Dual or Single Supply

Enhancing the micropower consumption and speed capabilities of the HA-5141/42/44 is its ability to operate over a wide range of supplies. It can be operated in double supply mode from ±15V down to ±1.5V or in single mode from +30V down to +3V. The quiescent supply current (60µA/amp.) remains nearly constant over the entire supply range making it most suitable for operation in battery powered systems.

Making the Most of Micro Amps

To achieve high slew rate while requiring only 60µA to operate, the HA-5141/42/44 design utilizes a current amplifying front end. As can be seen in the simplified schematic under zero signal conditions, current source I_1 flows through D_1 and P_1 while I_1 flows through D_2 and P_2. This flow sets up a DC bias current of I_1 and I_2 through N_1 and N_2.

Under small signal conditons, the cross coupling of N_1 to P_1 and N_2 to P_1 establishes small signal currents i, and i_2 through collectors of N_1 to P_2 and N_2 and P_1 respectively. This differential current (i_1-i_2) is similar to a standard differential pair and is given by;

$$i_1 - i_2 = gm \text{ where } gm = f\ (hib)$$

However, under large signal inputs and unlike the standard differential pair, the maximum differential current is not limited by the DC biasing current sources. The maximum slewing current is limited only by the β of N_1 and is orders of magnitude larger than the DC biasing current.

For a standard differential pair under large signal conditions the differential current is given by;

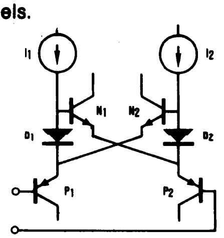
$$i_1 - i_2 = I_1 \tanh$$

$$\text{and } i_1 - i_{2max} = 2I_1$$

But for the HA-5141/42/44 the large signal differential current is;

$$i_1 - i_2 = I_1(e^{/vt} - e^{-v/vt})$$

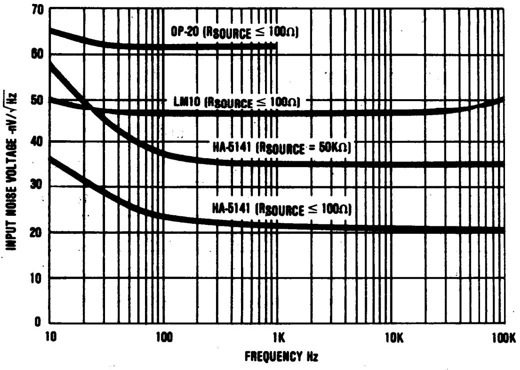
and i_1-i_2 increases exponentially until limited by β_{Ni}. The HA-5141/42/44 design utilizes two gain stages which allows for high DC gain at lower collector impedance levels. These lower impedance levels permit unstacked device design which allows for lower operating voltage levels.



HA-5141/2/44 CURRENT AMPLIFYING FRONT END

Noise Parameters Also Attractive

With rugged bipolar construction combined with the dielectric isolation technology, the HA-5141/42/44 design maintains noise characteristics comparable to amplifiers requiring much higher supply currents. The noise curves compare the HA-5141 with other amplifiers in its class. It is readily observed that the HA-5141 has lower noise components even with higher source impedances. With typical noise values of $23nV/\sqrt{Hz}$ and $.03pA/\sqrt{Hz}$ at 1KHz this device family is very "user friendly" to the portable system designer.



NOISE CURVES COMPARING HA-5141 WITH OTHER AMPLIFIERS

Other Useful Qualities

When operated in single supply mode this family of amplifiers is capable of output voltage swings from 0V to V(+) -1 Volt while sourcing 3mA output current. Their common range under single supply conditions is 0V to V(+) -1V. These qualities coupled with 60KHz full power bandwidth and 0.4MHz small signal bandwidth further widens the application range of the HA-5141/42/44.

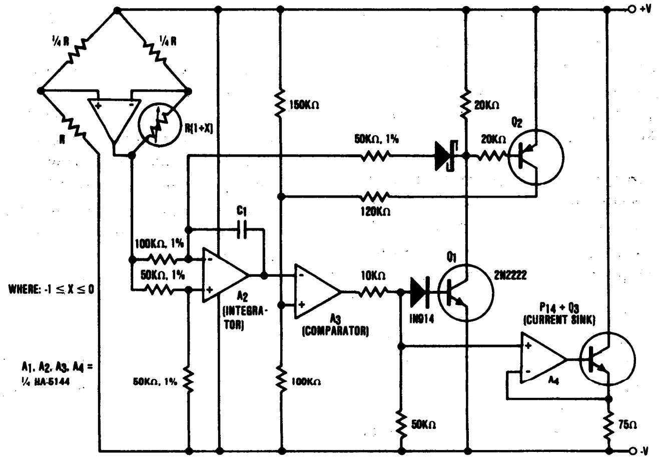
Applications

The flexibility and inherent qualities of the HA-5141/42/44 are most suitable for battery operated and/or low voltage systems such as remote electronic sensors or solar operated designs. The following applications are just a few of the many possibilities which can best utilize this amplifier's capabilities.

Application 1—Remote
Sensor Loop Transmitter

This circuit shows amplifier A_1 as a sensor amplifier in a bridge configuration. Amplifiers A_2 and A_3 are configured as a voltage to frequency converter and A_4 is used as the transmitter. This entire sensor/transmitter can be powered directly from a 4 to 20mA current loop.

The bridge configuration produces a linear output with respect to the changes in resistance of the sensor. The voltage at the output of A_1 causes the integrator output A_2 to ramp down until it crosses the comparator threshold voltage of A_3. A_3 turns on Q_1 and Q_2. Q_1 causes the output of A_2 to ramp up at a rate nearly equal to its negative slope while Q_2 provides hysteresis for the comparator. In addition, Q_1 and Q_2 help eliminate changes in power supply (loop) voltage. Amplifier A_4 and Q_3 are configured as a constant current sink which turns on when the comparator goes "high". The resulting increase in loop current transmits the frequency of the V to F converter back to the control circuitry.



REMOTE SENSOR — CURRENT LOOP TRANSMITTER

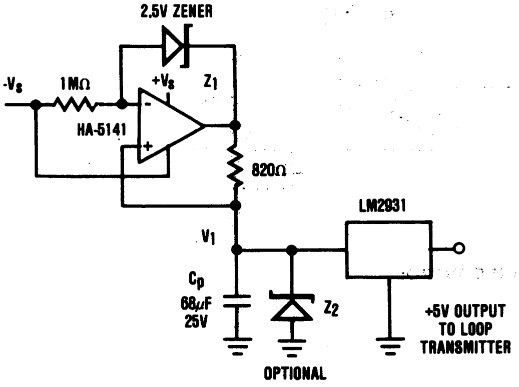
Application 2—Charge Pool Power Supply

It is usually desirable to have the remote transmitter of a 4 to 20mA current loop system powered directly from the transmission line. In some cases this is not possible due to high power requirements set by the remote sensor/transmitter system. In these cases an alternative to the seperate power supply is still possible. If the remote transmitter can be operated in a pulsed mode where it is active only long enough to perform its function, then a charge pool power supply can still allow the transmitter to be powered directly by the current loop. In this circuit a constant current I_1 is supplied to the charge pool capacitor (CP) by the HA-5141 (where $I_1 = 3mA$). The voltage V_1 continues to rise until the output of the HA-5141 approaches +Vs or the optional voltage limiting provides by Z_2. The LM2931 voltage requlator supplies the transmitter with a stable +5V supply from the charge collected by CP. Available power supply current is determined by the duration, allowable voltage droop on Cp, and required repetition rate. Example: If V_1 is allowed to droop 4.4V and the duration of operation is 1msec, the available power supply current is approximately $I_{ps} = C_p \frac{dV1}{dt} = 68\mu F \cdot \frac{4.4V}{1msec} = 30mA$.

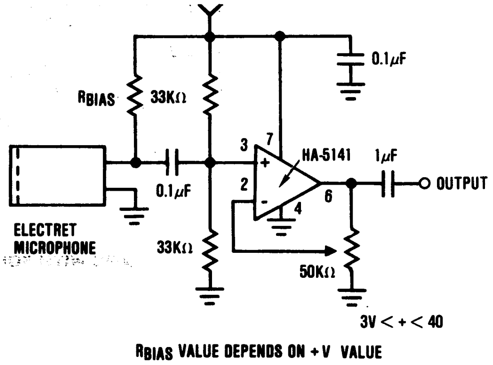
The repetition rate of operation is determined by the time required for the 3mA constant current source to restore V_1 to its previous value. In this example: $t = 68\mu F \cdot \frac{4.4V}{3mA} = 100msec$ is required.

Application 3—Low Power Microphone Amplifier

The HA-514X op amp is very well suited for use in audio applications which require high gain, bandwidth and speed at low voltages and with low power comsumption. Requirements such as these are usually found in battery, telephone line or solar powered circuits. The circuit below shows how the HA-5141 may be used to amplify the audio signal from an Electret microphone. This circuit may be operated with a single power supply voltage as low as 3V or as high as 40V and can provide over 25dB of gain over the audio frequency range. The 1V/μsec slew rate and low noise of the HA-5141 provides low distortion operation while only consuming about 60μA of supply current.



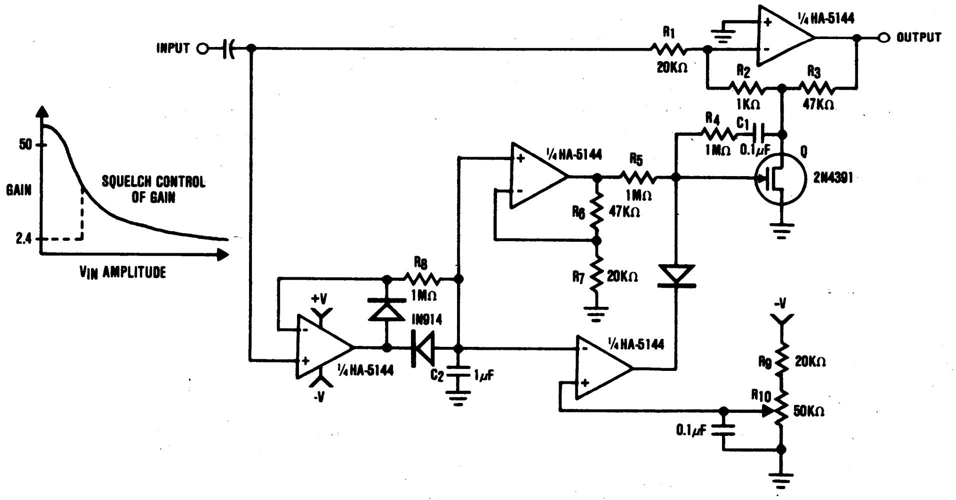
CHARGE POOL POWER SUPPLY FOR PULSED LOAD 4-20mA LOOP TRANSMITTER



LOW POWER MICROPHONE AMPLIFIER

Application 4—AGC with Squelch Control

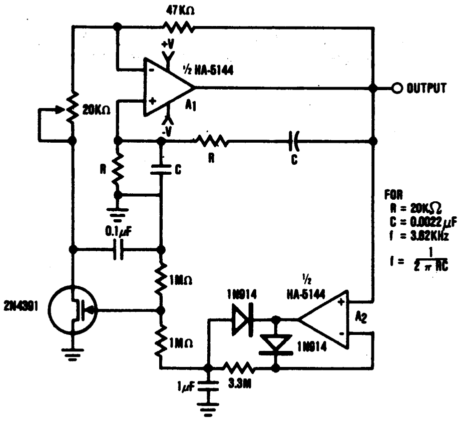
Automatic gain control is a very useful feature in a number of audio amplifier circuits such as tape recorders, telephone speaker phones, communication systems and P.A. systems. The circuits shown below consists of a HA-5144 quad op amp and a FET transistor used as a voltage controlled resistor to implement an A.G.C. circuit with squelch control. The squelch function helps eliminate noise in communications systems when no signal is present and allows remote hands free operation of tape recorder systems. Amplifier A_1 is placed in an inverting gain T configuration in order to provide a fairly wide gain range and to keep the signal level across the FET small. The small signal level across the FET and the addition of resistors R_5 and R_6 help reduce nonlinearities and distortion. Amplifier A_2 acts as a negative peak detector to keep track of signal amplitude. Amplifier A_3 may be used to amplify this peak signal if the cutoff voltage of the FET is higher than desired. Amplifier A_4 acts as a comparator in the squelch control section of the circuit. When the signal level falls below the voltage set by R10 the gate of the FET is pulled low turning it off completely and reducing the gain to 2.4. The output A_4 may also be used as a control signal in applications such as a hands free tape recorder system.


INPUT
R1
20KΩ
¼ HA-5144
OUTPUT
R2
1KΩ
R3
47KΩ
R4
1MΩ
C1
0.1μF
Q
2N4391
¼ HA-5144
R5
1MΩ
R6
47KΩ
R7
20KΩ
R8
1MΩ
1N914
+V
-V
¼ HA-5144
C2
1μF
¼ HA-5144
-V
R9
20KΩ
R10
50KΩ
0.1μF
50
GAIN
2.4
SQUELCH CONTROL OF GAIN
VIN AMPLITUDE

AGC WITH SQUELCH CONTROL

Application 5—Low Voltage Wein Bridge Oscillator

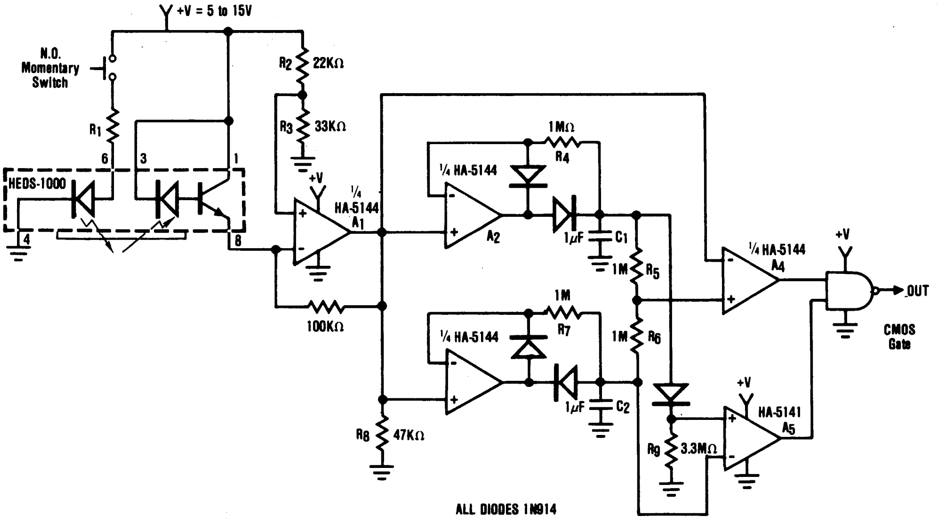
The circuit shown to the right utilizes a HA-5142 dual op amp and FET to produce a low voltage, low power Wein bridge sine wave oscillator. Resistors R and capacitors C control the frequency of oscillation while the FET, used as a voltage controlled resistor, maintains the gain of A_1 at exactly 3 to sustain oscillation. The 20K pot may be used to vary the signal amplitude. The HA-5142 has the capability to operate down to ±1.5V supplies and this circuit will produce a low distortion sine wave output while drawing only 120μA of supply current.


47KΩ
+V
½ HA-5144
OUTPUT
20KΩ
A1
-V
R
C
R
C
FOR
R = 20KΩ
C = 0.0022μF
f = 3.62KHz
f = 1/2πRC
0.1μF
1MΩ
1N914
½ HA-5144
A2
2N4391
1MΩ
1N914
1μF
3.3M

LOW VOLTAGE WEIN BRIDGE OSCILLATOR

Application 6—Bar Code Scanner

The circuit shown below illustrates a method of interfacing a HEDS-1000 emitter-detector pair with a HA-5144 for use as a bar code scanner circuit. The HA-5144 is used as an amplifier system which converts the bar and space widths of the printed bar code into a pulse width modulated digital signal. Amplifier A_1 is used to amplify the current output of the detector. The output of A_1 is passed to two precision peak detector circuits which detect the positive and negative peaks of the received signal. Amplifier A_4 is used as a comparator whose reference is maintained at the midpoint of the peak to peak signal by resistors R_5 and R_6. This provides a more accurate edge detection and less ambiguity in bar width. Amplifier A_5 is used as an optional noise gate which only allows data to pass through the gate when the peak to peak modulation signal is larger than 1 diode drop. This circuit is operated by a single supply voltage with low power consumption which makes it ideal for battery operated data entry systems.


+V = 5 to 15V
N.O. Momentary Switch
R1
R2 22KΩ
R3 33KΩ
HEDS-1000
6
3
1
4
8
+V
¼ HA-5144 A1
100KΩ
R8 47KΩ
1MΩ R4
¼ HA-5144
A2
1µF C1
1M R5
1M R7
¼ HA-5144
1M R6
1µF C2
¼ HA-5144 A4
+V
OUT
CMOS Gate
+V
HA-5141 A5
R9 3.3MΩ
ALL DIODES 1N914

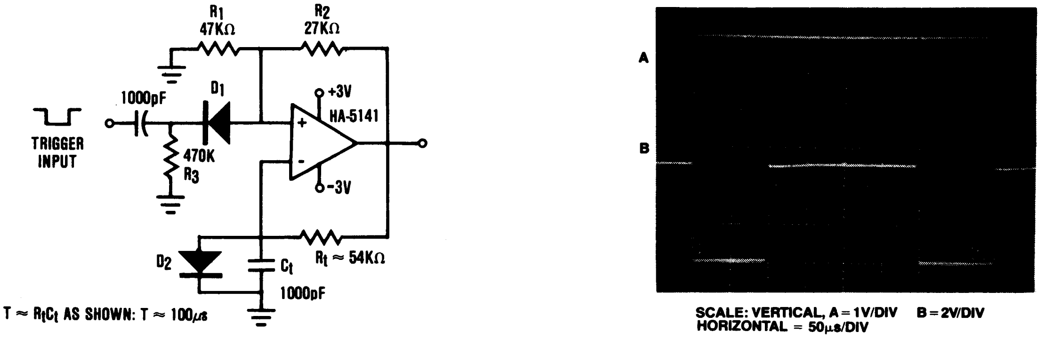
BAR CODE SCANNER

Application 7—Monostable Multivibrator

The circuit to the right illustrates the usefulness of the HA-5141 as a battery powered monostable. In this circuit the ratio is set to .632, which allows the time constant equation to be reduced to:

$$T = R_tC_t$$

D_2 is used to force the output to a defined state by clampinng the negative input at +0.6V. Triggering is set by C_1, R_3, and D_2. An applied trigger pulls the positive input below the clamp voltage (+0.6V) which cause the output to change state. This state is held because the negative input cannot "follow" the change due to R_t, C_t. As can be seen in the photograph, this particular circuit has a output pulse width set at approximately 100µs. Use of potentiometers for R_t and varible capacitors for C_t will allow for a wide variation in T.


R1 47KΩ
R2 27KΩ
1000pF
D1
+3V
HA-5141
TRIGGER INPUT
470K R3
-3V
D2
Ct
Rt ≈ 54KΩ
1000pF
T ≈ RtCt AS SHOWN: T ≈ 100µs
A
B

SCALE: VERTICAL, A = 1V/DIV B = 2V/DIV
HORIZONTAL = 50µs/DIV

MONOSTABLE MULTIVIBRATOR

Application 8—AC Coupled Dynamic Amplifier

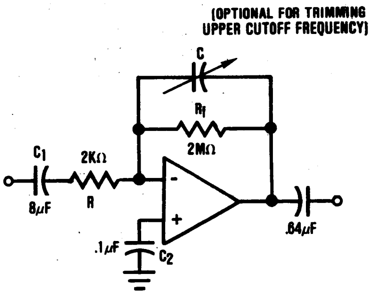
The circuit shown below is yet another of the many ways to utilize the advantages of HA-5141/42/44. This circuit would be most useful for biomedical instrumentation and acts as a bandpass filter with gain. Low frequency cutoff is set at 10Hz while the high frequency break point is given by the open loop roll off characteristic of the HA-5141/42/44. In this case, the AVc1 = -60dB the rolloff occurs at approximately 300Hz. This corner frequency may be trimmed by inserting a capacitor in parallel with R_f.

Acknowledgements

A. Russell Leath of Georgia Institute of Technology — Engineering Experiment Station, Atlanta, GA., developed an evaluated the circuits in this Application Note.

B. Don Jones, Jon Dutra, and David Graen, Harris Semiconductor, Analog Division, Field Application Engineers provided inputs leading to the development of the circuits in this Application Note.

C. Gerry Cotreau, Harris Semiconductor, Analog Division, provided inputs involving operation of the HA-5141/42/44 devices.



AC COUPLED DYNAMIC AMPLIFIER (A_{VCL} = -1000)

NOTICE: Information contained in application notes is intended solely for general guidance; use of the information for user's specific application is at user's risk.

APP NOTE

FOR YOUR INFORMATION

No. 545

Harris Analog

NEW MULTIPLEXERS SIMPLIFY SYSTEM DESIGN

By T. R. Fleming and T. M. Westenburg

INTRODUCTION

Monolithic analog multiplexers have been available since the early seventies. They provide simple switching functions and have undergone relatively few design changes. However, system designers have established three desireable attributes which widen these products. range of application and save board area where they are used.

- Latched channel address inputs
- Overvoltage protection
- High impedance at the channel inputs with power off

These features have been available separately,but only the new HI-50XL family from Harris Semiconductor combines all three in a single product.

Latches for the channel address are required in many cases, so these have been provided on-chip. (If not needed, they may be wired in the "transparent" mode). Overvoltage protection is needed when channel inputs connect directly to a user-accessable interface; having this protection built into the multiplexer often eliminates the need for external resistors and diodes. Finally, high analog input impedance with power off is very welcome in the design of redundant systems, where a powered-down standby MUX may be wired in parallel with an active one.

These products form a conventional multiplexer family: HI-506L/507L, 16 Channel Single Ended/8 Channel Differential versions; and HI-508L/509L, the 8 Channel SE/4 Channel Differential versions. The term "50XL" refers to this product family. In the following sections, the new switch is compared with older designs and the 50XL control signals are described. Next comes a discussion of tradeoffs associated with different methods of interface to a microprocessor system, and a detailed description of a typical application.

NEW SWITCH DESIGN

The switch cell of the 50XL has a different structure than earlier Harris designs (HI-50X, HI-50XA). The new switch (Figure 1) consists of an N-channel, P-channel and N-channel MOSFET in series, as opposed to the trnasmission gate configuration with an N and P-channel device in parallel. The series N-P-N switch offers much higher Off Isolation with power off and better fault performance. Channel overvoltage protection is inherent since at least one of the three MOSFETs will turn off in the presence of overvoltage.

For the conditions shown in Figure 1 (power on; switch closed), gate voltage for the outer N-channel MOSFETs is +15V. Therefore, channel resistance in the left hand device will increase as the analog input increases from zero, since V_{GS} is approaching the threshold value (approximately 2V). Similarly, the P-channel resistance increases as the input increases in the negative direction, yielding an overall variation of "ON Resistance" as shown in Figure 2. This variation restricts the useable signal range somewhat, but provides a natural "shutoff" for inputs which approach or exceed the supply voltages. Of particular interest is the behavior with power off, in which R_{ON} remains high for all values of input. Table 1 shows the conditions of a 50XL switch for all modes of operation and values of input voltage.

A further advantage for the 50XL switch over earlier designs is its higher OFF Isolation: -72dB with power, and -56dB with power off (V_{IN} = $3V_{rms}$ @ 500kHz). That is, switch feedthrough with the power off is less than 0.17%.

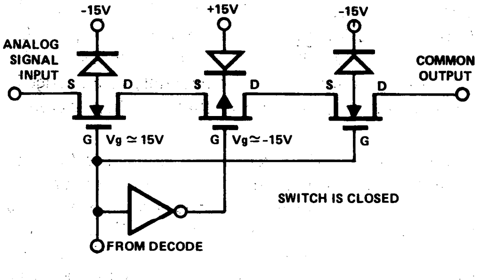


Figure 1. Switch Cell

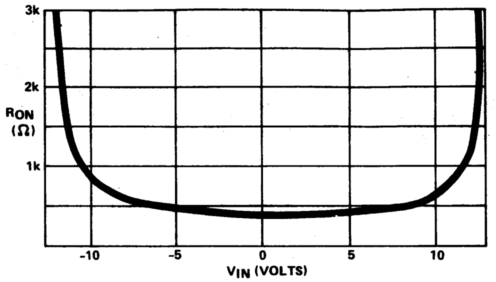


Figure 2. V_{IN} vs. R_{ON}

Table 1. 50XL Switch Behavior

MODE OF OPERATION	ANALOG INPUT, V_{IN}		
	NEGATIVE OVERVOLTAGE ($V_{IN} \leq$ -14V)	NORMAL OPERATION (-10V $\leq V_{IN} \leq$ +10V)	POSITIVE OVERVOLTAGE ($V_{IN} \geq$ +14V)
Power On; Switch Closed	OXO	OOO	XOO
Power On; Switch Open	OXX	XXX	XXX*
Power Off	OXX	–	XXX*

(Switch MOSFETs: N-P-N, where X = OFF; O = ON)
* State of the P-channel MOSFET is indeterminate.

CONTROL SIGNALS

The Address inputs A_0, A_1, A_2, A_3 and Enable are latched into an internal buffer when $\overline{WR}$ goes from low to high. These digital inputs are DTL, TTL and CMOS compatible. Each latch output is level shifted into the decode section, which activates the appropriate channel, (if any). The device may be reset (all channels OFF) by taking $\overline{RS}$ low. Usually, $\overline{RS}$ is tied to the system reset line to assure that all channels are OFF following a turn-on of power. The reset ($\overline{RS}$) line may also be tied to the power supply with a resistor and capacitor to provide a delay from initial power-up. Refer to Figure 3.

The reset function overrides all others, just as $\overline{WR}$ (Write) overrides the address inputs (A_0 - A_3 and EN are ignored when $\overline{WR}$ is high). With $\overline{WR}$ low and $\overline{RS}$ high, the switches respond immediately to a change in channel address; i.e., the latches are "transparent".

Members of the 50XL family are easily interfaced to a microprocessor system. The channel select lines may be tied directly to either the address or the data bus. No I/O interface device (PIA, PPI) is required since latches are provided on the HI-50XL chip. However, some additional hardware may be necessary for deriving the HI-50XL $\overline{WR}$ signal, depending on system requirements. Refer to Figure 4.

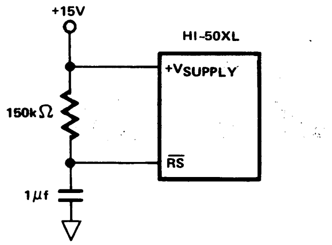
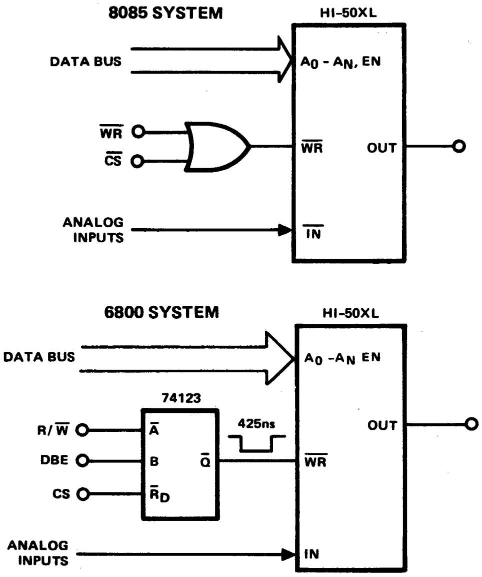


Figure 3. 50XL Switch Behavior



(MINIMUM DBE LOW TIME REQUIRED)

Figure 4. 50XL Control Requirements

THE 50XL-SYSTEM INTERFACE

There are perhaps eight basic ways to connect a 50XL multiplexer in a microprocessor system. Most of these are options common to the interface of any peripheral device, so the most appropriate method is usually indicated by the system hardware and its intended use.

To operate the 50XL, three functions must be provided - chip (device) selection, channel selection (A_0, A_1 . . . A_N, EN) and control ($\overline{WR}$, $\overline{RS}$). Channel selection is accomplished by a direct connection either to the data bus (simpler software) or to the address bus (higher clock speed allowable). For either case, a chip select is obtained in the usual way, using either an address bus decoder or the "bit flag" method, in which one address line is dedicated to the 50XL. Further, many systems will offer access to the 50XL through an option of either "memory mapping" or "I/O mapping", yielding eight different interface connections.

Four of these cases are illustrated in Figure 5, in which each HI-506L multiplexer is installed in the I/O space of an 8085 microprocessor. Channel selection is by the data bus (#1,#2) and the address bus (#3,#4). Device selection is provided by an address decoder (#1,#3) and by the dedicated address line "bit flags" (#2,#4).

For each multiplexer, external gates and control lines are arranged to write a 5 bit word (A_0, A_1, A_2, A_3, EN) to the address inputs, and latch it by a low-to-high transition at MUX's $\overline{WR}$ input. The 50XL requires a minimum 300ns for this WR pulse, and if necessary, a monostable multivibrator (one-shot) may be added to extend the pulse's duration. To clarify these system timing relationships, the parameters relevant to an 8085 I/O Write operation are shown in Figure 6, along with two selected waveforms from Figure 5 and the 50XL Write Pulse. As an alternative, however, the timing requirements may easily be met using a programmable peripheral interface device (PPI, PIA, or equivalent).

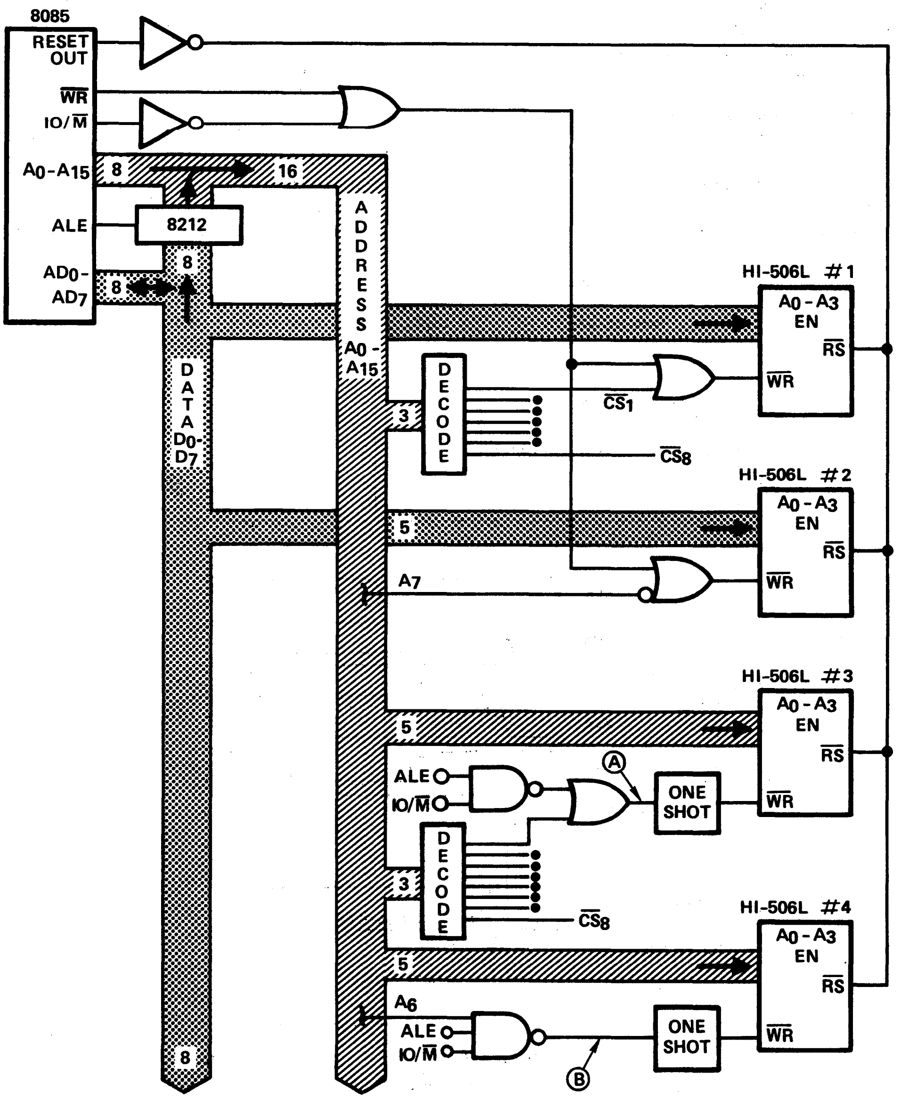

8085
RESET OUT
WR
IO/M
A0-A15
ALE
AD0-AD7
8
16
8212
8
8
ADDRESS A0-A15
DATA D0-D7
HI-506L #1
A0-A3
EN
RS
WR
DECODE
3
CS1
CS8
HI-506L #2
5
A7
HI-506L #3
5
ALE
IO/M
A
ONE SHOT
DECODE
3
CS8
HI-506L #4
5
A6
ALE
IO/M
ONE SHOT
B
8

Figure 5. 50XL Interface Examples

SYSTEM APPLICATION EXAMPLE

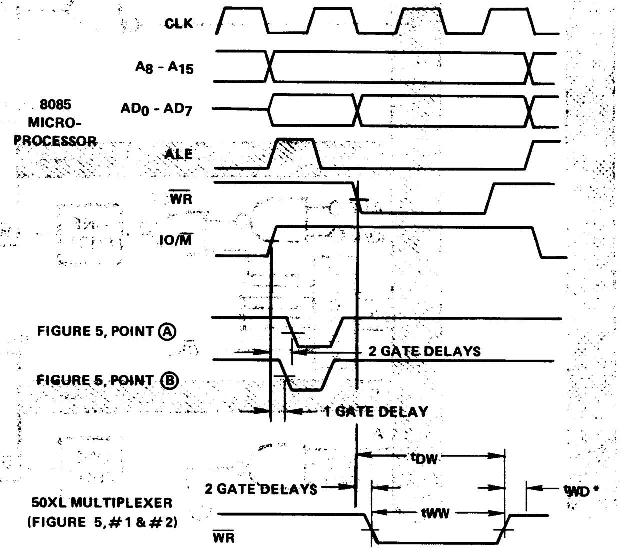
Figure 7 includes two separate data acquisition systems controlled by an 8085 microprocessor. In the upper system, 16 analog channels are multiplexed into a Sample/Hold - A/D Converter combination which provides sample rates as high as 2.7kHz per channel. In the lower system, two HI-506Ls are operated as a single 32 channel multiplexer, delivering the analog signal through a buffer amplifier directly to an A/D converter. Bandwidth of these 32 analog signals is limited since no Sample/Hold is used (for 12 bit accuracy, BW must not exceed 2 hertz). However, each channel may be digitized every 736 μs, for a 1.36kHz sample rate.

In each system of Figure 7, control of the HI-506L multiplexer is as shown in Figure 5, # 2. That is, the latched address inputs are connected directly to the data bus for channel selection, and a single bit of the I/O address is used as a chip select. (Up to eight peripherals may be controlled in this manner). The multiplexer's WR input is derived by appropriate gating of this chip select with the 8085 WR and IO/M signals.

In the upper system a D-type flip-flop simultaneously initiates a conversion and switches the Sample/Hold to Hold. This is acceptable since the Hold mode settling is only 185ns, and at least 1μs will elapse before the converter's first bit decision. Similarly, the lower system uses a flip-flop to initiate conversions and another flip-flop to control the HI-200 switch, forming a 32 channel multiplexer.

The two multiplexers in the lower system are operated in parallel so two analog signals are always presented to the analog switch. Crosstalk in the switch is not a concern since only low BW signals are involved. As an alternative, one may eliminate the HI-200 switch and its flip-flop by connecting the MUX outputs together and using the ENable controls to enable one multiplexer at a time. However, output capacitances add together to increase the output time constant. Additional settling time must be allowed for the multiplexer, so the result is a lower channel rate than with the HI-200 switch arrangement.

PARAMETER	TYPICAL +25°C	MIN LIMITS FULL TEMP. RANGE	UNITS
t_{WW}, Write Pulse Width	155	300	ns
t_{DW}, A, EN Data Valid To WRITE (Stabilization Time)	85	225	ns
t_{WD}, A, EN Data Valid After WRITE (Hold Time)	20	100	ns
t_{RS}, RESET Pulse Width (not shown)	250	400	ns



*TO MEET THE MINIMUM t_{WD} REQUIREMENT, 8085 CLK MUST NOT EXCEED 2MHz.

Figure 6. Timing Requirements.

Initiation of a Read operation by the processor toggles a flip-flop in each system, setting the converters to Read and (for the upper system) switching the Sample/Hold to Sample. Finally, each converter's STATUS output is inverted and tied directly to one of the processor's interrupt request terminals, with higher priority to the upper converter. The processor may execute instructions until a conversion is completed in either system - then it vectors to a Read routine, stores the data, and triggers another conversion. Each result will occupy two bytes of memory since a 12 bit word must be transmitted on an 8 bit data bus. The HI-574A accomplishes this by monitoring the A_0 address line with its A_0 control input, allowing the converter to route the two bytes into consecutive memory locations.

Machine language routines suitable for exercising the system of Figure 7 are listed in the following section. Also, detailed parametric limits for the HI-506L and HI-507L multiplexers are listed in Figure 8.

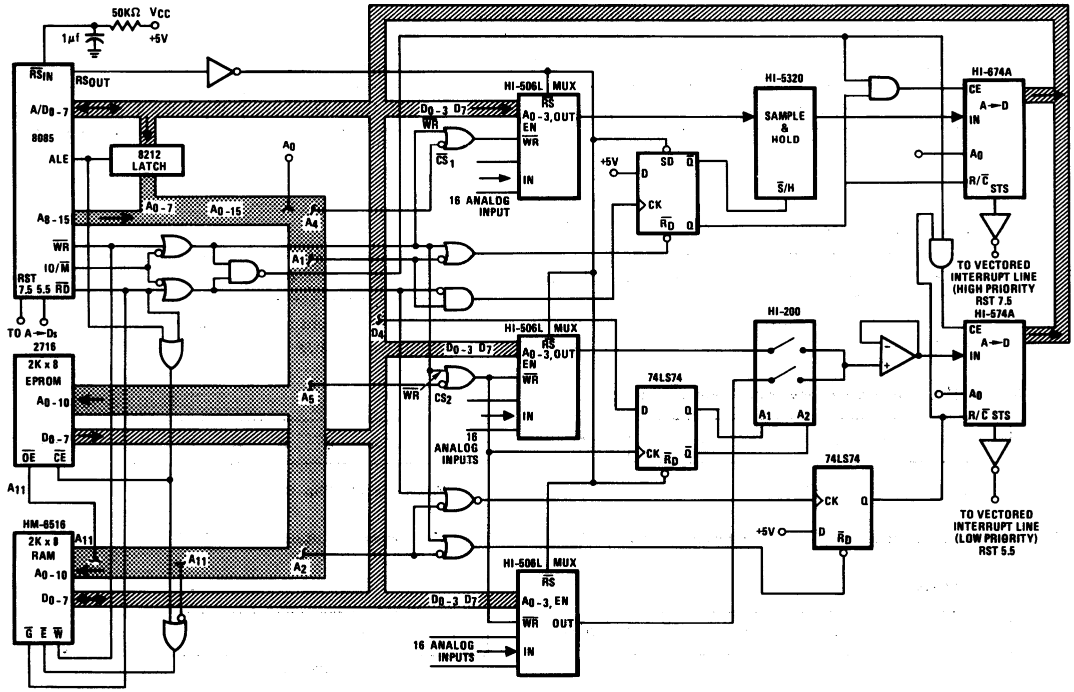
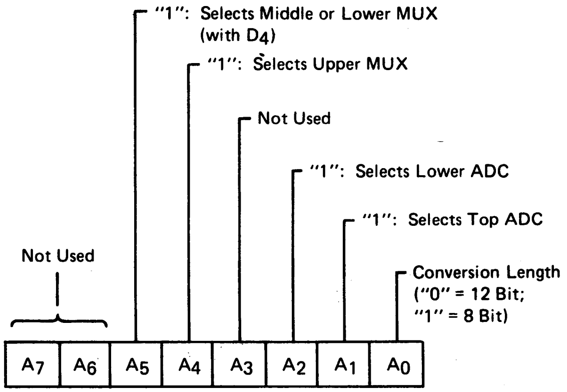
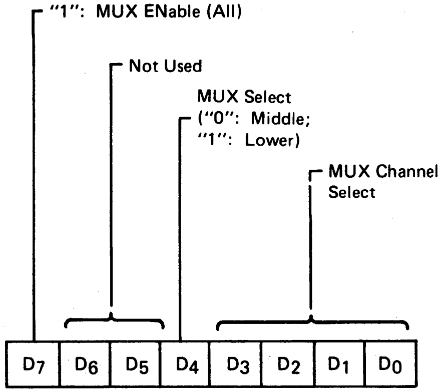

50KΩ VCC
1μf
+5V
RSIN
RSOUT
A/D0-7
8085
ALE
8212 LATCH
A8-15
WR
IO/M
RST 7.5 5.5
RD
TO A→Ds
2716
2K x 8 EPROM
A0-10
D0-7
OE CE
A11
HM-6516
2K x 8 RAM
A0-10
D0-7
G E W
A0-7
A0-15
A0
A4
A1
A5
A2
A11
D4
HI-506L MUX
RS
A0-3, OUT
EN
WR
IN
D0-3 D7
CS1
CS2
16 ANALOG INPUT
16 ANALOG INPUTS
+5V
SD Q̄
D
CK
RD Q
HI-5320
SAMPLE & HOLD
S/H
HI-674A
CE
A→D
IN
A0
R/C STS
TO VECTORED INTERRUPT LINE (HIGH PRIORITY) RST 7.5
HI-574A
HI-200
A1 A2
74LS74
TO VECTORED INTERRUPT LINE (LOW PRIORITY) RST 5.5

Figure 7. HI-50XL System Application.

SOFTWARE CONTROL

These brief assembly routines implement the basic operations required in Figure 7. Since hardware connections commit various lines of the address and data buses to specific jobs, control information may be conveyed to the system components by individual bit signals on these buses. The programmer simply writes an appropriate control word to the location of a given component. Control words are composed according to the bit information shown below:


"1": Selects Middle or Lower MUX (with D4)
"1": Selects Upper MUX
Not Used
"1": Selects Lower ADC
"1": Selects Top ADC
Not Used
Conversion Length ("0" = 12 Bit; "1" = 8 Bit)
A7
A6
A5
A4
A3
A2
A1
A0


"1": MUX ENable (All)
Not Used
MUX Select ("0": Middle; "1": Lower)
MUX Channel Select
D7
D6
D5
D4
D3
D2
D1
D0

OPERATIONS

1. Select Channel 5 of upper MUX:

X	X	0	1	0	0	0	0	= 10 HEX	1	X	X	X	0	1	0	1	= 85 HEX

```
MVI    A, 85H        Move control word to Accumulator
OUT    10H           Write word to MUX
```

2. S/H to HOLD and start a conversion, upper converter:

X	X	X	X	X	X	1	0	= 02H	X	X	X	X	X	X	X	X	= 00H

```
OUT    02H           Write word to Flip-flop
```

3. Read output of top converter, following an interrupt via 8085 RST7.5 input. (Converter output is 1101 0110 1001.):

Read 1st byte –

X	X	X	X	X	X	1	0	= 02H	1	1	0	1	0	1	1	0	= D6H

(8MSBs)

Read 2nd byte –

X	X	X	X	X	X	1	1	= 03H	1	0	0	1	0	0	0	0	= 90H

(4LSBs)

Interrupt RST7.5 causes a JUMP to the following service routine:

```
IN     02H           Read first byte
MOV    D, A          Move data to D register pair
IN     03H           Read second byte
MOV    E, A          Move data to E register pair
MVI    A, 1AH        Move control word to Accumulator
SIM                  Reset Interrupt
(Store data instructions)
RET                  Return
```

X	X	1	0	X	X	X	X	= 20H

1	X	X	[illegible]

```
MV1     A, 9EH          Move control word to Accumulator
OUT     20H             Write word to MUX
```

5. Initiate a conversion in lower converter:

X	X	X	X	X	1	0	0	= 04H

X	X	X	X	X	X	X	X	00H

6. Read output of lower converter following an interrupt via 8085 RST5.5 input:

This is accomplished with a routine identical to that in Operation // 3, except location 04H is used instead of 02H, and 05H instead of 03H.

APP NOTE

FOR YOUR INFORMATION

No. 548

Harris Analog

A DESIGNERS GUIDE FOR THE HA-5033 VIDEO BUFFER

Carl Wolfe

Introduction

Harris Semiconductor is an industry leader in the high speed, wideband, monolithic operational amplifier market. Due to the high performance of Harris products, designers in the more specialized areas of electronics have shown interest in utilizing these products in their applications. One such area is video design. In an effort to address this market, Harris has introduced the HA-5033 video buffer.

This paper will discuss the HA-5033 design and provide additional performance characteristics not shown in the data sheet.

HA-5033 Description

The HA-5033 is a unity gain monolithic I.C. designed for any application requiring a fast wideband buffer. A voltage follower by design, this product is optimized for high speed 50Ω and 75Ω coaxial cable driver applications common in color video systems.

Critical performance characteristics are summarized in Table 1. Outstanding differential phase/gain characteristics combined with an output current capability of ±100mA makes the HA-5033 an excellent choice for the line driver applications required in video circuit design.

PARAMETER	MIN	TYP	MAX	UNITS
Input Offset Voltage			15	mV
Input Bias Current			35	μA
Differential Phase		.1		degree
Differential Gain		.1		%
Slew Rate (±15V)	1000			V/μS
Output Current		±100		mA
Bandwidth (small signal)		250		MHz
Bandwidth (V_{IN} = 1 V_{RMS})		65		MHz
Supply Current			20	mA

TABLE 1. HA-5033 SPECIFICATIONS: T_A = +25°C; $\pm V_{SUPPLY}$ = ±12V (UNLESS OTHERWISE SHOWN)

Other features, which include a minimum slew rate of 1000V/μs, make the HA-5033 useful in high speed A/D data conversion and sample/hold circuits.

The HA-5033 is offered in two package configurations, the T0-8 metal can and the 8 pin epoxy Mini-Dip. The pinouts for each package are illustrated in Figure 1.

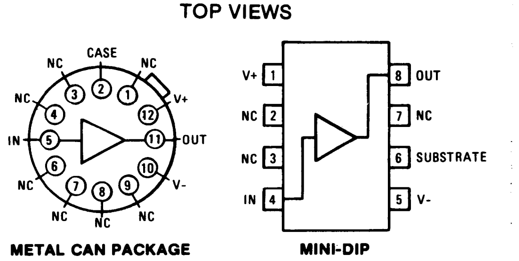


FIGURE 1. HA-5033 PINOUTS: T0-8 METAL CAN-PIN COMPATIBLE WITH THE LH0033 HYBRID. 8 PIN MINI-DIP - FABRICATED USING A COPPER LEAD FRAME. ADVANTAGES INCLUDE EXCELLENT THERMAL CHARACTERISTICS AND BOARD SPACE SAVINGS.

The high performance of this product (summarized in Table 1) is the result of the Harris High Frequency Dielectric Isolation Process. A major feature of this process is that it provides both PNP and NPN high frequency transistors which make wide bandwidth designs, such as the HA-5033, practical.

A Closer Look

Most manufacturer's data sheets provide a schematic diagram and depending upon the complexity of the product, this schematic may be comprehensive or possibly a simplified version. Schematics are a visual means of presenting information, ranging from reliability data, such as transistor counts, to circuit information for circuit analysis or computer simulation. But the most important reason for the schematic is to communicate to the customer the internal structure of the product and therefore, some insight into its operation.

At first glance, a schematic may appear as nothing more than a collection of resistors and transistors. But upon closer examination, particular areas of operation should become evident. Using the HA-5033 as an example (Figure 2), it will be shown that the HA-5033 consists of a signal path, bias network, and performance optimization circuitry.

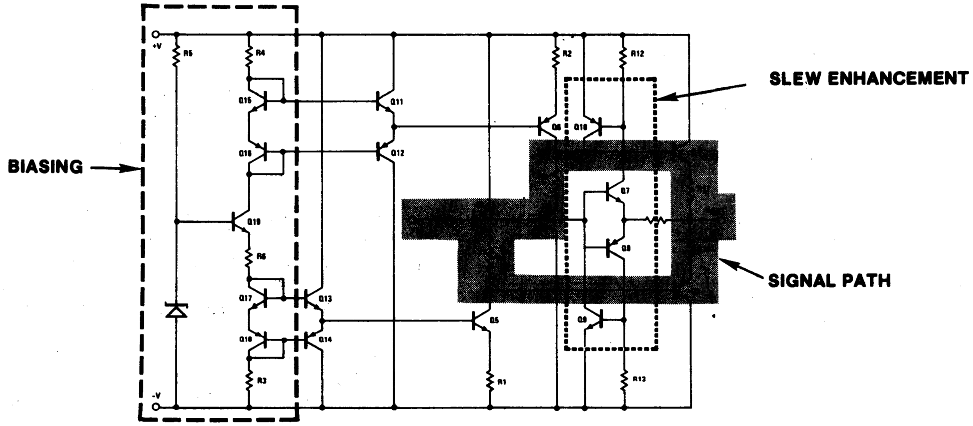


FIGURE 2. HA-5033 SCHEMATIC: VIDEO BUFFER DESIGN CONSISTS OF THREE OPERATING AREAS; SIGNAL PATH, BIAS NETWORK AND PERFORMANCE OPTIMIZATION CIRCUITRY.

Signal buffering is accomplished by cascading two emitter followers. In order to achieve symmetrical positive and negative output drive capability, two pairs are paralleled. The first pair consists of Q1 and Q4 for positive drive while the second pair Q2, Q3, provide negative drive. The emitter resistors of Q1, Q2 ensure stability with respect to load resistance, enhance differential phase/gain performance, and stabilize the quiescent operating point. This signal path has been high-lighted on the schematic.

The bias circuitry consists primarily of the diode-biasing located on the left portion of the schematic along with transistors Q5, Q6. This circuitry ensures the designed performance of the other active elements.

The performance optimization circuits are a slew enhancement circuit and a bias network buffer circuit. The transistors Q7, Q8, Q9 and Q10 are for slew enhancement. If the input voltage exceeds the output by one V_{BE}, Q7 will turn on Q10, which in turn provides extra base drive to Q1. Similary, Q9 will supply extra base drive to Q2.

Transistors Q11, Q12, Q13 and Q14 prevent high frequency or transient signals from affecting the bias circuitry. This prevents C_{CB} multiplication of current sources Q5 and Q6, which also improves differential gain/phase performance.

Note that output current limiting was not designed into the HA-5033. If there is a possiblity of the output being shorted to ground or the supplies, external current limiting will be necessary.

Any designer interested in using the HA-5033 should be aware of a characteristic related to output transistor operation. As the data sheet performance curves (reproduced in Figure 3) show, the output swing is a function of frequency. These curves show the point at

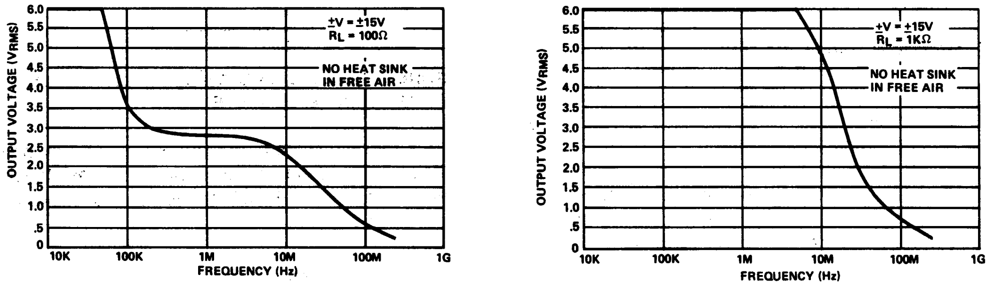
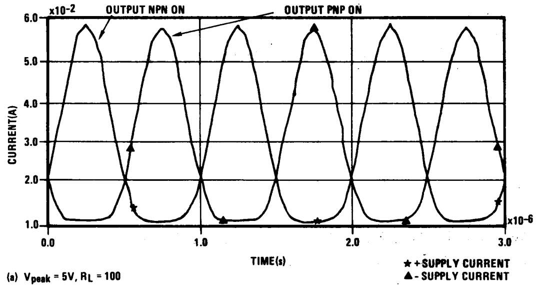
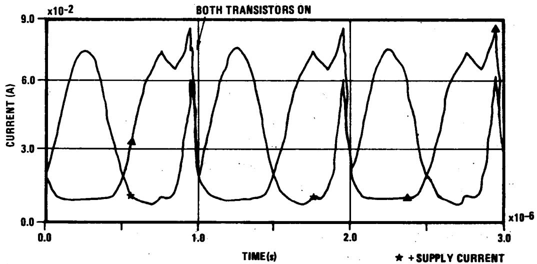


FIGURE 3. OUTPUT SWING VS. FREQUENCY PERFORMANCE CURVES: CURVES SHOW POINT OF OBSERVABLE DISTORTION FOR GIVEN FREQUENCY. OPERATION BEYOND THE CURVES SHOWN WILL APPROACH CONDITIONS WHERE OUTPUT TRANSISTORS ARE SIMULTANEOUSLY ON. THE RESULTING INCREASE IN CHIP TEMPERATURE WILL LEAD TO THERMAL RUNAWAY.

which observable distortion occurs for a given frequency. However, if the signal amplitude, signal frequency or both are increased beyond the curves shown, thermal "runaway" will occur. This is due to both the NPN and PNP output transistors approaching a condition of being simultaneously on. This condition has been computer simulated and the results are shown in Figure 4.



(a) V_{peak} = 5V, R_L = 100



(b) V_{peak} = 7V, R_L = 100

FIGURE 4. OUTPUT TRANSISTOR COMPUTER SIMULATION RESULTS

This condition occurs if the frequency of the analog signed does not allow sufficient time for the output PNP transistor to turn off. The frequency which causes this "push-push" output stage can be determined by using the following relationship,

$$\text{Full Power Bandwidth (FPB)} = \frac{SR}{2\pi V_p}$$

Where:
SR = Slew Rate
V_p = Analog Signal Peak Voltage

Therefore, the designer can determine the approximate frequency of thermal runaway by supplying the peak analog voltage and measuring the buffer slew rate for a particular application.

For example, the slew rate for the HA-5033 with a load of R_L = 1K ohm and C_L = 1000pF was measured to be 83 V/µS. The FPB for a 5V peak analog signal was calculated,

$$FPB = \frac{83V/\mu S}{2\pi(5V)} = 2.6MHz$$

So the estimated frequency of thermal runaway for the given conditions is 2.6MHz. Measurements in the lab resulted in a thermal runaway frequency equal to 2.5MHz.

Although the FPB relationship gives the designer a method of estimating the frequency of thermal runaway, it is recommended that the HA-5033 be operated to the left of the curves shown in Figure 3. Heat sinking the buffer will not prevent this condition from occuring.

The purpose of heat sinking a semiconductor is to maintain the device junction temperature below a specified maximum limit. This is a thermal problem and can be evaluated using the thermal analog of Ohms Law illustrated in Figure 5.

Where:
P_{dmax} = Power Dissipated ($P_{DC} + P_{AC}$), Watts
T_j = Maximum Junction Temperature, °C
T_a = Ambient Temperature, °C
$\theta_{j\text{-}c}$ = Junction to Case Thermal Resistance, °C/W
$\theta_{c\text{-}s}$ = Case to Heat Sink Thermal Resistance, °C/W
$\theta_{s\text{-}a}$ = Heat Sink to Ambient Thermal Resistance, °C/W

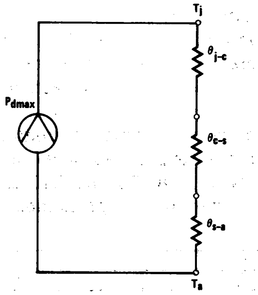


FIGURE 5. THERMAL ANALOG OF OHMS LAW: SEMICONDUCTOR /HEAT SINK SYSTEM

In this thermal system, current is replaced by power, voltage by temperature, and electrical resistance by thermal resistance. By using Figure 5, the following expression is derived,

$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j\text{-}c} + \theta_{c\text{-}s} + \theta_{s\text{-}a}}$$

This expression allows the designer to determine the maximum power dissipation of a semiconductor/heat sink system.

The expression for the semiconductor in free air is,

$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j\text{-}a}}$$

In order to make use of these expressions, the following information is required. $\theta_{j\text{-}c}$ and T_{jmax}, from the semiconductor manufacturer and $\theta_{c\text{-}s}$ and $\theta_{s\text{-}a}$, from the heat sink manufacturer.

For the Harris HA-5033, the maximum junction temperature is $T_{jmax} = 200^oC$. The thermal impedances for the HA-5033 in the T0-8 metal can package are $\theta_{j\text{-}c} = 31^oC/W$ and $\theta_{j\text{-}a} = 99^oC/W$. The epoxy mini-dip thermal impedances are $\theta_{j\text{-}c} = 27^oC/W$ and $\theta_{j\text{-}a} = 90^oC/W$.

Recommended heat sinks for the HA-5033 in the T0-8 metal can package are the Thermalloy 2240A[1] and IERC-UP-T08-51CB[2] (base), IERC-UP-C7 (top). Thermal impedances are $\theta_{s\text{-}a} = 27^oC/W$ and $\theta_{s\text{-}a} = 10^oC/W$, respectively. $\theta_{c\text{-}s}$ is dependent upon the type of insulator or thermal joint compound used. Both products are two piece heat sinks, but differ in design.

By using the given product information and supplying an operating ambient temperature, the designer can determine the maximum power the system will dissipate and not exceed the maximum junction temperature.

For example, Figure 6 shows the maximum power dissipation for the HA-5033 in a T0-8 metal can package to be 1.75W at 25°C.

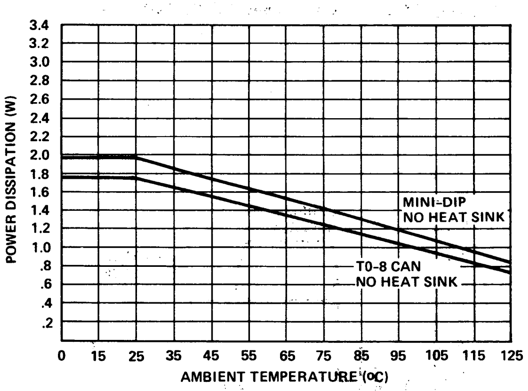


FIGURE 6. HA-5033 MAXIMUM POWER DISSIPATION VS AMBIENT TEMPERATURE: FREE AIR

The maximum power dissipation of the HA-5033/2240A heat sink system is calculated to be,

$$P_{dmax} = \frac{200-25}{31 + 27} = 3.01W$$

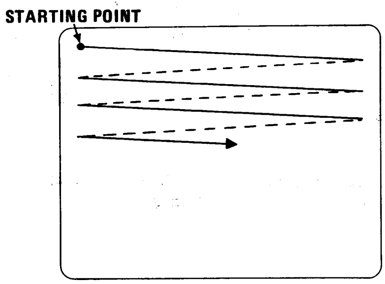
Therefore, the HA-5033 used with the Thermalloy 2240A can dissipate 3.0W at 25°C and not exceed the maximum junction temperature of 200°C.

The power dissipation limits shown in Figure 6 and those determined with the heat sink apply for both quiescent and load related power. Therefore,

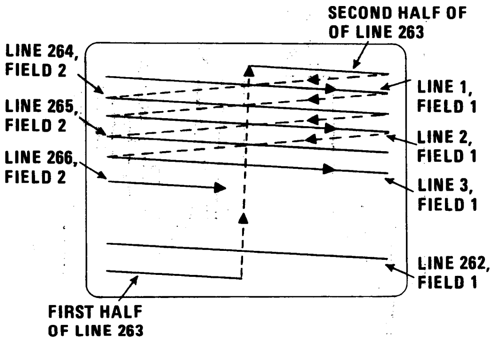
$$P_{dmax} > P_{DC} + P_{AC}$$
$$P_{DC} = (+V)(+I) + (-V)(-I)$$
$$P_{AC} = (1/T)_0\int^T v(t)\, i(t)\, dt$$

Video Performance

The images which appear on your television picture tube are created by a process called scanning[3]. Scanning is a method of recreating the optical image of a scene one line at a time. Referring to Figure 7a, an electron beam moves or "scans" from left to right and quickly returns to a position below its starting spot. This process continues until the bottom of the picture is reached and the beam returns to the original top left hand position. This method is called sequential scanning.



SEQUENTIAL SCANNING



INTERLACED SCANNING

FIGURE 7. SCANNING SEQUENCE

Incorporated into present television broadcast standards is a technique called interlaced scanning. Interlaced scanning recreates the scene by providing two half scans. As shown in Figure 7b, the first scan traces out the odd numbered lines, the second scan fills in the even numbered lines. This technique avoids the flicker problem and excessive bandwidths required for similar picture definition using sequential scanning.

The United States NTSC (National Television Systems Committee) broadcast standard is a 525 line standard. Each scan consists of 262½ lines. The first scan is known as field one, the second, field two. Therefore, the complete picture consists of two fields.

The first 21 lines of each field are blank. Those lines are left open and are not used to broadcast video information. Instead, these lines contain other important information, such as sync pulses, data transmission, and test signals. The test signals contained in these lines are called the Vertical Interval Test Signals (VITS)[4,5], which allows real-time monitoring of the television broadcast signal quality. These test signals were used to evaluate the video performance of the HA-5033.

Four test signals are commonly used in the vertical interval. They are the multiburst, color bar, composite and vertical interval reference. These test signals are shown in Figures 8 through 11.

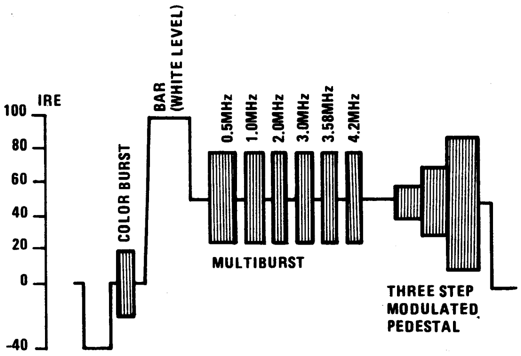

IRE
100
80
60
40
20
0
-40
COLOR BURST
BAR (WHITE LEVEL)
0.5MHz
1.0MHz
2.0MHz
3.0MHz
3.58MHz
4.2MHz
MULTIBURST
THREE STEP MODULATED PEDESTAL

FIGURE 8. MULTIBURST SIGNAL (FIELD 1, LINE 17) ALLOWS FREQUENCY RESPONSE CHECKS

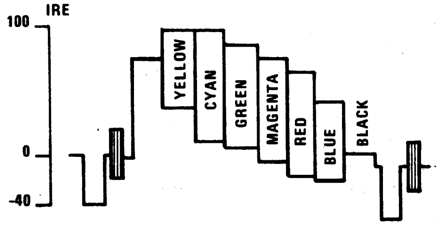

IRE
100
0
-40
YELLOW
CYAN
GREEN
MAGENTA
RED
BLUE
BLACK

FIGURE 9. COLOR BAR (FIELD 2, LINE 17) ENABLES MONITORING OF COLOR TRANSMISSION QUALITY

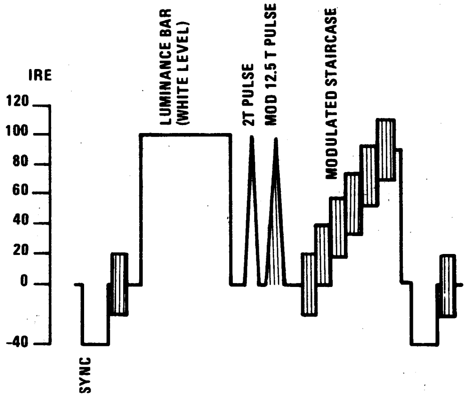

IRE
120
100
80
60
40
20
0
-40
SYNC
LUMINANCE BAR (WHITE LEVEL)
2T PULSE
MOD 12.5 T PULSE
MODULATED STAIRCASE

FIGURE 10. COMPOSITE SIGNAL (FIELD 1, AND 2, LINE 18) DESIGNED FOR GAIN AND TIME DELAY TESTS

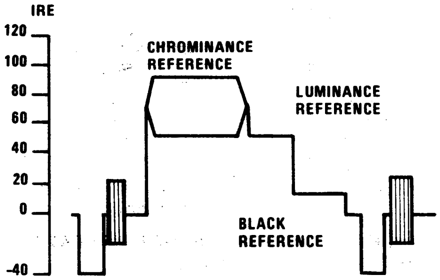
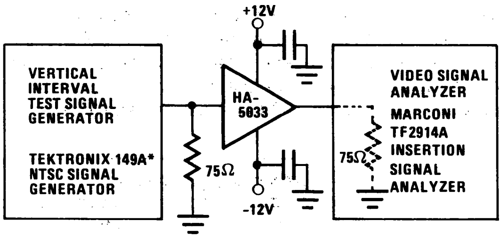

IRE
120
100
80
60
40
20
0
-40
CHROMINANCE REFERENCE
LUMINANCE REFERENCE
BLACK REFERENCE

FIGURE 11. VERTICAL INTERVAL REFERENCE SIGNAL (FIELD 1 AND 2, LINE 19) PROVIDES COLOR AND GAIN REFERENCES

Each test signal was created to allow various distortions to be measured without interfering with the normal video transmission. These signal distortions which exist in television systems are defined as linear or non-linear. Non-linear distortion, such as differential phase and gain, vary with the amplitude of the picture signal. Linear distortions, usually dependent upon frequency response, are independent of signal level. For example, the multiburst test signal is very useful for frequency response checks, where as the composite signal contains signals for checking gain error.

Determining the HA-5033's performance level with respect to the NTSC standard required the definition of a measurement method. Test equipment was needed that would produce the necessary NTSC test signals and also monitor the device under test performance. The test configuration, shown in Figure 12 consisted of a Tektronix 149A NTSC^6 generator and Marconi TF 2914A video analyzer^7.


VERTICAL INTERVAL TEST SIGNAL GENERATOR
TEKTRONIX 149A* NTSC SIGNAL GENERATOR
+12V
HA-5033
75Ω
-12V
VIDEO SIGNAL ANALYZER
MARCONI TF2914A INSERTION SIGNAL ANALYZER
75Ω

*TEKTRONIX 1910 NTSC DIGITAL GENERATOR RECOMMENDED

FIGURE 12. HA-5033 NTSC PERFORMANCE TEST CONFIGURATION

The TF 2914A has the capability of measuring 24 separate video parameters. Other advantages include direct readout and much more accuracy than possible using scope methods. Table 2 lists the video parameters tested on the HA-5033 along with the particular VITS utilized by the TF 2914A.

VIDEO PARAMETER	VERTICAL INTERVAL TEST SIGNAL USED
Luminance Bar Amplitude	Luminance Bar, Composite Signal (Fig. 10)
Sync Amplitude	Sync Pulse, Composite Signal (Fig. 10)
2T Pulse to Bar Ratio	2T Pulse/Luminance Bar, Composite Signal (Fig. 10)
Chrominance to Luminance Gain Inequality	Chrominance Component Amplitude of the 12.5T Pulse and Luminance Bar Amplitude, Composite Signal (Fig. 10)
Chrominance to Luminance Delay	Time Difference of Chrominance and Luminance Components of the 12.5T Pulse, Composite Signal (Fig. 10)
Luminance Non-Linearity	Largest and Smallest Step Amplitude of the Modulated Step Staircase, Composite Signal (Fig. 10)
Signal to Noise Ratio	Luminance Bar Level to Noise Voltage, Composite Signal (Fig. 10)
Chrominance to Luminance Crosstalk	Chrominance Component of 3 Step Modulated Pedestal and Luminance Bar, Multiburst Signal (Fig. 8)
Low Frequency Error	Amplitude of Low Frequency Signals
Bar Tilt	Difference of Luminance Bar Amplitude, Composite Signal (Fig. 10)
2T K Factor	2T Pulse, Composite Signal (Fig. 10)
Differential Gain	Amplitude Deviation of Modulated Step Staircase, Composite Signal (Fig. 10)
Differential Phase	Phase Deviation of Modulated Step Staircase, Composite Signal (Fig. 10)
Flag	Luminance Amplitude, Multiburst Signal (Fig. 8)
Multiburst 1-6	Amplitude of Each Frequency Burst, Multiburst Signal (Fig. 8)
Color Reference Burst Amplitude	Color Burst Amplitude, Multiburst Signal (Fig. 8)

TABLE 2. TF 2914A VIDEO MEASUREMENT PARAMETERS REFERRED TO VERTICAL INTERVAL TEST SIGNALS

Since the TF 2914A measurement includes any inaccuracies of the NTSC signal generator, a "delta" measurement was neccesary. The NTSC generator was connected directly to the analyzer and the results recorded. Next, the HA-5033 was inserted and the results recorded. The difference between the two readings was considered the actual HA-5033 performance. Table 3 lists the video performance results of the HA-5033.

VIDEO PARAMETER	HA-5033	UNITS
Luminance Bar Amplitude	93.6	IRE*
Sync Amplitude	37.5	IRE
2T Pulse to Bar Ratio	99.9	IRE
Chrominance to Luminance Gain Inequality	99.9	IRE
Chrominance to Luminance Delay	1.5	nS
Luminance Non-Linearity	0.1	%
Signal-to-Noise Ratio	66	db
Chrominance to Luminance Crosstalk	51.6	IRE
Low Frequency Error	0.3	mv
Bar Tilt	0.3	IRE
2T K Factor	0.1	K
Differential Gain	0.1	%
Differential Phase	0.1	degree
Flag	99.5	IRE
Multiburst 1 Amplitude	49.2	IRE
Multiburst 2 Amplitude	49.3	IRE
Multiburst 3 Amplitude	51.0	IRE
Multiburst 4 Amplitude	50.4	IRE
Multiburst 5 Amplitude	49.7	IRE
Multiburst 6 Amplitude	50.0	IRE
Color Reference Burst Amplitude	40.4	IRE

TABLE 3. HA-5033 NTSC VIDEO PERFORMANCE

* IEEE Standard 205-1958 defines the levels of television video signal in terms of IRE units.
100 IRE units = 0.714V, P-P

Applying The HA-5033

The most important consideration when designing with the HA-5033 is layout. The wide bandwidth of the buffer necessitates that high frequency layout procedures be followed. Recommended procedures include the use of a ground plane, minimization of all lead lengths, avoiding sockets, and proper power supply decoupling.

Standard practice in RF/Video layout is the use of a ground plane. A ground plane minimizes distributed circuit capacitance and inductance which degrade high frequency performance. The ground plane can also incorporate the metal case of the HA-5033, since pin #2 is internally tied to package. This feature allows the user to make contact between the ground plane and the package which extends shielding, provides additional heat sinking and eliminates the use of a socket. IC sockets contribute bandwidth limiting interlead capacitance and should be avoided.

For the epoxy mini-dip, additional heatsinking can be derived from soldering the no connection pins #2, 3, and 7 to the ground plane. Also, pin #6 can be tied to either supply, grounded or left open. But to optimize device performance and improve isolation, it is recommended that this pin be grounded.

Another method of enhancing device performance is power supply decoupling. For the HA-5033, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from .01 to .1 μF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1μF or larger will optimize low frequency performance. It is also recommended that the bypass capacitors be connected as close to the HA-5033 as possible, preferably directly to the supply pins.

Finally, keeping all lead lengths as short as possible will minimize distributed capacitance and reduce board space. It is essential that the guidelines discussed above be followed to avoid marginal performance.

Another consideration when applying the HA-5033 is load capacitance. Although the HA-5033 is designed to handle load capacitance values up to .01μF, it has a worst case stability region in the area of 50pF. The computer simulation of the HA-5033 frequency response in Figure 13 illustrates the gain peaking which occurs in the 150MHz region.

There are three suggested methods of dealing with this particular characteristic of the HA-5033. Isolating the load capacitance from the buffer output is the object of the first method. This is accomplished by placing a series resistor between the output and the load.

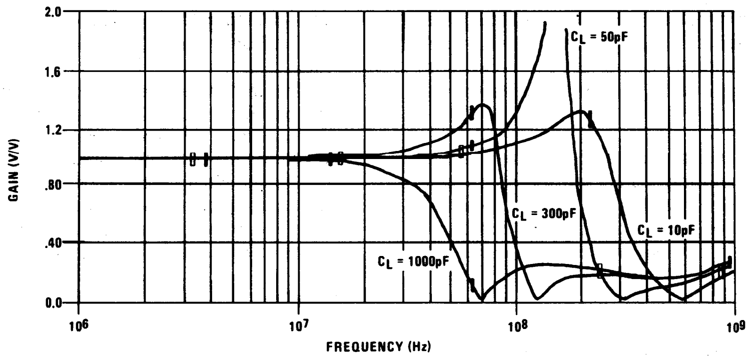


FIGURE 13. COMPUTER SIMULATION OF HA- 5033 GAIN CHARACTERISTICS VS FREQUENCY AND LOAD CAPACITANCE

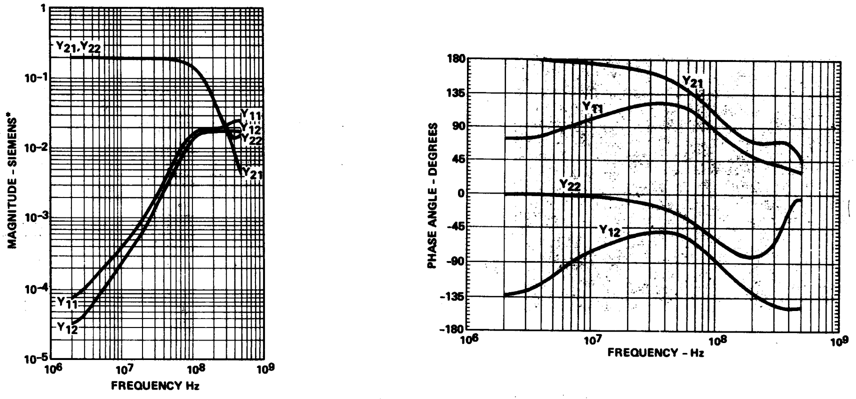
A second technique utilizes the HA-5033 frequency response with respect to load capacitance. Referring once again to Figure 13, notice that the gain peaking is removed with additional load capacitance. This is the basis of method two, adding additional load capacitance to approach a region of stability.

A drawback to adding more load capacitance is that the buffer's dynamic characteristic will degrade and bandwidth performance will be less than data sheet specifications. The third method solves this trade-off by using a "bootstrap" technique of adding capacitance from input to output. This method achieves stability without sacrificing performance.

An explanation of why adding capacitance will stabilize the HA-5033 can be found in the Y parameter data shown in Figure 14. The expression for the buffer gain in terms of Y parameter is:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{-Y_{21}}{Y_{22} + Y_L}$$

Y_{21} = Forward Transmittance
Y_{22} = Output Admittance
Y_L = Load Admittance



*SIEMENS = Ω^{-1}

FIGURE 14. HA-5033 Y PARAMETER DATA

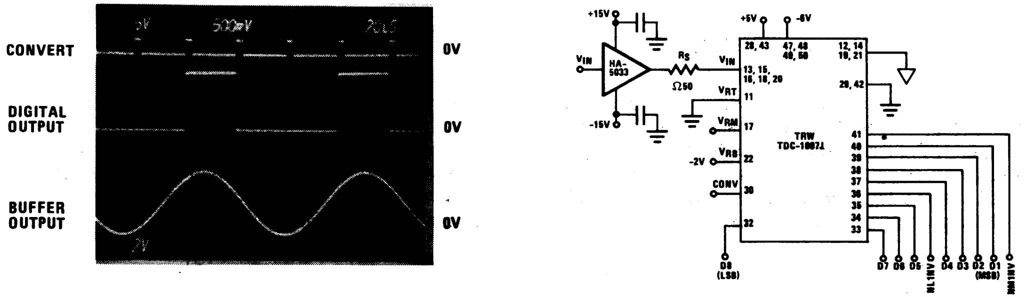
Notice that the load admittance, Y_{22}, phase becomes inductive ($-jY_L = -90^\circ$) at high frequency. So if the load, Y_L, is capacitive ($+jY_C = +90^\circ$) and the sum of $Y_{22} + Y_L$ become small, peaking occurs. Adding additional capacitance changes the effective phase angle and peaking can be reduced.

Using the HA-5033 as the analog input buffer of a flash converter is an example of application where the suggested stabilization methods are useful. Although its been stressed to keep all distributed capacitance to a minimum to optimize device operation, the load which a flash converter presents to the buffer represents a greater concern.

Flash or parallel converters are a special case, since the analog input circuit must drive a non-linear input impedance[8]. This non-linearity is due to the potential input impedance changes of the 255 parallel comparators which comprise the converter analog input. In addition to the non-linearity, the input capacitance of these converters tends to be relatively large, 100-300pF.

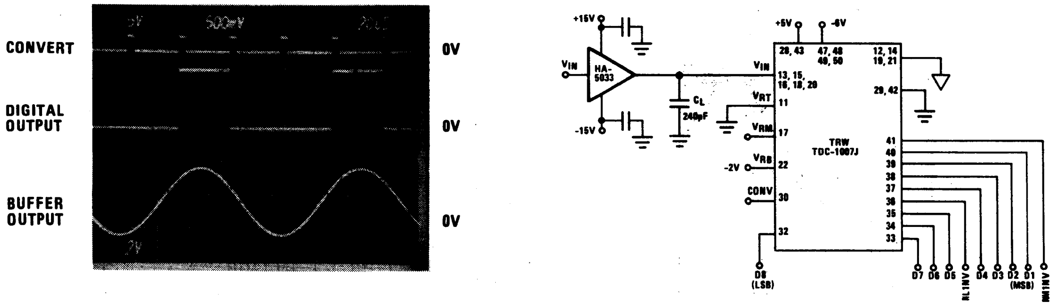
Example of the various stabilization methods tested with the TWR 1007 8 bit video flash converter are shown in Figure 15. Figure 15a illustrates the series resistor method. 15b is the load capacitance method and 15c is the bootstrap method. Photographs of the experimental results show the analog input sampling convert signal (pin 30), the MSB digital output (D1 pin 40), and the buffer output (converter input).

It is recommended that a complete evaluation for each method be conducted to determine the optimum component values. The value of the series resistor will depend upon the input capacitance of the particular converter used. A suggested starting value is 50ohms. With the capacitance methods, the distributed capacitance of the layout will affect component values. These experimental results were obtained using C = 240pf.



CONVERT
DIGITAL OUTPUT
BUFFER OUTPUT
0V
0V
0V
5V
500mV
2V
+15V
-15V
VIN
HA-5033
RS
Ω50
+5V
-6V
TRW TDC-1007J
VIN
VRT
VRM
VRB
CONV
-2V
D8 (LSB)
D7 D6 D5 D4 D3 D2 D1 (MSB)

FIGURE 15a. ENHANCING 5033 PERFORMANCE IN FLASH CONVERTER APPLICATIONS: SERIES RESISTOR METHOD



CONVERT
DIGITAL OUTPUT
BUFFER OUTPUT
0V
0V
0V
5V
500mV
2V
+15V
-15V
VIN
HA-5033
CL
240pF
+5V
-6V
TRW TDC-1007J
VIN
VRT
VRM
VRB
CONV
-2V
D8 (LSB)
D7 D6 D5 D4 D3 D2 D1 (MSB)

FIGURE 15b. LOAD CAPACITANCE METHOD

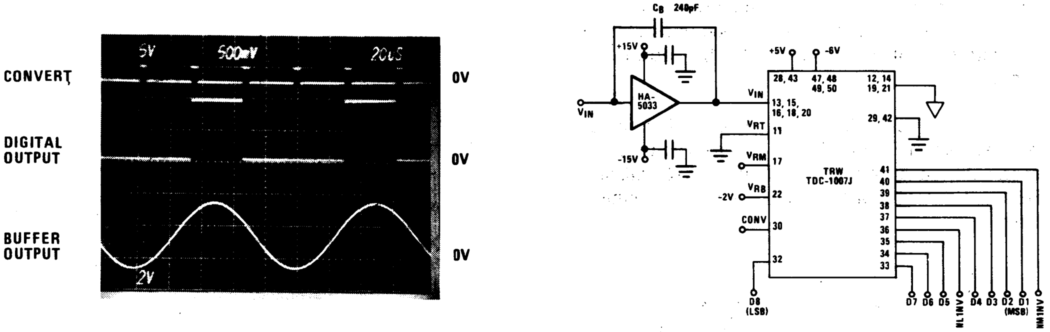
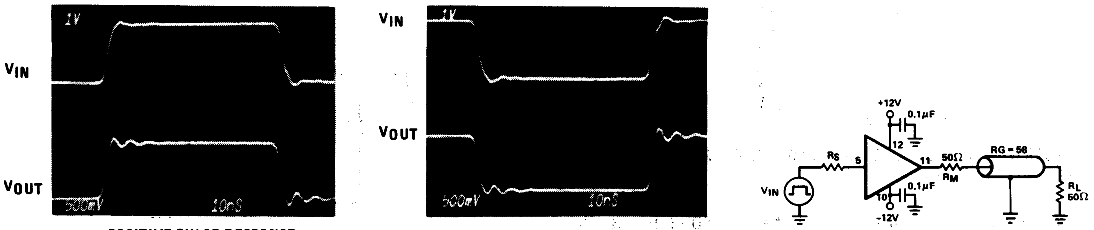

CONVERT
DIGITAL OUTPUT
BUFFER OUTPUT
0V
0V
0V
5V
500mV
20μS
2V
CB 240pF
+15V
-15V
HA-5033
VIN
+5V
-5V
28, 43
47, 48
49, 50
12, 14
19, 21
13, 15, 16, 18, 20
29, 42
VRT
11
VRM
17
VRB
-2V
22
CONV
30
32
TRW
TDC-1007J
41
40
39
38
37
36
35
34
33
D8 (LSB)
D7 D6 D5
D4 D3 D2 D1 (MSB)
NLINV
NMINV

FIGURE 15c. BOOTSTRAP CAPACITANCE METHOD

The signal levels in most video applications are 1V p-p or less. Although the HA-5033 was shown with ±15V power supplies in the converter applications, lower power supplies will accommodate these video signal levels. For example, at ±5V power supplies, the HA-5033 can swing ±2V into a 75 ohm load.

The HA-5033 is an excellent high speed line device capable of driving 50 ohm and 75 ohm coaxial cable. These type of drive requirements are common in video circuit design. Figures 15 and 16 illustrate two typical application examples. Figure 15 is an example of a 50 ohm system using the HA-5033 alone. R_m matches the buffer output impedance to the cables characteristic impedance. Depending upon the response required, this resistor may not be necessary. If used, the output voltage will be one half the input voltage.


VIN
VOUT
1V
500mV
10nS
VIN
VOUT
1V
500mV
10nS
+12V
0.1μF
12
RS
6
11
50Ω
RM
RG - 58
VIN
0.1μF
10
-12V
RL
50Ω

POSITIVE PULSE RESPONSE
$T_A = 25^\circ C$
$R_S = 50\Omega$
$R_M = R_L = 50\Omega$
$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = \frac{1}{2} V_{IN}$

NEGATIVE PULSE RESPONSE
$T_A = 25^\circ C$
$R_S = 50\Omega$
$R_M = R_L = 50\Omega$
$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = \frac{1}{2} V_{IN}$

FIGURE 15. VIDEO COAXIAL LINE DRIVER - 50 OHM SYSTEM

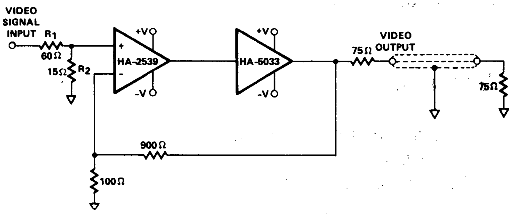

VIDEO SIGNAL INPUT R1
60Ω
15Ω
R2
+V
HA-2539
-V
+V
HA-5033
-V
VIDEO OUTPUT
75Ω
75Ω
900Ω
100Ω

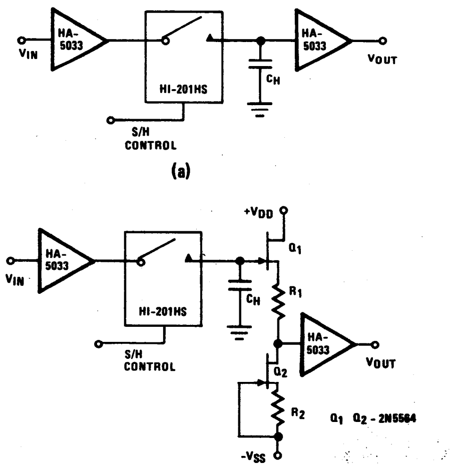
FIGURE 16. VIDEO GAIN BLOCK

Figure 16 illustrates the use of the buffer within the feedback loop of an operational amplifier. This configuration provides additional output current capability for the HA-2539 op amp and gives the designer voltage gain control.

Another application which utilizes the HA-5033's output drive capability is the high speed sample and hold circuit shown in Figure 17. The input buffer provides drive current to the hold capacitor while the output buffer functions as a data line driver. The switching element in this application is the HI-201HS high speed CMOS switch which contributes it's own benefits to the application[9]. Depending upon the application requirements, using the HA-5033 as the output buffer in Figure

17a may not be acceptable. Lab tests have shown that the input bias current of the HA-5033 becomes a factor for low values of hold capacitance (< .01μF) during the hold mode.

A solution is to add a low bias current F.E.T. input stage, as shown in Figure 17b. Q1 acts as a voltage follower and Q2 is a current source. Matching Q1, Q2 and R1, R2 are important considerations in order to minimize offset voltages.

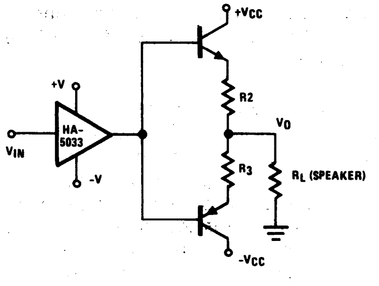


(a)

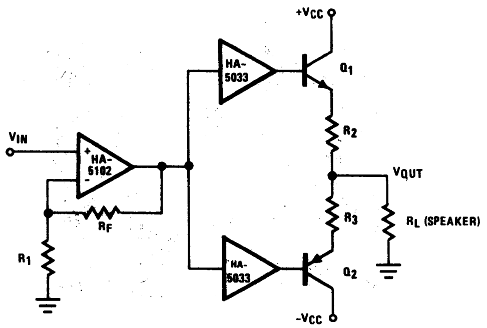
(b)

FIGURE 17a. HIGH SPEED SAMPLE/HOLD (b) MODIFIED OUTPUT BUFFER

When the drive capability of the HA-5033 is insufficient, consider adding an external output stage. Figure 18a illustrates an example where a push-pull complementary output stage has been added to the HA-5033. Although unable to drive the low impedances of speakers, typically 4-8 ohm, the buffer can be used to drive audio output transistors. A variation of this configuration is shown in Figure 18b, where separate buffers individually drive each transistor base. A low noise input stage is provided by the HA-5102.



(a)



(b)

FIGURE 18. AUDIO DRIVERS

A common method of achieving an audio oscillator circuit is to use a transistor or IC amplifier with LC or RC feedback. An alternative technique of generating sinusoidal waveforms, using the HA-5033, is shown in Figure 19. Crystal oscillators offer improved frequency stability over time and temperature. This particular oscillator configuration[10] produces an 18.18 MHz, 2.8V_{p-p} sinusoidal waveform into a 1K ohm load.

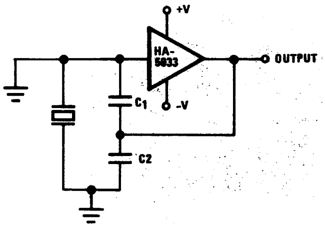


FIGURE 19. CRYSTAL OSCILLATOR: ±V = ±15V, C1 = 12pF, C2 = 39pF, 18MHz QUARTZ CRYSTAL

Conclusion

The HA-5033 is a high performance integrated circuit presently being utilized in a wide variety of applications. This paper has provided additional information to aid designers in applying the HA-5033 video buffer in future applications.

References

1. Thermalloy Semiconductor
   Accessories Catalog
   Thermalloy Inc. Dallas, Texas.
2. Heat Sink/Dissipator Products and
   Thermal Management Guide
   International Electronic Research Corp.
   Burbank, California

3. William L. Hughes, "Television Fundamentals and Standards" Electronic Engineers Handbook ed. Donald G. Fink (McGraw-Hill, 1975) p. 20-3
4. "VITS Analysis for TV Screening" Tektronix Application Note #T900, 1978
5. "Video Facility Testing/Technical Performance Objectives." NTC Report No. 7, Published by the Public Broadcasting Service for the NTC, 1976.
6. Tektronix 1984 Product Catalog.
7. Marconi Instruments 1983-84 Product Catalog.
8. "Monolithic Video A/D Converter", TRW TDC1007J Data Sheet, 1978.
9. "New High Speed Switch Offers Sub-50ns Switching Time" Harris Application Note 543, 1983.
10. Tor Hougen, "Keep Your Oscillator Simple", EDN, June, 1984, p. 236-238.

Further Reading

1. "TV/Video Sync Primer", Hewlett-Packard Product Note 005-1, 1981.
2. Stu Rasmussen and Clifford B. Schrock "Television Operational Measurements, Video and RF for NTSC Systems" Tektronix, 1980.
3. "Electrical Performance Standards for Television Relay Facilities" Electronic Industries Association Standard RS-250-B, 1976.
4. L. E. Weaver, Television Video Transmission Measurements, (London, Marconi Instruments, 1971).
5. F. F. Mazda, ed., Electronic Engineers Reference Book, 5th ed. (London Butterworth, 1982).

Acknowledgements

1. Technical contributions of John Prentice and Robert Junkins.
2. Sales and Technical Staff of Marconi Instruments.

NOTICE: Information contained in application notes is intended solely for general guidance; use of the information for user's specific application is at user's risk.

APP NOTE

FOR YOUR INFORMATIO

No. 549

Harris Analog

THE HC-550X TELEPHONE SUBSCRIBER LINE INTERFACE CIRCUITS (SLIC)

Geoff Phillips, C. Eng., M.I.E.E.

1.0 Introduction

The HC-550X family of telephone subscriber line interface circuits (SLIC) integrate most of the BORSCHT functions of the traditional hybrid and transformer interface circuits onto one chip. The circuits are manufactured in a 200V dielectric isolation (DI) process and together with a secondary protection diode bridge give 1kV of isolation from lightning induced faults between the subscriber loop and the telephone office.

The BORSCHT functions provided are:

- BATTERY FEED WITH LOOP CURRENT LIMITING
- OVERVOLTAGE PROTECTION
- RINGING
- SUPERVISION/SIGNALING
- HYBRID

The HC-5502A is intended for use in systems utilizing single ended tip (positive side) injected ringing and limits the short loop current to 30mA; the HC-5504 is intended for use in ring side (negative side) injected ringing systems and will limit the short loop current to 40mA. It should be noted that the HC-5504 can also be configured to operate in switches employing either of the two single ended ringing methods and in balanced ringing systems.

This note will describe each subfunction of the SLIC and will discuss several system design features, including balance networks and complex impedance matching.

2.0 An Overview of the Basic Phone Loop And Its Environment

Figure 1 illustrates a simplified telephone network. Each subscriber is connected via a 2 wire (2W) loop to a switch office which provides intersubsciber loop switching and signal processing (analog and/or digital).

The SLIC is the primary interface between the 4 wire (4W) (ground referenced) low voltage switch environment and the 2W ("floating") high voltage loop environment.

The loop consists of a wire A (the tip wire), the telephone set or its equivalent, and wire B (the ring wire). A DC voltage is applied across the tip and ring wires at the line card which is housed in the telephone office: The battery is usually a nominal -48V, and is often called the quiet or talking battery. When the telephone is off-hook, a DC path is established around the loop. DC loop current will flow around the loop from tip feed to ring feed. This is called Battery Feed.

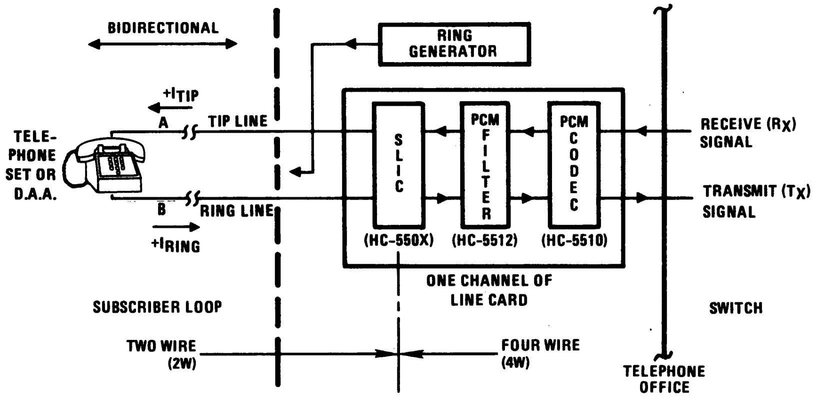

BIDIRECTIONAL
RING GENERATOR
+ITIP
A
TIP LINE
TELE-PHONE SET OR D.A.A.
B
RING LINE
+IRING
SLIC
PCM FILTER
PCM CODEC
(HC-550X)
(HC-5512)
(HC-5510)
RECEIVE (RX) SIGNAL
TRANSMIT (TX) SIGNAL
ONE CHANNEL OF LINE CARD
SUBSCRIBER LOOP
SWITCH
TWO WIRE (2W)
FOUR WIRE (4W)
TELEPHONE OFFICE

FIGURE 1. SIMPLIFIED TELEPHONE NETWORK.

The SLIC must be able to sense this DC current and flag the switch controller: This is referred to as Switch Hook Detection (SHD). It tells the switch controller that the line is busy, and is a supervisory function.

The subscriber set is often located very close to the switch office. Thus, the loop resistance will be very low and the SLIC should incorporate a feedback network that will limit the loop current to a specified maximum to prevent battery power drain and minimize power dissipation at the board level. The HC-550X SLICs sense the loop current and adjust the voltage on the ring side of the line to cause line current saturation.

The telephone can be rung by switching a ring relay to connect a ring generator to the loop. The on-off switching of the relay (cadencing) is controlled by the Ring Command (RC) input which gates the relay driver output. When the user answers the telephone, the ring relay is automatically tripped, the ring command signal is inhibited and the 2W loop is made ready for voice transmission. Voice signals are transmitted onto the loop by directly modulating the DC feed. This AC voice signal is coupled to the users earpiece via a transformer in the telephone set. Voice transmission for the 2W to the 4W system is called the hybrid function. For 2W to 4W transmission, the subscriber talking into his set modulates the resistance of the telephone microphone. This causes AC current in the loop which is sensed by the SLIC and transmitted as a ground referenced voltage signal to the signal processing electronics within the switch.

Subscriber loops are usually measured in terms of loop resistance. The nominal loop length is 1200 ohms. Owing to the length of the lines and their location near power lines, common mode or longitudinal currents are often induced. The SLIC has to distinguish between these noise signals (longitudinal) and the transversal signals, and reject the unwanted longitudinal components: this is a measure of the SLIC's longitudinal balance. The primary noise sources are 60/50Hz power lines, cable cross talk, and R.F. transmissions. The Harris SLICs will accomodate 15mA$_{RMS}$ of noise currents on each side of the loop.

The line is also subjected to lightning strikes. Together with primary and secondary protection networks, the SLIC must withstand 1kV peak of lightning induced energy. In fact, the plastic encapsulated Harris SLIC can withstand a 1kV peak strike with a small signal diode bridge providing voltage clamping, and current steering.

3.0 The Harris HC-550X

The HC-550X family of SLICs are primarily intended for use within Private Branch Exchanges (PBX) although they can be used in the larger switch networks found in Central Offices (C.O.).

Figure 2 shows the functional schematic of the SLIC. The subfunctions to be described are:

A. Line Feed Amplifiers
B. Transversal Amplifiers
C. Loop Current Limiting: Metallic, Fault and Thermal Limiting
D. Ring Trip and Ground Key Detection
E. Spare or Uncommitted Operational Amplifier
F. Logic Network

3.1 Line Feed Amplifiers

The line feed amplifiers are high power op amps, and are connected to the subscriber loop through 300 ohms of feed resistance; the configuration is shown in Figure 3. The feed resistors provide a 600 ohm balanced load for the 2W to 4W transmission, and limit longitudinal currents; the two resistors immediately adjacent to the feed amplifiers function as sense resistors for 2W to 4W transmission and signalling purposes.

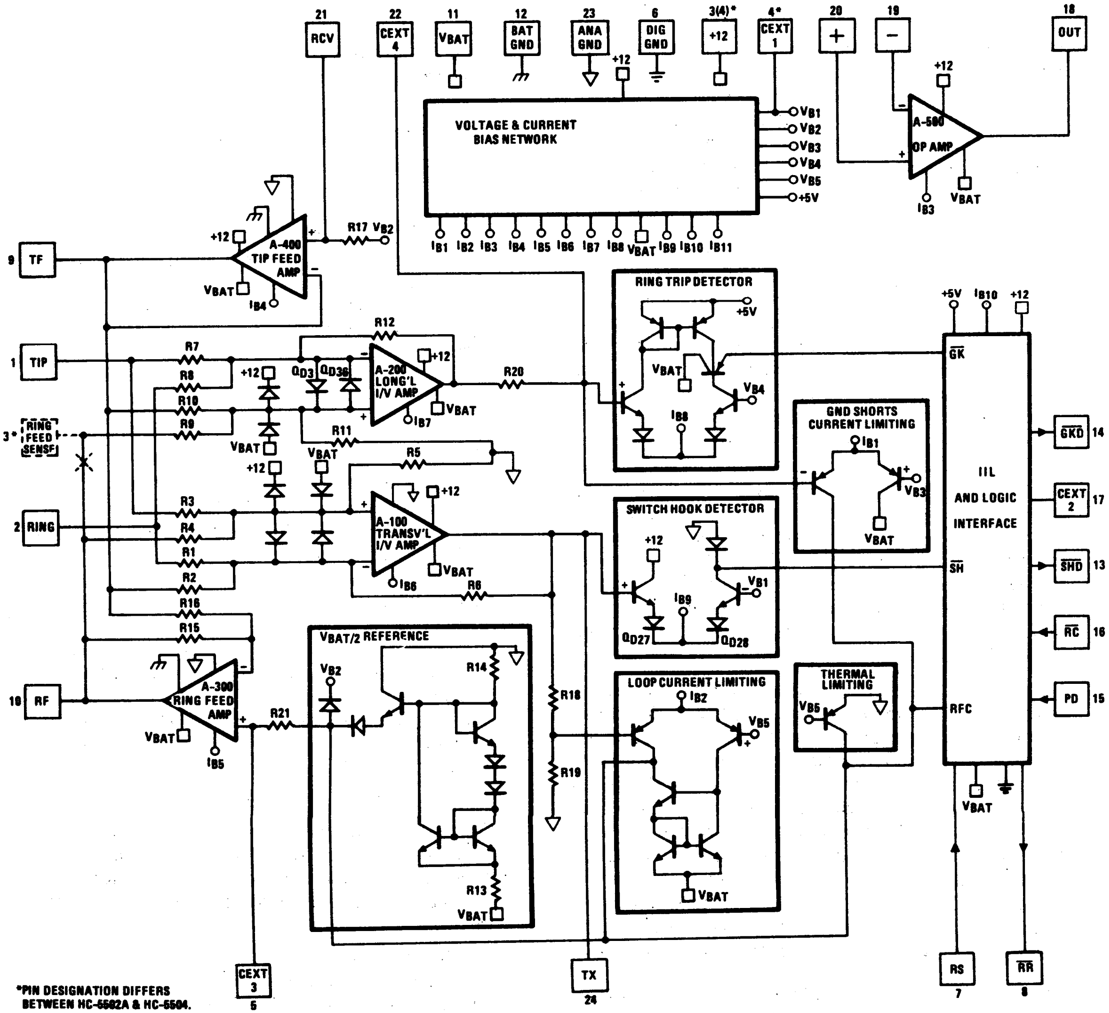
The tip feed amplifier is configured as a unity gain non-inverting buffer. A -4V bias (derived from the negative battery (V_{B-}) in the bias network) is applied to the input of the amplifier. Hence, the tip feed DC level is at -4V. The principal reason for this offset is to accomodate sourcing and sinking of longitudinal noise currents up to 15mA$_{RMS}$ without saturating the amplifier output. The tip feed amplifier also feeds the ring feed amplifier, which is configured as a unity gain inverting amplifier as seen from the TF amplifier. The noninverting input to the RF amp is biased at a VB-/2. Looking into this terminal the amplifier has a noninverting gain of 2. Thus, the DC output at ring feed is:

$$V_{RF}(DC) = (4 + VB-) \text{ Volts}$$

For a -48 volt battery, V_{RF} = -44 volts. Hence, the nominal battery feed across the loop provided by the SLIC is 40 volts. When the subscriber goes off-hook this DC feed causes current (metallic current) to flow around the loop.

The received audio signal V_{RX} from the switch is fed into the tip feed amplifier and appears at the TF terminal. It is also fed through the ring feed amplifier and is inverted. Thus, a differential signal of 2V_{RX} appears across the line: for a 600 ohm line this compensates the 6dB loss due to the 600 ohms of line feed resistance. The V_{RX} signal causes AC audio currents to flow around the loop which are then AC coupled to the earpiece of the telephone set. Figure 4 shows the single ended AC equivalent circuit of the subscriber loop for voice transmission. In the general case the signal design equation for 4W to 2W transmission is given by:

$$V_{LINE} = \left(\frac{Z_{LINE}}{600 + Z_{LINE}}\right) x\ 2V_{RX}$$


21
RCV
22
CEXT 4
11
VBAT
12
BAT GND
23
ANA GND
6
DIG GND
3(4)*
+12
4*
CEXT 1
20
+
19
−
18
OUT
+12
VOLTAGE & CURRENT BIAS NETWORK
VB1
VB2
VB3
VB4
VB5
+5V
IB1 IB2 IB3 IB4 IB5 IB6 IB7 IB8 VBAT IB9 IB10 IB11
A-500 OP AMP
IB3
VBAT
9
TF
A-400 TIP FEED AMP
R17 VB2
IB4
1
TIP
R7
R8
R10
R9
3*
RING FEED SENSE
R12
QD3
QD36
A-200 LONG'L I/V AMP
IB7
R20
R11
R5
2
RING
R3
R4
R1
R2
R16
R15
A-100 TRANSV'L I/V AMP
IB6
R6
RING TRIP DETECTOR
+5V
VB4
IB8
GND SHORTS CURRENT LIMITING
IB1
VB3
SWITCH HOOK DETECTOR
VB1
IB9
QD27
QD28
+5V IB10 +12
GK
IIL AND LOGIC INTERFACE
SH
RFC
GKD 14
CEXT 2 17
SHD 13
RC 16
PD 15
10
RF
A-300 RING FEED AMP
IB5
R21
VBAT/2 REFERENCE
VB2
R14
R13
R18
R19
LOOP CURRENT LIMITING
IB2
VB5
THERMAL LIMITING
VB5
CEXT 3
5
TX
24
RS
7
RR
8

*PIN DESIGNATION DIFFERS BETWEEN HC-5502A & HC-5504.

FIGURE 2. SLIC FUNCTIONAL SCHEMATIC.

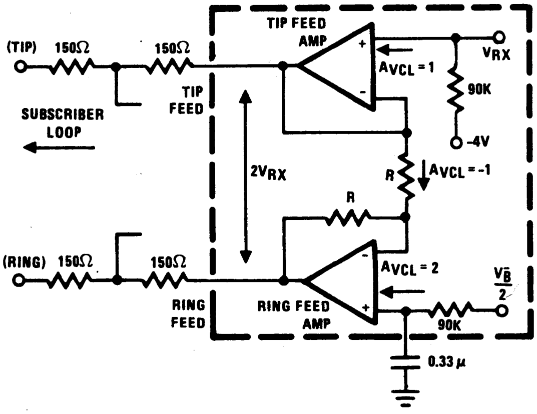

(TIP) 150Ω
150Ω
TIP FEED
AMP
AVCL = 1
VRX
90K
-4V
SUBSCRIBER LOOP
TIP FEED
2VRX
R
R
AVCL = -1
(RING) 150Ω
150Ω
AVCL = 2
VB/2
RING FEED
RING FEED AMP
90K
0.33μ

FIGURE 3. LINE FEED AMPLIFIERS.

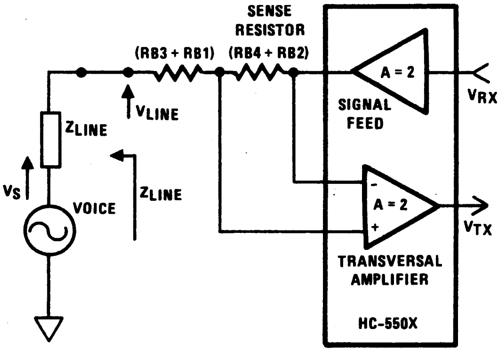

SENSE RESISTOR
(RB3 + RB1)
(RB4 + RB2)
A = 2
SIGNAL FEED
VRX
VLINE
ZLINE
VS
VOICE
ZLINE
A = 2
VTX
TRANSVERSAL AMPLIFIER
HC-550X

FIGURE 4. SINGLE ENDED AC SIGNAL EQUIVALENT CIRCUIT.

3.2 The Transversal Amplifier (TA)

Whereas the feed amplifiers perform the 4W to 2W transmission function, the transversal amplifier acts as the 2W to 4W hybrid. The TA is a summing amplifier configured to reject common mode signals. It will thus reject 2W common mode signals. Figure 4 shows the single ended signal transmission path. Given below is the design equation of the 2W to 4W signal transmission. It can be seen that RB2 and RB4 act as loop current sense resistors, and that the voice signal output of the amplifier is a function of the differential voltages appearing across RB2 and RB4.

Thus, the transversal amplifier also has a DC output proportional to the metallic current in the loop. The output voltage is given by:

$$V_{TX} = 2(I_{TIP} + I_{RING})\ (R_{B2} + R_{B4})$$

where I_{TIP} and I_{RING} are assumed positive as indicated in Figure 1. This DC level is used as an input to a comparator whose output feeds into the logic circuitry as SH. This signal is used to gate SHD.

Voice signals on the loop are transformed by the TA into ground referenced signals as shown by the above equations. Since the TA output has a DC offset it is necessary to AC couple the output to any external circuitry. Note, that during 4W to 2W transmission, the transversal amplifier will have an audio signal at its output proportional to the 4W audio receive signal and the loop's equivalent AC impedance. This is called the transhybrid return, and must be cancelled (or balanced) out to prevent an echo effect. This is discussed more fully in Section 4 under Transhybrid Balancing.

3.3 Loop Current Limiting

The nominal loop length is equivalent to an 1800 ohm load across the feed amplifiers However, on a short loop the line resistance often approaches zero. Thus, a need exists to control the maximum DC loop current that can flow around the loop to prevent an excessive current drain from the system battery. This limit is typically specified between 30mA and 40mA for general PBX applications. Figure 5 depicts the feedback network that modifies the RF voltage as a function of metallic current. Figure 6 illustrates the loop current characteristics as a function of line resistance.

As indicated above, the TA has a DC voltage output directly proportional to the loop current. This voltage level is scaled by R19 and R18. The scaled level forms the 'Metallic' input to one side of a Transconductance Amplifier. The reference input to this amplifier is

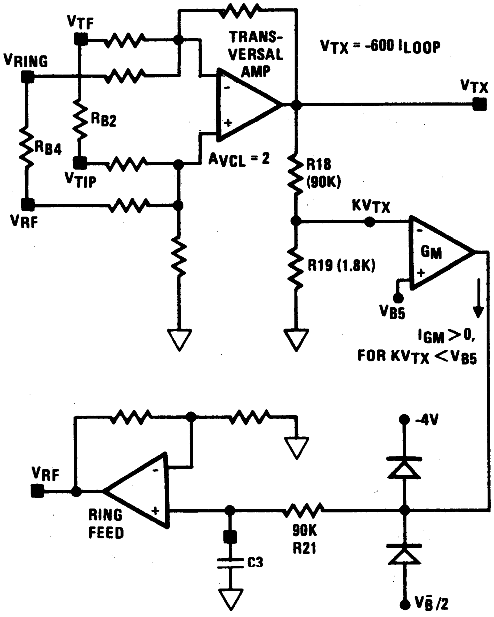

VTF
VRING
TRANS-VERSAL AMP
VTX = -600 ILOOP
VTX
RB2
RB4
AVCL = 2
VTIP
R18 (90K)
VRF
KVTX
GM
R19 (1.8K)
VB5
IGM > 0, FOR KVTX < VB5
-4V
VRF
RING FEED
90K R21
C3
VB/2

FIGURE 5. LOOP CURRENT LIMIT CONTROL.

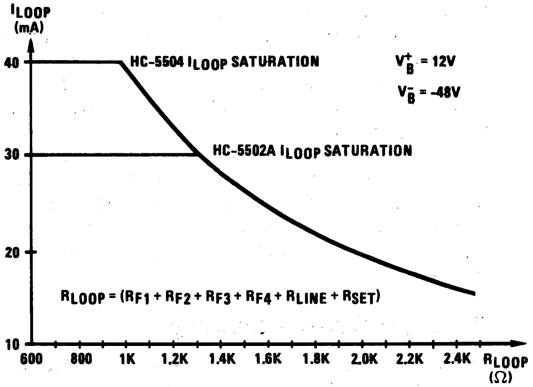


FIGURE 6. DC LOOP CURRENT CHARACTERISTICS.

generated in the bias network, and is equivalent to 30mA or 40mA loop current, typically, for the HC-5502A and HC-5504, respectively. When the metallic input exceeds the set reference level, the transconductance amplifier sources current. This current will charge C3 in positive direction causing the RF (Ring Feed) voltage to approach the TF (Tip Feed), effectively reducing the battery feed across the loop which will limit the DC loop current. C3 will continue to charge until an equilibrium level is attained at $I_{LOOP} = I_{LOOP}$ MAXmA. The time constant of this feedback loop is set by R21 (90K ohm) and C3 which is nominally 0.33μF.

The RF voltage level is also modified to reduce or control loop current during ring line faults (e.g. ground or power line crosses), and thermal overload. Figure 2 illustrates this. It can be seen that the thermal and fault current circuitry works in parallel with the transconductance amplifier.

3.4 Longitudinal Amplifier

The longitudinal amplifier is an op amp configured as a closed loop differential amplifier with a nominal gain of 0.1 (HC-5504) or 0.581 (HC-5502A). The output is a measure of any imbalance between I_{TIP} and I_{RING} as described in Figure 1. The transfer function of this amplifier is given by:

$$V_{LONG} = K(I_{TIP} - I_{RING})150$$

Where K is the gain factor of the amplifier. The gain factor is much less than one since ring voltage (up to $150V_{peak}$) can appear at the Ring or Ring Feed Sense terminals and are attenuated to protect the amplifier.

The longitudinal amplifier's principle functions are Ring Trip Detection (RTD) and Ground Key Detection (GKD). GKD provides a means for the subscriber to flag a PBX attendant and is used extensively in Europe: The ring line is grounded at the telephone set via a push switch incorporated within the telephone. This causes a DC current imbalance between the tip and ring sides of the loop which gives rise to a negative voltage at the output of the longitudinal amplifier. The output of the amplifier after being filtered by R20 and C4 to attenuate AC signals is fed into a detector whose output GK gates the necessary logic to drive GKD or inhibit the ring relay driver to remove ringing signals from the line in an off-hook condition. In order to prevent false ground key owing to line noise or during ring trip, the internal GKD logic is delayed via C2. An internal current source of 5μA has to charge C2 up to a 5V level before allowing the ground key signal to propagate. Thus, for C2 = 0.15μF, a delay of 150ms is established.

Ringing the line and Ring Trip Detection are discussed more fully in Section 4.

3.5 Uncommitted Op Amp

An uncommitted op amp is provided on the chip. This is a standard op amp with an output swing of ±5V. It is primarily intended to be used to balance the transhybrid return signal discussed in Section 3.2 above. The amplifier has an offset voltage of 10mV; an open loop gain of 66dB; a GBW product of 2MHz; slews at 1V/μs typically, and has a ±2mA output current drive capability.

3.6 The Logic Network

The logic network utilizes I^2L logic. All external inputs and outputs are LS TTL compatible: the relay driver is an open collector output that can sink 60mA with a V_{CE} of 1V.

Figure 7 is a schematic of the combination logic within the network. The external inputs RC (Relay Control) and PD (Power Denial) allow the switch controller to ring the line or deny power to the loop, respectively. The Ring Synchronization input (RS) facilitates switching of the ring relay near a ring current zero crossing in order to minimize inductive kick-back from the telephone ringer.

The internal inputs SH and GK control ring trip and provide supervisory flags to the system controller via the Switch Hook Detect (SHD) and Ground Key Detect (GKD) outputs.

4.0 Designing with the Harris SLIC

General application circuits for the HC-5502A and HC-5504 SLICs are given in Figures 8 and 9. In this section, several specific design and application areas will be discussed:

A. Ringing the Line

B. Power Denial

C. Transhybrid and Longitudinal Balance

D. Complex Impedance Matching

E. Surge Protection

4.1 Ringing The Line

The HC-5502A is used for tip injected ringing (also called single ended ground referenced ringing), and the HC-5504 is used for ring injected or single ended

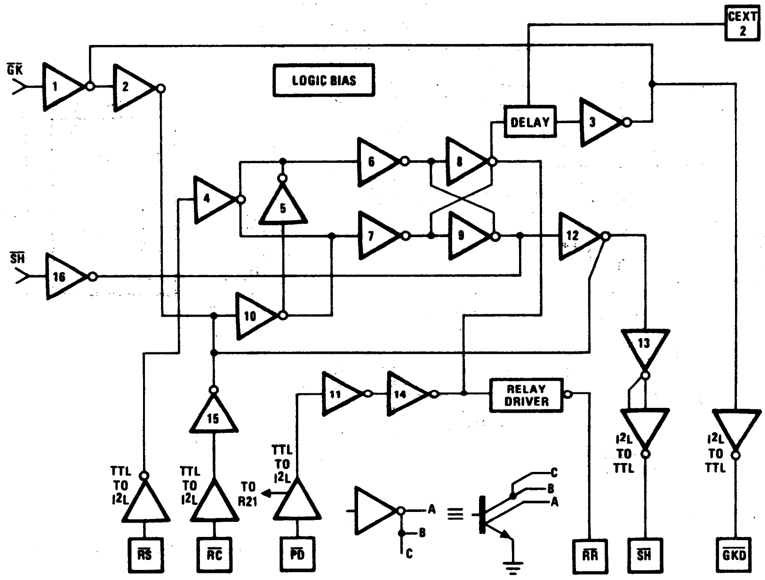
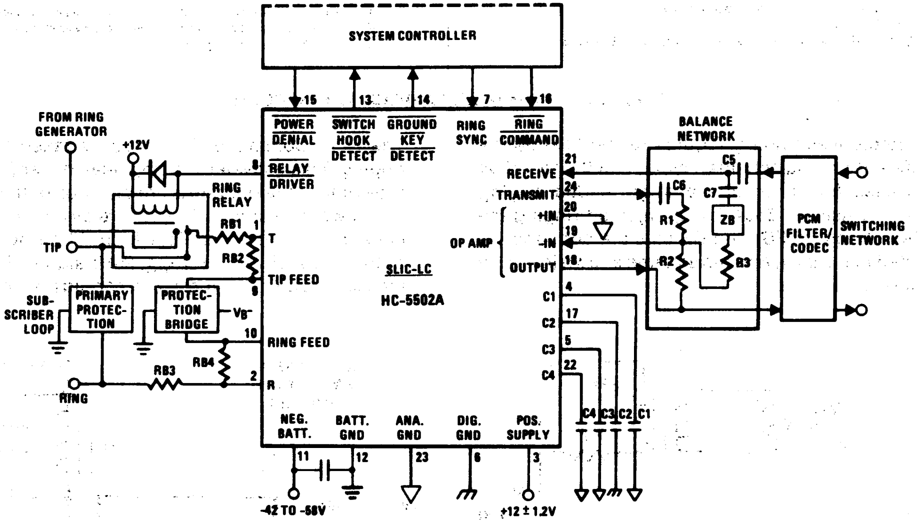

CEXT 2
GK
LOGIC BIAS
DELAY
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
SH
RELAY DRIVER
I2L TO TTL
I2L TO TTL
TTL TO I2L
TTL TO I2L
TTL TO I2L
TO R21
A
B
C
≡
C
B
A
RS
RC
PD
RR
SH
GKD

FIGURE 7. HC-5502A/04 LOGIC GATE SCHEMATIC.


SYSTEM CONTROLLER
15
13
14
7
16
POWER DENIAL
SWITCH HOOK DETECT
GROUND KEY DETECT
RING SYNC
RING COMMAND
FROM RING GENERATOR
+12V
RING RELAY
8
RELAY DRIVER
RB1
1
T
TIP
RB2
9
TIP FEED
SUB-SCRIBER LOOP
PRIMARY PROTECTION
PROTECTION BRIDGE
VB-
10
RING FEED
RB3
RB4
2
R
RING
SLIC-LC
HC-5502A
21
RECEIVE
24
TRANSMIT
20
+IN
OP AMP
19
-IN
18
OUTPUT
4
C1
17
C2
5
C3
22
C4
BALANCE NETWORK
C5
C6
C7
R1
ZB
R2
R3
PCM FILTER/CODEC
SWITCHING NETWORK
C4
C3
C2
C1
NEG. BATT.
BATT. GND
ANA. GND
DIG. GND
POS. SUPPLY
11
12
23
6
3
-42 TO -58V
+12 ± 1.2V

TYPICAL COMPONENT VALUES

C1 = 0.5µF ①

C2 = 0.15µF, 10V

C3 = 0.3µF, 30V

C4 = 0.5µF to 1.0µF, ± 10%, 20V (Must be nonpolarized)

C5 = 0.5µF, 20V

C6 = C7 = 0.5µF (10% Match Required) ②, 20V

C8 = 0.01µF, 100V

R1 → R3 = 100kΩ (0.1% Match Required, 1% Absolute Value), ZB = 0 for 600Ω Terminations ②

RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required, 1% Absolute Value)

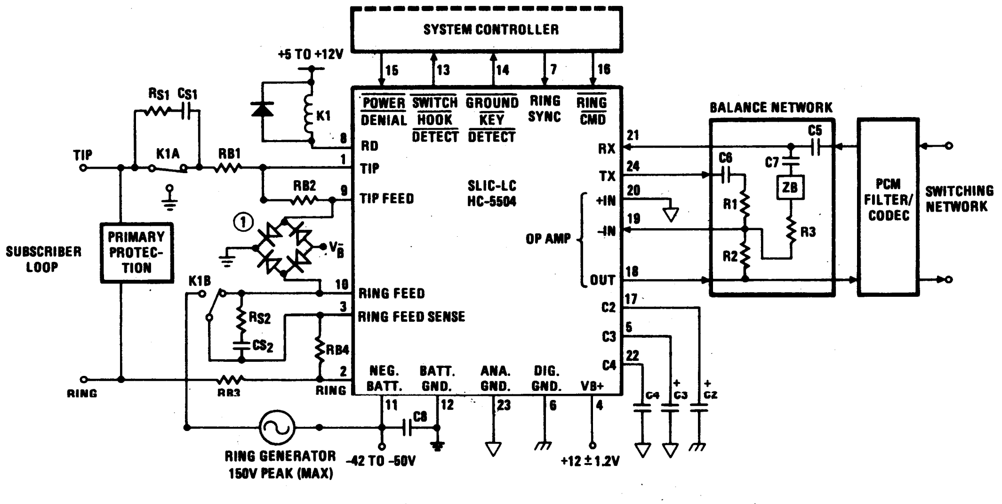
R_S = 1KΩ, C_S = 0.1µF, 200V Typically, Depending on V_{RING} and Line Length.

NOTES:

① C1 is an optional capacitor used to improve +12V supply rejection. This pin must be left open if unused.

② To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6 - R1 and R2 and C7 - ZB - R3, to match in impedance to within 0.3%. Thus, if C6 and C7 are 1µF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -22V step when the loop is closed and that too large a value for C6 may produce an excessively long transient at the op amp output to the PCM filter/CODEC. A 0.5µF and 100KΩ gives a time constant of 50msec.

FIGURE 8. HC-5502A LINE APPLICATION CIRCUIT.


SYSTEM CONTROLLER
+5 TO +12V
15
13
14
7
16
RS1 CS1
K1
8
TIP
K1A
RB1
1
RB2
9
POWER DENIAL
SWITCH HOOK DETECT
GROUND KEY DETECT
RING SYNC
RING CMD
RD
TIP
TIP FEED
SLIC-LC
HC-5504
①
V_B^-
SUBSCRIBER LOOP
PRIMARY PROTECTION
K1B
10
RING FEED
3
RING FEED SENSE
RS2
CS2
RB4
2
RING
RB3
RING
NEG. BATT.
BATT. GND.
ANA. GND.
DIG. GND.
VB+
11
12
23
6
4
C8
RING GENERATOR
150V PEAK (MAX)
-42 TO -50V
+12 ± 1.2V
BALANCE NETWORK
21
RX
24
TX
20
+IN
19
-IN
OP AMP
18
OUT
17
C2
5
C3
22
C4
C5
C6
C7
ZB
R1
R2
R3
PCM FILTER/ CODEC
SWITCHING NETWORK
C4
C3
CZ

TYPICAL COMPONENT VALUES

C2 = 0.15μF, 10V
C3 = 0.3μF, 30V
C4 = 0.5μF, 20V
C5 = 0.5μF, 20V
C6 = C7 = 0.5μF (10% Match Required) ②
C8 = 0.01μF, 100V
R1 = R2 = R3 = 100k (0.1% Match Required, ZB = 0 for 600Ω Terminations ②
RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required)
R_{S1} = R_{S2} = 1KΩ Typically
C_{S1} = C_{S2} = 0.1μF, 200V typically, depending on V_{RING} and Line Length.

NOTES:

① Secondary protection diode bridge recommended is an MDA 220 or similar.

② To obtain the specified transhybrid loss of 40dB it is necessary for the 3 legs of the balance network, C6 - R1 and R2 and C7 - ZB - R3, to match in impedance to within 0.3%. If C6 and C7 are 1μF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -22V step when the loop is closed. Too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC. A 0.5μF and 100kΩ gives a time constant of 50msec. The uncommited op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.

FIGURE 9. HC-5504 LINE APPLICATION CIRCUIT.

battery referenced ringing. Figures 10 and 11 show the two different ringing schemes. Note, that the HC-5504 can be used for either of the single ended ringing schemes: to use the 5504 for tip injected ringing the Ring Feed Sense (RFS) and RF pins are permanently connected externally, and the scheme shown in Figure 10 adopted.

The Ring Command (RC) input is taken low during ringing. This activates the ring relay driver (RR) output providing the telephone is not off-hook or the line is not in a power denial state. The ring relay connects the ring generator to the subscriber loop. The ring generator output is usually an $80V_{RMS}$, 20Hz signal. For use with the Harris SLIC, the ring signal should not exceed 150V

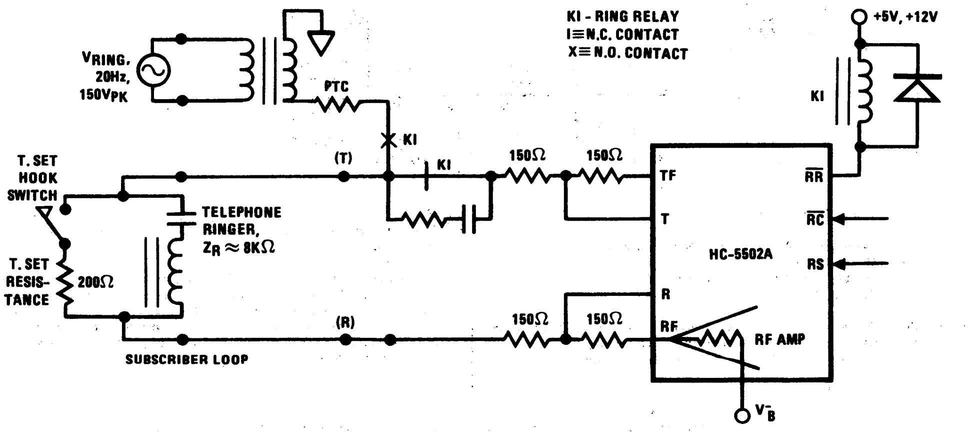
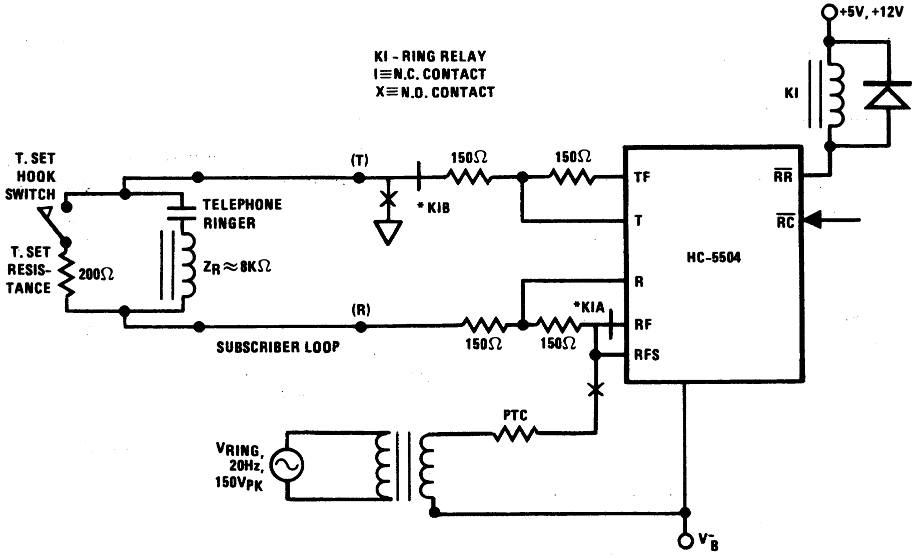

V_{RING}, 20Hz, $150V_{PK}$
PTC
KI - RING RELAY
I≡N.C. CONTACT
X≡N.O. CONTACT
+5V, +12V
KI
KI
(T)
KI
150Ω
150Ω
T. SET HOOK SWITCH
TELEPHONE RINGER, $Z_R \approx 8K\Omega$
T. SET RESISTANCE
200Ω
(R)
150Ω
150Ω
SUBSCRIBER LOOP
TF
T
R
RF
RR
RC
RS
HC-5502A
RF AMP
V_B^-

FIGURE 10. HC-5502A TIP INJECTED SINGLE ENDED RINGING.



*RC SNUBBER PLACED ACROSS NC CONTACTS

FIGURE 11. HC-5504 RING INJECTED SINGLE ENDED RINGING.

peak. Since the telephone ringer is AC coupled, only ring current will flow. For the HC-5502A SLIC, the ring current is sunk by the ring feed amplifier output stage whereas for the HC-5504 the ring path flows directly into V_{B-} via a set of relay contacts. The high impedance terminal RFS exists on the HC-5504 so that the low impedance RF node can be isolated from the hot end of the ring path in the battery referenced ring scheme.

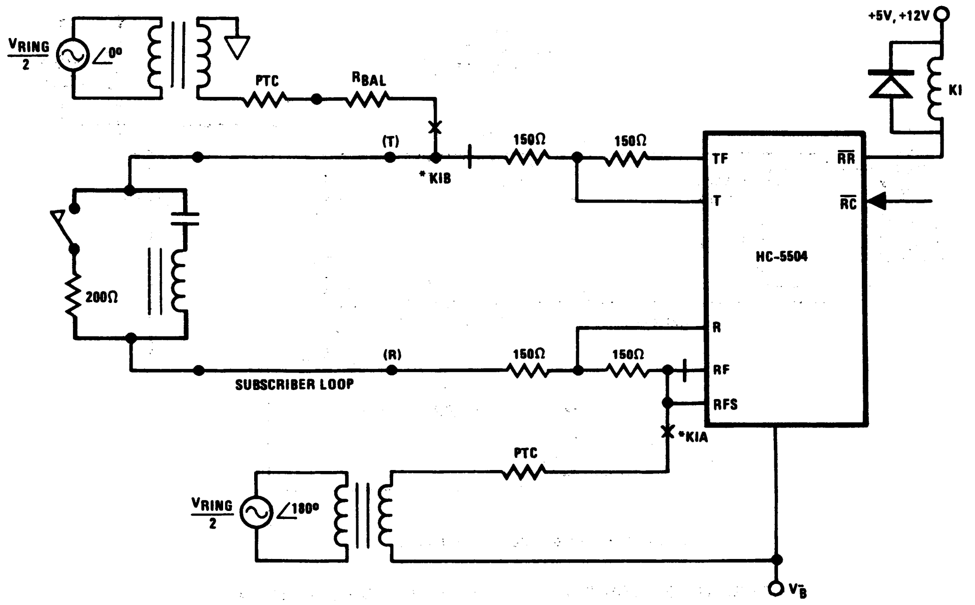
The AC ring current flowing in the subscriber circuit will be sensed across RB4, and will give rise to an AC voltage at the output of the longitudinal amplifier. R19 and C4 attenuate this signal before it reaches the ring trip detector to prevent false ring trip. C4 is nominally set at 0.47μF but can be increased towards 1μF for short lines or if several telephones are connected in parallel across the line in order to prevent false or intermittent ring trip.

When the subscriber goes off-hook, a DC path is established between the output winding of the ring generator and the battery ground or V_{B-} terminal. A DC longitudinal imbalance is established since no tip feed current is flowing through the tip feed resistors. The longitudinal amplifier output is driven negative. Once it exceeds the ring trip threshold of the ring trip detector, the logic circuitry is driven by GK to trip the ring relay establishing an off-hook condition such that SHD will become active as loop metallic current starts to flow.

In addition to its ability to be used for tip or ring injected systems, the 5504 can also be configured for systems utilizing balanced ringing. Figure 12 shows such an application. The main advantage of balanced ringing is that it tends to minimize cross coupling effects owing to the differential nature of the ring tone across the line.

Figure 13 illustrates the sequence of events during ring trip with ring synchronization for a tip injected ring system. Note, that owing to the 90° phase shift introduced by the low pass filter (R19, C4) the RS pulse will occur at the most negative point of the attenuated ring signal that is fed into the ring trip detector. Hence, when DC conditions are established for RTD, the AC component actually assists ring trip taking place. For a ring side injected ring system, the RS pulse should occur at the positive zero crossing of the ring signal as it appears at RFS. If ring synchronization is not used, then the RS pin should be held permanently to a logic high of 5V nominally: ring trip will occur asynchronously with respect to the ring voltage. Ring trip is guaranteed to take place within three ring cycles after the telephone going off-hook.

It is recommended that an RC snubber network is placed across the ring relay contacts to minimize inductive kick-back effects from the telephone ringer. Typical values for such a network are shown in Figure 9.



* RC SNUBBER PLACED ACROSS N.C. CONTACTS

FIGURE 12. HC-5504 BALANCED RINGING CONFIGURATION.

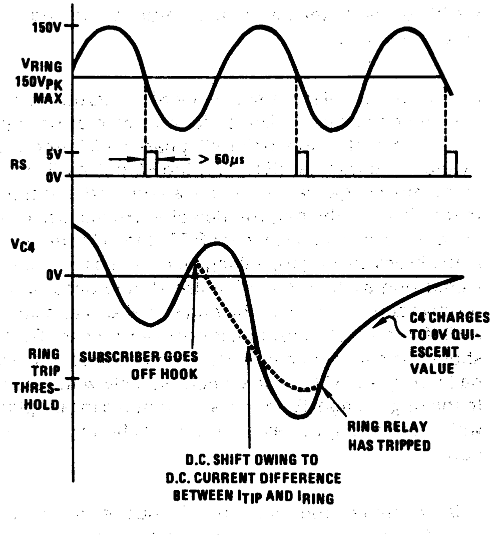


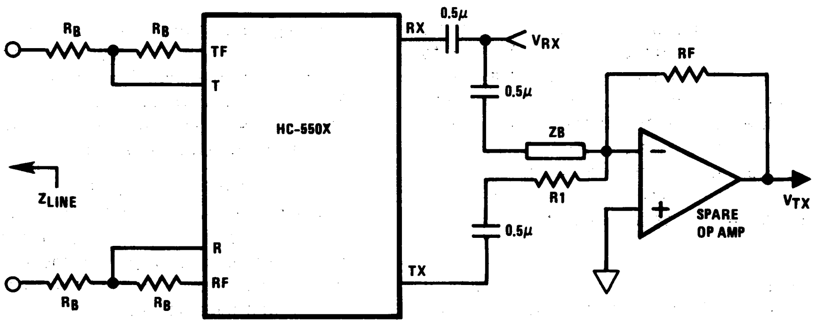
FIGURE 13. RING TRIP SEQUENCE.

4.2 Power Denial (PD)

Power denial limits power to the subscriber loop: it does not power down the SLIC, i.e. the SLIC will still consume its normal on-hook quiescent power during a power denial period. This function is intended to "isolate" from the battery, under processor control, selected subscriber loops during an overload or similar fault status.

If PD is selected, the logic circuitry inhibits RC and switches in a current source to C3. The capacitor charges up to a nominal -3.5V at which point it is clamped. Since TF is always biased at -4V, the battery feed across the loop is essentially zero, and minimum loop power will be dissipated if the circuit goes off-hook. No signalling functions are available during this mode.

After power denial is released (PD = 1), it will be several hundred milliseconds (300ms) before the RF output reaches its nominal battery setting. This is due to the RC time constant of R21 and C3.



$Z_B = R1 \left(\frac{4R_B + Z_L}{8R_B}\right)$ WHERE $R_B = 150$

$\therefore$ IF $Z_L = 4R_B$ (i.e. 600Ω LINE)
THEN $Z_B = R1$

IN GENERAL CASE IF R1 IS SCALED TO $R1 = 8KR_B$

$Z_B = K(4R_B + Z_L)$ WHERE $K = 10, \rightarrow 100$

FIGURE 14. SLIC TRANSHYBRID BALANCE EQUATIONS.

4.3 Transhybrid Loss And Longitudinal Balance

During 4W to 2W transmission, the 4W signal is returned to the transmit output: this is called transhybrid return: it is not a reflection from the line as it will only occur if the loop is closed. In order to prevent echo and instability in the switch, this returned signal must be balanced out before it reaches the filter/CODEC. The level of the returned signal is given below, and a balancing network utilizing the on-chip spare op amp is indicated in Figure 14. Since the returned received signal's amplitude and phase are a function of the line's A.C. impedance, the balance network is a function of the same.

For a resistive line, the two arms of the balance network (Figure 14) are also resistive. In the simplest case, for a 600 ohm system, the two parts of the summing network have equi-resistance values. For a transhybrid balance greater than 36dB, component tolerances of ±0.5% are recommended. Both arms of the summing network are capacitively coupled since the TA and TF amplifiers have output and input D.C. biases, respectively. The values of the capacitors are chosen to prevent degradation of the audio frequency response. For capacitive values of 0.5μF, components with tolerances of 10% can be used since at voice band frequencies the reactance of the capacitor has minimal effect on the impedance of the balance network.

The transhybrid returned signal is given by:

$$V_{TX} = -V_{RX} \left(\frac{4R}{2R + Z_L}\right)$$

where $R = (R_{B1} + R_{B2}) = (R_{B3} + R_{B4})$, and

Z_L = Line Impedance

For the balance network, the general equation is given by:

$Z_B = 2R + Z_L$ with $R1 = 4R$ in Figure 14.

A full derivation of the balance equation is given in Appendix A. A measure off this balance is known as transhybrid loss. For a 600 ohm resistive line, a balance of 40dB at 1kHz is attainable. In practice owing to variations in lines and telephone sets the balance is usually lower than in the ideal case: A balance in the order of 25dB will often be measured and accepted.

By switching out the balance network, it is possible for the controller to conduct loop back tests providing the loop can be closed via a test relay in the line card.

Longitudinal balance is equivalent to common mode rejection ratio. Looking into the line card tip and ring terminals towards the SLIC, the 2W balance is a function of the impedance match between tip and ring to ground. The 4W balance is a funciton of the 2W balance, and the matching of the feedback resistor ratios around the transversal amplifier. (The TA itself must also exhibit a CMRR in excess of the required longitudinal balance.) The SLIC user can only control the matching of the feed resistors. For a nominal 60dB of rejection, these must match within 0.1%. The on-chip resistors are thin film SiCr resistors and are matched within 0.1%. The amplifier has a CMRR of 70dB giving a typical 4W balance of 60dB.

4.4 Complex Impedance Matching

The SLIC is usually used in systems that have a line characteristic impedance of 600 ohms resistive. Thus, the 4 × 150 ohms feed resistors present a balanced 600 ohms load to the line. If the characteristic impedance of the line varies from 600 ohms but remains resistive, then this can be compensated for by increasing or decreasing the value of R_{B1} and R_{B3}. For example, if the line is defined as 900 ohms resistive, then R_{B1} and R_{B3} could be increased to 300 ohms each and the line will be matched. The increase in feed resistance could impact the DC performance on long lines.

In case of lines having a complex characteristic impedance the SLIC circuit can be configured to adequately match the line. Figure 15 shows a typical equivalent line impedance as defined in many European countries. Figure 16 illustrates the circuitry required to match and balance such a line. The component design equations are given below. A qualitative description is given of the circuit to explain its operation; a full mathematical derivation is given in Appendix A.

For the equivalent impedance shown in Figure 15, it can be seen that at low frequencies, the impedance will increase and become more resistive as the voice frequency increases, the reactance of C_L decreases, thus the line impedance will also decrease. In order to match the line impedance, a feedback network is required that provides low frequency positive feedback and high frequency negative feedback. The scheme of Figure 16 does this. An additional op amp is required to realize the circuit.

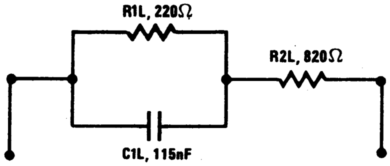


FIGURE 15. TYPICAL EQUIVALENT COMPLEX LINE IMPEDANCE.

The degree of match over the voice band is a function of the R and C component tolerances and the degree of approximation to their theoretical values. The curves in Figure 17 show typical matching characteristics. The objective is to maximize the 2W return loss. Some values are indicated in Figure 17.

Resistor RS in Figure16 is added to ensure circuit stability. A nominal value of 300 ohms is advised which will not effect the A.C. performance of the circuit. Capacitor CF can be used to optimize the transmit signal's frequency response. This is caused by non-realization of ideal component values. CF adds a pole to the circuit which compensates this non-flat response. (See Figure 18). For complex impedance applications a certain amount of circuit optimization will be required by the user in order to obtain an adequate 2W return loss performance and a satisfactory transmit frequency response.

As indicated, the above method for matching complex lines requires an additional op amp to the SLICs on board op amp. It also requires several capacitors whose values are often non-standard. Also, tightly toleranced capacitors are expensive. A second method exists to match the line, it minimizes the number of capacitors to the number of capactive elements within the line's equivalent impedance model. (There is usually one capacitive element.) Assuming just one capacitor in the line impedance network, the capacitor's value can be scaled to a standard value which will improve the performance of the circuit. A

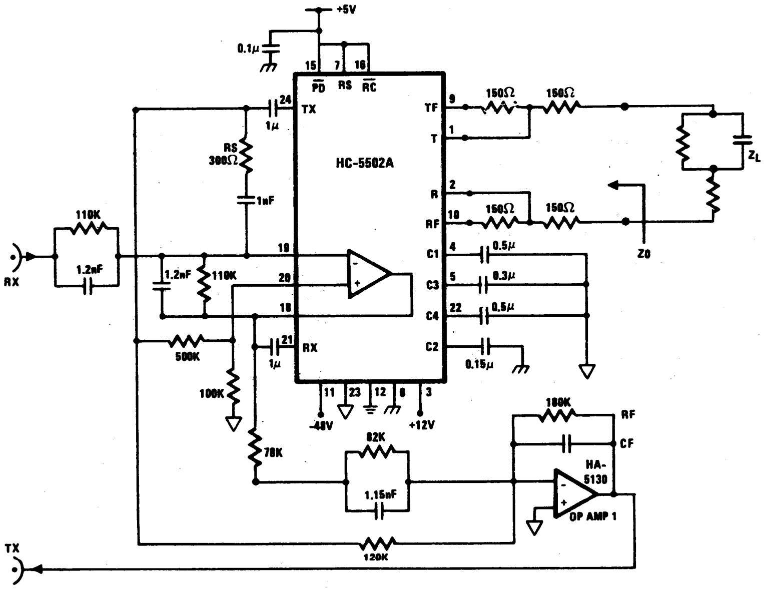


FIGURE 16. COMPLEX LINE IMPEDANCE TRANSFORM CIRCUIT HC-5502A.

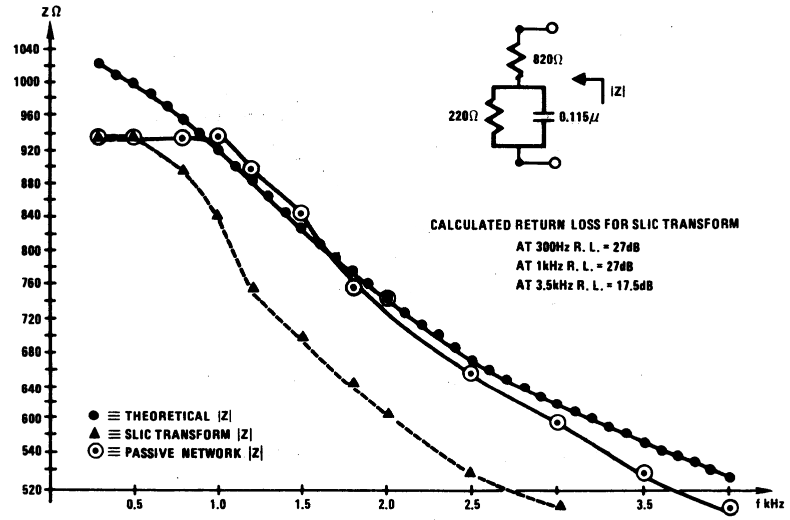


FIGURE 17. |Z| vs. FREQUENCY

second additional external op amp is necessary; however, the ease of implementation and the performance attained could warrant this overhead. The mathematical derivation of this method is given in Appendix B together with an application circuit.

4.5 Line Fault Protection

The subscriber loop can exist in a very hostile electrical environment. It is often in close proximity to very high voltage power lines, and can be subjected to lightning induced voltage surges. The SLIC has to provide isolation between the subscriber loop and the telephone office. Methods for dealing with longitudinally induced power frequency currents and excessive DC line current have been discussed.

The most stringent line fault condition that the SLIC has to withstand is that of the lightning surge.

The Harris monolithic SLIC in conjuction with a simple low cost diode bridge can achieve up to 1KV of isolation between the loop and switch office. The level of isolation is a function of the packaging technology and geometry together with the chip layout geometries. One of the principal reasons for using DI technology for fabricating the SLIC is that it lends itself most readily to manufacturing monolithic circuits for high voltage applications.

Figures 8 and 9 show general application circuits for the HC-5502A and HC-5504 SLICs. A secondary protection diode bridge is indicated which protects the feed amplifiers during a fault. Figure 19 illustrates more clearly the fault current paths during a lightning or transient high voltage strike. Most line systems will have primary protection networks. They often take the form of a carbon block or arc discharge device. These limit the fault voltage to 500V - 1000V peak before it reaches the switch line cards. Thus when a transient high voltage fault has occurred, it will be transmitted as a wave front down the line. The primary protection network limits the voltage to 500V to 1000V. The attenuated wave front will continue down the line towards the SLIC. The feed amplifier outputs appear to the surge as very low impedance paths to the system battery. Once the surge reaches the feed resistors, fault current will flow into or out of the feed amplifier output stages until the relevant protection diodes switch on. Bench measurements have indicated peak fault currents of up to 150mA into and out of the SLIC during the finite turn on time of the diode bridge. Once the necessary diodes have started to conduct all the fault current will be handled by them. The geometry of the SLIC and its package has been designed to withstand the full rated peak fault voltage at its tip (T) and ring (R) terminals: for ceramic packages this is 500V peak, and for plastic (or epoxy) packaged SLICs this is 1000V peak. The circuits are rated against standard lightning characteristics defined by Figure 20. The ceramic package contains an air gap whereas the plastic packages contain no void. The dielectric constant of air is lower than that of the epoxy and it is this which breaks down at lower voltages than the plastic compound.

If the user wishes to characterize SLIC devices under simulated high voltage fault conditions on the bench, he should ensure that the negative battery power supply has sufficient current capability to source the negative peak fault current and low series inductance. If this is not the case, then the battery supply could be pulled more negative and destroy the SLIC if the total (V_{B+} + V_{B-}) voltage across it exceeds 80V.

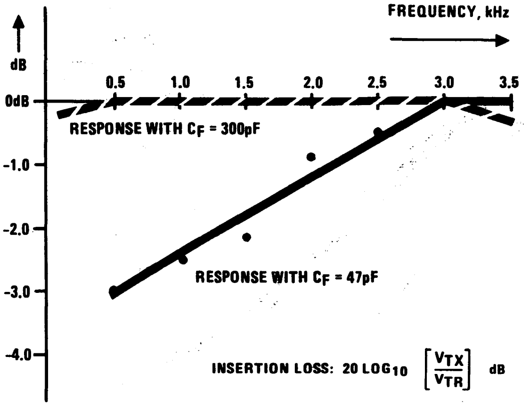


FIGURE 18. TWO WIRE - FOUR WIRE TRANSMISSION:

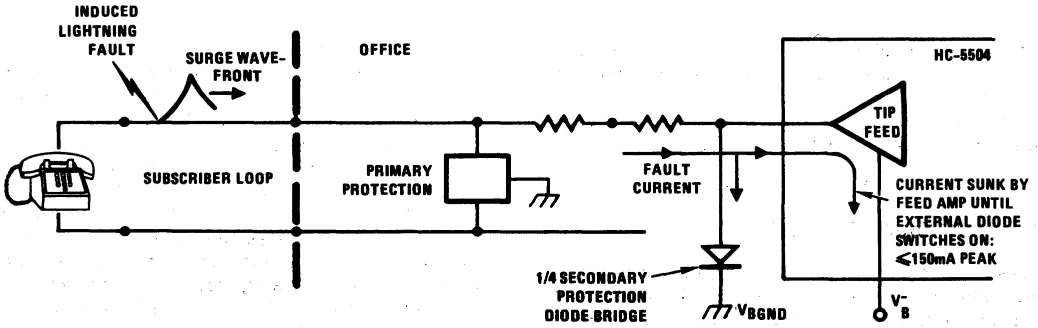

INDUCED
LIGHTNING
FAULT
SURGE WAVE-FRONT
OFFICE
HC-5504
TIP FEED
SUBSCRIBER LOOP
PRIMARY PROTECTION
FAULT CURRENT
CURRENT SUNK BY FEED AMP UNTIL EXTERNAL DIODE SWITCHES ON: ≤150mA PEAK
1/4 SECONDARY PROTECTION DIODE BRIDGE
V_{BGND}
V_B^-

FIGURE 19. FAULT PROTECTION

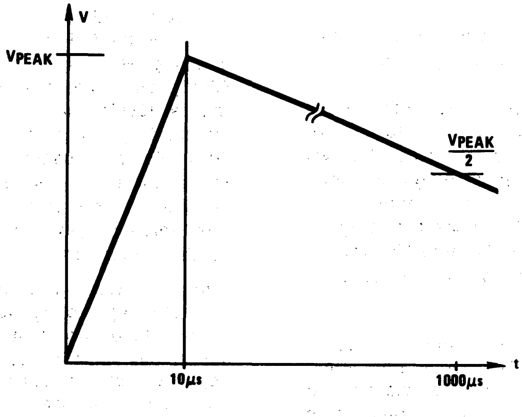


FIGURE 20. SIMULATED LIGHTNING STRIKE WAVEFORM.

APPENDIX A

BALANCING AND IMPEDANCE MATCHING THE HC-550X SLIC

1. Evaluating balance network for HC-5502A/HC-5504 SLIC.

   The Figure A1 schematic illustrates the general 4W to 2W signal implementation of a SLIC IC.

   In order to achieve transhybrid rejection of the Rx signal, the op amp configuration needs to be implemented in order to subtract out any portion of the Rx signal that might appear at the TX terminal of the SLIC. The value of Z_B is a function of Z_L; a general derivation of Z_B is given in Figure A2. Consider the single ended signal path equivalent circuit of the HC-550X.

   For V_{RX} only we require $V_T = 0$.

$$V'_{TX} = \left(\frac{R}{2R + Z_L}\right) \times 2V_{RX} \quad ; \quad V_{TX} = \left(\frac{-4R}{2R + Z_L}\right) \times V_{RX}$$

For $V_T = 0$ we must have the condition:

$$\frac{V_{RX}}{Z_B} = \frac{V_{TX}}{R1} \qquad \text{where } V_{TX} = f(V_{RX})$$

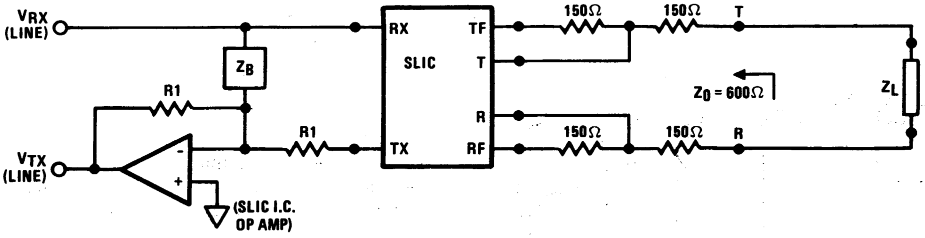
$$\frac{V_{RX}}{Z_B} = \left[V_{RX} \times \left(\frac{4R}{2R + Z_L}\right)\right] / R1$$

$$Z_B = R_1 \times \left(\frac{2R + Z_L}{4R}\right)$$

Thus if $Z_L = 2R$ ...(i.e. 600 ohm) then $Z_B = R1$

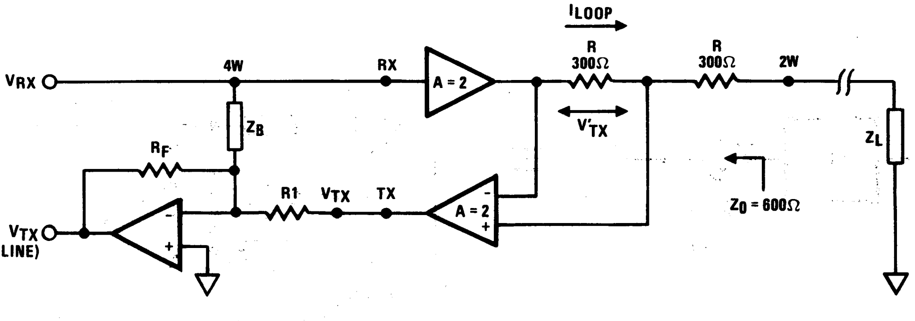
For general case let $R1 = 4R$

$Z_B = 2R + Z_L$



V_{RX} (LINE)
Z_B
R1
R1
V_{TX} (LINE)
(SLIC I.C. OP AMP)
RX
SLIC
TX
TF
T
R
RF
150Ω
150Ω
T
150Ω
150Ω
R
Z_0 = 600Ω
Z_L

FIGURE A1.



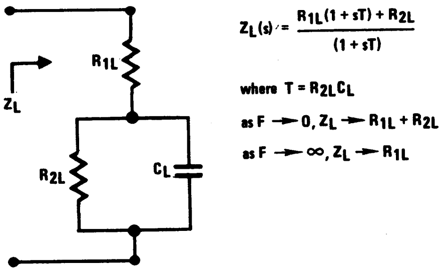
I_{LOOP}
V_{RX}
4W
RX
A = 2
R 300Ω
R 300Ω
2W
V'_{TX}
Z_B
R_F
R1
V_{TX}
TX
A = 2
V_{TX} (LINE)
Z_0 = 600Ω
Z_L

FIGURE A2.

2. Matching complex line/load configurations... For some users it is necessary for the SLIC to appear as a complex impedance looking into SLIC from the 2W line in order to match complex line impedances.

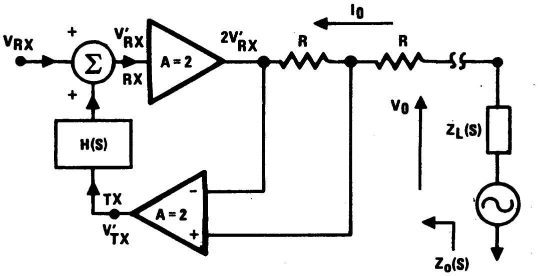
Consider a typical complex line configuration, see Figure A3.

By implementing positive and negative feedback around the V_{RX} to V_{TX} loop, the output impedance of the SLIC can be transformed to match Z_L. Again, consider the single ended signal path equivalent circuit of the SLIC together with a feedback network H(s), as shown in Figure A4.



Z_L
R_{1L}
R_{2L}
C_L
$Z_L(s) = \frac{R_{1L}(1+sT)+R_{2L}}{(1+sT)}$
where $T = R_{2L}C_L$
as $F \rightarrow 0, Z_L \rightarrow R_{1L} + R_{2L}$
as $F \rightarrow \infty, Z_L \rightarrow R_{1L}$

FIGURE A3.



V_{RX}
+
V'_{RX}
RX
+
A = 2
$2V'_{RX}$
I_0
R
R
V_0
$Z_L(S)$
H(S)
TX
V'_{TX}
A = 2
-
+
$Z_0(S)$

FIGURE A4.

Assume transmission only; $V_{RX} = 0$.

H(s) network will provide positive and negative feedback to give $Z_0(s)$

$$V_0 = 2RI_0 + 2V'_{RX}$$
$$V'_{RX} = HV'_{TX} = 2HI_0R$$
$$V_0 = 2RI_0 + 4HI_0R$$
$$Z_0 = V_0/I_0$$
$$Z_0 = 2R(1+2H)$$
$$H = (Z_0 - 2R)/4R \qquad \text{(A)}$$

Figure A5 indicates that network H can be configured as follows to provide required positive and negative feedback.

$$i_1 + i_2 = -i_3$$

$$\left(\frac{V'_{TX} - KV'_{TX}}{Z_1}\right) + \left(\frac{V_{RX} - KV'_{TX}}{Z_2}\right) = \frac{KV'_{TX} - V'_{RX}}{Z_2}$$

For $V_{RX} = 0$ and defining $H = V'_{RX}/V'_{TX}$ the above equation reduces to:

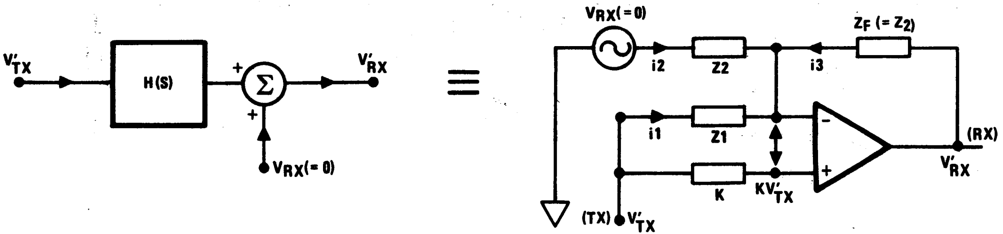
$$H = K\left[\frac{2Z_1 + Z_2\left(1 - \frac{1}{K}\right)}{Z_1}\right] \qquad \text{(B)}$$

Equations (A) and (B) are equivalent. Equation (A) can be expanded for a particular Z_0 requirement. Equation (B) can then be manipulated so that terms and coefficients of the two final equations can be compared to solve for Z_1, Z_2 and K.

EXAMPLE

This example is given for the complex impedance considered above.

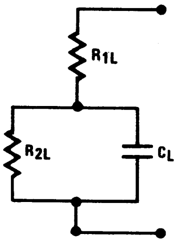
Require Z_0 to appear as in Figure A6.



V'_{TX}
H(S)
+
Σ
+
V'_{RX}
$V_{RX}(=0)$
≡
$V_{RX}(=0)$
i2
Z2
i3
$Z_F (= Z_2)$
i1
Z1
K
KV'_{TX}
-
+
(RX)
V'_{RX}
(TX)
V'_{TX}

$Z_F = Z_2$ in order to maintain $|V_{RX}|$ signal at RX pin as it appears on 4W line.

FIGURE A5.



$$Z_0 (= Z_L) = \frac{R_{1L}(1 + sT) + R_{2L}}{(1 + sT)}$$

where $T = R_{2L}C_L$

FIGURE A6.

From Equation A, it can be shown that for Z_O above

$$H = \left(\frac{R_{1L} + R_{2L} - 2R}{4R}\right) \times \frac{\left(1 - sT\left[\frac{2R - R_{1L}}{R_{1L} + R_{2L} - 2R}\right]\right)}{(1 + sT)} \qquad (C)$$

Consider Equation (B). Assume Z_1 and Z_2 have the form N_x/D_x. Thus Equation (B) reduces to:

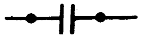
$$H = K\left[\frac{2N_1D_2 + N_2D_1(1 - 1/k)}{N_1D_2}\right] \qquad (D)$$

Comparing terms in Equations C and D:

$N_1D_2 = (1 + sT)$

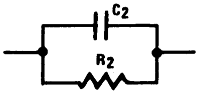
Let $N_1 = 1$, Z_1 and Z_2 can be configured thus:

$Z_1 \longrightarrow$ C_1



$= \frac{1}{sC_1} = \frac{N_1}{D_1}$

$Z_2 \longrightarrow$



$= \frac{R_2}{1 + sT_2} = \frac{N_2}{D_2}$

Substituting for Z_1 and Z_2, equation D reduces to:

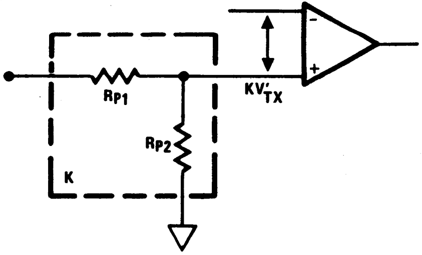
$$H = 2K \times \left[\frac{i - sR_2\left(C_1\left[\frac{1 - K}{2K}\right] - C_2\right)}{(1 + sT_2)}\right] \qquad (E)$$

Comparing terms in equations (C) and (E), the following working formula for Z_1 and Z_2 and K are derived:

Z_2: $R2 = R_{2L}$ (1)

$C_2 = C_{2L}$ (2)

K: K is a constant and is configured as a potential divider.

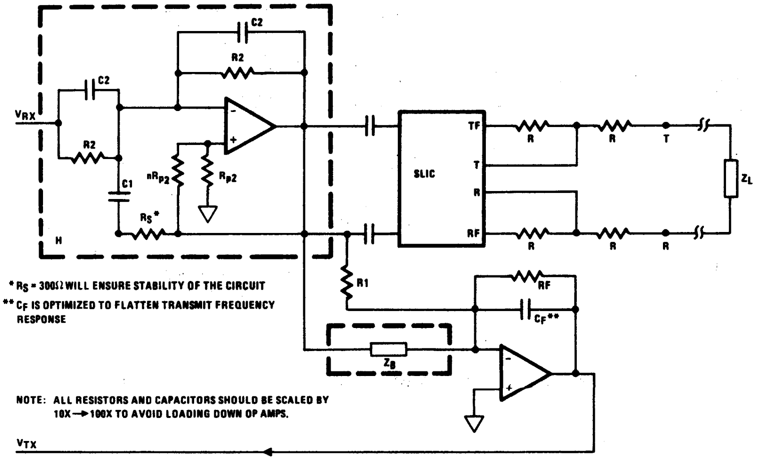


if $R_{P1} = \frac{R_{P2}}{n}$ where n is an integer

then $\frac{2n}{1 + n} = \frac{(R_{1L} + R_{2L}) - 2R}{4R}$ (3)

Z_1: $C_1 = C_{2L}\left[\frac{2R_{2L}}{10R - (R_{1L} + R_{2L})}\right]$ (4)

The final circuit configuration will take account of the complex impedance transform network, and the balance network derived in Equation 1. The circuit is illustrated in Figure A7.



*RS = 300Ω WILL ENSURE STABILITY OF THE CIRCUIT
**CF IS OPTIMIZED TO FLATTEN TRANSMIT FREQUENCY RESPONSE

NOTE: ALL RESISTORS AND CAPACITORS SHOULD BE SCALED BY 10X → 100X TO AVOID LOADING DOWN OP AMPS.

FIGURE A7. BALANCING AND MATCHING THE HC-550X SLIC

APPENDIX B
COMPLEX LINE IMPEDANCE MATCHING WITH SLIC

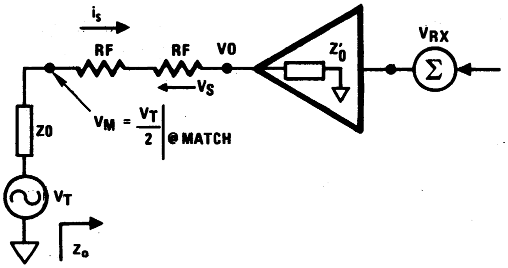

is
RF
RF
VO
Z'0
VRX
Σ
VS
ZO
VM = VT/2 | @ MATCH
VT
Zo

FIGURE B1. TWO TO FOUR WIRE TRANSMISSION. SINGLE ENDED AC EQUIVALENT CIRCUIT OF SUBSCRIBER LOOP.

Consider Figure B1. Assume $V_{RX} = 0$. (2W to 4W transmission)

At match:

$$i_s = \frac{V_T}{2Zo} = \frac{Vm}{Zo}$$

$$Zo = 2R_F + Zo'$$

$$Zo' = \frac{Vo}{i_s}$$

$$Vo = Zo'.\ i_s = i_sZo - 2i_sR_F$$

but $Vm = i_sZo$; $\therefore Vo = Vm - 2i_sR_F$ Equation (1)

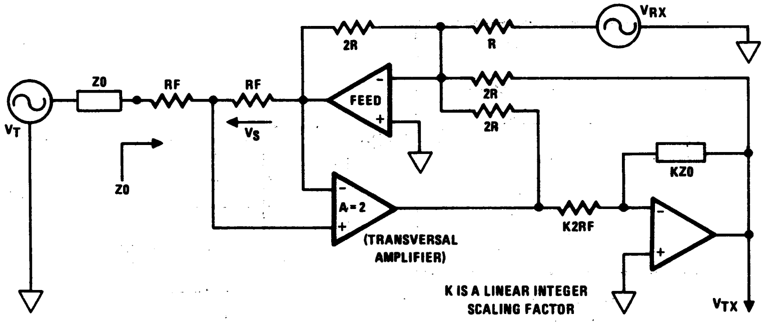
$Vs = i_sRF$, $\therefore Vs = \dfrac{R_F}{(2R_F + Zo')} \times Vm$

$$\therefore\ Vm = (isR_F)\frac{(2R_F + Zo')}{RF} \qquad \text{Equation (2)}$$

(2) in (1) for Vm, and Zo = 2RF + Zo'

$$Vo = 2Vs\left(\left(\frac{Zo}{2RF}\right) - 1\right)$$

This matching equation can be realized as shown in Figure B2.


VRX
2R
R
ZO
RF
RF
FEED
2R
2R
VT
VS
ZO
KZO
A=2
(TRANSVERSAL AMPLIFIER)
K2RF
VTX

K IS A LINEAR INTEGER SCALING FACTOR

FIGURE B2. FOUR WIRE TO TWO WIRE TRANSMISSION

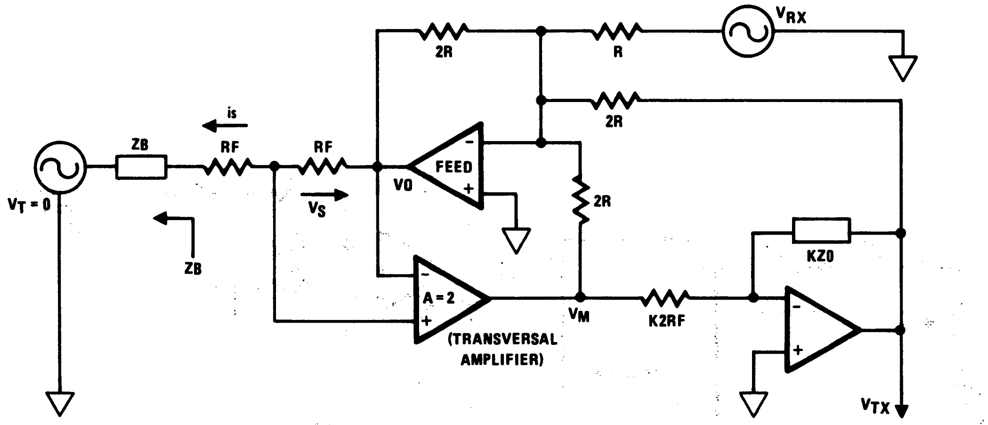


FIGURE B3.

Transhybrid Balance

Consider Figure B3. Evaluate V_{TX} in terms of V_{RX}, in order to establish transhybrid balance equation.

For general case, let line transhybrid impedance be Z_B.

$$V_o = -2\left[V_{RX} + \frac{V_m}{2} + \frac{V_{TX}}{2}\right] \quad \text{Equation (1)}$$

$$V_m = -2V_s = \frac{-2R_F}{2R_F + Z_B} \times V_o$$

$$V_{TX} = \frac{(Z_o)}{(2R_F + Z_B)} \times V_o \quad \text{Equation (2)}$$

From Equation (1):

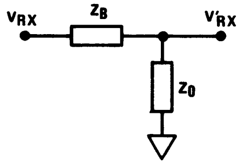
$$V_{RX} = -\left[\frac{V_o}{2} + \frac{V_m}{2} + \frac{V_{TX}}{2}\right]$$

$$2V_{RX} = -\left[\frac{Z_B + Z_o}{2R_F + Z_B}\right] \times V_o$$

$$V_{RX} = \frac{-(Z_B + Z_o)}{2(2R_F + Z_B)} \times V_o \quad \text{Equation (3)}$$

Compare Equations (2) and (3): we need to scale Equation (3) by:

$$Z_o\left(\frac{2}{Z_B + Z_o}\right)$$ in order to equate to Equation (2).



V_{RX} = EQUATION (3).

$$V'_{RX} = \frac{Z_o}{2(2R_F + Z_B)} \times V_o$$

$$\therefore V'_{RX} = \frac{-V_{TX}}{2};$$

Transhybrid balance can be achieved using simple summing amplifier network.

If $Z_B = Z_o$ then Equation (3) becomes:

$$V_{RX} = \frac{-(Z_o)}{(2R_F + Z_o)} \times V_o \quad \text{Equation (4)}$$

and Equation (2) becomes:

$$V_{TX} = \frac{Z_o}{2R_F + Z_o} \times V_o \quad \text{Equation (5)}$$

$\therefore V_{TX} = -V_{RX}$ and TH balance is achieved using resistive summing amp network. The complete application circuit is shown in Figure B4.

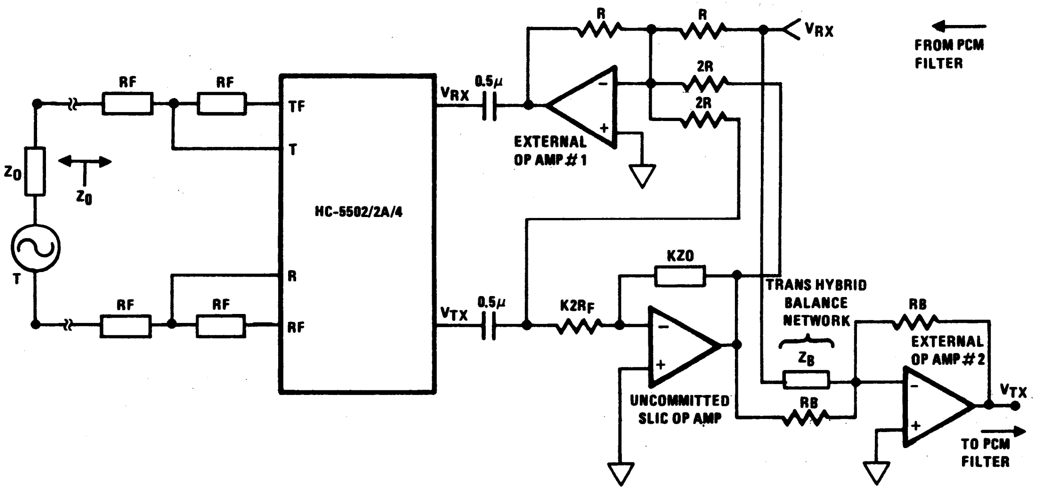

R
R
VRX
FROM PCM FILTER
2R
2R
RF
RF
0.5μ
TF
T
VRX
EXTERNAL OP AMP # 1
Z0
Z0
HC-5502/2A/4
T
KZ0
R
TRANS HYBRID BALANCE NETWORK
RF
RF
VTX
0.5μ
K2RF
RB
RF
EXTERNAL OP AMP # 2
ZB
VTX
UNCOMMITTED SLIC OP AMP
RB
TO PCM FILTER

FIGURE B4. APPLICATION OF SECOND LINE IMPEDANCE MATCHING ALGORITHIM.

NOTICE: Information contained in application notes is intended solely for general guidance; use of the information for user's specific application is at user's risk.

APP NOTE

FOR YOUR INFORMATION

No. 550

Harris Analog

USING THE HA-2541

Alan W. Hansford

Introduction

In response to an industry wide need for a faster, unity gain stable, monolithic operational amplifier, Harris Semiconductor has designed and manufactured the HA-2541 device.

This fully differential op amp has an unprecedented set of dynamic parameters which should be most useful for demanding designs in video, data acquisition, robotics, and RF systems. These devices' capabilities may also be utilized when existing systems must be upgraded or modified for additional performance.

The HA-2541's outstanding features include 90ns settling time, 300V/μs slew rate, and 40MHz unity gain bandwidth, which until recently, could only be achieved through hybrid configurations.

The applications information which follows, points in the direction where a vast number of application circuits await the HA-2541.

Prototyping

As with any high performance device, care should be taken in prototyping so as not to undermine the performance characteristics of the HA-2541. Several simple do's and don'ts should avoid most design problems. Standard high frequency layout techniques are strongly recommended in order to gain the full benefit of the HA-2541's capabilities. The first is proper mounting of the HA-2541 through a ground plane. Since sockets tend to extend the lead length and increase parasitic capacitance, they are not recommended. If sockets must be used, Teflon types are preferred. The mounting of the feedback components should be as close as practical to the HA-2541 and on Teflon standoffs.

The wide bandwidth of the HA-2541 makes it prone to unwanted high frequency poles if large value feedback resistors are used (10K ohms). This calls for low value film type resistors. Actual component values may depend heavily on layout implementation. It is therefore suggested that early prototyping be done to verify the quality of operation and to optimize component values. Additionally, power supply decoupling as close to the power pins as possible, is recommended.

Thermal Considerations

In order to achieve the 300V/μsec slew rate that the HA-2541 is capable of, a high quiescent power level was needed. This, along with the high output capacity of the HA-2541, means that the package must dissipate a large amount of heat.

The device's junction temperature upper limit is 175°C. This places a restriction on the power output at elevated ambient temperatures. The charts below mark the acceptable region of operation with and without a heat sink (Thermalloy 2240A or 6007 are acceptable units and the ones used in the construction of the charts). The curves assume proper installation including the use of heat conductive compounds to facilitate the energy transfer.

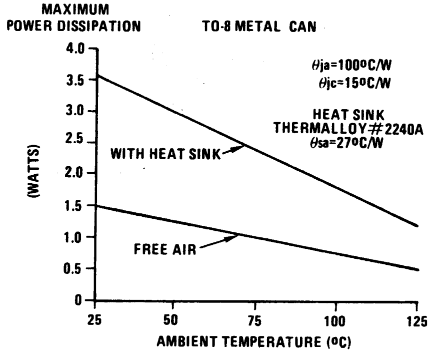


CHART 1. T0-8 METAL CAN

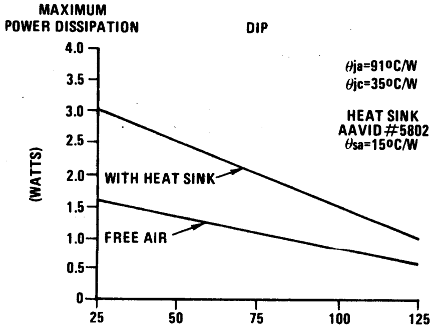


CHART 2. 14 PIN DIP PACKAGE

Performance Enhancements

The HA-2541, like any other high performance device, has certain design features, which give the HA-2541 its excellent wideband performance. Although the HA-2541 has been laser trimmed to minimize offset voltage, an external potentiometer connection has been provided to reduce this even more. Figure 1 illustrates the suggested offset adjustment.

The input DC performance is improved by the use of balanced input impedances on the two input terminals of the device. Figure 2 illustrates this technique which greatly reduces any effects caused by the input offset currents.

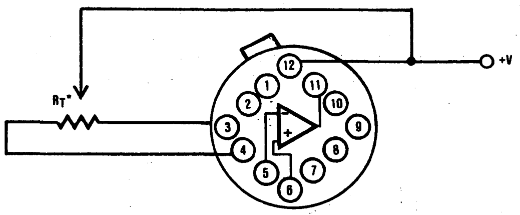
The input signal can be given even more isolation from the effects of input bias currents with the use of FET buffered inputs as shown in Figure 3. The reduction of the input bias currents is quite large, which makes the FET HA-2541 combination an excellent choice for low current applications such as atomic particle detectors (radiation counter circuitry).

Applications

The HA-2541 is a very versatile device with applications in nearly every area of its bandwidth. Perhaps one of the best ways to gain some familiarity with the part is by examining its use in some of the more straightforward applications. The Wein Bridge oscillator in Figure 4 is just such an application.

The HA-2541 is well suited for use as the heart of an oscillator circuit. In spite of the rudimentary diode limiting provided by R_3 - R_7 and D_1 & D_2, a good quality sine wave of 40MHz is readily attainable with an upper limit of 50MHz which exceeds the unity gain bandwidth of the HA-2541.

R_1C_1 and R_2C_2 provide the required regenerative feedback needed for adequate frequency stability. In theory the feedback network requires a gain of three to sustain oscillation. However, the practical gain needed is just over three and is provided for by R_8 and R_9.



*Offset Adjustment Range Is Approximately ± 8mV for RT = 5KΩ

FIGURE 1. SUGGESTED METHOD FOR NULLING V_{OS}

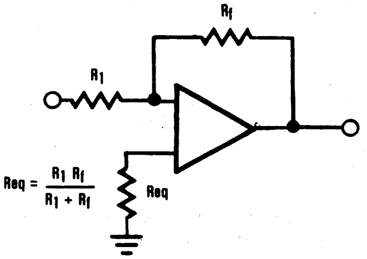
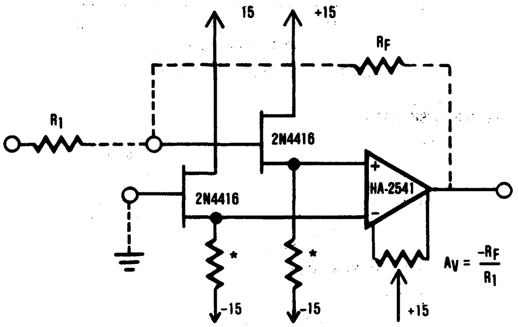


FIGURE 2. MINIMIZING THE EFFECTS OF OFFSET CURRENT



*Value should be determined experimentally for optimum performance.

FIGURE 3. BUFFERING THE HA-2541 INPUTS WITH FETS.

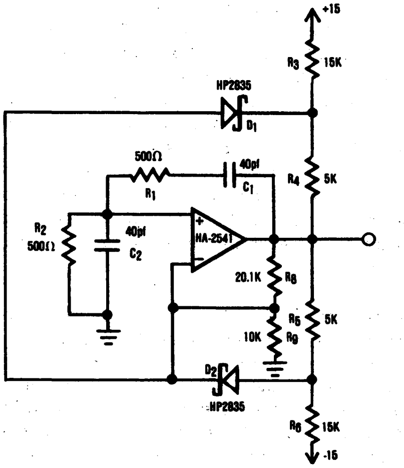


FIGURE 4. 40MHz WEIN BRIDGE OSCILLATOR

High power amplifiers and buffers are in use in a wide variety of applications. Many times the "high power" capability is needed to drive large capacitive loads as well as low value resistive loads. In both cases the final driver stage is usually a power transistor of some type, but because of their inherently low gain, several stages of pre-drivers are often required. The HA-2541, with its 10mA output rating, is powerful enough to drive a power transistor without additional stages of current amplification. This capability is well demonstrated with the high power buffer circuit in Figure 5.

The HA-2541 acts as the pre-driver to the output power transistor. Together, they form a unity gain buffer with the ability to drive three 50 ohm coaxial cables in parallel, each with a capacitance of 2000pF. The total combined load is 16.6 ohms and 6000pF capacitance.

Video

One of the primary uses of the HA-2541 is in the area of video applications. These applications include signal construction, synchronization addition and removal, as well as signal modification. A wide bandwidth device such as the HA-2541 is well suited for use in this class of amplifier. This, however, is a more involved group of applications than ordinary amplifier applications since video signals contain precise DC levels which must be retained.

The addition of a clamping circuit restores DC levels at the output of an amplifier stage. The simple form of the circuit is shown in Figure 6A with a capacitor and analog switch added to the inverting amplifier configuration. The switch closes during a certain portion of the incoming signal. This causes the capacitor to charge to a value which represents the 0V reference of the input waveform. The shorting action of the switch causes the output of the HA-2541 to go to 0V during the 0V reference of the input signal.

This simple amplifier/clamping circuit has several drawbacks. The largest is the drain on the holding capacitor by the input bias currents of the HA-2541, with the resulting change in the reference voltage. This condition is easily addressed with the use of an HA-5320 sample and hold. The low output impedance of the sample and hold can easily provide the required input bias current for the HA-2541 without draining the holding capacitor. The result is a constant DC reference between the scan lines of the video signal.

The second drawback of the simple amplifier/clamp results from the color synchronization information being transmitted along with the 0 Volt DC reference level. By closing the analog switch, the color burst is passed through the low impedance capacitor to ground and consequently lost. This situation is remedied by placing a 3.57MHz trap in series with the analog switch and holding capacitor. This will block the color burst signal and allow it to be passed to the output as an amplified signal. Figure 6B shows both the "trap" and the sample and hold reference additions to the simple amplifier with DC restore.

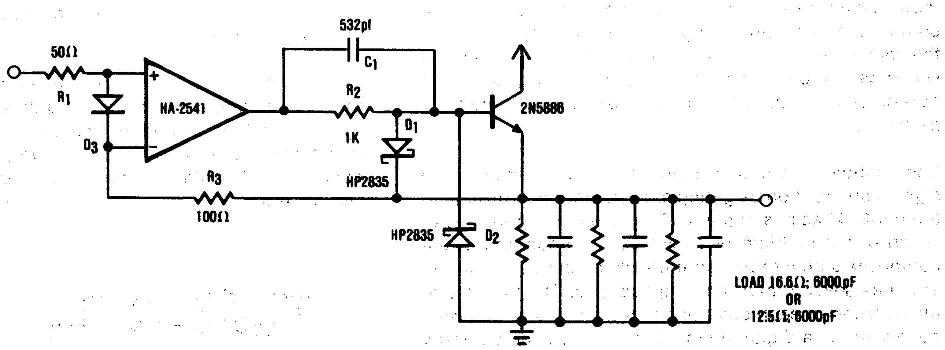


FIGURE 5. DRIVING POWER TRANSISTORS TO GAIN ADDITIONAL CURRENT BOOSTING

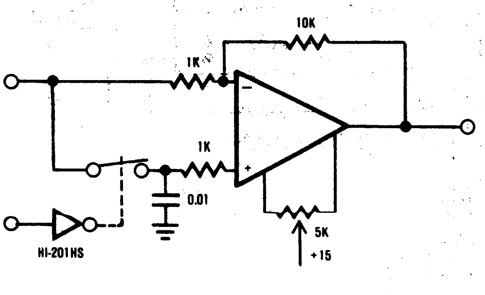


FIGURE 6A. SIMPLE DC RESTORER

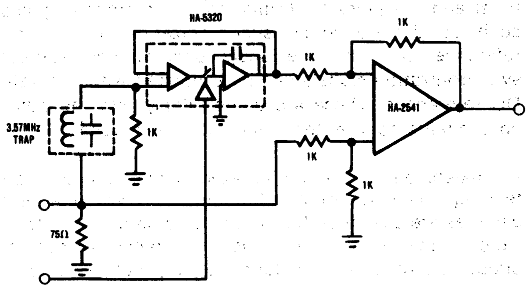


FIGURE 6B. IMPROVED VIDEO DC RESTORER

The amplifier designs to this point work with the full video signal or the "composite" signal. The HA-2541 has several applications one stage back, in the construction of the composite signal itself.

The composite video signal has several components which must be combined to create the final waveform. One that has already been used is the 0 volt reference and the color burst combination. Two others are the horizontal synchronization pulse and the video picture information.

The circuit in Figure 7 is a traditional summing amplifier configuration with the addition of the now familiar DC clamping circuit. The operation is quite simple in that each component (synchronization, color burst, picture information, etc.) of the composite video signal is applied to its own input terminal of the amplifier. These combine algebraically and form the composite signal at the output. The clamping circuit (if used) restores the 0 volt reference of the composite signal.

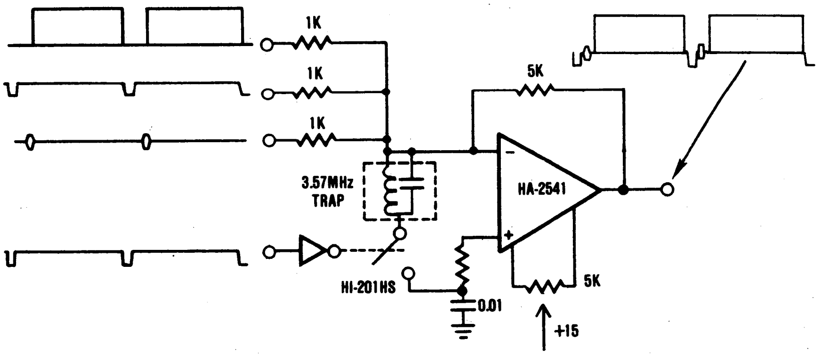


FIGURE 7. SUMMING AMPLIFIER FOR COMPOSITE VIDEO PLUS CLAMPING CIRCUIT

One drawback resulting from the algebraic addition of the input waveforms is the requirement that each input component exist only during the period that it is needed in the composite signal. An example of this is the color burst which can be present at its input terminal only during its portion of the composite signal since no gating circuitry is available.

The multiplexer circuit in Figure 8 can be used for video signal construction by gating each component through to the HA-2541 as it is required. The inherent channel separation of the multiplexer allows each component of the composite signal to be continuously present at the input. This has several important implications. The first is that the duration of each component of the signal is precisely controlled by a digital timing chain (which can be easily reproduced at remote locations with high precision). Second, the only analog signals needed are the color burst and the picture information. All reference signals such as the horizontal synchronization, the 0 volt reference, and the previously unmentioned vertical synchronization signals can be simulated with accurate DC references. These are gated, along with the other components, to form the composite video signal.

An extension of the multiplexed signal construction technique is a type of signal modification. When several cameras are used together without a common synchronization signal, they are not easily combined for special effects and switching. A solution to this problem would be to strip the synchronization pulses off of each of the incoming camera waveforms and apply a new common synchronization pulse. The new pulse will enable switching equipment to combine the separate signals for whatever effect is needed.

It should be noted that widely varying horizontal speeds may necessitate the use of analog delay chains with the synchronization technique. This will produce pictures of compatible quality and proportion (vertical speed is more constant and contains a dead zone for any differences, vertical retrace).

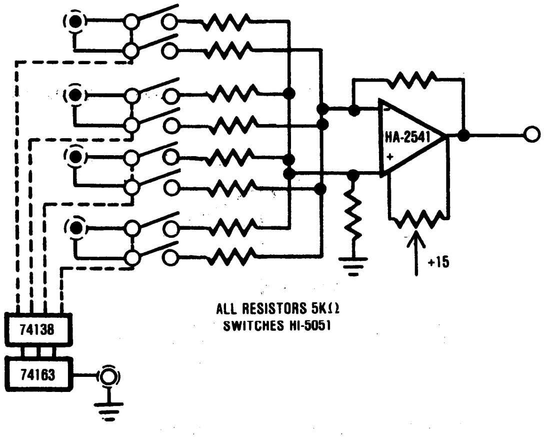


FIGURE 8. MULTIPLEXING WITH HA-2541

The multiplexer system used for video signal construction has other applications of interest. The concept of combining several channels into one can be reversed to form a demultiplexer, where the function is to take several combined channels and separate them into their original form. This type of application can be implemented to solve some well-known industrial problems.

The multiplexer/demultiplexer scheme is readily adapted to the industrial remote controller system where several sensors must communicate over transmission lines to the controller. With the multiplexer/demultiplexer configuration a very large number of sensors are able to communicate with the controller over extended distances through a single coaxial line.

The wide bandwidth of the HA-2541 coupled with its high output rating make it an excellent component of multiplexed data systems. Several schemes of signal switching can be used at the multiplexer end of the system. The HI-5051 switch is well suited for this application especially in the differential configuration shown in Figure 8. The charge injection due to switching channels in and out of the circuit is minimized in this differential mode. A reset pulse aligns the system synchronization and provides the basis for channel separation in the demultiplexer section. As the channels are sequentially placed at the HA-2541 input, they are transmitted to the demultiplexer circuit. In Figure 9 the HA-5320 sample and hold acts as a buffer for each channel and provide a reference source when the other channels are being addressed. Another plus in this demultiplexer circuit is the capability of "de-glitching" the information by simply shifting the clocking rate so as to place all channels in the hold mode during the presence of input spikes.

Write Amplifier

The recent proliferation of industrial and computerized equipment containing programmable memory has increased the need for reliable recording media. The magnetic tape medium is presently one of the most widely used methods. The primary component of any magnetic recording mechanism is the "write" mechanism. In support of this area the circuit of Figure 10 is presented.

The concept of the write generator is very basic. The digital input causes both a change in the output amplitude as well as a change in frequency. This type of operation is accomplished by altering the value of a resistor in the standard twin tee oscillator. An HI-201 analog switch was used to facilitate the switching action. The effect of the external components on the feedback network requires R_{6A} and R_{6B} to be much smaller than would normally have been expected when using the twin tee feedback scheme.

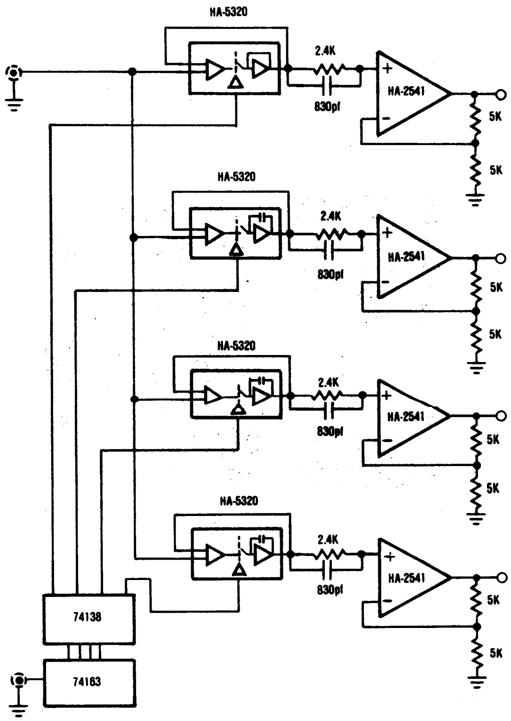


FIGURE 9. DEMULTIPLEXING WITH HA-2541

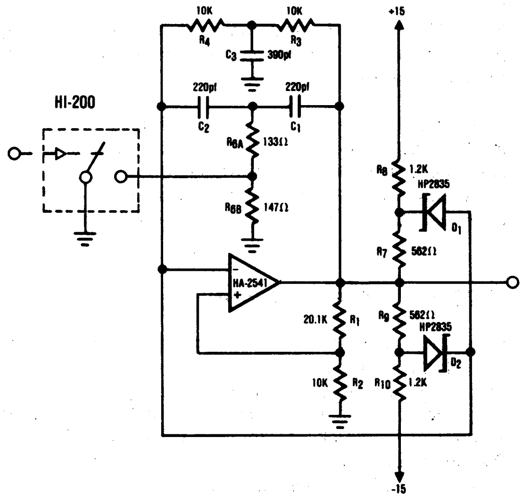


FIGURE 10. USING HA-2541 AS A WRITE AMPLIFIER

The output seen in the photograph of Figure 11 is limited with the aid of D_1, D_2 and R_4-R_7. This is aided by fixing the gain of the amplifier to just over three with R_8 and R_9.

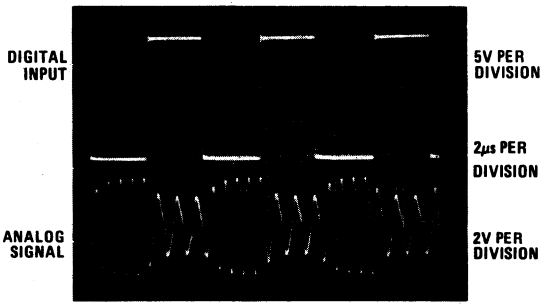


FIGURE 11. DIGITALLY CONTROLLED OUTPUT OF WRITE AMPLIFIERS

Composite Amplifier

The wide bandwidth of the HA-2541 can be used to extend the dynamic range of other useful but frequency limited amplifiers. The HA-5170 is an excellent example of this adaptation. The precision DC characteristic of the HA-5170 are augmented by the bandwidth of the HA-2541. This produces a composite amplifier which approximates the DC performance of the HA-5170 and the frequency range of the HA-2541.

The circuit in Figure 12 has been optimized for operation in the neighborhood of 15MHz. Optimization is quite simple and is accomplished largely through C_A. If a lower frequency region of operation is desired, an additional capacitor, C_2, will give greater flexibility in the choice of component values.

Programmable Amplifier

Often a circuit will be called upon to perform several functions. In these situations the variable gain configuration of Figure 13 may be quite useful. This programmable gain stage depends on CMOS analog switches to alter the amount of feedback and thereby the gain of the stage. Placement of the switching elements inside relatively low current area of the feedback loop, minimizes the effects of bias currents and switch resistance on the calculated gain of the stage. Voltage spikes may occur during the switching process, resulting in temporarily reduced gain because of the make-before-break operation of the switches. This can be minimized by providing a separate voltage divider network for each switched gain.

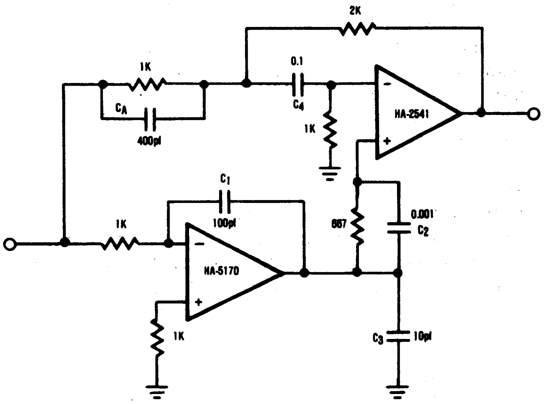


FIGURE 12. COMPOSITE AMPLIFIER

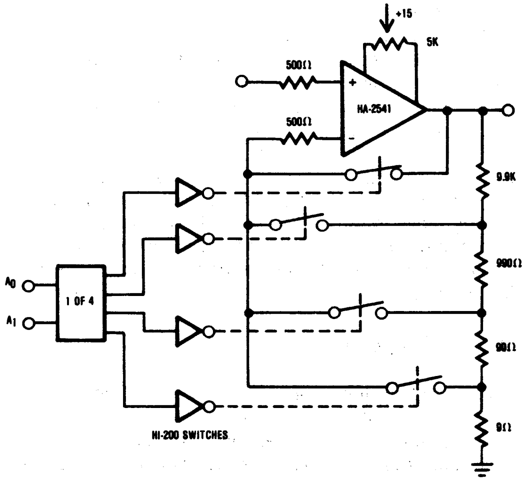


FIGURE 13. A GAIN PROGRAMMABLE HA-2541

References

1. William L. Hughes, "Television Fundamentals and Standards" Electronic Engineers Handbook ed. Bonald G. Fink (McGraw-Hill, 1975) p. 20-3.

2. Thermalloy Semiconductor Accessories Catalog, Thermalloy Inc. Dallas, Texas.

3. Arthur B. Williams, "Designers Handbook of Integrated Circuits." (McGraw-Hill, 1984) pps. 1-10, 1-27.

APP NOTE

FOR YOUR INFORMATION

APP. NOTE 552

No. 552

Harris Analog

USING THE HA-2542

Dick Whitehead

Introduction

In the multi-faceted electronics industry, there are many circuit applications which require the capabilities of two or more types of operational amplifiers in the same location. To fulfill this need, design engineers are usually challenged with fabricating a discrete amplifier design or selecting an expensive hybrid amplifier which appears to be an "ALL-IN-ONE" type of amplifier.

The Harris HA-2542 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Offset voltage nulling and bandwidth controls add flexibility when the HA-2542 is used in performance-tailored applications.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2542 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

Prototyping Guidelines

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include: 1) mounting the device through a ground plane: 2) connecting unused pins to the ground plane: 3) mounting feedback components on Teflon standoffs and/or locating these components as close to the device as possible; 4) placing power supply decoupling capacitors from device supply pins to ground.

As a result of speed and bandwidth optimization, the HA-2542's case potential, when powered-up is equal to the V- potential. Therefore, contact with other circuitry or ground should be avoided.

Heat Sinking

To drive heavy loads found in typical coaxial cable systems, the HA-2542 may require heat sinking to avoid exceeding its maximum junction temperature (+175°C). Figure 1 shows maximum power dissipation curves derived for the HA-2542 with and without the recommended heat sink. Should another type of heat sink be used, then the following expression should be used to determine maximum power dissipation.

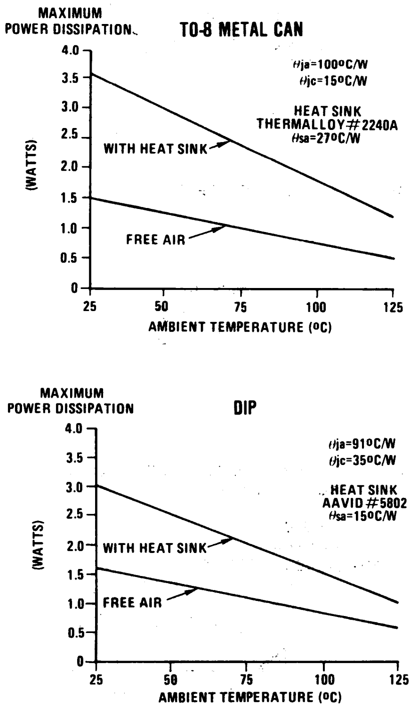


FIGURE 1. HA-2542 MAXIMUM POWER DISSIPATION CURVES

$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j\text{-}c} + \theta_{c\text{-}s} + \theta_{s\text{-}a}}$$

Where: T_{jmax} = maximum junction temperature of the device

T_A = Ambient

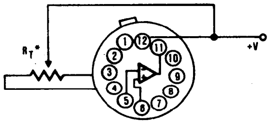
$\theta_{j\text{-}c}$ = Junction to case thermal resistance

$\theta_{c\text{-}s}$ = Case to heat sink thermal resistance

$\theta_{s\text{-}a}$ = Heat sink to ambient thermal resistance

Performance Enhancements

DC errors can be reduced and AC stability increased by recommended adjustments to the control points made available in the HA-2542 device. The suggested method for nulling the offset voltage of HA-2542 is shown in Figure 2, while Figure 3 suggests the method for controlling the bandwidth. Figure 4 shows normalized AC parameters versus compensation capacitance. Experimental results indicated that approximately 17pF was necessary to stabilize the HA-2542 for unity gain operation.



*OFFSET ADJUSTMENT RANGE IS APPROXIMATELY ±15mV FOR R_T = 5KΩ.

FIGURE 2. SUGGESTED OFFSET VOLTAGE ADJUSTMENT

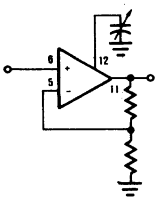


FIGURE 3. SUGGESTED METHOD FOR INCREASING AC STABILITY

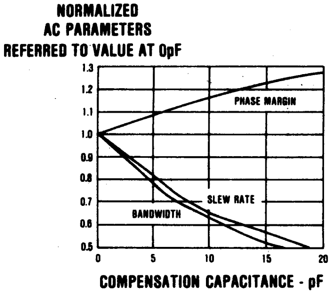
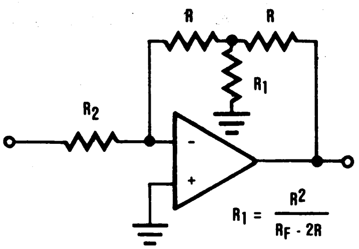


FIGURE 4. NORMALIZED AC PARAMETERS

For best high frequency performance, feedback resistor values should be restricted to minimal values. Values below 5KΩ are recommended to reduce possibilities of introducing unwanted poles into the application's transfer function. Figure 5 indicates how high values for closed loop gain can be implemented, while maintaining feedback element values. This method is called "T network" feedback and values for the resistors can be derived from the following expression.

$$R_1 = \frac{R^2}{R_f - 2R}$$

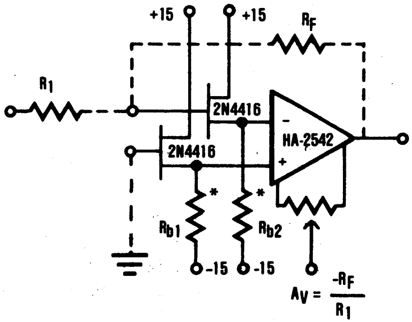
Where: R_f is the value of feedback resistance to be reduced and R is a value preselected by the designer.



WHERE R IS PRESELECTED AND R_F IS DESIRED FEEDBACK RESISTOR VALUE.

FIGURE 5. KEEPING FEEDBACK VALUES LOW

Utilizing some relatively familiar techniques, the input bias currents of the HA-2542 can be sharply reduced. Figure 6 employs discrete FETs to provide input bias currents in the pA range without appreciably diminishing the AC performance.



*R_{b1} AND R_{b2} SHOULD BE DETERMINED EXPERIMENTALLY FOR BEST RESULTS.

FIGURE 6. USING DISCRETE FETs TO REDUCE THE HA-2542's INPUT BIAS CURRENT

Composite amplifiers are hybrid "marriages" between precision and wideband operational amplifiers. Using the HA-2542 as the AC device in the composite amplifier shown in Figure 7 provides an additional dimension to its

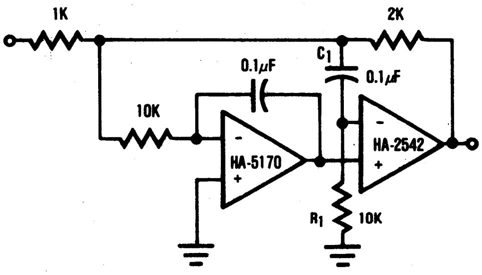


FIGURE 7. COMPOSITE AMPLIFIER CIRCUIT REDUCES DC ERRORS

capabilities. Now, the hybrid represents a precision type, high speed, wideband, power amplifier.

In this circuit, high frequency amplification tasks are performed by the HA-2542 and are set by combination R_1-C_1. The HA-5170 acts as the DC amplifier providing precision type input parameters while cascading its DC gain with that of the HA-2542. This cascade of gains develops very high loop gain for the composite amplifier.

Applications

Most attractive to the video system designer is the HA-2542's combination of speed, bandwidth, and output drive capability. Augmenting these features are much desired differential gain and phase specifications of 0.1% and 0.2 degrees respectively. Previously these parameters could only be provided by hybrid or discrete component circuitry. A primary application which fully utilizes these features is the coaxial cable driver.

The configuration shown in Figure 8 represents a simple multi-channel security system. The HA-2542 is being operated at a closed loop gain of 2 and is driving a balanced coaxial line system which appears as a 50Ω load. The signal throughput from the multiplexer input to the coaxial outputs is 1. Experimental results showed that coaxial line lengths could exceed 100 feet without adversely affecting video signal quality.

HA-2542 is capable of $2V_{p-p}$ signals to 16MHz in this configuration. Resistor R_B is used to trim overall system gain to prevent color saturation if the cameras and monitors are color types. The controller to the multiplexer could be one of several variations including remote, remote wired, or automatically time sequenced.

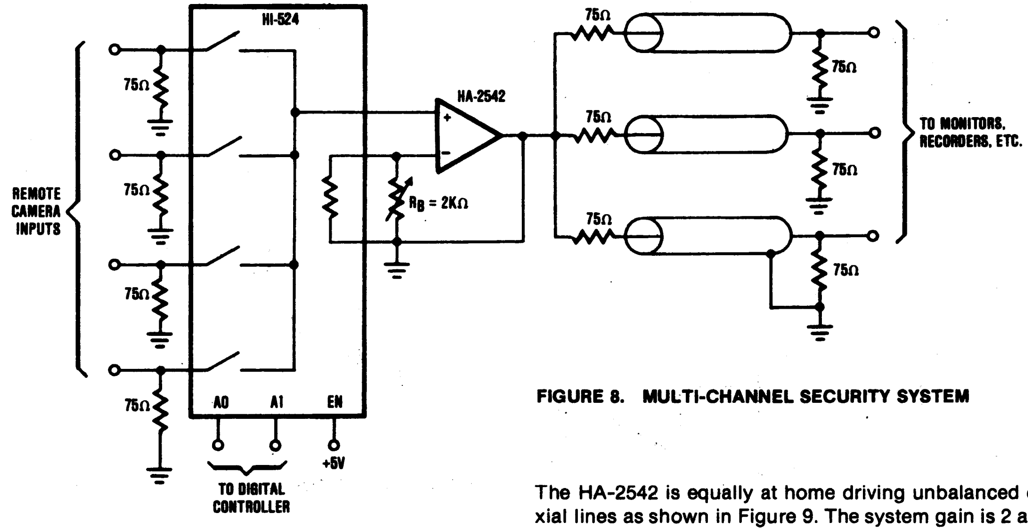


FIGURE 8. MULTI-CHANNEL SECURITY SYSTEM

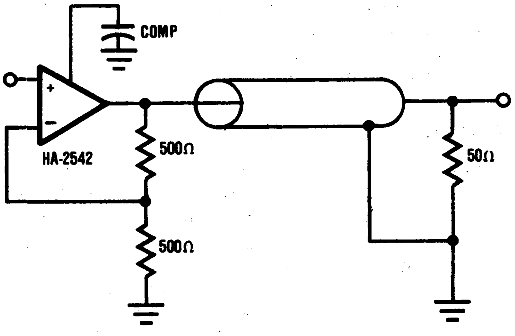


FIGURE 9. DRIVING UNBALANCED COAXIAL CABLES

The HA-2542 is equally at home driving unbalanced coxial lines as shown in Figure 9. The system gain is 2 and, depending on cable length, compensation capacitance may be necessary to provide additional stability. In this configuration, the HA-2542 can delivery $10V_{p-p}$ signals at frequencies above 8MHz. For this application, power requirements will usually necessitate the use of heat sinking for the HA-2542.

Another video type application requiring an op amp with excellent speed and output drive is the analog input driver of a flash converter circuit. Figure 10 shows the HA-2542 buffering the input of an 8-bit flash converter. Because of the heavy input capacitance (100pF - 300pF) and high number of individual internal comparator inputs (255), the impedance of the input is non-linear. A typical high speed op amp used in this configuration would exhibit oscillation tendencies regardless of compensation and isolation techniques used. The photograph shown in Figure 10 indicates that the HA-2542 is very stable in this application.

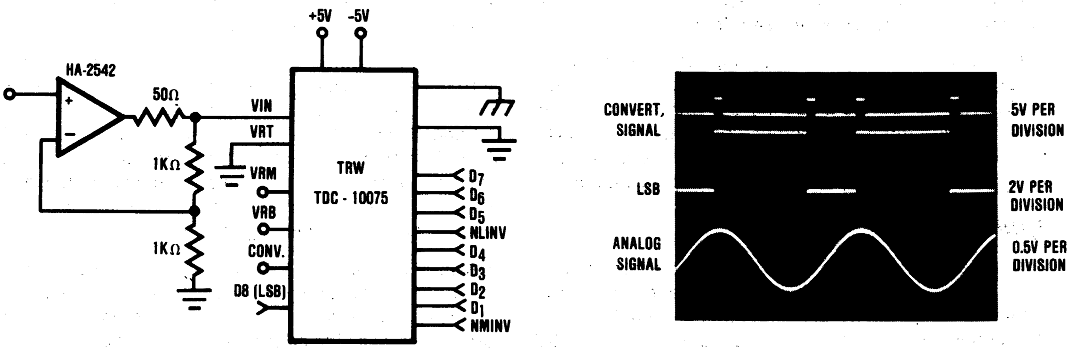

+5V
-5V
HA-2542
+
-
50Ω
1KΩ
1KΩ
VIN
VRT
VRM
VRB
CONV.
D8 (LSB)
TRW
TDC - 10075
D7
D6
D5
NLINV
D4
D3
D2
D1
NMINV
CONVERT, SIGNAL
LSB
ANALOG SIGNAL
5V PER DIVISION
2V PER DIVISION
0.5V PER DIVISION

FIGURE 10. DRIVING THE NON-LINEAR INPUT IMPEDANCE OF FLASH CONVERTERS (ONE INPUT SHOWN)

Power Supply

The HA-2542 with its excellent output current could also be used as a power source in DC power supply systems. In Figure 11, a simplified digitally programmable power supply is shown which utilizes the high output current capabilities of the HA-2542. Combination R_1-R_2 sets the gain of the amplifier, while V_{REF} and the "weighted" resistor ladder permit the HI-201 to perform digital selection of the voltage to be used.

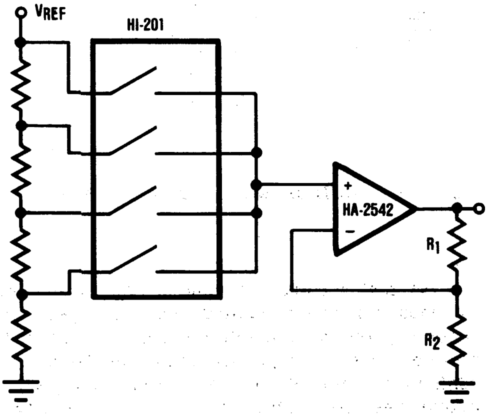

VREF
HI-201
+
HA-2542
-
R1
R2

FIGURE 11. DIGITALLY PROGRAMMABLE POWER SUPPLY

Audio

In studio quality audio systems, the HA-2542 could be readily used in driver applications such as a speaker driver. Figure 12 shows a method which increases the power capability of a drive system for audio speakers. In this circuit two HA-2542s are used to operate on half cycles only, which greatly increases their power handling capability. "Bridging" the speaker as shown makes 200mA of output current available to drive the load. The HA-5102 is used as an AC coupled, low noise, preamplifier which drives the bridge circuit.

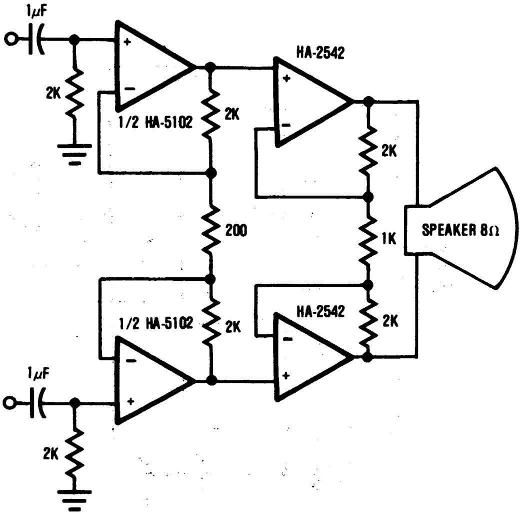
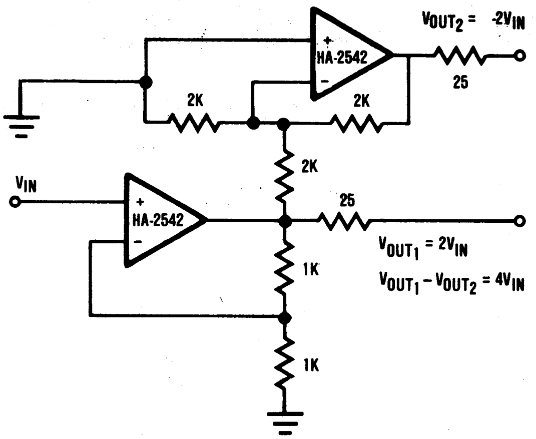

1µF
2K
+
-
1/2 HA-5102
2K
HA-2542
+
-
2K
200
1K
SPEAKER 8Ω
HA-2542
2K
1/2 HA-5102
2K
-
+
1µF
2K

FIGURE 12. BRIDGE LOAD DRIVE FOR AUDIO CIRCUITS

Another variation of the bridged load type circuit is shown in Figure 13a. In this circuit the load voltage is increased by a factor of 4. The HA-2542s are connected in a manner such that the output voltages will be equal in amplitude and opposite in phase. This circuit can also be used to drive long lengths of twisted shielded pair cable.

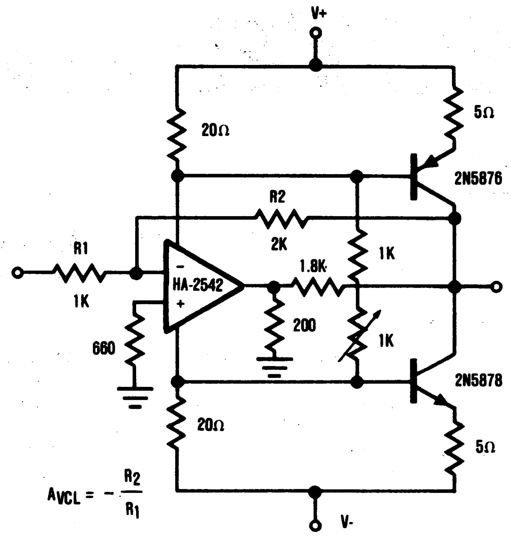
Boosting Output Current

If the excellent output current of the HA-2542 requires boosting because of extreme loading, then the configuration shown in Figure 13b could be used. In this circuit, the HA-2542 drives the high power transistor stage and provides circuit gain. With the power transistors shown, the output drive is increased to several amps. Speed and power bandwidth have not been appreciably affected. Boosting the output current to these higher levels provides for additional implementation into DC motor drive or bridge transducer drive circuits.



$V_{OUT2} = -2V_{IN}$
HA-2542
2K
2K
25
2K
V_{IN}
HA-2542
25
$V_{OUT1} = 2V_{IN}$
$V_{OUT1} - V_{OUT2} = 4V_{IN}$
1K
1K

FIGURE 13A. DIFFERENTIAL CIRCUIT FOR LINE DRIVING

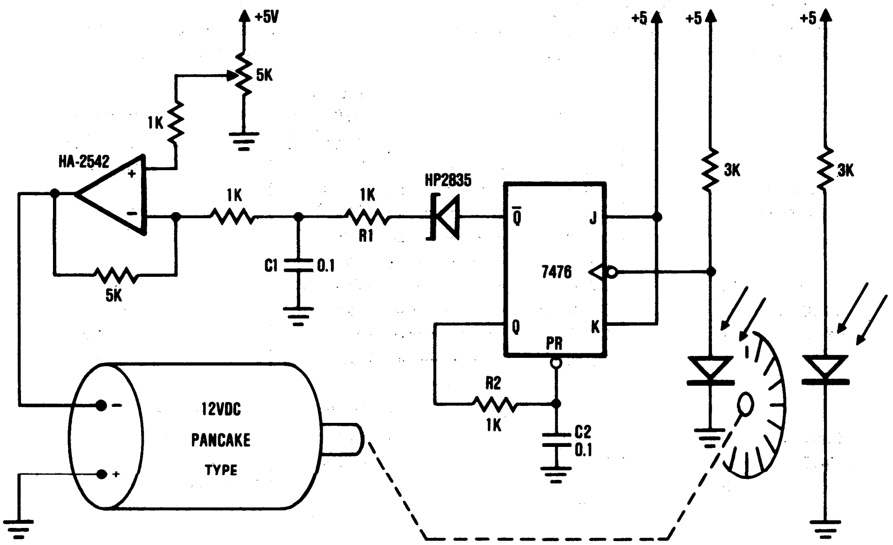


V+
20Ω
5Ω
2N5876
R2
2K
R1
1K
HA-2542
1.8K
1K
660
200
1K
2N5878
20Ω
5Ω
$A_{VCL} = -\frac{R_2}{R_1}$
V-

FIGURE 13B. DRIVER STAGE FOR HIGH POWER TRANSISTORS

The output drive capability of the HA-2542 is highly suitable for direct drive applications of small DC motors and, since it is an operational amplifier, it can also perform the function of motor speed control. This type of closed loop system can be found throughout the robotics and media recording industries.

The system shown in Figure 14 consists of the HA-2542, a small 12V DC motor, and a position encoder. During operation, the encoder causes a series of "constant width" pulses to charge C_1. The integrated pulses develop a reference voltage which is proportional to motor speed and is applied to the inverting input of HA-2542. The non-inverting input is held at a constant voltage which represents the desired motor speed. A difference between these two inputs will send a corrected drive signal to the motor which completes the speed control system loop.



+5V
5K
1K
HA-2542
1K
1K
R1
HP2835
C1
0.1
5K
$\overline{Q}$
J
7476
Q
K
PR
R2
1K
C2
0.1
+5
+5
+5
3K
3K
12VDC
PANCAKE
TYPE

FIGURE 14. CONTROLLING DC MOTOR SPEED WITH HA-2542

APP NOTE
FOR YOUR INFORMATION

No. 553
Harris Analog

HA-5147, ULTRA LOW NOISE AMPLIFIER

By Alan Hansford

Introduction

Engineers interested in precision signal processing will find the HA-5147, with its unique features, very interesting. Utilizing an advanced design with special device geometries, the HA-5147 has moved the Harris dielectric process into a new arena of both speed and precision. Perhaps one of the most remarkable features of the HA-5147 is its ultra low noise performance, which makes it the first monolithic amplifier to combine speed, precision, and ultra low noise operation (Figure 1).

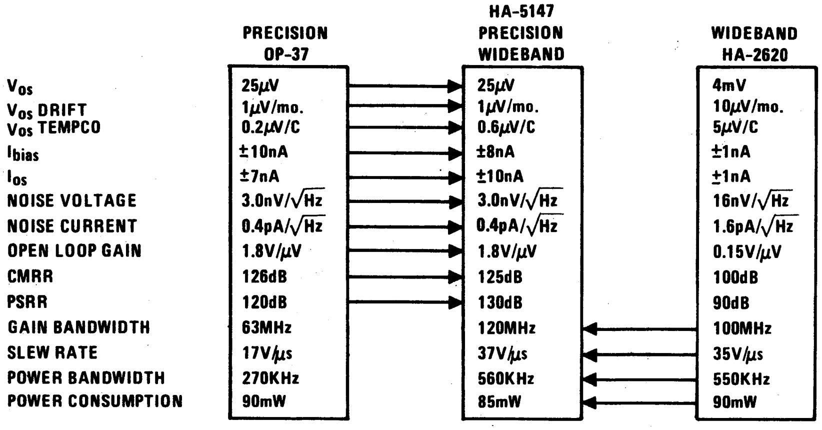
To realize this device, intense attention was given to the "total" design from input to output (Figure 2).

The input stage consists of a cross-coupled differential pair which provides a very high CMRR (125dB) through the use of CASCODE circuits. Effective use of the bias current cancellation scheme also keeps the bias currents to a mere 10nA. With laser trimming of the load resistors R1 and R2, the offset voltage is kept below 25µV at 25°C. The entire input stage has been optimized for low noise operation and is largely responsible for the amplifier's ultra low noise voltage of $3.0\text{nV}/\sqrt{\text{Hz}}$ @ 1KHz. Low frequency noise, on the other hand, is particularly important in DC applications and the HA-5147's 2.7Hz lower noise corner will prove quite beneficial for many users.

The loading on R1 and R2 is kept to a minimum through the use of emitter followers between the input stage and the second differential pair. C4 provides a feedforward path around the second stage at high frequencies and feeds into the level shifter and current mirror section. This portion of the design provides a differential to single-ended conversion and relies on C2 to tailor the rolloff of the second stage. Two vertically-constructed PNP transistors within the level shifter dramatically increase the frequency response of the amplifier compared to that of other construction techniques.

Emitter followers in the fourth stage reduce the capacitive loading effects of C1 by providing a separate driver for C1 and the output stage. The output stage here is a high speed buffer that employs complementary transistors as well as short circuit protection.

The high performance features of the HA-5147 have quite clearly moved this device closer to the "ideal" than any other amplifier in its class. Yet, with some simple external components, this device can be positioned even closer to the "ideal." An offset nulling potentiometer can reduce V_{OS} (Figure 3a), while the already hefty output stage (I_{out} = 20mAmin) can be boosted without reducing the excellent speed and bandwidth characteristics (Figure 3b).



	PRECISION OP-37	HA-5147 PRECISION WIDEBAND	WIDEBAND HA-2620
V_{OS}	25µV	25µV	4mV
V_{OS} DRIFT	1µV/mo.	1µV/mo.	10µV/mo.
V_{OS} TEMPCO	0.2µV/C	0.6µV/C	5µV/C
I_{bias}	±10nA	±8nA	±1nA
I_{os}	±7nA	±10nA	±1nA
NOISE VOLTAGE	$3.0\text{nV}/\sqrt{\text{Hz}}$	$3.0\text{nV}/\sqrt{\text{Hz}}$	$16\text{nV}/\sqrt{\text{Hz}}$
NOISE CURRENT	$0.4\text{pA}/\sqrt{\text{Hz}}$	$0.4\text{pA}/\sqrt{\text{Hz}}$	$1.6\text{pA}/\sqrt{\text{Hz}}$
OPEN LOOP GAIN	1.8V/µV	1.8V/µV	0.15V/µV
CMRR	126dB	125dB	100dB
PSRR	120dB	130dB	90dB
GAIN BANDWIDTH	63MHz	120MHz	100MHz
SLEW RATE	17V/µs	37V/µs	35V/µs
POWER BANDWIDTH	270KHz	560KHz	550KHz
POWER CONSUMPTION	90mW	85mW	90mW

FIGURE 1.
The HA-5147 combines the qualities of precision Op Amps with those of the wideband speed category.

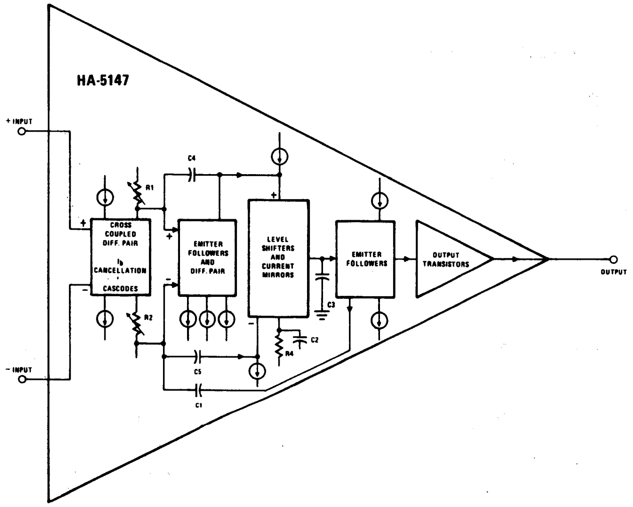


FIGURE 2.

Intense attention was given to the "total" design from inputs to output.

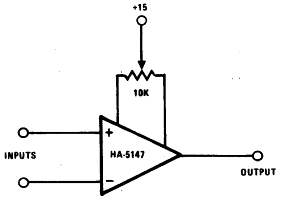


FIGURE 3a.

Nulling the HA-5147's offset voltage to 0 volts brings it closer to "ideal"

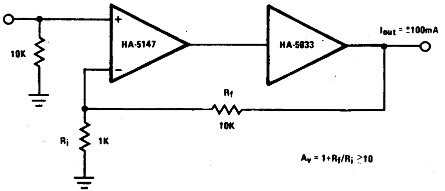


FIGURE 3b.

The HA-5147's output current can be boosted to ±100mA by using the HA-5033. AC performance is not affected.

Low Noise Design

Since the HA-5147 is a very low noise operational amplifier, low noise design techniques must be used to make the most of this feature. There are two primary means of keeping noise down, one requires the amplifier inputs to look into low source resistances and the other requires bandwidth limiting by filtering. A short outline of noise prediction will be presented here to support these concepts.

Noise can be divided into several categories, which include thermal noise (white noise) and flicker noise (pink noise or 1/f noise). The feedback components are strongly dominated by thermal noise making thermal noise the most important of these from a system design standpoint (an exception to this are high gain DC amplifiers which require low 1/f noise as measured by the noise corner"). Flicker noise is more a function of the amplifier construction quality, and system design variations are less effective in reducing this type of noise.

Noise is usually rated in one of two ways. The first is RMS voltage or current (a measure of peak-to-peak noise in a given bandwidth) and the second is by noise density spectrum in $V/\sqrt{Hz}$ and $A/\sqrt{Hz}$ (a measure of the spectral content of the noise in the frequency domain). The two rating schemes are related, with RMS noise levels generated from the integration of the noise density spectrum over a desired frequency bandwidth.

As an illustration of noise prediction, the noise density for the standard inverting amplifier configuration (Figure 4a) will be determined. The total noise is derived from the combination of several noise sources, only three of which are of any significance. These are the amplifier's noise voltage, the thermal noise of the feedback components, and the noise generated by the current noise of the amplifier within the feedback components.

The total noise is defined as the square root of the sum of the squares of the individual noise terms.

$$E_n = G\sqrt{(E_{amp})^2 + (E_{\substack{\text{feedback}\\\text{network}}})^2 + (E_{\substack{\text{current noise in}\\\text{feedback network}}})^2}$$

E_n = total noise

G = gain of stage

E_{amp} = amplifier noise voltage........$3.0nV/\sqrt{Hz}$ @ f > 1KHz

$E_{\substack{\text{feedback}\\\text{network}}} = \sqrt{4KTR_{eq}}$ where... $K = 1.381E\text{-}23$, $T = 300$, $R_{eq} = R \| R_f$

$E_{\substack{\text{current noise in}\\\text{feedback network}}} = I_{noise} R_{eq}$

$I_{noise} = 0.4pA/\sqrt{Hz}$ @ f > 1KHz

or more specifically . . .

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}R_{eq})^2}$$

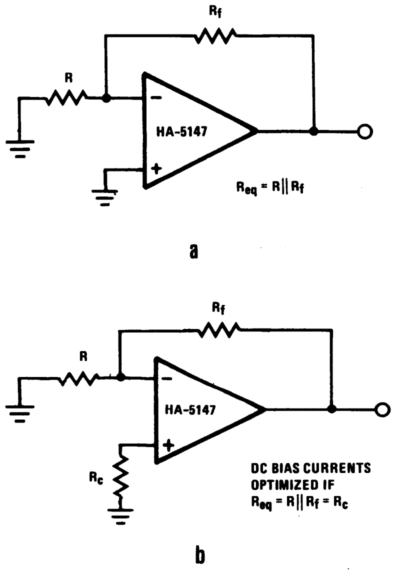


FIGURE 4. NOISE PREDICTION CIRCUITS

A reasonable estimate of noise levels can be generated with these two basic amplifier circuits.

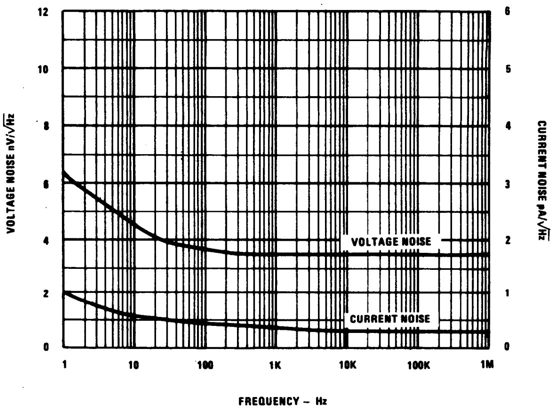


FIGURE 5. HA-5147 NOISE CHARACTERISTICS

The HA-5147's exceptional noise characteristics may be used to improve existing and new high quality audio systems.

Both the amplifier noise voltage and noise current are constant above 1KHz and rise slightly for lower frequencies (Figure 5). The resistor thermal noise is derived from the parallel combination of the feedback network (R_{eq}) and several constants (4KT). The third noise term again uses the equivalent resistance of the feedback network (R_{eq}) as well as the current noise generated at the input terminals of the amplifier.

It should be evident from the above formula that extremely large values of R_{eq} (especially over 10Kohm) will dominate the noise density while low values for R_{eq} will yield to the amplifier's own noise characteristics. Note the asyptotic convergence of the noise voltages in Figures 3a-3c at low values of R_{eq}.

A second circuit (Figure 4b) balances the effects of input bias currents by placing a resistor R_c, equal to R_{eq}, between the non-inverting input and ground. While reducing DC errors, this configuration adds two additional terms to the noise formula.

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}R_{eq})^2 + R_c\,4KT + (I_{noise}R_c)^2}$$

The original contributors to output noise remain as before and the additional terms represent the thermal contribution by R_c and the associated amplifier current noise seen through that resistor. To optimize DC design, $R_{in} \parallel R_f = R_{eq} = R_c$, therefore the noise density equation reduces to . . .

$$E_n = G\sqrt{(E_{amp})^2 + 2R_{eq}4KT + 2(I_{noise}R_{eq})^2}$$

Again the relationship between large values of R_{eq} and a high noise density spectrum remains.

RMS noise is derived in part as the integral of the noise density spectrum over a given bandwidth. Below is the complete expression . . .

$$E_{rms}\text{ (from } f_0 \text{ to } f_1) = \sqrt{\int_{f_0}^{f_1} E_{\substack{\text{noise}\\\text{density}\\\text{spectrum}}}^{2}\,df}$$

The strict integration assuming E_n is constant works well for f_0 above ≈ 1KHz. Both the amplifier's noise voltage and the noise current increase for frequencies below 1KHz. This makes for difficult integration since complicated expressions for I_{noise} and E_{amp} must be generated. To avoid this problem, graphical integration techniques or sampled methods can be used with great success.

The curves in Figures 6a-6c illustrate the relationship between the RMS noise and R_{eq} for both amplifier designs. It should be apparent from the predicted RMS noise curves that increased bandwidth causes an increase in noise voltage. An interesting effect of this relationship is that only absolute bandwidth (f_1-f_0) is important. The general frequencies of interest (if they are above 1KHz) are irrelevant. More simply, 100Hz of bandwidth near 10KHz contains as much noise as 100Hz of bandwidth near 1MHz. This implies that bandwidth should be restricted with appropriate high and low pass filtering, if the lowest noise voltages are to be attained.

From the previous discussion, it is apparent that low noise designs require low resistor values. This is not to say that high gain should be avoided, just that low input and source resistance values are required for low noise opera-

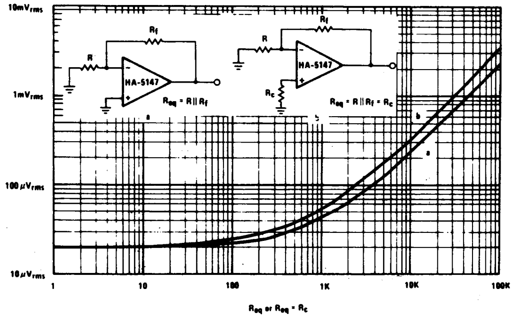


FIGURE 6a. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 10KHz - 500KHz for HA-5147.

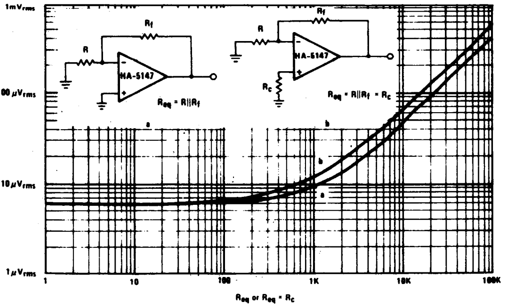


FIGURE 6b. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 20Hz - 20KHz for HA-5147.

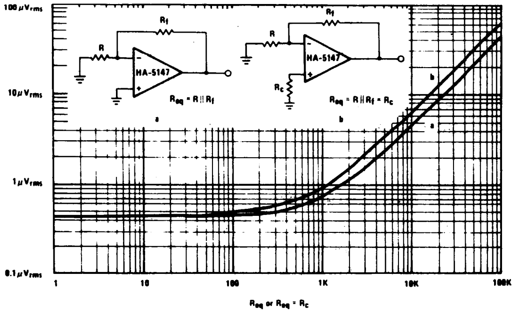


FIGURE 6c. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 10Hz - 100Hz for HA-5147.

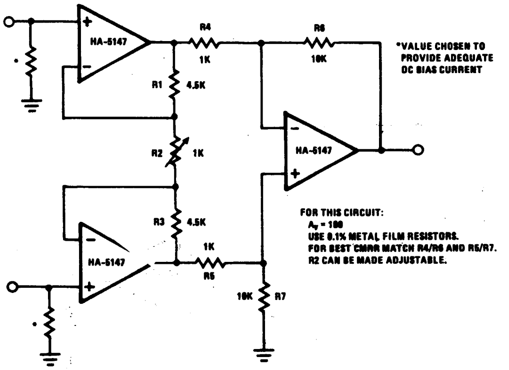

HA-5147
R4
1K
R6
10K
R1
4.5K
R2
1K
R3
4.5K
1K
R5
10K
R7
*VALUE CHOSEN TO PROVIDE ADEQUATE DC BIAS CURRENT
FOR THIS CIRCUIT:
A_V = 100
USE 0.1% METAL FILM RESISTORS.
FOR BEST CMRR MATCH R4/R6 AND R5/R7.
R2 CAN BE MADE ADJUSTABLE.

FIGURE 7. INSTRUMENTATION AMPLIFIER

Thanks to higher speed and more bandwidth, this standard three amplifier instrumentation amplifier will have 10MHz bandwidth and 550KHz power bandwidth.

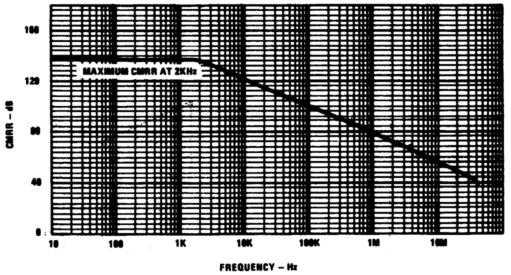


FIGURE 8. HA-5147 CMRR VS. FREQUENCY

The instrumentation amplifier's maximum CMRR can now be moved to much higher frequencies when using the HA-5147.

tion. Closer examination of the RMS noise formula will also show that limiting bandwith, with filtering, will also reduce noise levels. Additionally, metal film and wirewound resistors have lower excess noise (a component of resistor noise in addition to thermal noise) than carbon resistors and are therefore preferred.

Applications

Heavily used throughout the world of signal processing is the instrumentation amplifier and it is this particular circuit that can best utilize all of the features of the HA-5147. By using the HA-5147, the standard 3 amplifier instrumentation circuit (Figure 7) is now able to extend its bandwidth to 10MHz or its power bandwidth to 500KHz. Additionally, the maximum CMRR (>120dB) is extended to higher frequencies (Figure 8). Other "error producing" input referred parameters of the HA-5147 such as noise, V_{OS}, I_{bias}, V_{OS} drift and temperature coefficients have been minimized, thus maximizing the capabilities of this application.

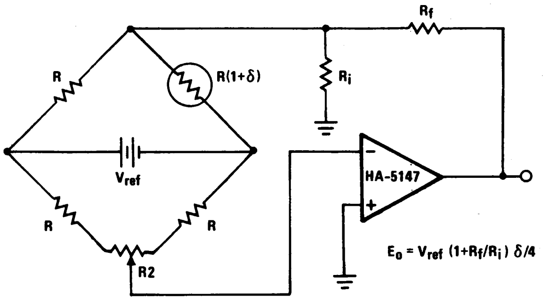


FIGURE 9. LOW LEVEL BRIDGE AMPLIFIER

Very small bridge signals are sensed and amplified accurately when using the precision performance of the HA-5147

Another circuit requiring very accurate amplification of its signal is the transducer bridge amplifier (Figure 9). The HA-5147, shown in an inverting bridge amplifier configuration, is recommended when it is necessary to detect very small bridge level signals. Its high open loop gain (>120dB), low noise, and excellent values for V_{OS}, V_{OS} drift, and bias current provide exceptional sensitivity to the smallest transducer variations. Full scale calibration of this circuit is made possible by placing a small valued potentiometer in series with R_i. Nulling is accomplished with R2.

The high slew rate (37V/μs) and the excellent output current drive (±20mA min.) make HA-5147 highly suitable as an input output buffer amplifier for analog multiplexers (Figure 10). The precision input characteristics of the HA-5147 help simplify system "error budgets" while its speed and drive capabilities provide fast charging of the multiplexer's output capacitance. This eliminates any increased multiplexer acquisition time, which can be induced by more limited amplifiers. The HA-5147 accurately transfers information to the next stage while effectively reducing any loading effects on the multiplexer's output.

Staying within the realm of signal processing, another standard and much used circuit configuration can be enhanced by the speed and precision of the HA-5147. A precision threshold detector (Figure 11) requires low noise, low and stable offset voltage, high open loop gain, and high speed. These requirements are met by the HA-5147, while adding excellent CMRR and PSRR to the list. The standard variations of this circuit can easily be implemented using the HA-5147. For example, hysteresis can be generated by adding R1 to provide a small amount of positive feedback. The circuit becomes a pulse width modulator if V_{ref} and the input signal are left to vary. Although the output drive capability of this device is excellent, the optional buffering circuit may be used to drive heavier loads while preventing loading effects on the amplifier.

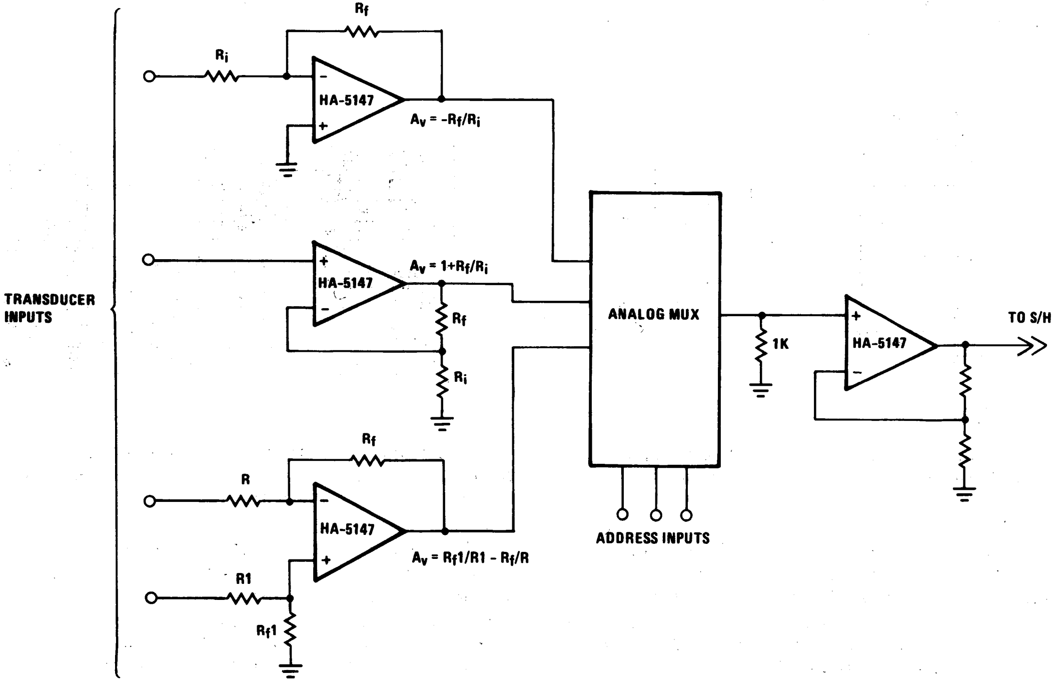


FIGURE 10. HIGH SPEED INPUT/OUTPUT ANALOG MULTIPLEXER BUFFERING

Reduced "error" budgets and higher speeds of operation are easily achieved when the combined speed and precision of the HA-5147 are used in these buffer amplifier applications.

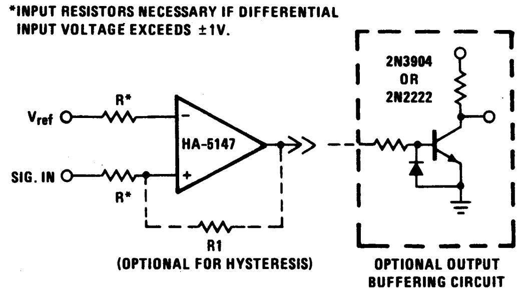

*INPUT RESISTORS NECESSARY IF DIFFERENTIAL INPUT VOLTAGE EXCEEDS ±1V.
V_{ref}
R*
SIG. IN
R*
HA-5147
R1
(OPTIONAL FOR HYSTERESIS)
2N3904
OR
2N2222
OPTIONAL OUTPUT BUFFERING CIRCUIT

FIGURE 11. PRECISION THRESHOLD DETECTOR

This device can be used to increase response times while maintaining precise detection.

Engineers working with professional audio designs will find the HA-5147 highly desirable for many of their applications. With its exceptional noise characteristics (Figure 5), wide power bandwidth (500KHz), and modest power consumption (85mW), this device can be used as a high quality audio preamplifier or as an intermediate stage gain block. A circuit similar to that in Figure 3b can be incorporated into studio or stage monitors.

The audio preamplifier of Figure 3b has a limited output current range. The audio power amplifier in Figure 12 overcomes this limitation and can provide an even greater boost to the HA-5147. Q1 and Q2 are a complementary pair arranged in a push pull manner, with R1 and R2 providing the necessary drive current. The maximum output voltage corresponds to the minimum output current since

$$(15\text{-}V_{be}\text{-}V_o)/R1$$

is the drive current to the transistors. D1 and D2 insure the proper biasing of the transistors as well as a clean crossover from Q1 to Q2.

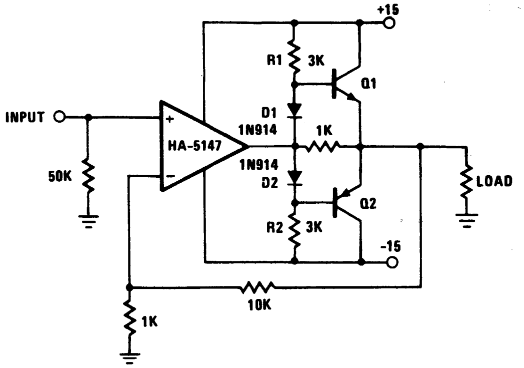

+15
R1
3K
Q1
INPUT
D1
1N914
1K
HA-5147
50K
1N914
D2
LOAD
Q2
R2
3K
-15
10K
1K

FIGURE 12. HIGH POWER AMPLIFIER

The additional drive capability of the power transistors allows the HA-5147 to drive very heavy loads.

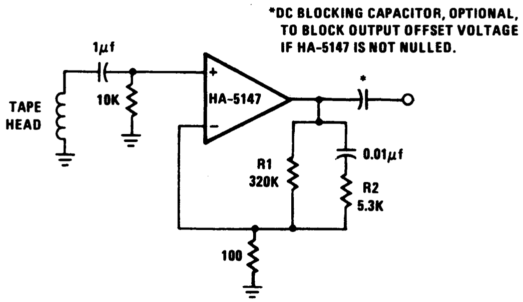

*DC BLOCKING CAPACITOR, OPTIONAL, TO BLOCK OUTPUT OFFSET VOLTAGE IF HA-5147 IS NOT NULLED.
1μf
TAPE HEAD
10K
HA-5147
*
0.01μf
R1
320K
R2
5.3K
100

FIGURE 13. PROFESSIONAL AUDIO NAB TAPE PLAYBACK PREAMPLIFIERS

This NAB tape playback preamplifier fully utilizes the speed, bandwidth, and noise features of the HA-5147

An audio circuit which can make maximum use of the speed, bandwidth, and low noise of the HA-5147 is the NAB tape playback preamplifier (Figure 13). This circuit is configured to provide low frequency boost to 50Hz, flat response to 3KHz, and high frequency attenuation above 3KHz. Compensation for variations in tape and tape head performance can be achieved by trimming R1 and R2.

Signal generation applications will also find this high precision device useful. As an astable multivibrator (Figure 14) the power bandwidth of the HA-5147 extends the circuit's frequency range to approximately 500KHz. R_t can be made adjustable to vary the frequency if desired. Any timing errors due to V_{OS} or I_{bias} have been minimized by the precision characteristics of the HA-5147. D1 and D2, if used, should be matched to prevent additional timing errors. These clamping diodes may be omitted by tying R_t and the positive feedback resistor Rf directly to the output.

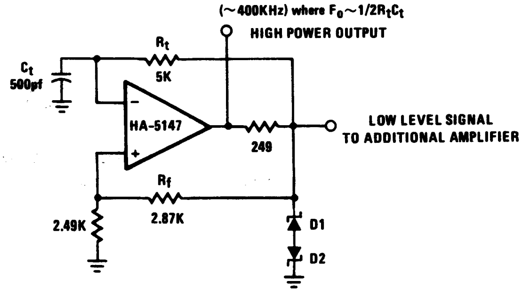
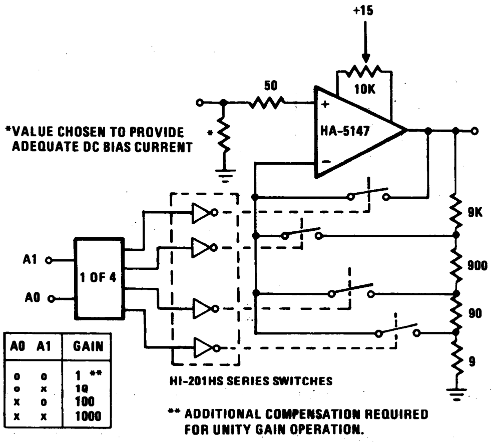

(~400KHz) where F_o~1/2R_tC_t
HIGH POWER OUTPUT
R_t
5K
C_t
500pf
HA-5147
249
LOW LEVEL SIGNAL TO ADDITIONAL AMPLIFIER
R_f
2.87K
2.49K
D1
D2

FIGURE 14. ASTABLE MULTIVIBRATOR

Higher frequencies of operation and reduced timing errors make the HA-5147 an attractive building block in signal generation applications.


+15
50
10K
HA-5147
*VALUE CHOSEN TO PROVIDE ADEQUATE DC BIAS CURRENT
9K
900
90
9
A1
A0
1 OF 4
HI-201HS SERIES SWITCHES
** ADDITIONAL COMPENSATION REQUIRED FOR UNITY GAIN OPERATION.

A0	A1	GAIN
o	o	1 **
o	x	10
x	o	100
x	x	1000

FIGURE 15. PROGRAMMABLE AMPLIFIER

Variable gain of 1, 10, 100, 1000 is achieved by selecting the proper amount of feedback with the use of analog switches.

Often a circuit will be called upon to perform several functions. In these situations the variable gain configuration of Figure 15 may be quite useful. This programmable gain stage depends on CMOS analog switches to alter the amount of feedback and thereby the gain of the stage. Placement of the switching elements inside the relatively low current area of the feedback loop, minimizes the effects of bias currents and switch resistance on the calculated gain of the stage. Voltage spikes may occur during the switching process, resulting in temporarily reduced gain because of the make-before-break operation of the switches. This can be minimized by providing a separate voltage divider network for each level of gain.

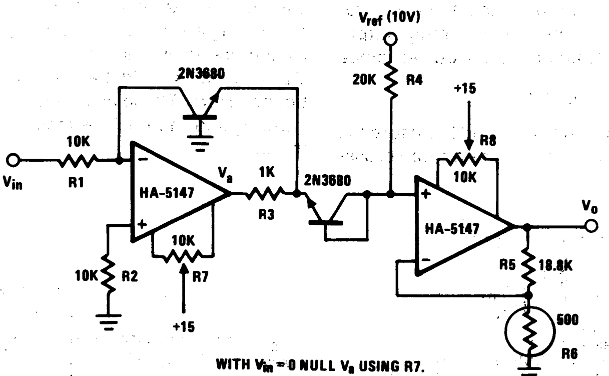
Many signal processing applications depend on low noise characteristics for their operation. One such application involves logrithmic amplifiers. The input sensitivity range is governed by the system noise in such a circuit. The HA-5147, with its low noise characteristics, can extend the basic sensitivity of the common logrithmic amplifier (Figure 16). The circuit uses a matched pair of transistors to offset the effects of temperature and quiescent currents. The final expression for V_{out} reduces to ....

$$V_{out} = -0.259(1 + R_5/R_6)\ln[0.5\ V_{in}/V_{ref}]$$

or using the schematic values ...

$$V_{out} = -\ln[0.2V_{in}]$$

R6 should be temperature dependent if the expression for V_{out} is to hold over an extended temperature range. The overall sensitivity is from a few millivolts to about twice V_{ref}.


V_{ref} (10V)
20K
R4
+15
R8
10K
2N3680
10K
V_{in}
R1
HA-5147
V_a
1K
R3
2N3680
HA-5147
V_o
10K
R7
10K
R2
+15
R5
18.8K
500
R6

WITH V_{in} = 0 NULL V_a USING R7.
WITH V_{in} = $0.5V_{ref}$ NULL V_o USING R8.

FIGURE 16. LOGRITHMIC AMPLIFIER

The matched pair of transistors makes this a very temperature stable logrithmic amplifier.

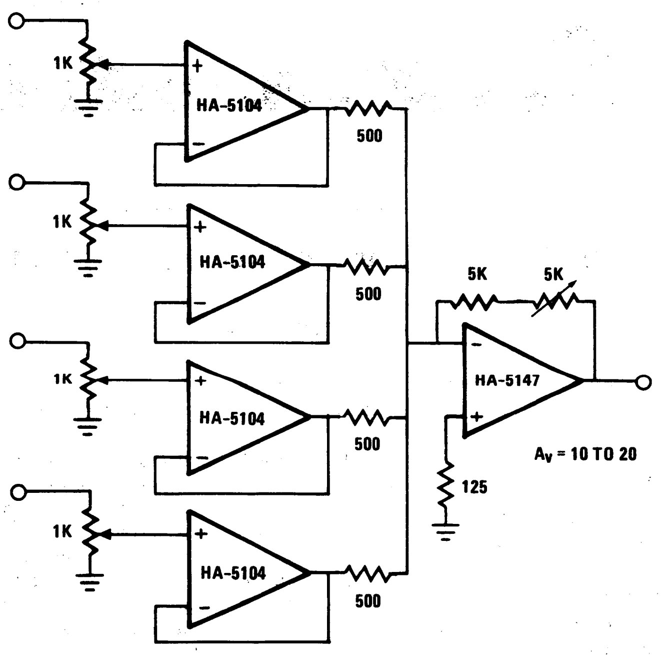


FIGURE 17. INPUT BUFFERED MIXER

Several signals can be combined using this circuit with a minimum of channel cross-talk.

A high signal to noise ratio is important in signal construction and combination. The HA-5147 aids in lowering overall system noise and thereby raises system sensitivity. The signal combination circuit in Figure 17 incorporates input buffering with several other features to form a relatively efficient mixer stage.

The potentiometer used for each channel allows for both variable input levels as well as a constant impedance for the driving source. The buffers serve mainly to prevent reverse cross-talk back through the resistor network. This allows for the combination of varying strength signals without reverse contamination. The gain of the final stage is set at a minimum of 10 and can be adjusted to as much as 20. This allows a great deal of flexibility in combining a vast array of input signals.

References

D-C Amplifier Noise Revisited, Al Ryan & Tim Scranton Analog Dialog, 1969.

Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design, New York: John Wiley and Sons, 1973.

Instruction Manual, model 2173C Transistor Noise Analyzer Control Unit. Quan-Tech, Division of KMS Industries. Whippany, New York.

APP NOTE
FOR YOUR INFORMATION

No. 554
Harris Analog

LOW NOISE FAMILY HA-5102/04/12/14

by Alan Wayne Hansford

The HA-5102/04/12/14 series is comprised of four separate products designed to meet a wide range of needs. This is accomplished, in part, by offering two groups, the HA-5102/04, each with 3V/μSec slew rate and the HA-5112/14, each with 20V/μSec slew rate.

HA-5102	Dual Amplifier	3V/μSec	Unity Gain Stable
HA-5104	Quad Amplifier	3V/μSec	Unity Gain Stable
HA-5112	Dual Amplifier	20V/μSec	Gains 10 or more
HA-5114	Quad Amplifier	20V/μSec	Gains 10 or more

The entire series shares a common design with the size of the interval compensation capacitor the only difference. The noise voltage and noise current will therefore be the same across the series. With a very low noise input stage at just 4.0nV/$\sqrt{Hz}$ @ 1KHz, the HA-5102/04/12/14 is an excellent choice in applications where a high signal-to-noise ratio is critical, as in professional audio circuits and transducer monitors.

In addition to identical noise performance within the series, the HA-5102/04/12/14 all share common DC specifications with 0.5mV of offset voltage and 130nA of bias current. The high open loop gain, 250KV/V, together with the choice of compensation levels, will allow the HA-5102/04/12/14 series to meet a wide range of requirements.

Low Noise Design

Since the HA-5102 is a very low noise operational amplifier, low noise design techniques must be used to make the most of this feature. There are two primary means of keeping noise down, one requires the amplifier inputs to look into low source resistances and the other requires bandwidth limiting by filtering. A short outline of noise prediction will be presented here to support these concepts.

Noise can be divided into several categories, which include thermal noise (white noise) and flicker noise (pink noise or1/f noise). The feedback components are strongly dominated by thermal noise making thermal noise the most important of these from a system design standpoint (an exception to this are high gain DC amplifiers which require low 1/f noise as measured by the "lower 1/f noise corner"). Flicker noise is more a function of the amplifier construction quality, and system design variations are less effective in reducing this type of noise.

Noise is usually rated in one of two ways. The first is RMS voltage or current (a measure of peak-to-peak noise in a given bandwidth) and the second is by noise density spectrum in V/$\sqrt{Hz}$ and A/$\sqrt{Hz}$ (a measure of the spectral content of the noise in the frequency domain). The two rating schemes are related, with RMS noise levels generated from the integration of the noise density spectrum over a desired frequency bandwidth.

As an illustration of noise prediction, the noise density for the standard inverting amplifier configuration (Figure 1a) will be determined. The total noise is derived from the combination of several noise sources, only three of which are of any significance. These are the amplifier's noise voltage, the thermal noise of the feedback components, and the noise generated by the current noise of the amplifier within the feedback components.

The total noise is defined as the square root of the sum of the squares of the individual noise terms.

$$E_n = G\sqrt{(E_{amp})^2 + (E_{\substack{\text{feedback}\\ \text{network}}})^2 + (E_{\substack{\text{current noise in}\\ \text{feedback network}}})^2}$$

E_n = total noise

G = gain of stage

E_{amp} = amplifier noise voltage........4.0nV/$\sqrt{Hz}$ @ $f > 1KHz$

$E_{\substack{\text{feedback}\\ \text{network}}} = \sqrt{4KTR_{eq}}$ where... $K = 1.381E-23$, $T = 300$, $R_{eq} = R \| R_f$

$E_{\substack{\text{current noise in}\\ \text{feedback network}}} = I_{noise} R_{eq}$

$I_{noise} = 0.56pA/\sqrt{Hz}$ @ $f > 1KHz$

or more specifically . . .

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise} R_{eq})^2}$$

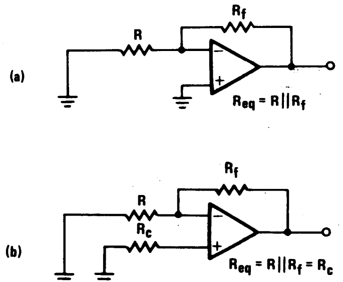


FIGURE 1.

A reasonable estimate of noise levels can be generated with these two basic amplifier circuits.

Both the amplifier noise voltage and noise current are constant above 1KHz and rise slightly for lower frequencies (Figure 2). The resistor thermal noise is derived from the parallel combination of the feedback network (R_{eq}) and several constants (4KT). The third noise term again uses the equivalent resistance of the feedback network (R_{eq}) as well as the current noise generated at the input terminals of the amplifier.

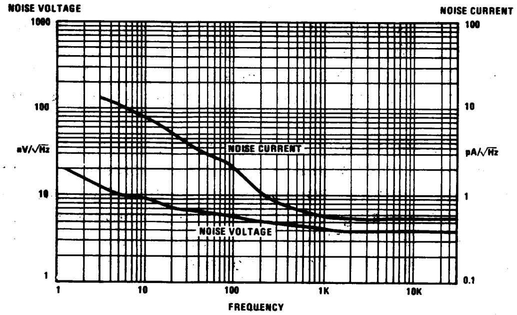


FIGURE 2.

Noise current and voltage for HA-5102/04/12/14.

It should be evident from the above formula that extremely large values of R_{eq} (especially over 10Kohm) will dominate the noise density while low values for R_{eq} will yield to the amplifier's own noise characteristics. Note the asyptotic convergence of the noise voltages in Figures 3a-3c at low values of R_{eq}.

A second circuit (Figure 1b) balances the effects of input bias currents by placing a resistor R_C, equal to R_{eq}, between the non-inverting input and ground. While reducing DC errors, this configuration adds two additional terms to the noise formula.

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}R_{eq})^2 + R_C\,4KT + (I_{noise}R_C)^2}$$

The original contributors to output noise remain as before and the additional terms represent the thermal contribution by R_C and the associated amplifier current noise seen through that resistor. To optimize DC design, $R_{in} \,||\, R_f = R_{eq} = R_C$, therefore the noise density equation reduces to ...

$$E_n = G\sqrt{(E_{amp})^2 + 2R_{eq}4KT + 2(I_{noise}R_{eq})^2}$$

Again the relationship between large values of R_{eq} and a high noise density spectrum remains.

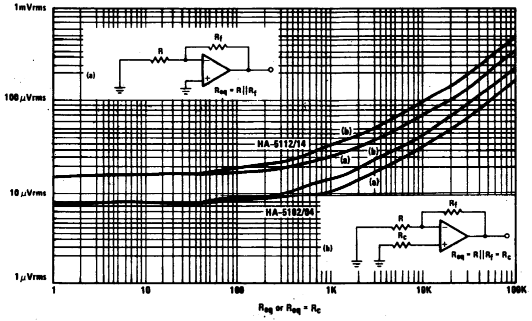


FIGURE 3a. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 0.1Hz-50KHz for HA-5102/04 and 0.1Hz-250KHz for HA-5112/14.

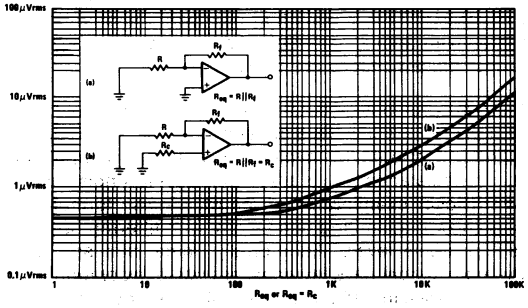


FIGURE 3b. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 20Hz-20KHz for HA-5102/04/12/14.

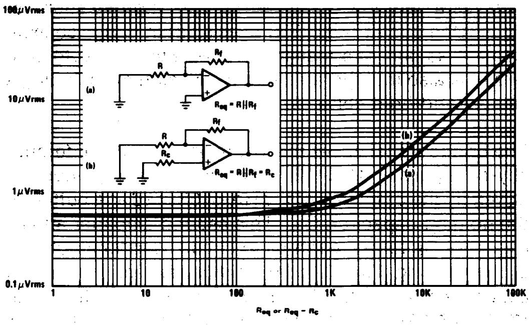


FIGURE 3c. PREDICTED NOISE

Predicted RMS noise at output for bandwidth of 20Hz-100Hz for HA-5102/04/12/14.

RMS noise is derived in part as the integral of the noise density spectrum over a given bandwidth. Below is the complete expression...

$$E_{rms} \text{ (from } f_0 \text{ to } f_1) = \sqrt{\int_{f_0}^{f_1} E_{\substack{\text{noise}\\\text{density}\\\text{spectrum}}}^{2}\, df}$$

The strict integration assuming E_n is constant works well for f_0 above ≈1KHz. Both the amplifier's noise voltage and the noise current increase for frequencies below 1KHz. This makes for difficult integration since complicated expressions for I_{noise} and E_{amp} must be generated. To avoid this problem, graphical integration techniques or sampled methods can be used with great success.

The curves in Figures 3a-3c illustrate the relationship between the RMS noise and R_{eq} for both amplifier designs. It should be apparent from the predicted RMS noise curves that increased bandwidth causes an increase in noise voltage. An interesting effect of this relationship is that only absolute bandwidth (f_1-f_0) is important. The general frequencies of interest (if they are above 1KHz) are irrelevant. More simply, 100Hz of bandwidth near 10KHz contains as much noise as 100Hz of bandwidth near 1MHz. This implies that bandwidth should be restricted with appropriate high and low pass filtering, if the lowest noise voltages are to be attained.

From the previous discussion, it is apparent that low noise designs require low resistor values. This is not to say that high gain should be avoided, just that low input and source resistance values are required for low noise operation. Closer examination of the RMS noise formula will also show that limiting bandwidth, with filtering, will also reduce noise levels. Additionally, metal film and wirewound resistors have lower excess noise (a component of resistor noise in addition to thermal noise) than carbon resistors and are therefore preferred.

Applications

Electronic scales have come into wide use and the HA-5102, as a very low noise device, can improve such designs. One circuit (Figure 4) uses a strain gauge sensing element as part of a resistive Wien-bridge. An auto-zero circuit is also incorporated into this design by including a sample-and-hold network.

The bridge signal drives the inverting input of a differentially-configured HA-5102. The non-inverting input is driven by the other half of the HA-5102 used as a buffer for the holding capacitor, C_h. This second amplifier and its capacitor C_h form the sampling circuit used for automatic output zeroing. The 20Kohm resistor between the holding capacitor C_h and the input terminal, reduces the drain from the bias currents. A second resistor R_9 is used in the feedback loop to balance the effect of R_8. If R_7 is approximately equal to the resistance of the strain gauge, the input signal from the bridge can be roughly nulled with R_6.

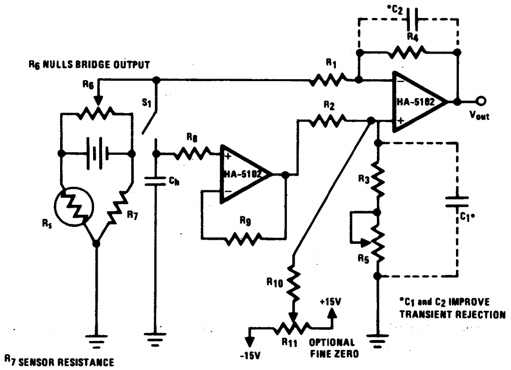


FIGURE 4.

Auto-zeroing scale circuit uses a strain gauge/bridge arrangement to improve sensitivity.

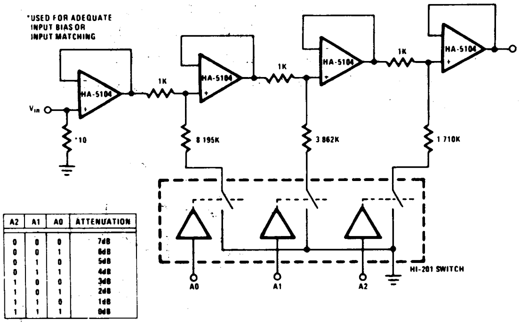
With very close matching of the ratio R_4/R_1 to R_3/R_2, the output offset can be nulled by closing S_1. This will charge C_h and provide a 0 volt difference to the inputs of the second amplifier, which results in a 0 volt output. In this manner, the output of the strain gauge can be indirectly zeroed. R_{10} and potentiometer R_{11} provide an additional mechanism for fine tuning V_{out}, but they may also increase offset voltage away from the zero point. C_1 and C_2 reduce the circuit's susceptibility to noise and transients.

The rise of digital equipment and computers, has created an entire realm of signal processing equipment. In most cases the computer requires elaborate circuitry to bridge over into the analog domain. The digitally programmable attenuator (Figure 5) is a rather simple circuit that still allows a great deal of control of analog signals.

The first stage is a simple buffer used to isolate the signal source from the attenuator stages to follow. Each of the subsequent stages is preceded by a voltage divider formed by two resistors and CMOS switch. Provided that the CMOS switch for each stage is "closed", the drive signal will be attenuated according to the basic voltage divider relationship at each stage. In the event a switch is "open" nearly all of the signal strength will be passed to the next stage through the 1K resistor. The amplifiers act as buffers for the divider networks and reduce interaction between stages. Eight levels of attenuation are possible with the circuit as illustrated in Figure 5, but more stages could be added. Each divider network must be closely matched to the resistor ratios shown or the level of attenuation will not match the levels in the logic chart.

Audio Applications

The HA-5102/04/12/14 series lends itself to audio designs. This is due in large part to the low noise characteristics of the series. With 4.0nV/$\sqrt{Hz}$ @ 1KHz, very low noise designs can be realized with little effort. This allows more attention to be placed on the quality of the designs.


*USED FOR ADEQUATE INPUT BIAS OR INPUT MATCHING
HA-5104
HA-5104
HA-5104
HA-5104
1K
1K
1K
V_{in}
V_{out}
*10
8 195K
3 862K
1 710K
A0
A1
A2
HI-201 SWITCH

A2	A1	A0	ATTENUATION
0	0	0	7dB
0	0	1	6dB
0	1	0	5dB
0	1	1	4dB
1	0	0	3dB
1	0	1	2dB
1	1	0	1dB
1	1	1	0dB

FIGURE 5.

Several resistors may be combined to obtain the precise resistor values used in this precision attenuator or a potentiometer may prove adequate.

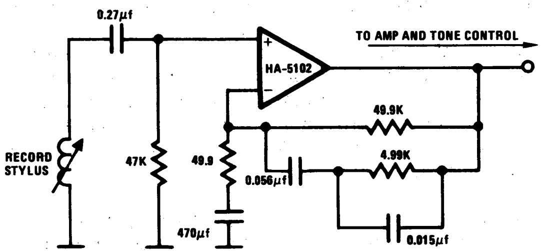

0.27μf
TO AMP AND TONE CONTROL
HA-5102
49.9K
4.99K
RECORD STYLUS
47K
49.9
0.056μf
470μf
0.015μf

FIGURE 7.

The RIAA amplifier provides industry standard signal correction for vinyl record recordings.

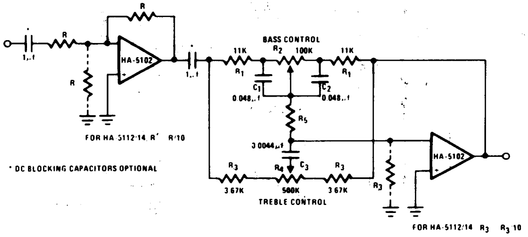

R
R
R
1μf
HA-5102
1μf
BASS CONTROL
11K
R_2 100K
11K
R_1
R_1
C_1
C_2
0.048μf
0.048μf
R_5
0.0044μf
C_3
R_3
R_4
R_3
3.67K
500K
3.67K
TREBLE CONTROL
R_3
HA-5102
FOR HA-5112/14 R' R/10
* DC BLOCKING CAPACITORS OPTIONAL
FOR HA-5112/14 R_3 R_3/10

FIGURE 6.

The tone correction circuit requires a low impedance driving source, yet it provides a great deal of control over the output waveform.

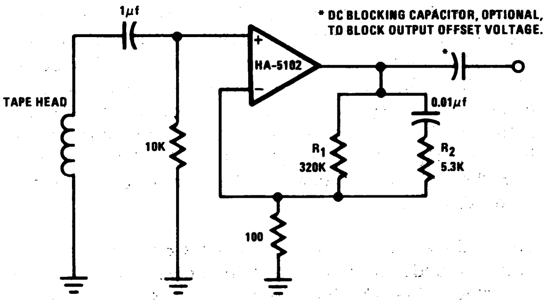

1μf
* DC BLOCKING CAPACITOR, OPTIONAL, TO BLOCK OUTPUT OFFSET VOLTAGE.
HA-5102
TAPE HEAD
10K
0.01μf
R_1 320K
R_2 5.3K
100

FIGURE 8. PROFESSIONAL AUDIO NAB TAPE PLAYBACK PREAMPLIFIER

This NAB tape playback preamplifier fully utilizes the speed, bandwidth, and noise features of the HA-5102.

The following group of designs point to some of the applications in which the HA-5102/04/12/14 series can improve performance without major circuit alterations. They depend, in part, on the ±20V/μSec slew rate of the HA-5112/14, which will allow a small signal to be passed without distortion up to 12MHz. The bandwidth of these devices is more than adequate for audio use. The HA-5102/04 will pass a full 10V signal out to 200KHz without distortion and at unity gain. Many other uses for these devices exist. The audio applications simply suggest the more likely uses for the series.

Tone correction of an audio signal is an application that relies on both the low distortion and the low noise of the HA-5102. The Baxandal-type circuit in Figure 6 uses input buffering because of the relatively low input impedance of the RC networks. The output stage is basically a summation amplifier with the high frequency contribution varied by the treble control and the low frequency by the bass control. The component values given in Figure 6 allow ±12dB of gain over the audio range.

One of the more common audio applications is signal correction for recording and playback. Several standard circuits are available and the HA-5102 should prove an excellent centerpiece for these. One such circuit is the RIAA preamplifier used to match the frequency characteristics of vinyl records and phonograph cartridges.

The RIAA circuit essentially provides low frequency boost below 318Hz and high frequency attenuation above 3150Hz. Recent modifications to the response standard include a 31.5Hz peak gain region to reduce DC oriented distortion from external vibration. The circuit in Figure 7 provides the desired response and with the extra amplifier of the HA-5102, the package can economically provide an additional stage of gain and isolation for a cleaner response and pickup.

The NAB (magnetic tape standard) amplifier circuits are also well suited for use with the HA-5102 (Figure 8). The NAB preamplifier is configured to provide low frequency boost to 50Hz, flat response to 3KHz, and high frequency attenuation above 3KHz. Compensation for variations in tape and tape head performance can be achieved by trimming R_1 and R_2.

The low noise characteristics of the HA-5102 family lead to low system noise and improved signal to noise ratios. This has become increasingly more important as the various recording mediums have progressed to the point of near perfection, at least so far as the ear is concerned.

At the other end of the audio spectrum, opposite the playback arena, is initial sound generation and the microphone. The HA-5104/14 is a very practical choice for a dynamic microphone preamplifier (Figure 9). The relatively simple design allows for DC coupling of both input and output.

The microphone sees an input impedance equal to $R_1 + R_2$ (2Kohm). The input impedance of the amplifier group is not matched to the 600ohm impedance of the microphone. This is because the instrumentation amplifier does not rely on input power, but rather input voltage alone for its driving source. In many cases the frequency range of the microphone will be extended with the reduced loading.

R_5, R_6, and R_7 provide stable DC gain in conjunction with R_3 and R_4, which form the DC feedback network around the first two amplifiers. R_7 also controls the DC offset at the output. R_8, R_9, and C_3 provide the proper AC gain above 0.6Hz. R_{14} is tuned for maximum CMRR by matching the feedback element ratios of the third amplifier $[R_{11}/R_{10} = (R_{13} + R_{14})/R_{12}]$. With a total gain of 4dB, the 2mV microphone signal is increased to the standard $1V_{rms}$ output.

The optional output stage provides a 600ohm matched output impedance to maximize the power transfer to the next stage. The HA-5104 and the HA-5114 will both function well in this circuit. There will, however, be an extra unused amplifier. To avoid this unused amplifier the tone correction circuit in Figure 6 is recommended for use with the fourth amplifier. If the HA-5114 is used, the DC gain resistors R' and R3' in Figure 6 must be used with the tone correction circuit to insured proper DC stability.

One of the most useful circuits in audio filtering is the Biquad. This universal filter offers low pass, high pass, band pass, band elimination, and all pass functions. The HA-5104 is an excellent choice for the four amplifier Biquad circuit in Figure 10. This is due in large part to the low noise and high slew rate characteristics of the HA-5104, both of which reduce distortion effects.

The Biquad consists of two successive integration stages followed by an inverting stage. The entire group has a feedback loop from the front to the back consisting of R_1 which is chiefly responsible for controlling the center frequency, ω_o. The first stage of integration is termed a "poor" integrator because of R_2 which limits the range of integration. R_2 and C form the time constant of the first stage integrator with R_3 influencing the gain (H) almost directly. The band pass function is taken after the first stage with the low pass function taken after the third stage. The remaining filter operations are generated by various combination of the three stages.

The Biquad is "orthogonally" tuned, meaning that ω_o, Q, and gain (H) can all be independently adjusted. The component values in Figure 10 will allow ω_o to range from 40Hz to 20KHz. The other component values give an adequate range of operation to allow for virtually universal filtering in the audio region. ω_o, Q, and gain (H) can all be independently adjusted by adjusting R_1 - R_3 respectively and in succession.

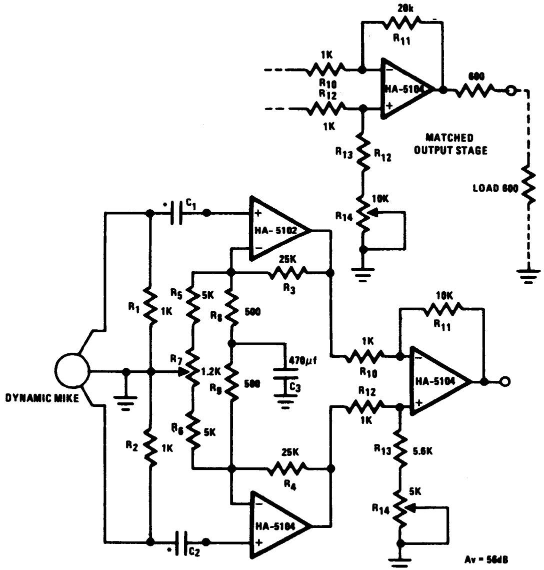
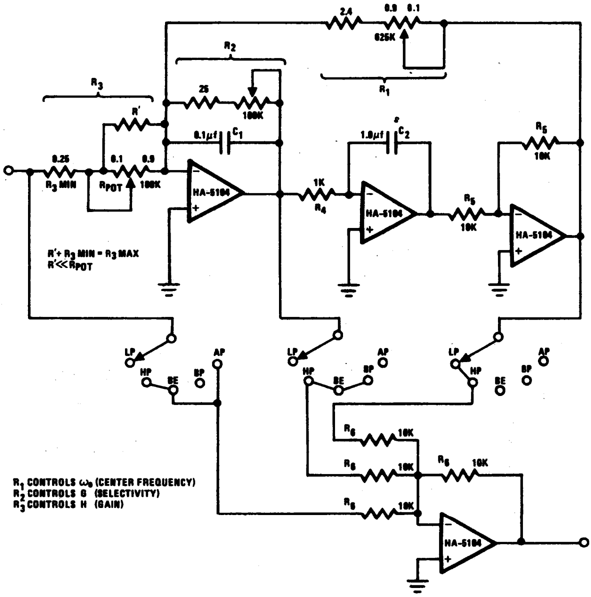

20k
R11
1K
R10
R12
1K
HA-5104
600
MATCHED OUTPUT STAGE
R13
R12
LOAD 600
10K
R14
C1
HA-5102
25K
R3
R5
5K
R1
1K
R8
500
470µf
C3
R7
1.2K
R9
500
DYNAMIC MIKE
R6
5K
R2
1K
25K
R4
HA-5104
C2
10K
R11
1K
R10
R12
1K
HA-5104
R13
5.6K
5K
R14
Av = 56dB

FIGURE 9.

The dynamic microphone preamplifier does not use a transformer which reduces both complexity and cost.


2.4
0.9 0.1
625K
R1
R2
25
100K
R3
R'
0.1µf
C1
0.25
R3 MIN
0.1 0.9
RPOT
100K
HA-5104
R'+ R3 MIN = R3 MAX
R'≪RPOT
1K
R4
1.0µf
C2
HA-5104
R5
10K
R5
10K
HA-5104
LP
AP
HP
BE
BP
R6 10K
R6 10K
R6 10K
R6 10K
HA-5104
R1 CONTROLS ω0 (CENTER FREQUENCY)
R2 CONTROLS Q (SELECTIVITY)
R3 CONTROLS H (GAIN)

The biquad offers a universal filter with ω_o, Q, and gain "orthogonally" tuned.

The standard Biquad circuit in Figure 10 uses three stages of inverting amplifiers. This produces negative feedback for stability (any odd number of stages would produce the same effect). There, however, is no restriction such that only inverting stages must be used. The standard Biquad of Figure 10 has been altered in Figure 11 by combining the function of the last two stages into one non-inverting integrator. This reduces the number of amplifiers required for the band pass function to just two. The bandpass transfer function is of course altered to reflect the consolidation of the last two stages and is as follows...

$$\frac{V3}{V1} = \frac{-R_1R_2R_3Cs}{(R_1R_2R_3R_4CC)s^2 + (R_1R_2R_3R_4C)s + 2R_2R_3}$$

$$= \frac{-(1/R_3C)s}{s^2 + (1/R_2C)s + 2/R_1R_4CC}$$

$$= \frac{+H\omega_o{}^2}{s^2 + (\omega_o/Q)s + \omega_o{}^2}$$

therefore....

$$\omega_o = \sqrt{2/R_1R_4CC}$$

$$Q = \sqrt{2R_2{}^2/R_1R_4}$$

$$H = -R_1R_4C/2R_3 \qquad \text{if } C_1 = C_2 = C$$

The two amplifier Biquad bandpass filter constructed around the HA-5102 can easily be incorporated into a ten band graphic equalizer. By restricting gain to ±12dB and requiring $Q \approx 1.7$, a very usable design can be generated. See Figure 12.

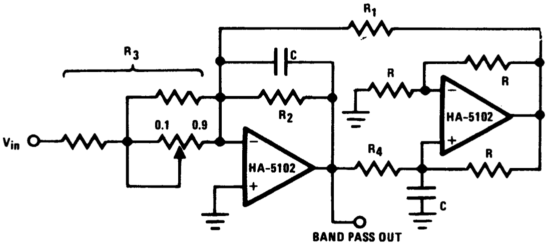


FIGURE 11.

The two amplifier biquad forms an economical band pass filter, which in this case is oriented towards a ten band equalizer.

A high signal to noise ratio is important in signal construction applications. The low noise aspect of the HA-5104 aids in lowering the system noise and thereby raises the system sensitivity. The signal combination circuit in Figure 13 incorporates input buffering with several other features to form a relatively efficient mixer stage.

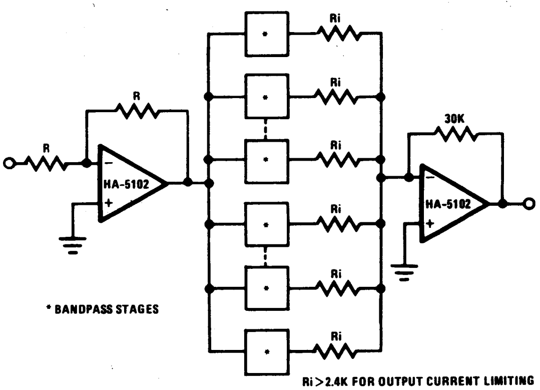


FIGURE 12.

The bandpass stages can be incorporated into a multiple band equalizer.

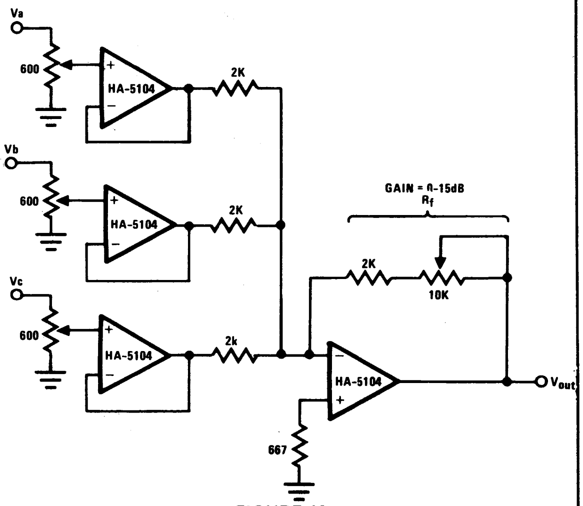


FIGURE 13.

The 600 ohm input impedance provides for proper audio level signal mixing using the HA-5104.

The circuit in Figure 13 uses buffer stages to prevent channel crosstalk back through the mixer resistor network. The potentiometers used for each stage allow for convenient signal strength adjustment while maintaining input impedance matching at the 600ohm audio standard. The feedback resistor R_f will permit the output signal gain to be as high as 15dB. The circuit in Figure 14 illustrates some of the other possible buffer combinations. These include a differential input stage, a voltage follower as well as both non-inverting and inverting stages. The allowable resistor ratios and recommended device types are also included. One restriction applies to this type of mixer network which is $R_g > 2.4$Kohm. This limits the worst case output current for each of the input buffers to less than 10mA.

The bulk of the HA-5102/04/12/14 series applications have involved audio uses. This does not represent the full range of application of the series. In general, most common amplifier applications, excluding video, could benefit from the group. The goal here was to introduce the designer to some of the more common and well know designs using the series, in hope of triggering interest for more exclusive uses.

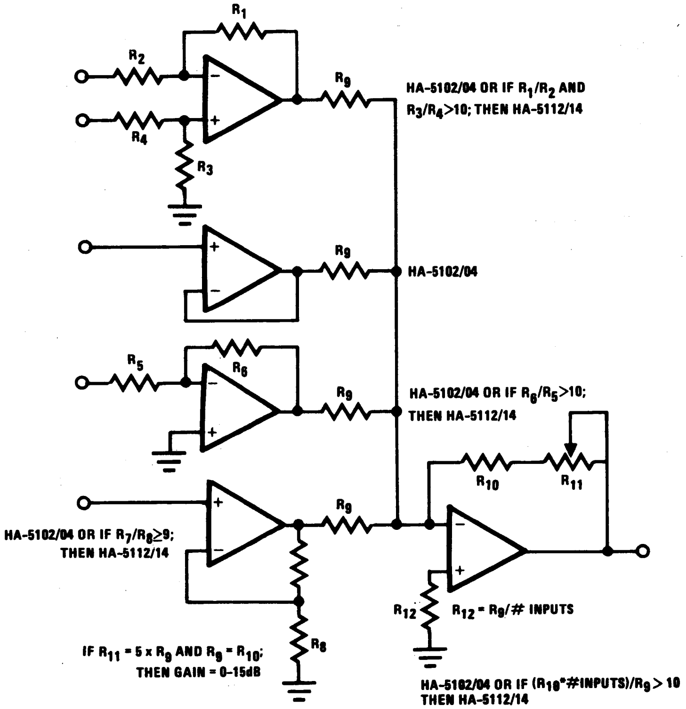

R_1
R_2
R_4
R_3
R_9
HA-5102/04 OR IF R_1/R_2 AND $R_3/R_4>10$; THEN HA-5112/14
R_9
HA-5102/04
R_5
R_6
R_9
HA-5102/04 OR IF $R_6/R_5>10$; THEN HA-5112/14
R_{10}
R_{11}
R_9
HA-5102/04 OR IF $R_7/R_8 \geq 9$; THEN HA-5112/14
R_{12}
$R_{12} = R_9/\#$ INPUTS
R_8
IF $R_{11} = 5 \times R_9$ AND $R_9 = R_{10}$; THEN GAIN = 0–15dB
HA-5102/04 OR IF $(R_{10} * \#\text{INPUTS})/R_9 > 10$ THEN HA-5112/14

FIGURE 14.

Universal mixer stage combines the more useable configurations of the HA-5102/04/12/14 family to meet most signal construction needs.

References

"D-C Amplifier Noise Revisited", Al Ryan & Tim Scranton Analog Dialog, 1969.

Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design, New York: John Wiley and sons, 1973.

Instruction Manual, model 2173C Transistor Noise Analyzer Control Unit. Quan-Tech, Division of KMS Industries. Whippany, New York.

M. E. VanValkenburg, Analog Filter Design, New York. Holt, Rinehart and Winston, 1982.

APP NOTE

FOR YOUR INFORMATION

No. 555

Harris Analog

ULTRA LOW BIAS AMPLIFIER, HA-5180

by Alan Wayne Hansford

Most amplifiers depend on the voltage at the inputs to determine the output voltage, and require a parasitic input bias current for proper operation. Typically these currents are in the μA range, but they needn't be so large. A very few devices fall into the ultra low bias current group which ranges from fA levels to a few pA. The HA-5180 is one of the few, with only 250fA of Bias current.

DC offset errors are created at the output of most amplifiers from the interaction of input bias currents with circuit resistances. If bias currents are significantly reduced, as with the HA-5180, the DC errors are also significantly reduced. This implies that with very low bias currents, larger resistances can be used without creating a DC error that exceeds normal bias current/resistance combinations. A great many high source impedance applications are only practical with some means of bias reduction, typically FET buffering. The ultra-low bias amplifiers, like the HA-5180, eliminate the need for FET buffering with its FET input stage. This makes the HA-5180 particularly well suited for atomic particle detectors and precision sampling circuits, to name two.

The outstanding features of the HA-5180 do not end simply at input bias current, but combine to form a very usable device. The Common Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio (PSRR) are both examples of this. The rejection of a common signal appearing at both input terminals of the device is 105dB (CMRR) and the rejection of power supply fluctuations is 110dB (PSRR). The open loop gain is a very respectable 1000KV/V. All of these outstanding features reflect the quality built into the HA-5180.

Given the type of device and the primary emphasis on low input bias currents, the HA-5180 has several other points worthy of praise. The basic speed of the device with a 2MHz bandwidth and a 7V/μSec slew rate, is above average and noteworthy for any amplifier. This becomes even more apparent in light of the low supply current (0.8mA). The relationship between supply current and speed usually implies that a high speed device requires a high supply current. Yet, the design of the HA-5180 has judiciously metered its use of available supply current to optimize speed at gains as low as unity.

Building Tips

The HA-5180 was designed with high performance in mind as indicated by its parameter list. The design enhancements did not stop at the drawing board however, and have been brought into the user's control. The most interesting development is the case connection to pin 8 of the can. By grounding the can through pin 8, a high level of shielding may be easily implemented. The effects of shielding should be further increased by using a grounding plane under the HA-5180. Both of these techniques will also improve the heat transfer away from the chip and package to extend the operational safety margins.

The remarkably low input bias currents are extremely important to many applications. They, in spite of their merit, can not stand alone in every circuit design. For this reason the voltage offset pins were included in the design of the HA-5180. With pins 1 and 5 (Figure 1), the offset voltage can be reduced below the very acceptable value of 100μV, establishing an amplifier with nearly ideal characteristics.

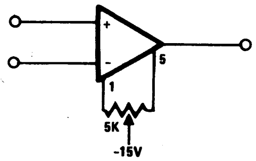


FIGURE 1.

Nulling the HA-5180s offset adjust to 0 volts brings it closer to the "ideal".

Low Noise Design

Since the HA-5180 is a moderately low noise operational amplifier, low noise design techniques must be used to make the most of this feature. There are two primary means of keeping noise down, one requires the amplifier inputs to look into low source resistances and the other requires bandwidth limiting by filtering. A short outline of noise prediction will be presented here to support these concepts.

Noise can be divided into several categories, which include thermal noise (white noise) and flicker noise (pink noise or 1/f noise). The feedback components are strongly dominated by thermal noise making thermal noise the most important of these from a system design standpoint (an exception to this are high gain DC amplifiers which require low 1/f noise as measured by the lower "1/f noise corner"). Flicker noise is more a function of the amplifier construction quality, and system design variations are less effective in reducing this type of noise.

Noise is usually rated in one of two ways. The first is RMS voltage or current (a measure of peak-to-peak noise in a given bandwidth) and the second is by noise density spectrum in $V/\sqrt{Hz}$ and $A/\sqrt{Hz}$ (a measure of the spectral content of the noise in the frequency domain). The two rating schemes are related, with RMS noise levels generated from the integration of the noise density spectrum over a desired frequency bandwidth.

As an illustration of noise prediction, the noise density for the standard inverting amplifier configuration (Figure 2a) will be determined. The total noise is derived from the combination of several noise sources, only three of which are of any significance. These are the amplifier's noise voltage, the thermal noise of the feedback components, and the noise generated by the current noise of the amplifier within the feedback components.

The total noise is defined as the square root of the sum of the squares of the individual noise terms.

$$E_n = G\sqrt{(E_{amp})^2 + (E_{\substack{\text{feedback}\\ \text{network}}})^2 + (E_{\substack{\text{current noise in}\\ \text{feedback network}}})^2}$$

E_n = total noise

G = gain of stage

E_{amp} = amplifier noise voltage.........$70nV/\sqrt{Hz}$ @ $f > 1KHz$

$$E_{\substack{\text{feedback}\\ \text{network}}} = \sqrt{4KTR_{eq}} \quad \text{where...} \quad K = 1.381E\text{-}23, \; T = 300, \; R_{eq} = R \,||\, R_f$$

$$E_{\substack{\text{current noise in}\\ \text{feedback network}}} = I_{noise} R_{eq}$$

$$I_{noise} = 0.01pA/\sqrt{Hz} \text{ @ } f > 1KHz$$

or more specifically . . .

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}R_{eq})^2}$$

Both the amplifier noise voltage and noise current are constant above 1KHz and rise slightly for lower frequencies (Figure 3). The resistor thermal noise is derived from the parallel combination of the feedback network (R_{eq}) and several constants (4KT). The third noise term again uses the equivalent resistance of the feedback network (R_{eq}) as well as the current noise generated at the input terminals of the amplifier.

It should be evident from the above formula that extremely large values of R_{eq} (usually over 10Kohm, but 1Megohm for the HA-5180) will dominate the noise density while low values for R_{eq} will yield to the amplifier's own noise characteristics. Note the asyptotic convergence of the noise voltages in Figures 4a-4c at low values of R_{eq}.

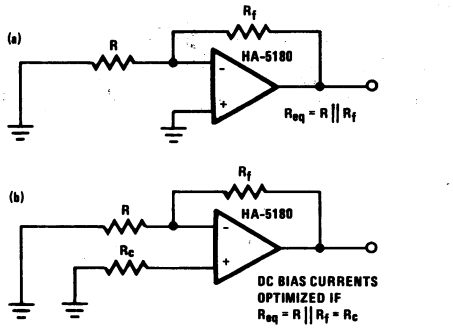


FIGURE 2. NOISE PREDICTION CIRCUITS

A reasonable estimate of noise levels can be generated with these two basic amplifier circuits.

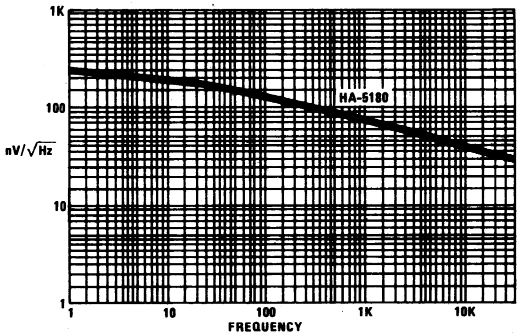


FIGURE 3. NOISE VOLTAGE

Due to the extremely low noise currents, only the voltage noise generates a significant contribution.

A second circuit (Figure 2b) balances the effects of input bias currents by placing a resistor R_C, equal to R_{eq}, between the non-inverting input and ground. While reducing DC errors, this configuration adds two additional terms to the noise formula.

$$E_n = G\sqrt{(E_{amp})^2 + R_{eq}4KT + (I_{noise}R_{eq})^2 + R_C\,4KT + (I_{noise}R_C)^2}$$

The original contributors to output noise remain as before and the additional terms represent the thermal contribution by R_C and the associated amplifier current noise seen through that resistor. To optimize DC design, $R_{in} \,||\, R_f = R_{eq} = R_C$, therefore the noise density equation reduces to ...

$$E_n = G\sqrt{(E_{amp})^2 + 2R_{eq}4KT + 2(I_{noise}R_{eq})^2}$$

Again the relationship between large values of R_{eq} and a high noise density spectrum remains.

RMS noise is derived in part as the integral of the noise density spectrum over a given bandwidth. Below is the complete expression...

$$E_{rms}\ (\text{from } f_0 \text{ to } f_1) = \sqrt{\int_{f_0}^{f_1} E_{\substack{\text{noise}\\\text{density}\\\text{spectrum}}}{}^2\, df}$$

The strict integration assuming E_n is constant works well for f_0 above ≈1KHz. Both the amplifier's noise voltage and the noise current increase for frequencies below 1KHz. This makes for difficult integration since complicated expressions for I_{noise} and E_{amp} must be generated. To avoid this problem, graphical integration techniques or sampled methods can be used with great success.

The curves in Figures 4a-4c illustrate the relationship between the RMS noise and R_{eq} for both amplifier designs. It should be apparent from the predicted RMS noise curves that increased bandwidth causes an increase in noise voltage. An interesting effect of this relationship is that only absolute bandwidth (f_1-f_0) is important. The general frequencies of interest (if they are above 1KHz) are irrelevant. More simply, 100Hz of bandwidth near 10KHz contains as much noise as 100Hz of bandwidth near 1MHz. This implies that bandwidth should be restricted with appropriate high and low pass filtering, if the lowest noise voltages are to be attained.

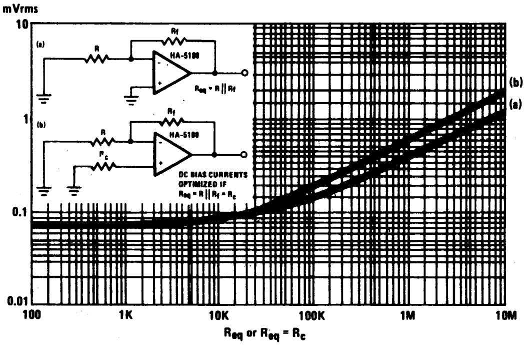


FIGURE 4a. PREDICTED NOISE

Predicted RMS noise at output of HA-5180 for a bandwidth of 0.1Hz-110KHz.

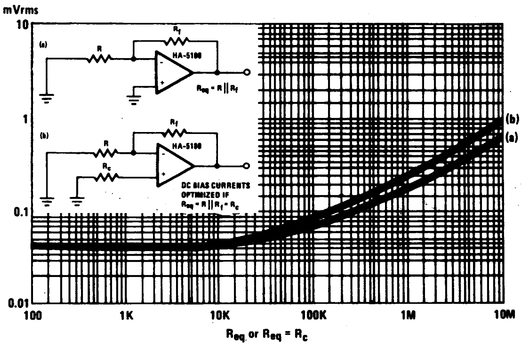


FIGURE 4b. PREDICTED NOISE

Predicted RMS noise at output of HA-5180 for a bandwidth of 20Hz-20KHz.

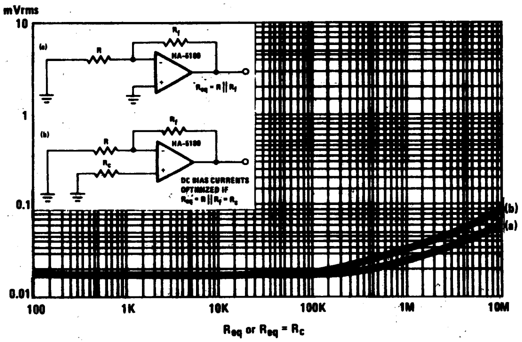
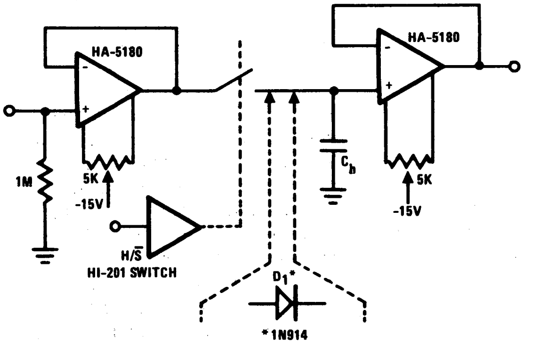


FIGURE 4c. PREDICTED NOISE

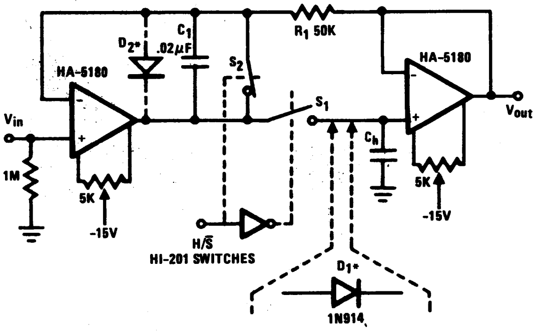
Predicted RMS noise at output of HA-5180 for a bandwidth of 20Hz-100Hz.



*Diode used for S/H peak detector

FIGURE 5a.

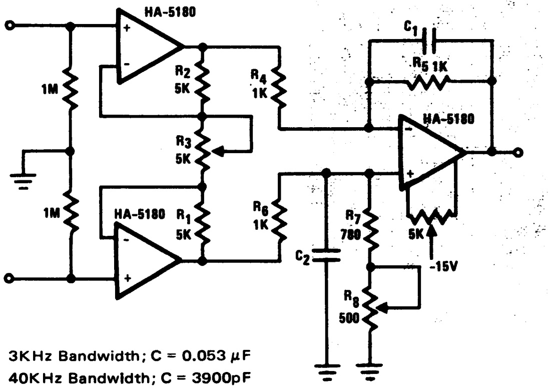
"Fast" sample-and-hold must be nulled using the offset potentiometers but offers very short aquisition times.



*Diodes used for S/H peak detector

FIGURE 5b.

"Precision" sample-and-hold is an excellent use of the HA-5180, but, because of the extended feedback, has greater overshoot.



3KHz Bandwidth; C = 0.053 µF
40KHz Bandwidth; C = 3900pF

FIGURE 6.

The standard three amplifier instrumentation configuration gives a multimeter preamplifier extremely high input impedance.

From the previous discussion, it is apparent that low noise designs require low resistor values. This is not to say that high gain should be avoided, just that low input and source resistance values are required for low noise operation. Closer examination of the RMS noise formula will also show that limiting bandwith, with filtering, will also reduce noise levels. Additionally, metal film and wirewound resistors have lower excess noise (a component of resistor noise in addition to thermal noise) than carbon resistors and are therefore preferred.

Applications

One of the most critical applications, relative to input bias currents, is the sample-and-hold. The HA-5180 requires such a low input bias current (250fA) that the drain on holding capacitors is all but eliminated. Figure 5 illustrates both a "precision" sample-and-hold as well as a "fast" sample-and-hold. Both circuits buffer the input voltage and the sampled voltage on C_h.

The "precision" circuit achieves a lower error voltage by closing the feedback loop around both amplifiers. This adds a delay to the feedback signal and increases the overshoot. The DC error voltages are reduced in this configuration and can be reduced further with the V_{OS} offset nulling potentiometers, hence the term "precision". C_1 improves transient response while R_1 provides isolation of the input and the output during the hold cycle. S_1 determines whether the holding capacitor C_h follows the input voltage or holds a previous value. The necessary feedback to the input buffer is provided by S_2 during the hold operation. D_1 converts the sample-and-hold into a peak voltage sample-and-hold. D_2 reduces the reverse saturation of the input buffer when used in the peak mode.

The "fast" sample-and-hold incorporates feedback around each amplifier separately. This makes for a much faster response, but does tend to increase DC error voltages. The effects of DC offset can be minimized with the V_{OS} offset nulling potentiometers. As with the precision sample-and-hold, S_1 controls the charging and holding operation of the holding capacitor C_h. D_1, as before, converts the circuit into a peak voltage sample-and-hold.

Like the sample-and-hold, the differential instrumentation amplifier relies on extremely high input impedance for effective operation. The HA-5180 with its JFET input stage, performs well as a multimeter preamplifier (Figure 6). The standard three amplifier configuration is used with very close matching of the resistor ratios R_5/R_4 and $(R_7 + R_8)/R6$, to insure high common mode rejection (CMRR). The gain is controlled through R_3 and is equal to $2R_1/R_3$. Additional gain can be had by increasing the ratios R_5/R_4 and $(R_7 + R_8)/R_6$.

The capacitors C_1 and C_2 improve the AC response by limiting the effects of transients and noise. Two suggested values are given for maximum transient suppression at frequencies of interest. Some of the faster

DVM's are operating at a peak sampling frequency of 3KHz, hence the 4KHz low pass time constant. The 40KHz low pass time constant for AC voltage ranges is an arbitrary choice, but should be chosen to match the bandwidth of the other components in the system. C_1 and C_2 may however, reduce CMRR for AC signals if not closely matched. Input impedances have also been added to provide adequate DC bias currents for the HA-5180 when open circuited.

Sensors And Transducers

Most passive transducers and sensors vary in resistance relative to light, sound, pressure, etc. Often the average resistance of the transducer is quite large. This presents a problem in the choice of an amplifier, since bias currents are typically high enough to create a significant error voltage ($V_{error} = I_{bias} \; R$). Extremely low input bias currents of the HA-5180 minimize this effect for the most part and allow for more conventional transducer and sensor circuits.

The circuit in Figure 7 uses a light sensitive cadmium sulfide cell to form a crude light level detecton module. If R, the sensor matching resistor, is equal to the "dark" resistance of the cadimum sulfide cell, the amplifier output will range from 0 volts to ≈12 volts as the light level ranges from "dark" to "bright". The circuit in Figure 8 operates in a similar manner but use the standard non-inverting configuration instead of the voltage follower configuration. This allows for variable gain. Although the "dark" resistance of the cadmium sulfide cell is only ≈7Kohms, the principles of operation apply to other types of detectors which require the high input impedance of the HA-5180 for reasonable linearity and useability.

An example of a high resistive value sensor that depends heavily on high amplifier input impedance is the pH probe and Detector, with the average probe resistance on the order of 100Megohms. The circuits in Figures 7 and 8 may still be used with this type of transducer, but a bridge circuit may prove more appropriate (Figure 9). The greatest sensitivity is achieved if R_1 is approximately equal to the probe resistance. The circuit can be "zeroed" with R_2 while the full scale voltage is controlled by R_5. The correlation between pH and output voltage may not be linear, which would necessitate a shaping circuit. A calibration scheme, using solutions of known pH, may prove adequate and more reliabile over a period of time due to probe variance.

The general schematic could be applied to strain gauges or any other type of resistive sensor. The key is the extremely low input bias current required by the HA-5180, which allows higher value resistances to be used without producing significant error voltages. This leads to more conventional designs with less exotic circuitry.

Along the same lines as the pH meter and light level detector, is the photo-diode current to voltage converter (Figure 10). One common use of this type of device is as a light to voltage converter for densitometers. This circuit depends on the light level/current relationship of a photo-diode. Since the diode will only pass as much current as the light level will allow, the diode becomes a light controlled current sink. A current source is summed along with the photo-diode current, and a difference current appears at the input of the HA-5180. Relying on ideal amplifier input impedance, which is nearly the case with the HA-5180, all of the difference current is applied to R_f. The output is then defined as . . .

$$V_{out} = (I_{ref} - I_d)R_f$$

Several current sources may be used. The simplest is a resistor with $I = (V_{CC} - V_{be})R$. A more accurate current source is the two transistor current mirror, where $I = (V_{CC} - V_{be})/R_{ref}$ (Figure 10). Since the controlling component, R_{ref}, is not in the current path for I, a more accurate summation at the amplifier input terminal can take place. The stage can be zeroed with R or R_{ref} as the case may be. The nulling potentiometer will provide the fine zero.

The precision integrator is a classic circuit which can also benefit from the JFET inputs of the HA-5180. The traditional relationship between C and R holds very well in one

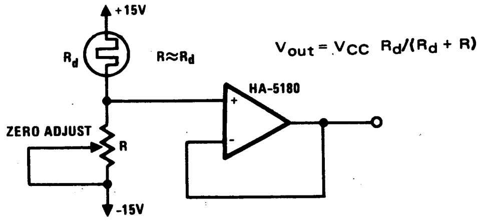


FIGURE 7.
Cadmium Sulfide cells control two light detection circuits.

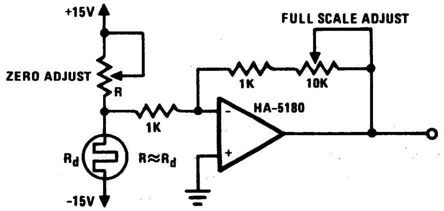
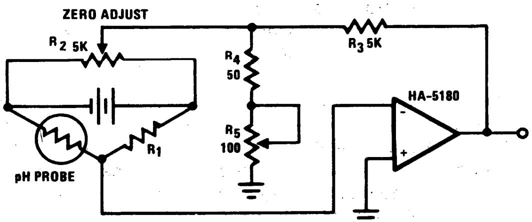


FIGURE 8.
Cadmium Sulfide cells control two light detection circuits.



$R_1 \approx R_{PROBE} \approx 100$Megohm

FIGURE 9.
Another popular sensor circuit is the bridge network. The pH probe can be replaced with nearly any resistive sensor.

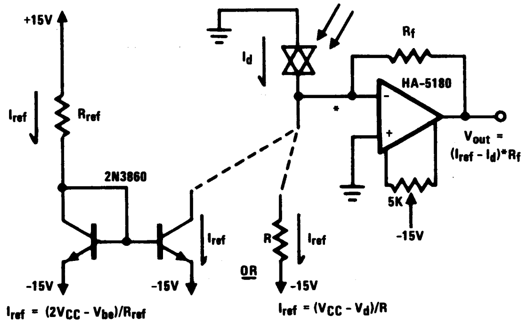

+15V
I_{ref}
R_{ref}
2N3860
-15V
-15V
I_{ref}
R
I_{ref}
OR
-15V
I_d
R_f
HA-5180
*
V_{out} = $(I_{ref} - I_d)*R_f$
5K
-15V
$I_{ref} = (2V_{CC} - V_{be})/R_{ref}$
$I_{ref} = (V_{CC} - V_d)/R$

FIGURE 10.

The low bias currents of the HA-5180 provide a nearly ideal summing point (*) for the circuit currents in this photo-diode current to voltage converter.

design (Figure 11), since the drain on C by the amplifier is so small. A second HA-5180 has been incorporated into this design to allow a threshold voltage to be adjusted. The threshold voltage is set while present at the input with S_1 and S_2 closed. S_1 is opened before S_2, then S_3 is closed momentarily to reset the output voltage. The stage will then take the time integral of the input signal relative to the threshold voltage. R_2 provides stable gain during the threshold setting procedure. The nulling potentiometer reduces the effects of V_{OS}.

The precision integrator can be converted into a precision timer with a few modifications. The reset switch used to discharge the capacitor C is used as the timer on reset switch. The output will be proportional to the elapse time as long as the input voltage is constant and not equal to the threshold voltage. If the timer needs a hold function, a switch must be inserted to isolate the capacitor C from the resistor R.

Many signal processing applications depend on low amplifier bias currents for their operation. One such design involves logarithmic amplifiers (Figure 12). The input sensitivity is governed by the system bias currents in such a circuit. The HA-5180, with its low input bias currents, can extend the sensitivity of the logarithmic current to voltage converter. The specific application may well be an atomic particle counter in which the current from the detector is converted into a voltage. For the design in Figure 12 the output voltage is defined as ...

$$V_O = -V_t(R_3 + R_4)/R_3 \ln[I_{in}/I_{ref}];\ \text{where } V_t = 0.0259\text{V}.$$

Using the schematic values, the expression reduces to .....

$$V_O = -\ln[2000 I_{in}]$$

This is a typical matched transistor pair logarithmic amplifier. The matching removes a constant from the output expression and improves temperature stability. The temperature stability will be even greater if R_t varies inversely with temperature.

The input range of this circuit can be extended by using another HA-5180 as a current preamplifier to the logarithmic converter, as shown in Figure 12.

The HA-5180 is an extremely powerful building block. The sample-and-hold and the precision integrator are examples of the low drain placed on circuit capacitors by the bias currents. The bias currents themselves are nearly low enough to class the HA-5180 as an "ideal amplifier" in that respect. The transducer applications illustrate the HA-5180's merit in this area. The list of applications and uses could continue on, but the material presented should allude to the general applications and uses of the HA-5180.

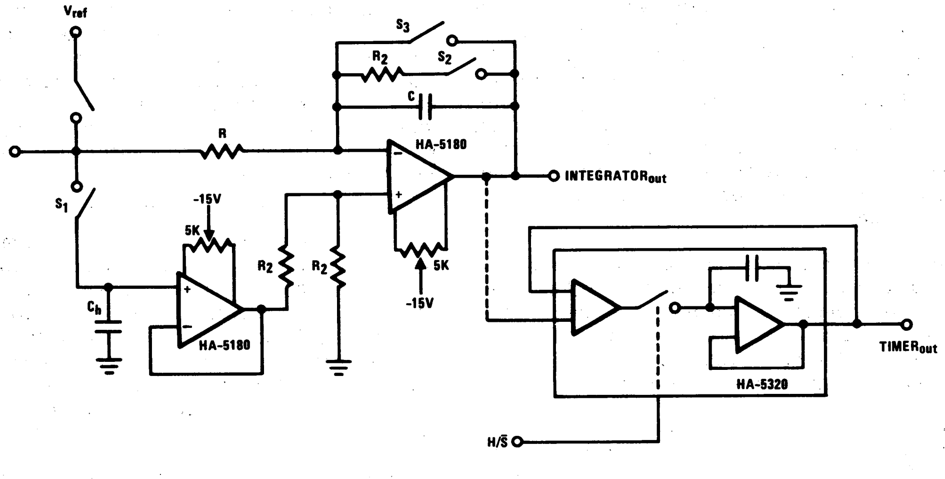


FIGURE 11.

S_1 and S_2 when closed, provide a threshold settling for this precision integrator while S_3 allows the output to be reset.

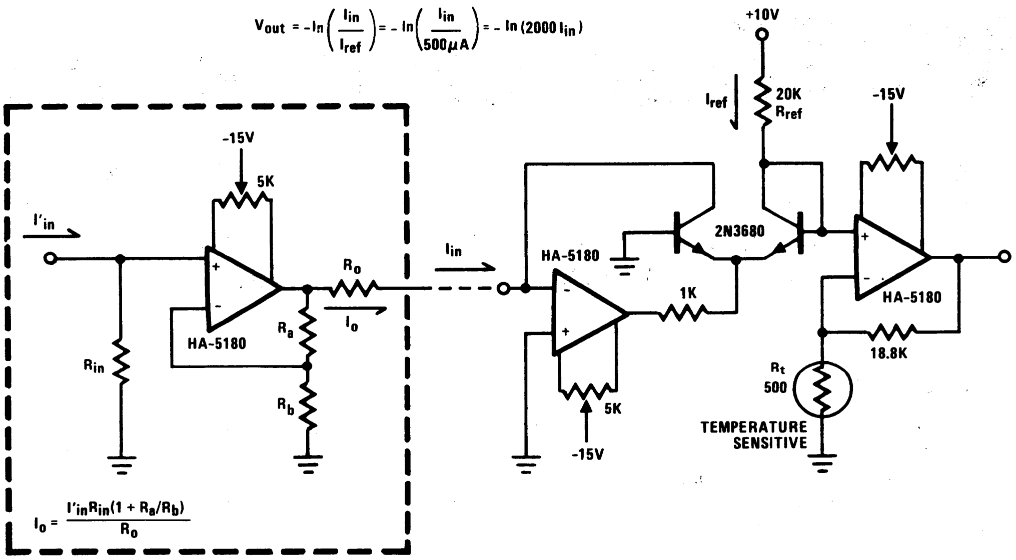

$V_{out} = -\ln\left(\frac{I_{in}}{I_{ref}}\right) = -\ln\left(\frac{I_{in}}{500\mu A}\right) = -\ln(2000\,I_{in})$
+10V
I_{ref}
20K
R_{ref}
-15V
-15V
5K
I'_{in}
I_{in}
HA-5180
2N3680
R_o
I_o
R_a
HA-5180
R_{in}
R_b
1K
HA-5180
18.8K
R_t
500
5K
-15V
TEMPERATURE SENSITIVE
$I_o = \frac{I'_{in}R_{in}(1 + R_a/R_b)}{R_o}$

FIGURE 12

Logarithmic current to voltage converter depends on the low bias currents of the HA-5180 for accuracy.

References

"D-C Amplifier Noise Revisited", Al Ryan & Tim Scranton Analog Dialog, 1969.

Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design, New York: John Wiley and sons, 1973.

Instruction Manual, model 2173C Transistor Noise Analyzer Control Unit. Quan-Tech, Division of KMS Industries. Whippany, New York.

APP NOTE

FOR YOUR INFORMATION

No. 560

Harris Analog

APPLYING THE HY-9590 ANALOG DATA ACQUISITION SIGNAL PROCESSOR

By John E. Sullivan

INTRODUCTION

The HY-9590 Analog Data Acquisition Signal Processor is a powerful building block for use in a Data Acquisition Subsystem (DAS), or in stand-alone operation. Incorporating a differential analog multiplexer, a programmable gain instrumentation amplifier and track and hold amplifier, the HY-9590 is an ideal signal conditioning element for a wide range of commercial, industrial and military applications.

FUNCTIONAL OPERATION OF THE HY-9590

As illustrated in Figure 1, the HY-9590 incorporates three primary components. An input multiplexer controls selection of the signal to be processed, the programmable gain instrumentation amplifier provides common mode signal rejection and gain while the track and hold amplifier stores the instantaneous signal level for final signal processing. Signal acquisition, including multiplexer, amplifier, and track and hold settling times, is less than $10\,\mu s$ to 0.01% accuracy.

The multiplexer selects one of eight possible differential analog input signals to be processed, or it can be disabled to the high impedance state. All analog input lines have full overvoltage protection and can tolerate inputs up to 20 volts in excess of the power supply voltages for extended periods and transient spikes up to several hundred volts.

Expansion lines, MUX OUT A and MUX OUT B, can be used either to expand the number of input channels or as monitor outputs. The multiplexer exhibits a nominal 1.2 kilohm ON resistance; therefore, when using MUX OUT A or MUX OUT B as monitor points, a high impedance monitor (> 1 megohm) should be used to minimize loading affects.

Select lines A_0, A_1 and A_2 operate in binary mode (000 selects channel 1 and 111 selects Channel 8). The enable line, when LOW, DISABLES the multiplexer and forces its output to the high impedance state. Both the select and enable lines have an operating range of V- to +0.8 volts for a logic 0 input and 4 volts to V+ for a logic 1 input. When driving these inputs with TTL logic, a 1K ohm pullup resistor is recommended to ensure proper switching. All unused inputs (both signal and control) can be hardwired to either V- or ground for a logic 0 and +5 volts (V_{CC}) or V+ for a logic 1.

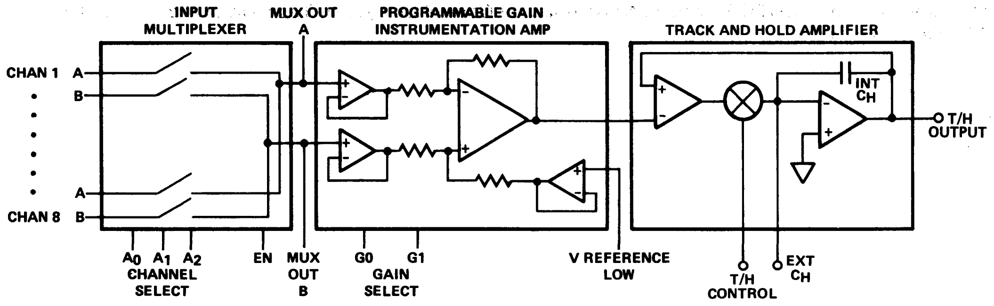


FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM

PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

The programmable gain instrumentation amplifier (PGA) operates in the true differential mode with A input signals being inverted and B input signals being noninverted. Some applications will have true differential input signals with an infinite impedance to ground. These applications should incorporate a 5 megohm resistor to ground from both the MUX OUT A and MUX OUT B outputs to allow amplifier bias currents to flow to ground.

The PGA has digitally selectable gains of -1, -2, -4 and -8 in binary format (00, G= -1; 11, G=-8). The digital control levels are identical to those of the input multiplexer, and as such require 1k ohm pullup resistors when driven from TTL logic.

The V_{REF} LOW line can be tied to ground or used for offset nulling as illustrated in Figure 2. Other configurations such as level shifting or quasi-differential outputs can also be implemented as shown in Figure 5.

TRACK AND HOLD AMPLIFIER

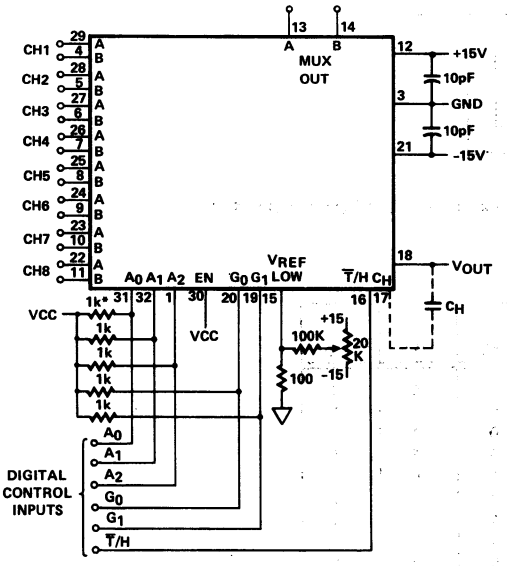
The track and hold amplifier stores and holds the instantaneous signal level applied to its input when the T/H line goes to a logic 1. The T/H mode control is fully TTL compatible and requires no pullup resistor, with the track mode defined as -5 to +0.8V and the hold mode defined as +2 to +7 volts.

This device includes an internal 100pF hold capacitor for fast acquisition time. For some applications, an external hold capacitor may be added to reduce droop rate and pedestal error at the expense of acquisition time. This capacitor should be selected for minimum dielectric absorption and leakage as found in teflon or polystyrene types.

The hold capacitor terminal (pin 17) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane. This is to prevent errors caused by nearby signal lines or power supply voltages.

Figure 3 illustrates the typical track and hold performance as a function of the hold capacitor. As the hold capacitor increases, the acquisition time also increases and the droop rate hold step error decreases.

The hold step voltage error is also a constant magnitude over the DC input range as shown in Figure 4. This error may be nulled out by using the V_{REF} output circuit as shown in Figure 2.



*THESE PULLUP RESISTORS ARE USED WHEN INTERFACING TTL LOGIC ONLY.

$V_{OUT} = G(B - A) + V_{REF}$
$G = -1, -2, -4, -8$

FIGURE 2 – TYPICAL CONFIGURATION

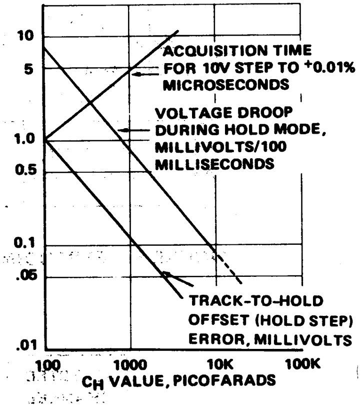


FIGURE 3 – TYPICAL TRACK AND HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR

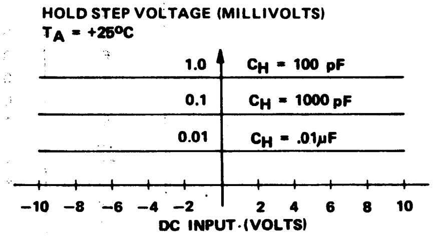


FIGURE 4 – HOLD STEP vs. INPUT VOLTAGE

APPLICATION HINTS

1. Expanding the Channel Capacity of the HY-9590

Figure 5 illustrates a typical HY-9590 with its channel capacity increased from 8 to 16 channels. Further expansion can easily be implemented by adding more address lines (each additional address line doubles the channel capacity) and the required control logic to enable each multiplexer. The limiting factor determining the number of additional multiplexers that can be used, is the parasitic capacitance caused by each additional multiplexer.

2. The HY-9590 in a Two-Chip DAS

The HY-9590, when teamed with the HI-674A A/D converter as illustrated in Figure 6 will provide a two-package DAS with 12-bit accuracy and a 65kHz throughput rate. The gain selection of the HY-9590 gives this system a dynamic range of 15 bits.

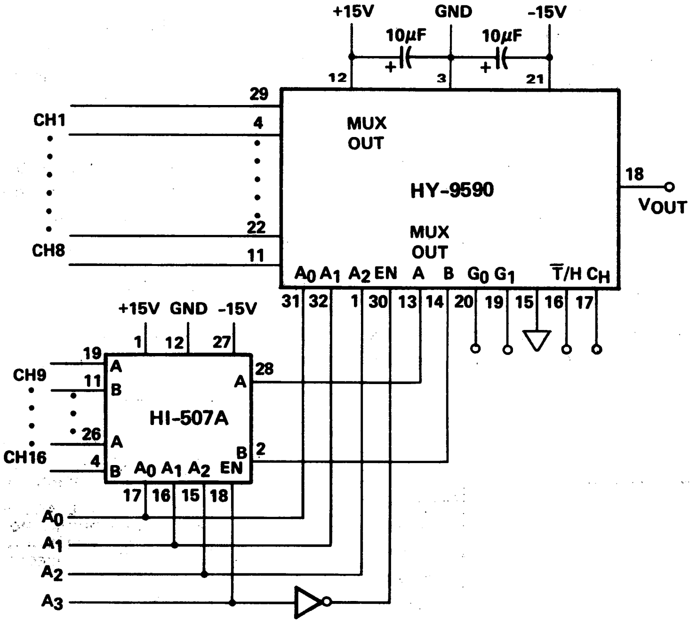

+15V
GND
-15V
10μF
10μF
+
+
12
3
21
29
CH1
4
MUX OUT
HY-9590
18
VOUT
22
MUX OUT
CH8
11
A0 A1 A2 EN A B G0 G1 T/H CH
31 32 1 30 13 14 20 19 15 16 17
+15V GND -15V
1 12 27
19
A
CH9
11
B
28
A
HI-507A
26
A
CH16
4
B
A0 A1 A2 EN
B
2
17 16 15 18
A0
A1
A2
A3

FIGURE 5 – EXPANDING THE HY-9590 TO 16 INPUT CHANNELS

SELECTED CHANNEL	A_3	A_2	A_1	A_0
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0
12	1	0	1	1
13	1	1	0	0
14	1	1	0	1
15	1	1	1	0
16	1	1	1	1

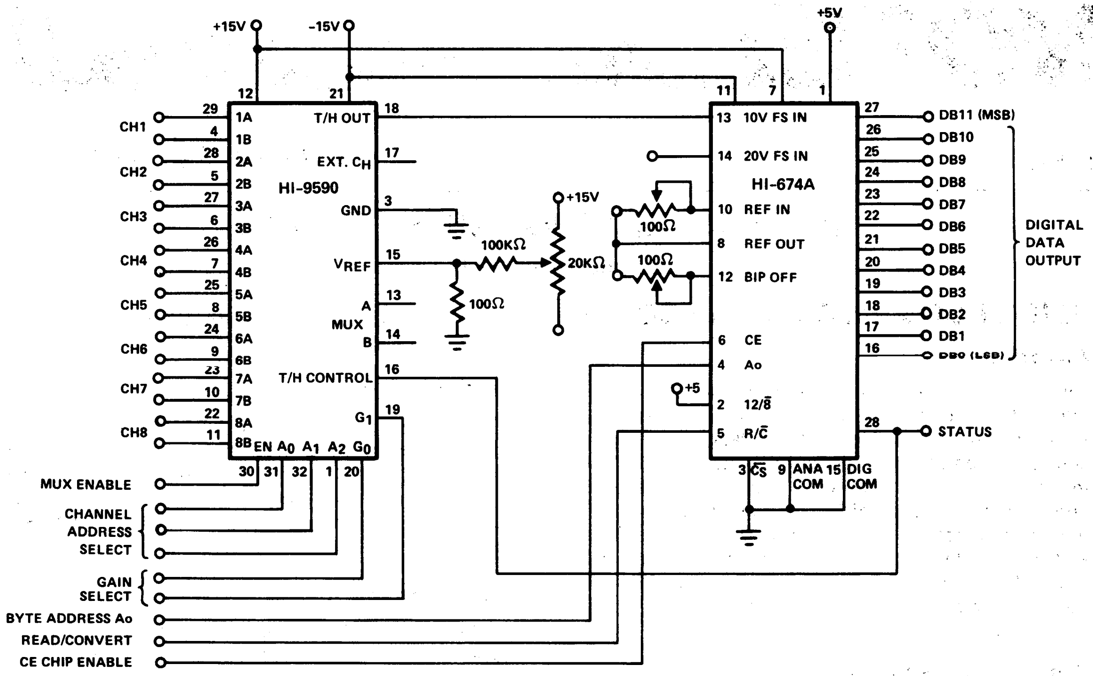

+15V
-15V
+5V
12
21
11
7
1
CH1
CH2
CH3
CH4
CH5
CH6
CH7
CH8
29
4
28
5
27
6
26
7
25
8
24
9
23
10
22
11
1A
1B
2A
2B
3A
3B
4A
4B
5A
5B
6A
6B
7A
7B
8A
8B
HI-9590
T/H OUT
18
EXT. C_H
17
GND
3
V_{REF}
15
A
13
MUX
B
14
T/H CONTROL
16
G_1
19
EN
A_0
A_1
A_2
G_0
30
31
32
1
20
+15V
100KΩ
20KΩ
100Ω
100Ω
100Ω
HI-674A
13 10V FS IN
14 20V FS IN
10 REF IN
8 REF OUT
12 BIP OFF
6 CE
4 Ao
+5
2 12/$\overline{8}$
5 R/$\overline{C}$
3 $\overline{CS}$
9 ANA COM
15 DIG COM
27
26
25
24
23
22
21
20
19
18
17
16
28
DB11 (MSB)
DB10
DB9
DB8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0 (LSB)
DIGITAL DATA OUTPUT
STATUS
MUX ENABLE
CHANNEL ADDRESS SELECT
GAIN SELECT
BYTE ADDRESS Ao
READ/CONVERT
CE CHIP ENABLE

FIGURE 6 – DATA ACQUISITION SYSTEM (USING ONLY 2 PACKAGES)

APP NOTE

FOR YOUR INFORMATION

No. 570

Harris Analog

UNDERSTANDING CODEC TIMING

D. J. Donovan and G. R. Davis

5510/11 COder/DECoder or CODEC

Introduction

Owing to the inherent complexity of CODEC designs, interpretation of functional descriptions and especially timing diagrams one might find in data sheets may be somewhat confusing. To better understand CODEC timing, this application note will provide a comprehensive and clear interpretation of CODEC timing sequences, and modes of operation. Application No. 574, Understanding PCM Coding, by D. J. Donovan is a suggested companion to this Application Note. To facilitate maximum comprehension, some key terms must be defined and understood.

Frame (Refer to Timing Diagram 1)

A frame is a repetitive group of PCM data that is the result of a single sampling of all voice channels, plus additional bit(s) for synchronization. The data rate determines the frames structure as follows:

USA (μ Law) Japan	8 bits/channel x 24 channels + 1 sync bit = 193 bits/frame x 8000 samples/sec. = 1.544MHz data rate. The HC-5510 uses μ-law coding.
Europe (A Law)	8 bits/channel x 32 channels = 256 bits/frame x 8000 samples/sec. = 2.048MHz data rate. The HC-5511 uses A-law coding.

Frame Synchronization Pulse FS_X, FS_R
(Refer to Timing Diagram 2)

The frame synchronization (frame sync) pulse is an 8kHz signal of varying duty cycle that determines the beginning of a frame. Assuming a 1.544MHz μ Law system, each frame contains 192 bits of voice data plus one bit for synchronization (from equation above). The digitized voice data is derived from multiplexing 24 separate voice channels, each of which is assigned one of 24 time slots by a system controller through a shared CODEC. Each time slot contains 8 bits of information representing one voice sample encoded by a CODEC.

The frame sync pulse must be used in conjunction with and synchronous to a master clock. The relationship of frame sync pulse edges to the master clock determines when PCM data is transferred onto the D_X data transmit bus or received from the D_R data receive bus.

Time Slot (Refer to Timing Diagram 1)

A Time Slot is that segment of time between two frame pulses where a CODEC is selected to encode or decode. Each time slot contains 8 bits of PCM data, the result of a single sample of one channel (CODEC). Transmit (D_X) and receive (R_X) may operate with different time slot assignments.

Time Slot Modes

The 5510/11 CODEC may operate in one of two time slot modes: a time slot assignment mode; or a fixed time slot mode.

Time Slot Assignment
(Refer to Timing Diagram 2)

Each CODEC must be assigned a time slot in which to operate. A CODEC may be assigned only one time slot during one frame period. Time slots are assigned by the pulsing of the CLKC pin, eight times within a 125μs period, while 8 bits of serial data are input on the DC pin, the serial control data input pin of the CODEC. The first two bits of serial data at DC setup the encoder, the decoder or both, for time slot assignment, and the remaining 6 bits tell the CODEC what time slot it is assigned (Refer to Table 1). A new time slot may be assigned every other frame.

Fixed Time Slot (Refer to Timing Diagram 3)

The CODEC may be operated in a mode such that the time from the beginning of a frame sync pulse to the point where PCM data is transferred onto the PCM highway does not change. The fixed time slot is normally time slot 1, which corresponds to the eight $CLK_{X/R}$ cycles starting one cycle from the nominal leading edge of FS_X or FS_R, respectively. The PCM data appears on D_X after the start of the frame sync pulse FS_X, and immediately after the rising edge of $CLK_{X/R}$ (see photo below). To operate in this mode, CLKC should be open or tied to VCC and the DC Pin, toggled to either power down the CODEC, or to assign time slot 1 to the encoder and the decoder (refer to Table 1). The photo below illustrates typical CODEC timing and PCM data (D_X) waveforms and their relationships for the fixed time slot operation mode.

Signalling SIG_X/SIG_R

(Refer to Timing Diagram 4)

Some CODECs may be used to transmit special signalling information during the 8th (LSB) bit of the PCM data stream in a particular time slot. This is accomplished by increasing the pulse width of the frame pulse to two or more $CLK_{X/R}$ pulses. This puts the CODEC into the signaling mode so that it will not decode the eighth bit as regular PCM data. The data present on SIG_X input during the 8th clock pulse of the time slot is inserted into the D_X data stream in the LSB position. The LSB data is latched during each time slot on the receive CODEC end and transferred to the SIG_R output. To minimize error, the PCM decoder will interpret the remaining LSB bit segment as 1/2, as opposed to a 1 or 0.

CLK_X/CLK_R

These are the master clocks used to run the encoder (X) or the decoder (R). They need not be synchronous.

CLKC

This is the control clock and is used to clock in the serial data present on the serial control port DC. This clock is used in conjunction with DC to assign time slots and to control power down.

Synchronous vs. Asynchronous

This is simply the difference in synchronizing CLK_X and CLK_R or running them asynchronously.

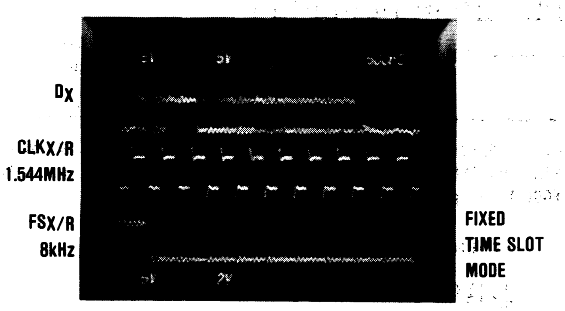
Power Down Methods

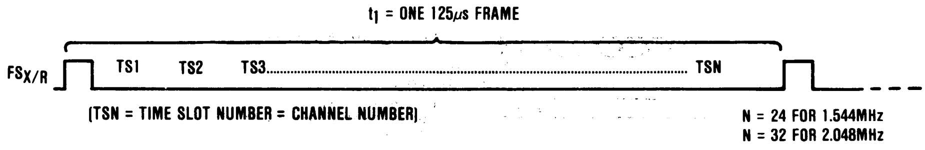
When power is first applied to the CODEC, it is placed in a power down mode. There are several ways to power down the CODEC from a normal operating mode, the most common of which is clocking in data on the DC pin using the CLK_C pin at an 8kHz rate. The negative edge of CLK_C shifts data on the DC pin into a serial control register, bit 1 first. If B1 and B2 are both 1's, the CODEC powers down and the remaining 6 bits are ignored.

The CODEC may be disabled without powering down simply by assigning it a time slot that does not exist. From Table 1, there are 64 possible time slots, only 24 (or 32 depending on total data rate) of which are valid. When a CODEC is assigned a non-valid time slot. *The system will not recognize the data.

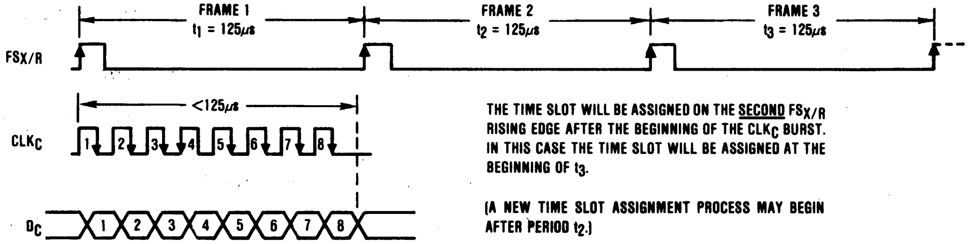
Timing Diagrams

The scope photo below illustrates various timing relationships within the CODEC. The frame sync pulse $FS_{X/R}$ is 8kHz (125µs), while the master clock is 1.544 MHz. In this case, the transmit and receive sections of the CODEC are synchronous, that is, they use the same clock. Notice the PCM data appears on the CODEC's D_X pin at the first rising edge of $CLK_{X/R}$, after an $FS_{X/R}$ pulse positive edge. The 8 segments of the D_X waveform represent 1 bit (MSB) for sign and 7 bits of PCM data assigned to timeslot 1 (TS1) or channel 1. This data is multiplexed with PCM data from other CODEC's, forming a continuous Time Division Multiplexed (TDM) PCM data bit stream for up to 24 (32 European) CODEC's. The effective data rate is 1.544 MHz (2.048 European).





TIMING DIAGRAM 1, FRAME ILLUSTRATION


FRAME 1
t_1 = 125μs
FRAME 2
t_2 = 125μs
FRAME 3
t_3 = 125μs
$FS_{X/R}$
<125μs
CLK_C
1
2
3
4
5
6
7
8
D_C
1
2
3
4
5
6
7
8

THE TIME SLOT WILL BE ASSIGNED ON THE SECOND $FS_{X/R}$ RISING EDGE AFTER THE BEGINNING OF THE CLK_C BURST. IN THIS CASE THE TIME SLOT WILL BE ASSIGNED AT THE BEGINNING OF t_3.

(A NEW TIME SLOT ASSIGNMENT PROCESS MAY BEGIN AFTER PERIOD t_2.)

THE FIRST CLK_C PULSE MAY BEGIN ANYWHERE WITH RESPECT TO $FS_{X/R}$. BUT THE ENTIRE CLK_C BURST MUST BE <125μs. CLK_C AND $FS_{X/R}$ ARE ASYNCHRONOUS.

PCM DATA APPEARS IN IT'S ASSIGNED TIME SLOT, AT THE D_X OR D_R PIN, AT THE BEGINNING OF t_4.

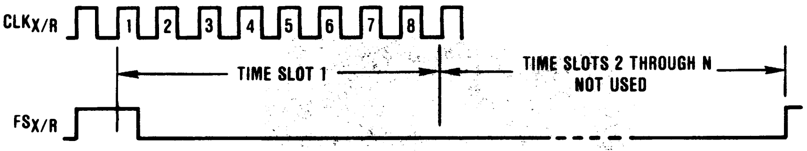
Note that D_X is not multiplexed onto $FS_{X/R}$.

TIMING DIAGRAM 2. TIME SLOT ASSIGNMENT

TABLE 1

B1	B2	ACTION
0	0	Assign Time Slot to Encoder and Decoder
0	1	Assign Time Slot to Encoder
1	0	Assign Time Slot to Decoder
1	1	Power-Down CODEC

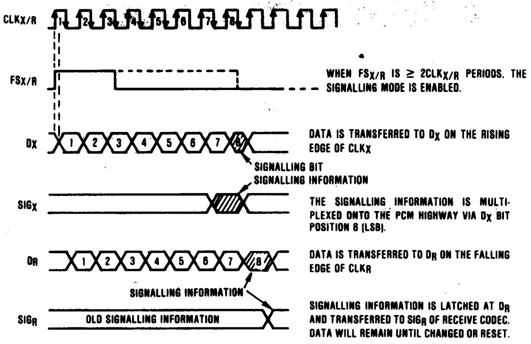
B3	B4	B5	B6	B7	B8	TIME SLOT
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64


$CLK_{X/R}$
1
2
3
4
5
6
7
8
TIME SLOT 1
TIME SLOTS 2 THROUGH N
NOT USED
$FS_{X/R}$

TIME SLOT 1 CORRESPONDS TO THE EIGHT $CLK_{X/R}$ CYCLES STARTING ONE CYCLE FROM THE NOMINAL LEADING EDGE OF $FS_{X/R}$.

N = 24 FOR 1.544MHz
N = 32 FOR 2.048MHz

TIMING DIAGRAM 3. FIXED TIME SLOT MODE


$CLK_{X/R}$
1
2
3
4
5
6
7
8
$FS_{X/R}$
D_X
1
2
3
4
5
6
7
8
SIGNALLING BIT
SIGNALLING INFORMATION
SIG_X
D_R
1
2
3
4
5
6
7
8
SIGNALLING INFORMATION
SIG_R
OLD SIGNALLING INFORMATION

WHEN $FS_{X/R}$ IS ≥ $2CLK_{X/R}$ PERIODS. THE SIGNALLING MODE IS ENABLED.

DATA IS TRANSFERRED TO D_X ON THE RISING EDGE OF CLK_X

THE SIGNALLING INFORMATION IS MULTIPLEXED ONTO THE PCM HIGHWAY VIA D_X BIT POSITION 8 (LSB).

DATA IS TRANSFERRED TO D_R ON THE FALLING EDGE OF CLK_R

SIGNALLING INFORMATION IS LATCHED AT D_R AND TRANSFERRED TO SIG_R OF RECEIVE CODEC. DATA WILL REMAIN UNTIL CHANGED OR RESET.

TIMING DIAGRAM 4. SIGNALLING MODE

No. 571

Harris Analog

USING RING SYNC WITH HC-5502A AND HC-5504 SLICs

Dave Donovan

Introduction

The ring synchronization (sync) input pin, is a TTL compatible clock input in both the HC-5502A and HC-5504 SLICs. It's purpose is to insure that the ring relay is activated or deactivated only when the instantaneous AC ring voltage, which may be as high as 150V peak, is at or near AC zero crossing.

If ring sync is not used, it must be tied high to insure proper ring trip. When used, it is important to consider at which zero crossing of the AC ring voltage, positive or negative, the ring sync signal must be synchronized with. Subsequent illustrations and equations highlight this consideration.

For detailed description of the ring trip sequence of events, refer to Application Note 549 by P. G. Phillips. Excerpts from the pertinent section are included below.

Ring Trip Sequence

The Ring Command (RC) input is taken low during ringing. This activates the ring relay driver (RR) output providing the telephone is not off-hook or the line is not in a power denial state. The ring relay connects the ring generator to the subscriber loop. The ring generator output is usually an $80V_{RMS}$, 20Hz signal. For use with the Harris SLIC, the ring signal should not exceed 150V peak. Since the telephone ringer is AC coupled, only ring current will flow. For the HC-5502A SLIC, the ring current is sunk by the ring feed amplifier output stage whereas for the HC-5504 the ring path flows directly into V_B- via a set of relay contacts. The high impedance terminal RFS exists on the HC-5504 so that the low impedance RF node can be isolated from the hot end of the ring path in the battery referenced ring scheme.

The AC ring current flowing in the subscriber circuit will be sensed across RB4, and will give rise to an AC voltage at the output of the longitudinal amplifier. R19 and C4 attenuate this signal before it reaches the ring trip detector to prevent false ring trip. C4 is nominally set at 0.47μF but can be increased towards 1μF for short lines or if several telephones are connected in parallel across the line in order to prevent false or intermittent ring trip.

When the subscriber goes off-hook, a DC path is established between the output winding of the ring generator and the battery ground or V_B- terminal. A DC longitudinal imbalance is established since no tip feed current is flowing through the tip feed resistors. The longitudinal amplifier output is driven negative. Once it exceeds the ring trip threshold of the ring trip detector, the logic circuitry is driven by GK to trip the ring relay establishing an off-hook condition such that SHD will become active as loop metallic current starts to flow.

Figure 1 illustrates the sequence of events during ring trip with ring synchronization. Note, that owing to the 90^o phase shift introduced by the low pass filter (R19, C4) the RS pulse will occur at the most negative point of the attenuated ring signal that is fed into the ring trip detector. Hence, when DC conditions are established for RTD, the AC component actually assists ring trip taking place. If ring synchronization is not used, then the RS pin should be held permanently to a logic high of 5V nominally: ring trip will occur asynchronously with respect to the ring voltage. Ring trip is guaranteed to take place within three ring cycles after the telephone going off-hook.

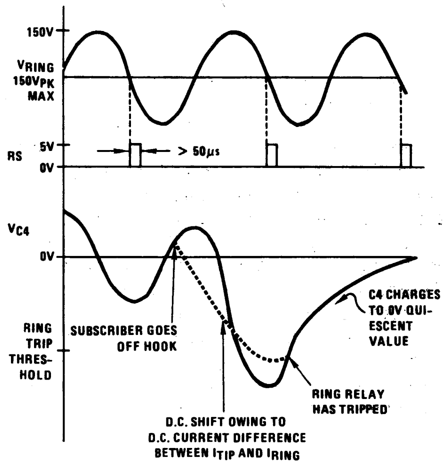
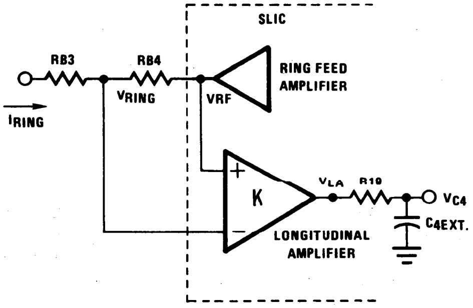


FIGURE 1. RING TRIP SEQUENCE.

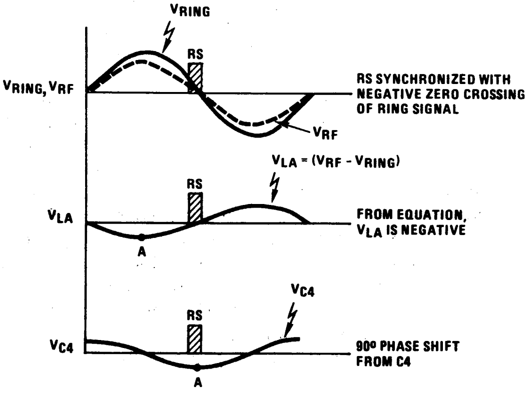
Case I: HC-5502A Tip Injected Ringing

$V_{LA} = (I_{RING} - I_{TIP})\ (RB4)\ (K)$
(During Ringing $I_{TIP} = 0$)
$V_{LA} = (I_{RING})\ (RB4)\ (K)$
$I_{RING} = (V_{RF} - V_{RING})/RB4$
$\therefore V_{LA} = (V_{RF} - V_{RING})\ K$



SLIC
RB3
RB4
VRING
VRF
RING FEED AMPLIFIER
IRING
+
K
−
VLA
R19
VC4
C4EXT.
LONGITUDINAL AMPLIFIER

FIGURE 2.



VRING
RS
VRING, VRF
RS SYNCHRONIZED WITH NEGATIVE ZERO CROSSING OF RING SIGNAL
VRF
VLA = (VRF - VRING)
RS
VLA
A
FROM EQUATION, VLA IS NEGATIVE
VC4
RS
VC4
A
90° PHASE SHIFT FROM C4

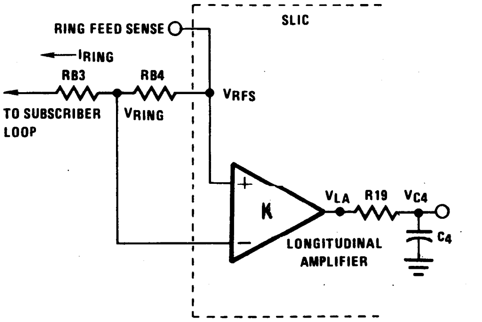
FIGURE 3.

For Case I, refer to Figures 2 and 3. In this situation the desired result is obtained, namely, that ring sync occurs during the negative peak of V_{C4}. This helps achieve ring trip faster because, once a subscriber goes off-hook, a negative DC shift is observed at V_{C4}. This shift approaches a comparator threshold in the ring trip detection circuit. If the negative peak of V_{C4}(AC) precedes the negative going DC shift at V_{C4}, one can achieve ring trip in a shorter time frame. Also this configuration allows ring trip to occur for long lines, in the order of 3000 ohms. At these line lengths, the DC negative shift will never reach the threshold because there is not enough DC current through the sense resistor, RB4. However, the negative peak of V_{C4} (AC) will cross the ring trip detector comparator threshold and ring trip will occur.

Conclusion 1: For this case make sure ring sync is synchronized with the negative zero crossing of V_{RING} as it appears on the line.

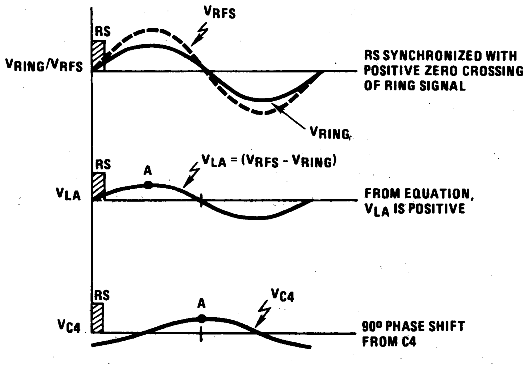
Case II: HC-5504 Ring Injected Ringing

$V_{LA} = (I_{RING} - I_{TIP})\ (RB4)\ (K)$
(During Ringing $I_{TIP} = 0$)
$V_{LA} = (I_{RING})(RB4)\ (K)$
$I_{RING} = (V_{RFS} - V_{RING})/RB4$
$\therefore V_{LA} = (V_{RFS} - V_{RING})\ K$



SLIC
RING FEED SENSE
IRING
RB3
RB4
VRFS
TO SUBSCRIBER LOOP
VRING
+
K
−
VLA
R19
VC4
C4
LONGITUDINAL AMPLIFIER

FIGURE 4.



VRFS
RS
VRING/VRFS
RS SYNCHRONIZED WITH POSITIVE ZERO CROSSING OF RING SIGNAL
VRING
RS
A
VLA = (VRFS - VRING)
VLA
FROM EQUATION, VLA IS POSITIVE
RS
A
VC4
VC4
90° PHASE SHIFT FROM C4

FIGURE 5.

For Case II refer to Figures 4 and 5. Here ring sync must be synchronized with the positive zero crossing of V_{RING} (AC) as it appears on the line so as to coincide with the negative peak of V_{C4} (AC), as in the previous case. One can see from Figure 5 that ring sync on the negative zero crossing would coincide with the positive peak of V_{C4}, inhibiting ring trip for loops greater than approximately 800 ohms.

Conclusion 2: For this case make sure ring sync is synchronized with the positive zero crossing of V_{RING} (AC.).

For all other ring configurations, namely, tip injected and balanced ringing for the 5504, if ring sync is used, it must be synchronized with the negative zero crossing of V_{RING}(AC).

Acknowledgement

The author wishes to thank Geoff Phillips for his contribution to this paper.

APP NOTE

FOR YOUR INFORMATION

No. 573

Harris Analog

THE HC-5560 DIGITAL LINE TRANSCODER

David J. Donovan

1.0 Introduction

The Harris HC-5560 digital line transcoder provides mode selectable, psuedo ternary line coding and decoding schemes for North American and European transmission lines. Coding schemes include Alternate Mark Inversion (AMI), Bipolar with N Zero Substitution (BNZS), and High Density Bipolar 3 (HDB3), used for transmission lines as follows:

AMI:	North American T1(1.544MHz) and T1C(3.152MHz) lines
B6ZS:	North American T2(6.3212MHz) lines
B8ZS:	North American T1(1.544MHz) lines
HDB3:	European PCM30(2.048 & 8.448MHz) CEPT lines. Recommended by CCITT.

The transcoder is a single chip, single supply device fabricated with standard cell CMOS. Features include simultaneous coding and decoding, asynchronous operation, loop back mode, transmission error detection, an alarm indication signal, and a full chip reset.

This application note will describe why coding for digital transmission is necessary, the types of coding, which is best, and why, and the functionality and applications of the HC-5560 digital line transcoder.

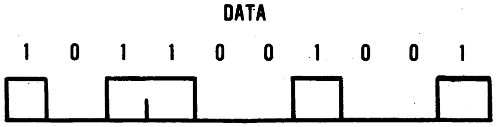
2.0 Why Line Coding?

Transmission of serial data over any distance, be it a twisted pair, fiber optic link, coaxial cable, etc., requires "maintenance" of the data as it is transmitted (through repeaters, echo cancellors etc.). The data integrity must be maintained through data reconstruction, with proper timing, and retransmitted. Line codes were created to facilitate this "maintenance".

In selecting a particular line coding scheme some considerations must be made, as not all line codes adequately provide the all important synchronization between transmitter and receiver. Other considerations for line code selection are noise and interference levels, error detection/checking, implementation requirements, and the available bandwidth.

2.1 Unipolar Coding

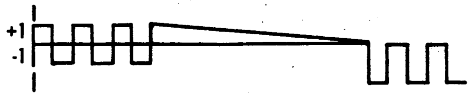
The most basic transmission code is unipolar or unbalanced coding whereby each discrete variable to be transmitted is assigned a different level, 0V and +3V, for example:



UNIPOLAR (UNBALANCED) SIGNAL

There are, however, a number of disadvantages:

- The average power (Ao/2) is two times other codes
- The coded signal contains DC and low frequency components. When long strings of zeros are present, a DC or baseline wander occurs. This results in loss of timing and data because a receiver/repeater cannot optimally discriminate ones and zeros.

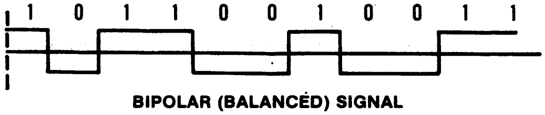


DC WANDER

- Repeaters/receivers require a minimum pulse density for proper timing extraction. Long strings of ones or zeros contain no timing information and lead to timing jitter and possible loss of synchronization.
- There is no provision for line error rate monitoring.

2.2 Bipolar Coding is Better

With bipolar, or balanced, coding, the same data may be transmitted more efficiently achieving the same error distance with half the power (Ao/4). This coding is often referred to as Non-Return to Zero (NRZ) coding as the signal level is maintained for the duration of the signal interval.



BIPOLAR (BALANCED) SIGNAL

Although bipolar coding is more efficient than unipolar, it still lacks provisions for line error monitoring, and is susceptible to DC wander and timing jitter.

The HC-5560 digital line transcoder provides a number of augmented bipolar coding schemes which:

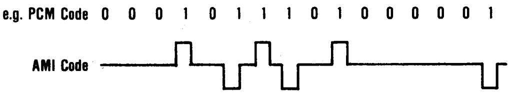
- Eliminate DC Wander
- Minimize Timing Jitter
- Provide for Line Error Monitoring

This is accomplished by introducing controlled redundancy in the code through extra coding levels.

3.0 Line Code Descriptions

The HC-5560 transcoder allows a user to implement any of the four line coding schemes described below.

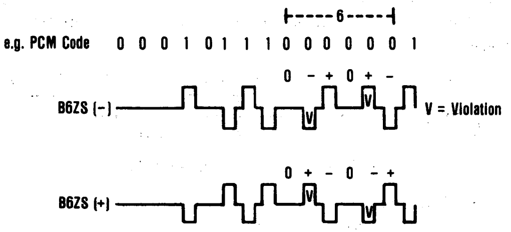
AMI, Alternate Mark Inversion, is used primarily in North American T1 (1.544MHz) and T1C (3.152MHz) carriers. Zeros are coded as the absence of a pulse and one's are coded alternately as positive or negative pulses. This type of coding reduces the average voltage level to zero to eliminate DC spectral components, thereby eliminating DC wander.



To facilitate timing maintenance at regenerative repeaters along a transmission path, a minimum pulse density of logic 1's is required. Using AMI, there is a possibility of long strings of zeros and the required density may not always exist, leading to timing jitter and therefore higher error rates.

A method for insuring a minimum logic 1 density by substituting bipolar code in place of strings of 0's is called BNZS or Bipolar with N Zero Substitution. B6ZS is used commonly in North American T2 (6.3212MHz) carriers. For every string of 6 zeros, bipolar code is substituted according to the following rule:

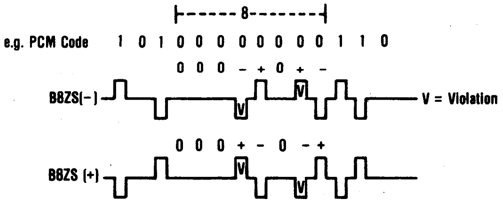
If the immediate preceding pulse is of (-) polarity, then code each group of 6 zeros as 0-+0+-, and if the immediate preceding pulse is of (+) polarity, code each group of 6 zeros as 0+-0-+. One can see the consecutive logic 1 pulses of the same polarity violate the AMI coding scheme.



B8ZS is used commonly in North American T1(1.544MHz) and T1C(3.152MHz) carriers. For every string of 8 zeros, bipolar code is substituted according to the following rules:

1) If the immediate preceding pulse is of (-) polarity, then code each group of 8 zeros as 000-+0+-.

2) If the immediate preceding pulse is of (+) polarity, then code each group of 8 zeros as 000+-0-+.

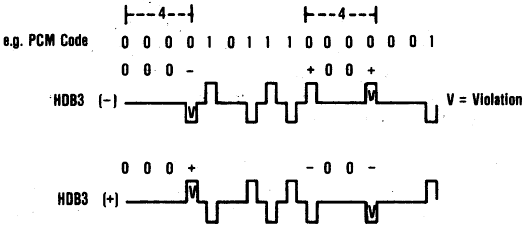


The BNZS coding schemes, in addition to eliminating DC wander, minimize timing jitter and allow a line error monitoring capability.

Another coding scheme is HDB3, high density bipolar 3, used primarily in Europe for 2.048MHz carriers. This code is similar to BNZS in that it substitutes bipolar code for 4 consecutive zeros according to the following rules:

1) If the polarity of the immediate preceding pulse is (-) and there have been an odd (even) number of logic 1 pulses since the last substitution, each group of 4 consecutive zeros is coded as 000-(+00+).

2) If the polarity of the immediate preceding pulse is (+) then the substitution is 000+(-00-) for odd (even) number of logic 1 pulses since the last substitution.



The 3 in HDB3 refers to the coding format that precludes strings of zeros greater than 3. Note that violations are produced only in the fourth bit location of the substitution code and that successive substitutions produce alternate polarity violations.

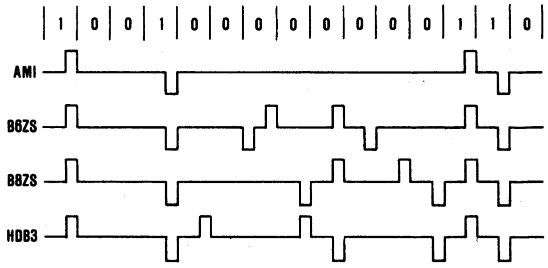


FIGURE 1. SUMMARY OF CODING SCHEMES PROVIDED BY THE HC-5560 TRANSCODER.

A summary graph of all four substitution coding schemes is illustrated in Figure 1. To simplify timing recovery, logic 1's are encoded with 50% duty cycle pulses.

4.0 Functional Description

The HC-5560 transcoder can be divided into six sections: transmitter(coder), receiver(decoder), error detector, all ones detector, testing functions, and output controls. A block diagram is shown in Figure 2.

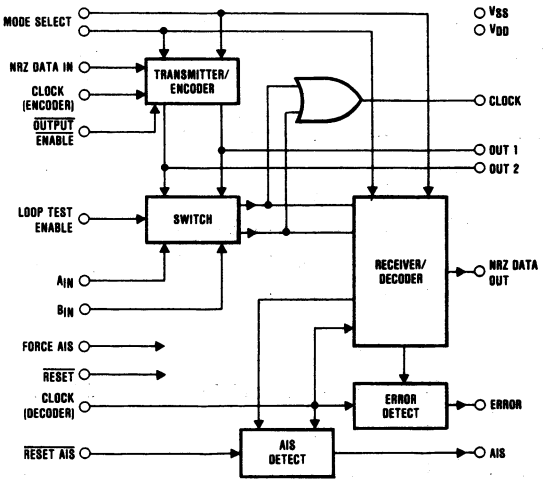


FIGURE 2. HC-5560 TRANSCODER FUNCTIONAL BLOCK DIAGRAM.

4.1 Transmitter (Coder)

The transmitter codes a non-return to zero (NRZ) binary unipolar input signal (NRZ IN) into two binary unipolar return to zero (RZ) output signals (OUT1, OUT2). These output signals represent the NRZ data stream modified according to the selected encoding scheme (i.e., AMI, B8ZS, B6ZS, HDB3) and are externally mixed together (usually via a transistor or transformer network) to create a ternary bipolar signal for driving transmission lines.

4.2 Receiver (Decoder)

The receiver accepts as its input the ternary data from the transmission line that has been externally split into two binary unipolar return to zero signals (A_{IN} and B_{IN}). These signals are decoded, according to the rules of the selected line code into one binary unipolar NRZ output signal (NRZ OUT).

The encoder and decoder sections of the chip perform independently (excluding loopback condition) and may operate simultaneously.

4.3 Error Detector

The Error output signal is active high for one cycle of CLK DEC upon the detection of any bipolar violation in the received A_{IN} and B_{IN} signals that is not part of the selected line coding scheme. The bipolar violation is not removed, however, and shows up as a pulse in the NRZ DATA OUT signal. In addition, the Error output signal monitors the received A_{IN} and B_{IN} signals for a string of zeros that violates the maximum consecutive zeros allowed for the selected line coding scheme (i.e., 8 for B8ZS, 6 for B6ZS, and 4 for HDB3). In the event that an excessive amount of zeros is detected, the Error output signal will be active high for one cylce of CLK DEC during the zero that exceeds the maximum number. In the case that a high level should simultaneously appear on both received input signals A_{IN} and B_{IN} a logical one is assumed and appears on the NRZ data out stream with the error signal active.

4.4 All Ones Detector

An input signal received at inputs A_{IN} and B_{IN} that consists of all ones (or marks) is detected and signalled by a high level at the alarm indication signal (AIS) output is set to a high level when less than three zeros are received during one period of Reset AIS immediately followed by another period of Reset AIS containing less than three zeros. The AIS output is reset to a low level upon the first period of Reset AIS containing 3 or more zeros.

4.5 Testing Functions

A logic high level on LTE enables a loopback condition where OUT1 is internally connected to input A_{IN} and OUT2 is internally connected to B_{IN} (this disables inputs A_{IN} and B_{IN} to external signals). In this condition, the input signal NRZ DATA IN appears at output NRZ DATA OUT (delayed by the amount of clock cycles it takes to encode and decode the selected line code). A decode clock must be supplied for this operation. The Reset input can be used to initialize this process.

4.6 Output Controls

The output controls are Output Enable and Force AIS. These pins allow normal operation, force OUT1 and OUT2 to zero, or force OUT1 and OUT2 to output all ones (AIS condition).

5.0 Applications

The HC-5560 transcoder is designed for use in North American and European PCM transmission lines where psuedo ternary line code substitution schemes are desired. Any equipment that interfaces to T1, T1C, T2 or PCM30 transmission lines may incorporate transcoders. Such equipment includes multiplexers, channel service units, echo cancellors, repeaters, etc. This section will illustrate and describe a basic circuit application, and various system level applications examples.

5.1 Basic Applications Circuit

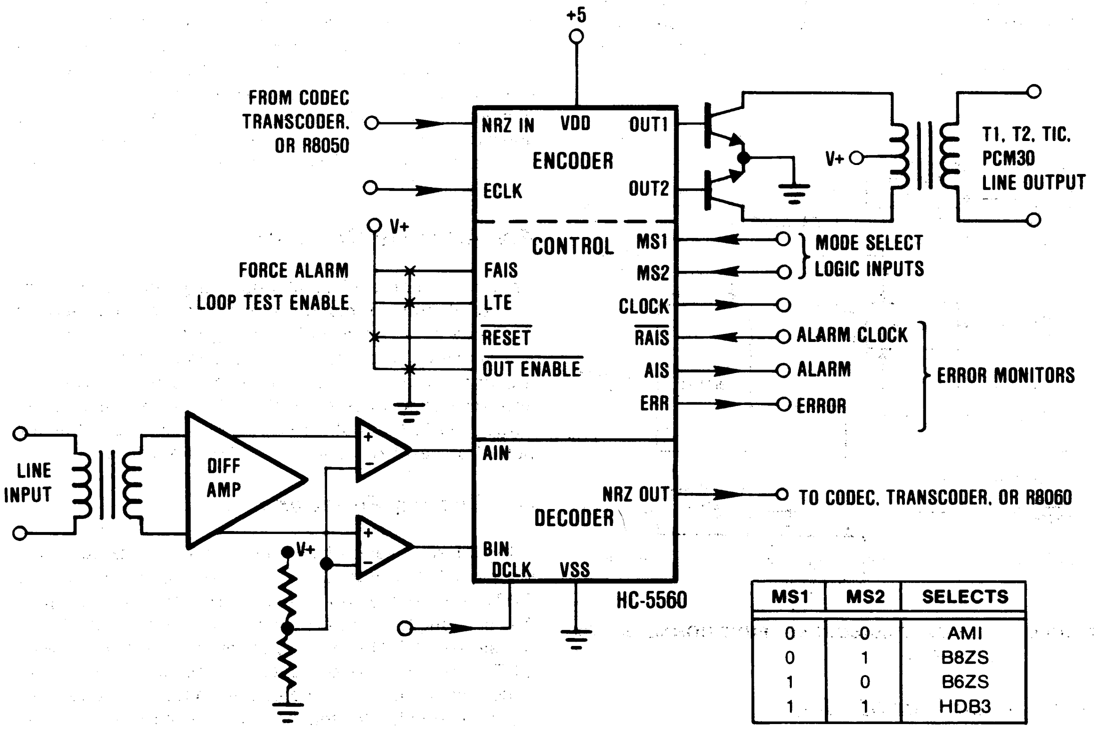
The basic applications circuit is shown in Figure 3. The encoder accepts serially clocked unipolar non-return to zero (NRZ/PCM) data at the NRZ IN pin and codes it into two unipolar return to zero (RZ) signals at pins Out1 and Out2. A coding scheme is chosen via mode select pins MS1 and MS2. Data is clocked in on the negative edge of ECLK and clocked out on the positive edge of ECLK. The outputs must be mixed externally, via a transistor/transformer network, to produce the ternary 'bipolar' code selected and to drive the transmission line. The length of Out1 and Out2 are set by the length of the positive ECLK pulse.

To decode ternary coded data, the signal must first be split into two unipolar signals and presented to the A_{IN} and B_{IN} pins. This may be accomplished by an amplifier with a differential output, and two comparators. Both inputs are sampled by the positive edge of DCLK. Decoded data is clocked out in NRZ form to the NRZ OUT pin on the positive edge of DCLK.

All the logic inputs and outputs are TTL compatible.

5.2 System Level Examples

Examples of system level transcoder applications are illustrated in Figure 4 through 8.


+5
FROM CODEC
TRANSCODER.
OR R8050
NRZ IN
VDD
OUT1
ENCODER
ECLK
OUT2
V+
T1. T2. TIC.
PCM30
LINE OUTPUT
V+
CONTROL
MS1
MS2
MODE SELECT
LOGIC INPUTS
FORCE ALARM
LOOP TEST ENABLE
FAIS
LTE
RESET
OUT ENABLE
CLOCK
RAIS
AIS
ERR
ALARM CLOCK
ALARM
ERROR
ERROR MONITORS
LINE
INPUT
DIFF
AMP
AIN
NRZ OUT
DECODER
BIN
DCLK
VSS
V+
TO CODEC. TRANSCODER. OR R8060
HC-5560

MS1	MS2	SELECTS
0	0	AMI
0	1	B8ZS
1	0	B6ZS
1	1	HDB3

FIGURE 3. BASIC TRANSCODER APPLICATIONS CIRCUIT.

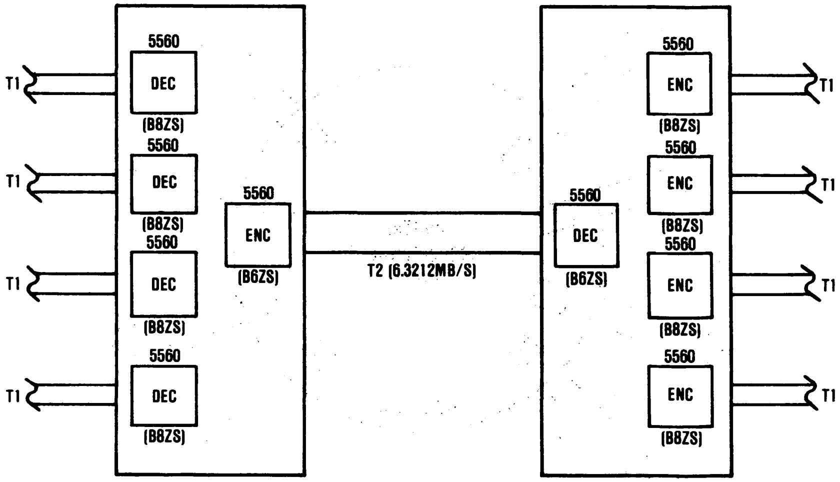

T1
T1
T1
T1
5560
DEC
(B8ZS)
5560
DEC
(B8ZS)
5560
DEC
(B8ZS)
5560
DEC
(B8ZS)
5560
ENC
(B6ZS)
T2 (6.3212MB/S)
5560
DEC
(B6ZS)
5560
ENC
(B8ZS)
5560
ENC
(B8ZS)
5560
ENC
(B8ZS)
5560
ENC
(B8ZS)
T1
T1
T1
T1

FIGURE 4. M12 MULTIPLEXER

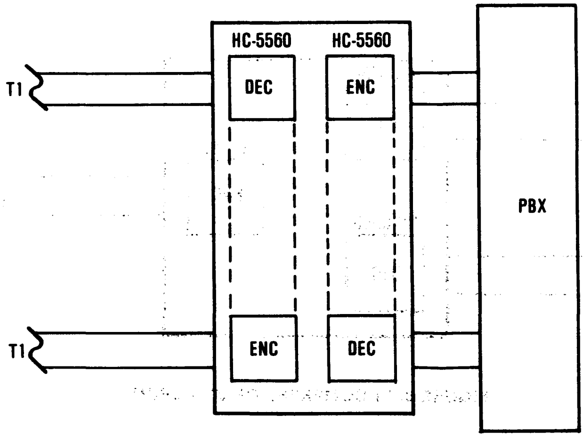

T1
T1
HC-5560
HC-5560
DEC
ENC
ENC
DEC
PBX

FIGURE 5. CHANNEL SERVICE UNIT (CSU)

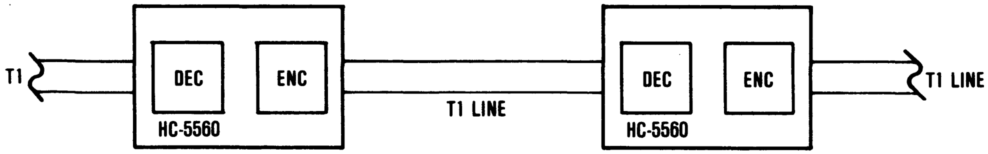

T1
DEC
ENC
HC-5560
T1 LINE
DEC
ENC
HC-5560
T1 LINE

FIGURE 6. ECHO CANCELLOR

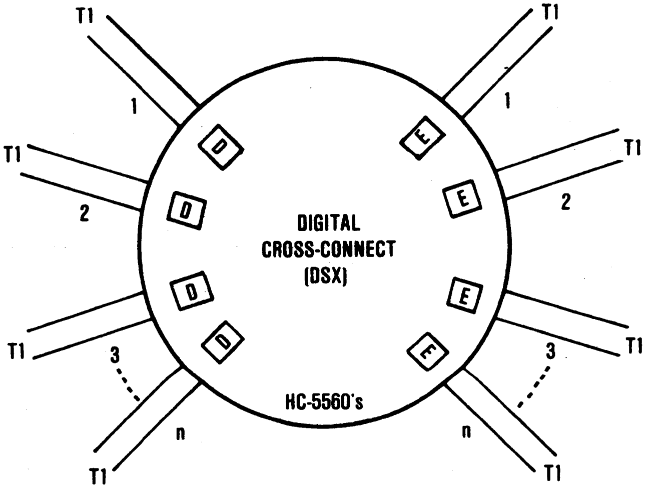

T1
1
T1
2
T1
3
n
T1
T1
1
T1
2
T1
3
n
T1
D
D
D
D
E
E
E
E
DIGITAL
CROSS-CONNECT
(DSX)
HC-5560's

FIGURE 7. DIGITAL CROSS CONNECT (DCS)

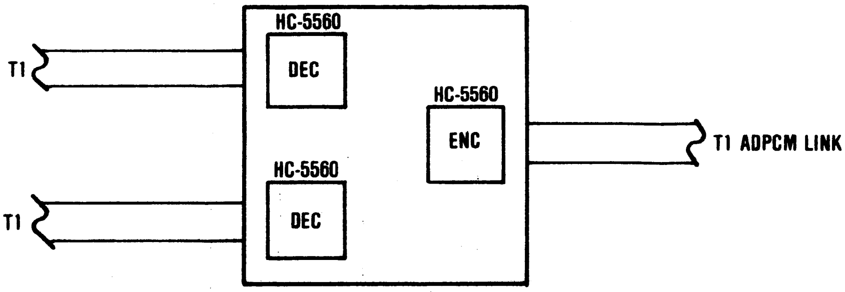

T1
T1
HC-5560
DEC
HC-5560
DEC
HC-5560
ENC
T1 ADPCM LINK

FIGURE 8. T1 COMPRESSION BY ADPCM

APP NOTE
FOR YOUR INFORMATION
No. 574
Harris Analog

UNDERSTANDING PCM CODING

David J. Donovan

1.0 Introduction

The process of converting analog voice signals into Time Division Multiplexed (TDM) Pulse Code Modulated (PCM) format is described and illustrated herein. Application Note No. 570, "Understanding CODEC Timing", by D.J. Donovan is recommended reading as accompaniment to this application note.

Analog time varying voice input information is transmitted over two-wire (2w) pairs (channels) from subscribers. The PCM filter band-limits voice signals to 4kHz, one per channel, and removes power line and ringing frequencies. Research has shown that voice transmission band-limited to 4kHz has enough fidelity for telephony purposes.

2.0 Sampling

The process of converting filtered voice information into a digitized pulse train format begins with sampling the voice signal at uniform intervals. These intervals are determined by the Nyquist Sampling Theorem, which simply states that any signal may be completely re-constructed from its representative sampling, if it is sampled at least twice the maximum frequency of interest. The telephone system, being a worldwide standard 8kHz sampling system, satisfies Nyquist, as all voice signals are band-limited to 4kHz. When the voice waveform is sampled, a train of short pulses is produced, each representing the amplitude of the waveform at the specific instant of sampling. This process is called Pulse Amplitude Modulation (PAM). The envelope of the PAM samples replicate the original waveform. Figures 1A thru 1D illustrate representative PAM samples for up to 24(30) individual voice channels in a μ-Law (A-Law) telephone system.

There are relatively large intervals between each PAM sample that may be used for transmitting PAM samples from other voice channels. Interleaving several voice channels on a common bus is the fundamental principle of Time Division Multiplexing (TDM). As the number of voice channels on the TDM bus increases, the time alloted to each sample is reduced, and bandwidth requirements increase (See Figure 1E).

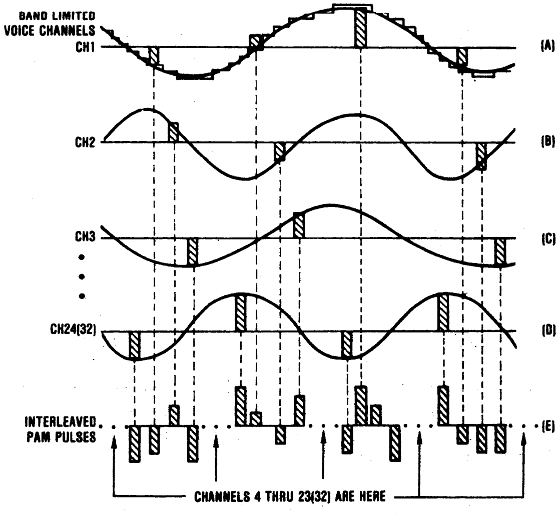


FIGURE 1 (A THROUGH E).

3.0 Quantizing

The PAM samples still represent the voice signal in analog form. For digital transmission, further processing is required. Pulse Code Modulation (PCM) is a technique used to convert the PAM samples to a binary weighted code for digital transmission. PCM coding is a two step process performed by the CODEC. The first step is quantization, where each sample is assigned a specific quantizing interval. The second step is PCM coding of the quantizing interval into an 8 bit PCM code word. Each is discussed in the text that follows.

Converting PAM samples to a digital signal involves assigning the amplitude of a PAM sample one of a whole range of possible amplitude values, which are divided into quantizing intervals. There are 256 possible quantizing intervals, 128 positive and 128 negative. The boundaries between adjacent quantizing intervals are called decision values.

If PAM samples are uniformly quantized, there will be situations where several different amplitude values will be assigned the same quantizing interval during encoding. Then, during decoding, one signal amplitude value is recovered for each quantizing interval which corresponds to the midpoint of the quantizing interval. This results in small discrepencies that occur between the original waveform and the quantized approximation; i.e., infinite analog levels in the original waveform being assigned finite quantizing intervals. These discrepancies result in a quantizing noise or quantizing distortion, the magnitude of which is inversely proportional to the number of discrete quantizing intervals. These noise signals may be of the same order of magnitude as the input signal, thereby reducing the signal to quantizing noise ratio to an intolerable level. For this reason non-uniform quantization is used. Large signals need a smaller number of quantizing intervals, while small signals require a larger number of quantizing intervals. Such a non-uniform quantization process is defined as companding characteristics by both Bell and CCITT.

The PCM CODEC performs this non-uniform or non-linear quantization through μ-Law or A-law companding characteristics shown in Figure 2. This process enhances lower amplitude signals, to allow them to compete with system noise, and attenuates higher amplitude signals, preventing them from saturating the system. This form of signal compression results in a relatively uniform signal to quantization noise ratio, approaching 40dB for a wide range of input amplitudes. Also, the dynamic range approaches that of a 13(11) bit A/D or 80(66)dB for μ-Law (A-Law) companding. The digital realization of this companding process is obtained by a segment and chord piecewise linear approximation to a semi-logarithmic function.

Both the μ-Law and A-law companding characteristics are composed of 8 linear segments or chords in each quadrant. Within each chord are 16 uniform quantization intervals, or steps. With μ-Law, moving away from the origin, each chord is twice the width of the preceding chord, and each group of 16 uniform steps is twice the width of the preceding group. It is also referred to as the 15 segment characteristic. The first chord about the origin in the positive and the negative quadrant are of the same slope and are therefore considered one chord (chord 0). With A-law, the first two chords and step groups in each quadrant are uniform. Successive chords and steps follow the same pattern as μ-Law. A-Law is referred to as the 13 segment characteristic. The first two chords about the origin in the positive quadrant, and the first two chords about the origin in the negative quadrant are all of the same slope and therefore are considered one chord (chord 1). There are 64 uniform steps in chord 1, 32 positive and 32 negative. However, for purposes of encoding and decoding samples that fall into the quantization intervals in chord 1, a different 3 bit chord code (refer to Figure 3) is assigned for the first segment of 16 uniform steps closest to the origin and the next segment moving away from the origin. Chord 1 in A-Law is twice that of chord 0 in μ-Law.

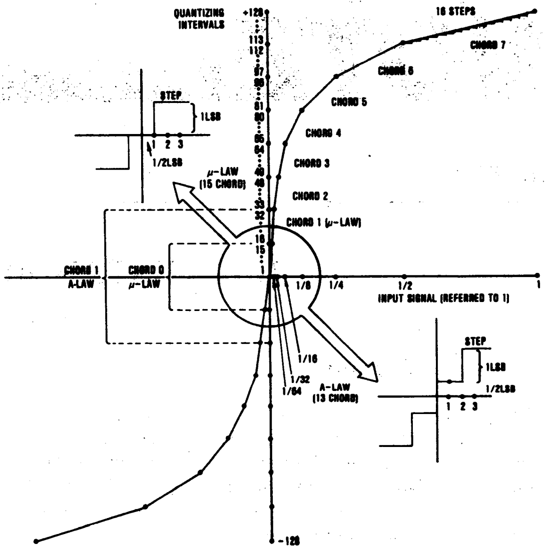


FIGURE 2.

The μ-Law companding characteristic is used primarily in North America and Japan, while A-Law is used primarily in Europe. The differences are minimal and are summarized below:

μ-Law

- Step sizes double for each successive chord
- Virtual edge = +/-8159 units
- Input level = 3.172dBm0
- 2 codes for 0 input

A-Law

- Step sizes double for each successive chord after the second chord
- Virtual edge = +/-4096 units
- Input level = 3.14dbm0
- No code for 0 input

The input level is determined with reference to the power level at the central office or 'switch'. That point is referred to as the zero transmission level point (0TLP). All CODEC measurements must be translated to the 0TLP. The unit of translated level is the dBm0 (dB relative to 1mW referred to a transmission level of 0TLP).

There is no absolute voltage standard for the CODEC, however, a standard exists relative to full scale. The point at which the CODEC begins to clip is called the virtual edge. It is measured in normalized voltage units or steps, +/-8159 steps for μ-Law and +/-4096 steps for A-Law. If a PAM sample representing the peak of a voice input signal hits the virtual edge of a μ-Law system, it has a relative power of +3.172dBm0. The corresponding A-Law relative power is +3.14dBm0. These numbers are chosen to minimize intrinsic gain error at 0dBm0 and 1000Hz.

4.0 Encoding

The second stage of conversion to binary PCM data for transmission involves the coding of the 256 quantizing intervals assigned to the individual PAM samples into 8 bit binary words (7 data bits plus 1 sign bit). The MSB in each word is a polarity bit indicating a 1 for positive quadrant quantizing intervals, and a 0 for negative quadrant quantizing intervals. The next three bits represent the chord, and the last four bits identify the step within the chord. The 8 bit PCM word partitioning is illustrated in Figure 3.

BIT NUMBER	1	2	3	4	5	6	7	8	
BIT WEIGHT-MSB	+/-	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LSB
	SIGN	CHORD			STEP				

FIGURE 3.

A-Law and μ-Law coding about the origin differ. μ-Law defines two codes for 0V input while A-Law defines no code for 0V input (see Figure 4). The two μ-Law zero codes represent a normal quantization step that is divided into halves by the y-axis of the companding curve (refer to Figure 2). These half steps represent the lowest resolvable signal of the μ-Law characteristic.

INPUT	BINARY EQUIV.	μ-LAW	A-LAW
+FULL SCALE	1111 1111	1000 0000	1010 1010
+CENTER	1000 0000	1111 1111	1101 0101
-CENTER	0000 0000	0111 1111	0101 0101
-FULL SCALE	0111 1111	0000 0000	0010 1010

FIGURE 4.

5.0 Multiplexing and Transmission

Each 8 bit PCM word is transmitted in its respective time slot, which is assigned to each CODEC by the system controller (See App. Note 570). A number of PCM words may be transmitted consecutively from different channels, creating a PCM TDM signal for transmission. Each CODEC channel has an average data rate of 8K samples/sec x 8 bits = 64kbits/s. This means that within a 1/8kHz = 125μs period, 24(30) PCM words of 8 bits each are transmitted consecutively in a μ-Law (A-Law) system.

5.1 μ-Law Systems

For μ-Law systems, the bus format allows 24 groups, or timeslots, of 8 bit PCM words, plus one synchronization (sync) bit for a total of 193 bits per frame (see Figure 5). This sync bit partitions the boundary between timeslots 24 and 1, and allows the time slot counter at the receive end to maintain sync with the transmit end. All signalling information is contained in bit 8 (LSB) of the PCM word. These multiplexed frames of 24, 193 bit channels constitute the 1.544MHz T1 transmission channel.

5.2 A-Law Systems

For A-Law systems, the bus format groups data into 32 timeslots of 8 bit PCM words each, giving 30 voice channels plus one 8 bit sync and alarm channel, and one 8 bit signalling channel. The sync and alarm, and signalling information are contained in channels 0 and 16, respectively (see Figure 5). Bits 2, 4, 6, and 8 are inverted for transmission per CCITT recomendation. These multiplexed frames of 32, 256 bit channels constitute the 2.048MHz PCM30-CEPT (Committee of European Postal and Telegraph) transmission channel.

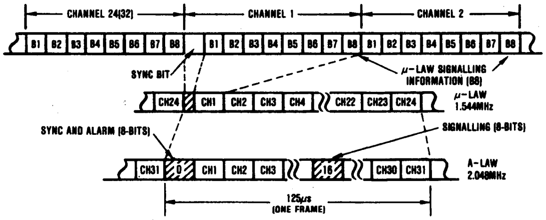


FIGURE 5.

6.0 Line Coding

PCM code generated by the CODEC function is in Non-Return to Zero (NRZ) format. It cannot effectively be transmitted directly on a transmission line because the signal contains a DC component and lacks timing information.

An additional coding step is necessary which converts NRZ code to a pseudo ternary code suitable for transmission. Practical coding schemes include Alternate Mark Inversion (AMI), Bipolar with N Zero Substitution (BNZS), and High Density Bipolar 3 (HDB3) coding. These schemes eliminate the dc component of NRZ code, thereby eliminating the troublesome dc wander phenomenon. They also provide a means for detecting line coding errors, and enhance synchronization between transmitter and receiver through reduction of timing jitter. For additional information, refer to Application Note 573, "The HC-5560 Transcoder", by D. J. Donovan.

7.0 Demultiplexing

After transmission, the CODEC must recover the 8 bit PCM words from the TDM signal, sort out, decode, and distribute the PCM information appropriately. The demultiplexing process is fully controlled electronically.

8.0 Decoding

The CODEC receive function allocates a signal amplitude to each 8 bit PCM word which corresponds to the midpoint of the particular quantizing interval. The expanding characteristic is the same as that for non-linear companding on the transmit side. If the LSB of a μ-Law PCM word contains signalling information, it is extracted by the CODEC, latched into a flip-flop, and distributed to the CODEC signalling output (Sig_R). This means that there is a lost bit (LSB) in the incoming PCM data stream during a signalling frame. The decoder interprets the missing LSB as a 1/2 (i.e. halfway between a 0 and a 1) to minimize noise and distortion. The PCM words are decoded in the order in which they are received and then converted to PAM pulses. The PAM pulses are summed, then low pass filtered, which smoothes the PAM envelope and reproduces the original voice signal.

APP NOTE

FOR YOUR INFORMATION

No. 576

Harris Analog

HC-5512C PCM FILTER CLEANS UP CVSD CODEC SIGNALS

P. G. Phillips and D. J. Donovan

The HC-5512 is a CMOS switched capacitor PCM Filter originally designed for use with the PCM CODEC to filter transmit and receive audio signals. The HC-5512C is a wider specification version of the HC-5512 that conveniently lends itself to be configured as a input/output filter for the HC-55564 CVSD. This offers the designer extremely high quality filter characteristics for a minimum component count and system cost.

The HC-5512C Filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate LC ladder filters with low component sensitivity. The IC contains two switched capacitor filters. The transmit filter is a fifth order elliptic low pass filter cascaded with a fourth order Chebyshev high pass filter. It has a flat band pass response and rejects signals of frequencies less than 200Hz and greater than 3.4kHz. The receive filter is a fifth order elliptic low pass filter with SINX/X compensation. The response of this filter can be tailored for CVSD use with an external RC network to flatten the SINX/X correction characteristic.

The HC-55564 is a half duplex modulator/demodulator CMOS integrated circuit used to convert voice signals into serial NRZ digital data and reconvert that data into voice. Continuously Variable Slope Deltamodulation (CVSD) is the method of conversion. As in any sampling system, the reconstituted signal contains noise due to switching. In addition, to prevent alias distortion, the input signal must be filtered to remove frequencies above one-half the sampling frequency. In order to minimize these unwanted noise frequencies, and to pre-condition the input signal, it is necessary to filter the input and the decoded output of the CVSD.

The transmit and receive filter responses are shown in Figures 1A and 1B. The transfer characteristic of the CVSD is illustrated in Figure 2. A suggested circuit configuration is shown in Figure 3.

The HC-5512C filter is configured such that it utilizes a 2.048MHz clock for the switched capacitors. A 16kHz or 32kHz sampling clock for the CVSD is easily derived as shown in Figure 3. A 32kHz sampling clock is recommended to enhance noise performance, frequency response, and dynamic range of the CVSD. For the circuit as shown the audio signal into the CVSD should be 1Vp-p over the 3.2kHz band to obtain a flat response. As can be seen from Figure 2, for lower frequency signals, higher signal levels can be used. However, an external compensation network is required to flatten the inherent SINX/X output response of the receive filter stage (see Figure 1B). R_A, R_B and C_A form a simple lead lag filter at the output of the receive filter in the HC-5512C. This introduces a pole at 1kHz and a zero at 3.3kHz in order to give some degree of compensation against the filter's SINX/X characteristics.

Transmit Filter Stage

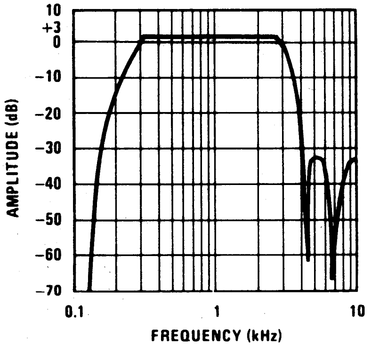


FIGURE 1A. TRANSMIT FILTER STAGE

Receive Filter Stage

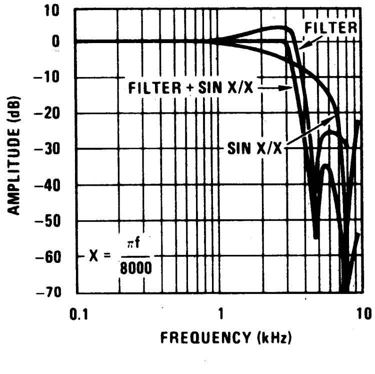


FIGURE 1B. RECEIVE FILTER STAGE

The CVSD is AC coupled to the filter since the audio in/out ports of the CVSD are DC biased at $V_{DD}/2$. (In fact, audio can be directly coupled to V_{FRI} if desired.) It is often necessary to provide a side tone back to the user headset so the speaker may hear his own voice, thus preventing a dead feeling in the instrument. The side tone is provided at the audio out pin of the CVSD during the encode operation and is of the same amplitude as the input signal, transfer gain excepted.

The CVSD has an Automatic Gain Control (AGC) output. The signal present is a digital output whose duty cycle is proportional to the average input audio level. The signal may be integrated to provide feedback information to an AGC amplifier or a voice level indicator.

The Force Zero (FZ) input to the CVSD is used to reset all the internal counters at the start of an encode or decode cycle to prevent momentary overload. It will also recover the part from a latch-up condition. Cycling FZ during power-up sequencing is recommended. A suggested power-up reset circuit is shown in Figure 3 on the FZ control line. During the time FZ is active (low), an alternating 1,0 quieting pattern appears at the NRZ output which is at half the sampling clock rate, and is decoded inaudible. The quieting pattern may also be generated by activating the Alternate Plain Text (APT) input (low), or by removing the signal from the audio input pin.

Additional information on CVSD is contained in Application Note 607.

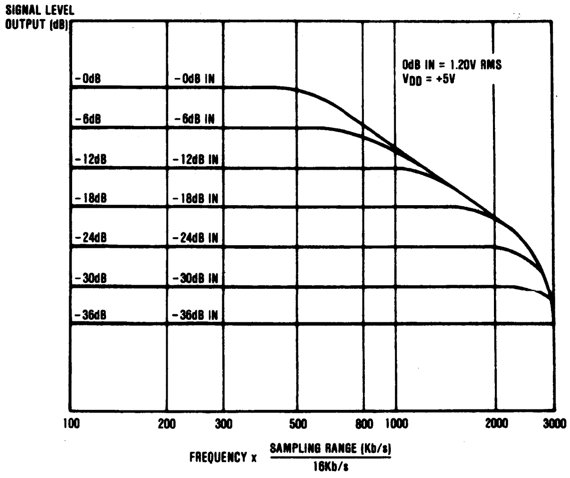


FIGURE 2. TRANSFER FUNCTION FOR CVSD AT 16KB

Illustrates the frequency response of the HC-55564 for varying input levels. To prevent slope overload (slew rate limiting) do not exceed the 0dB boundary. The frequency response is directly proportional to the sampling rate. The output levels were measured after filtering.

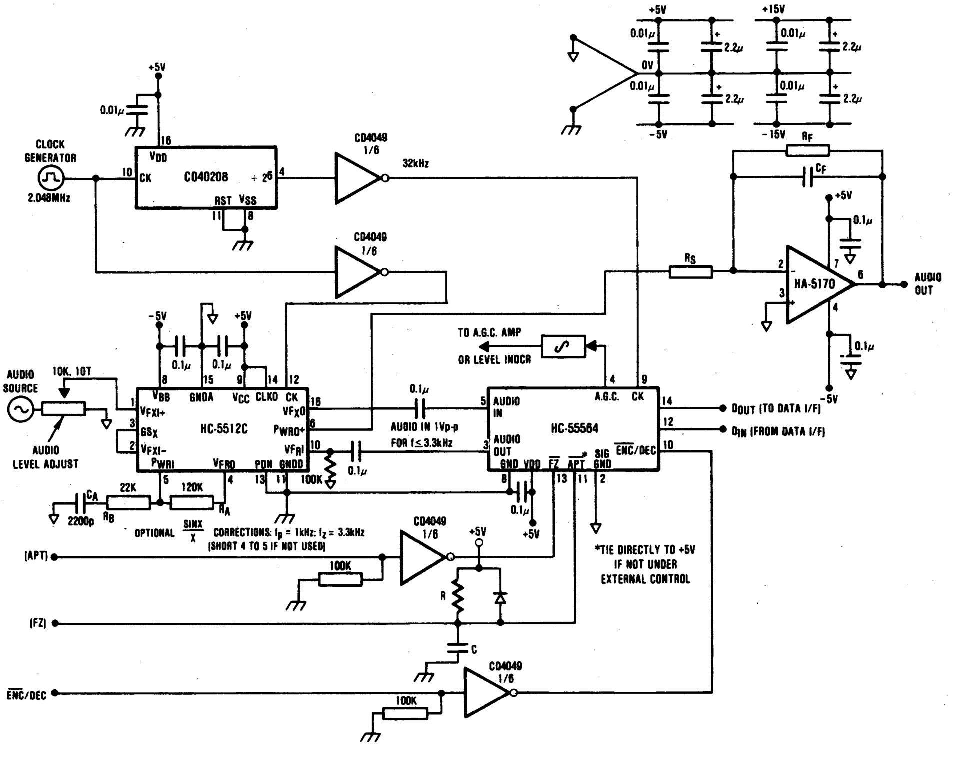

+5V
+15V
0.01μ
2.2μ
0V
-5V
-15V
R_F
C_F
0.1μ
R_S
HA-5170
AUDIO OUT
CLOCK GENERATOR
2.048MHz
V_{DD}
CK
CD4020B
÷ 2⁶
RST
V_{SS}
CD4049 1/6
32kHz
TO A.G.C. AMP OR LEVEL INDCR
AUDIO SOURCE
10K, 10T
AUDIO LEVEL ADJUST
V_{BB}
GNDA
V_{CC}
CLKO
CK
V_{FXI+}
V_{FXO}
GS_X
HC-5512C
$PWRO+$
V_{FXI-}
V_{FRI}
$PWRI$
V_{FRO}
PDN
GNDD
100K
22K
120K
C_A
R_B
R_A
2200p
OPTIONAL $\frac{SINX}{X}$ CORRECTIONS: I_P = 1kHz; I_Z = 3.3kHz (SHORT 4 TO 5 IF NOT USED)
AUDIO IN 1Vp-p FOR f≤3.3kHz
AUDIO IN
AUDIO OUT
A.G.C.
HC-55564
$\overline{ENC}$/DEC
GND
VDD
$\overline{FZ}$
$\overline{APT}$*
SIG GND
D_{OUT} (TO DATA I/F)
D_{IN} (FROM DATA I/F)
(APT)
(FZ)
$\overline{ENC}$/DEC
R
C
*TIE DIRECTLY TO +5V IF NOT UNDER EXTERNAL CONTROL

FIGURE 3. SUGGESTED CVSD-PCM FILTER INTERFACE

APP NOTE

FOR YOUR INFORMATION

No. 607

Harris Analog

DELTA MODULATION FOR VOICE TRANSMISSION

By Don Jones

INTRODUCTION TO DELTAMOD

Delta modulation has evolved into a simple, efficient method of digitizing voice for secure, reliable communications and for voice I/O in data processing.

To illustrate basic principles, a very simple delta modulator and demodulator are illustrated in Figure 1. The modulator is a sampled data system employing a negative feedback loop. A comparator senses whether or not the instantaneous level of the analog voice input is greater or less than the feedback signal. The comparator output is clocked by a flip-flop to form a continuous NRZ digital data stream. This digital data is also integrated and fed back to the comparator. The feedback system is such that the integrator ramps up and down to produce a rough approximation of the input waveform. An identical integrator in the demodulator produces the same waveform, which when filtered, reproduces the voice.

One can see that the digital data 0's and 1's are commands to the integrators to "go up" or "go down" respectively. Another way of looking at it is that the digital data stream also has analog significance; it approximates the differential of the voice, since analog integration of the data reproduces the voice.

Note that the integrator output never stands still; it always travels either up or down by a fixed amount in any clock period. Because of its fixed integrator output slope, the simple delta modulator is less than ideal for encoding human voice which may have a wide dynamic amplitude range.

The integrator cannot track large, high frequency signals with its fixed slope. Fortunately, human speech has statistically smaller amplitudes at higher frequencies, therefore an integrator time constant of about 1 millisecond will satisfactorily reproduce voice in a 3kHz bandwidth.

A more serious limitation is that voice amplitude changes which are less than the height of the integrator ramp during one clock period cannot be resolved. So dynamic range is proportional to clock frequency, and satisfactory range cannot be obtained at desirable low clock rates.

A means of effectively increasing dynamic range is called "companding" (compressing-expanding); where at the modulator, small signals are given higher relative gain, and an inverse characteristic is produced at the demodulator.

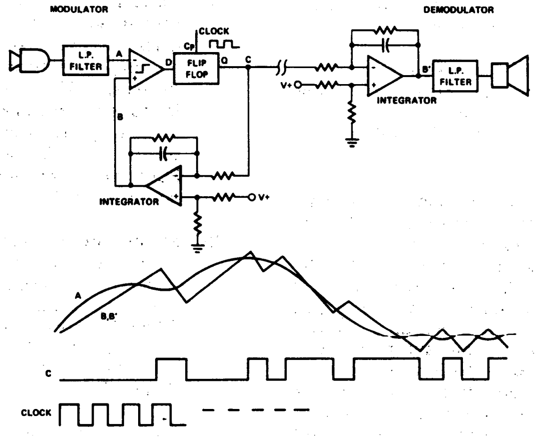
The CVSD: A popular effective scheme for companded delta modulation is known as CVSD (continuously variable slope deltamod) shown in Figure 2. Additional digital logic, a second integrator, and an analog multiplier are added to the simple modulator.

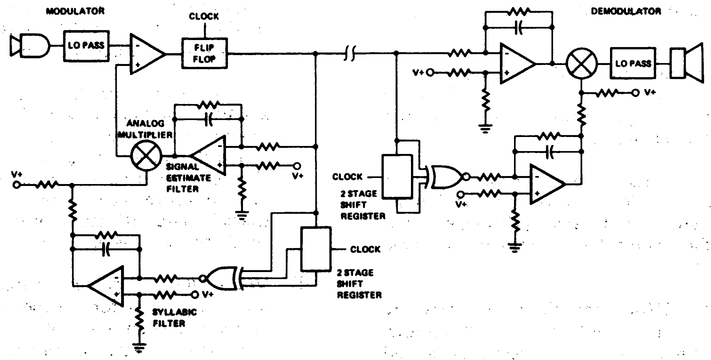
Under small input signal conditions, the second integrator (known as the syllabic filter) has no input, and circuit function is identical to the simple modulator, except that the multiplier is biased to output quite small ramp amplitudes giving good resolution to the small signals.

A larger signal input is characterized by consecutive strings of 1's or 0's in the data as the integrator attempts to track the input. The logic input to the syllabic filter actuates whenever 3 or more consecutive 0's or 1's are present in the data. When this happens, the syllabic filter output starts to build up, increasing the multiplier gain, passing larger amplitude ramps to the comparator, enabling the system to track the larger signal. Up to a limit, the more consecutive 1's or 0's generated, the larger the ramp amplitude. Since the larger signals increase the negative feedback of the modulator and the forward gain of the demodulator, companding takes place. By listening tests, the syllabic filter time constant of 4 to 10 milliseconds is generally considered optimum.

An outstanding characteristic of CVSD is its ability, with fairly simple circuitry, to transmit intelligible voice at relatively low data rates. Companded PCM, for telephone quality transmission, requires about 64K bits/sec data rate per channel. CVSD produces equal quality at 32K bits/sec. (However, at this rate it does not handle tone signals or phase encoded modem transmissions as well.)

CVSD is useful at even lower data rates. At 16K bits/sec the reconstructed voice is remarkably natural, but has a slightly "Fuzzy Edge". At 9.6K bits/sec intelligibility is still excellent, although the sound is reminiscent of a damaged loudspeaker. Of course, very sophisticated speech compression techniques have been used to transmit speech at even lower data rates; but CVSD is an excellent compromise between circuit simplicity and bandwidth economy.


MODULATOR
DEMODULATOR
L.P. FILTER
A
D
FLIP FLOP
CLOCK
Cp
Q
C
B
INTEGRATOR
V+
B'
L.P. FILTER
INTEGRATOR
V+
A
B,B'
C
CLOCK


MODULATOR
LO PASS
CLOCK
FLIP FLOP
DEMODULATOR
LO PASS
V+
V+
ANALOG MULTIPLIER
SIGNAL ESTIMATE FILTER
V+
V+
CLOCK
2 STAGE SHIFT REGISTER
V+
CLOCK
2 STAGE SHIFT REGISTER
V+
SYLLABIC FILTER

THE DIGITAL CVSD

Delta modulated data is in a form which can be digitally filtered with fairly simple circuitry. A compatible CVSD can be made using digital integrators and multipliers driving a digital-to-analog converter. The block diagram of the Harris HC-55564 monolithic CVSD is shown in Figure 3.

The CMOS digital circuit functions of Figure 3 closely parallel the equivalent analog function in Figure 2. The filters are single pole recursive types using shift registers with feedback. A digital multiplier feeds a 10 bit R-2R DAC which reconstructs the voice waveform. The DAC output is in steps, rather than ramps.

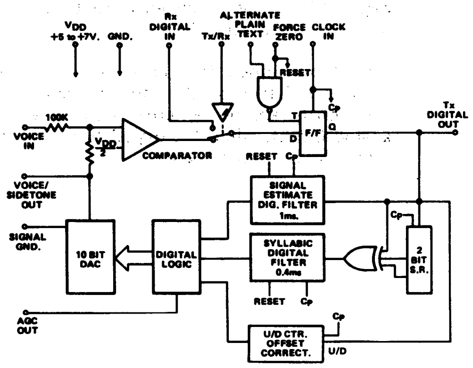

VDD +5 to +7V.
GND.
Rx DIGITAL IN
Tx/Rx
ALTERNATE PLAIN TEXT
FORCE ZERO
CLOCK IN
RESET
Cp
T
F/F
Q
D
Tx DIGITAL OUT
100K
VOICE IN
VDD/2
COMPARATOR
RESET
Cp
VOICE/ SIDETONE OUT
SIGNAL ESTIMATE DIG. FILTER 1ms.
Cp
SIGNAL GND.
10 BIT DAC
DIGITAL LOGIC
SYLLABIC DIGITAL FILTER 0.4ms
2 BIT S.R.
RESET
Cp
AGC OUT
Cp
U/D CTR. OFFSET CORRECT.
U/D

Figure 3 — HC-55564 CVSD Functional Diagram

The digital CVSD has a number of advantages over its analog counterpart, and has desirable features which would otherwise require additional circuitry:

1) The all CMOS device requires only 1mA current from a single +4.5V to +7V supply.

2) No bulky external precision resistors or capacitors are required for the integrators; time constants of the digital filters are set by the clock frequency and do not drift with time or temperature.

3) For best intelligibility and freedom from listener fatigue, it is important that the recovered audio is quiet during the pauses between spoken words. During quiet periods, an alternate "1", "0" pattern should be encoded, which when decoded and filtered will be inaudible. Achieving this in the analog CVSD requires that up and down ramp slopes are precisely equal and that offsets in the comparator and amplifiers are adjusted to zero. Improper adjustment or excessive component drift can result in noisy oscillations. In the digital design, comparator offset and drift are adjusted by a long up-down counter summed to the DAC to insure that over a period of time equal numbers of 1's and 0's are generated.

   An added feature is automatic quieting, where if the DAC input would be less than 2 LSB's the quieting pattern is generated instead. This has proven to aid intelligibility.

4) To prevent momentary overload when beginning to encode or decode, it is desirable to initialize the integrators. In the analog CVSD, external analog switches would be required to discharge the capacitors.

   In the digital CVSD, the filters are reset by momentarily putting the "Force Zero" pin low. At the same time, a quieting pattern is generated without affecting internal encoding by putting the "Alternate Plain Text" pin low.

5) In some analog CVSD designs, transient noise will be generated during recovery from a low frequency overdriven input condition. The digital CVSD has a clipped output with instant recovery, when overdriven.

6) Half-duplex operation (using the same device, switching between the encode and decode functions) requires external circuits with the analog CVSD, while the digital type is switched internally by a logic input.

APPLICATIONS OF DELTA MODULATION

1) **Telecommunications:** Digitized signals are easily routed and multiplexed with low cost digital gates. Voice channels may be easily added to existing multiplexed digital data transmission systems. The digital signals are much more immune to crosstalk and noise when transmitted over long distances by wire, R.F., or optical paths. CVSD has better intelligibility than PCM when random bit errors are introduced during transmission.

2) **Secure Communications:** Digital data can be quite securely encrypted using fairly simple standard hardware (Figure 4a). Scrambled speech for audio channels may also be accomplished by encoding into a shift register, then selecting different segments of the shifted data in pseudo-random fashion and decoding it (Figure 4b).

3) **Audio Delay Lines:** Although charge-coupled deviced (CCD) will perform this function, they are still expensive and choice of configurations is quite limited. Also, there is a practical limit to the number of CCD stages, since each introduces a slight degradation to the signal.

   As shown in Figure 5, the delay line consists of a CVSD modulator, a shift register and a demodulator. Delay is proportional to the number of register stages divided by the clock frequency. This can be used in speech scrambling, as explained above, echo supression in PA systems; special echo effects; music enhancement or synthesis; and recursive or nonrecursive filtering.

4) **Voice I/O:** Digitized speech can be entered into a computer for storage, voice identification, or word recognition. Words stored in ROM's, disc memory, etc. can be used for voice output. CVSD, since it can operate at low data rates, is more efficient in storage requirements than PCM or other A to D conversions. Also, the data is in a useful form for filtering or other processing.

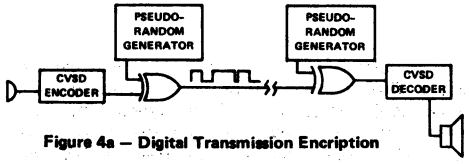


Figure 4a — Digital Transmission Encription

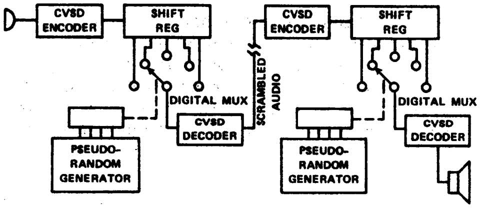


Figure 4b — Voice Transmission Scrambling

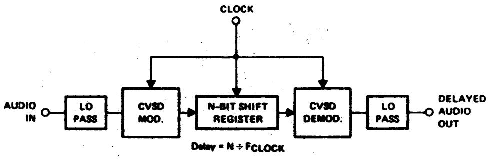


Figure 5 – Audio Delay Line

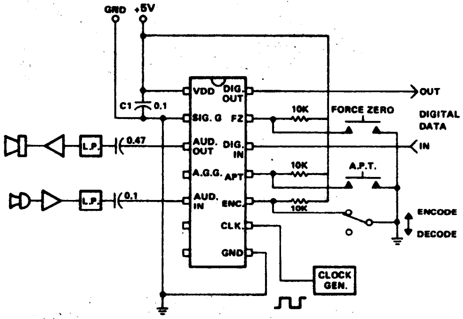


Figure 6 – CVSD Hookup for Evaluation

Figure 6 illustrates a simple evaluation breadboard circuit for the HC-55564. A single device is sufficient to evaluate sound quality, etc. since, when encoding, the feedback signal at pin 3 is identical to the decoded signal from a receiver. The following are some pointers for using the devices:

1) Power supply decoupling is essential with the capacitor (C1 in Figure 6) located close to the I.C.

2) Power to the I.C. must be present before the audio input, the clock, or other digital inputs are applied. Failure to observe this may result in a latchup condition, which is usually not destructive and may be removed by cycling the supply off, then on.

3) Signal ground (pin 2) should be externally connected to pin 8 and power ground. It is recommended for noise-free operation that the audio input and output ground returns connect directly to pin 2 and to no other grounds in the system. Pins 6 and 7 must be open circuited.

4) Digital inputs and outputs are similar to and compatible with standard CMOS logic circuits using the same supply voltage. The illustrated 10K pullup resistors are necessary only with mechanical switches, and are not necessary when driving these pins with CMOS. Unused digital inputs should be tied to the appropriate supply rail for the desired operation. TTL output, however, will require pullup resistors (about 1K) to obtain the required CMOS input levels. Pins 4 and 14 will drive CMOS logic, or each can drive one low power TTL input.

5) Capacitor coupling is recommended for the audio in and out (pins 3 and 5) as each pin is internally biased to about 1/2 the supply voltage.

6) The AGC output (pin 4) is a digital output, whose duty cycle is dependent on the average audio level. This may be externally integrated to drive an AGC preamplifier; or it could be used (through a buffer gate) to drive an LED indicator to indicate proper speaking volume.

7) To prevent generation of alias frequencies, the input filter should reduce the audio amplitude at frequencies greater than half the clock rate to less than 12 millivolts peak-to-peak.

8) The PCM Filter shown in the data sheet lends itself well as a cost-effective input/output filter to the CVSD.

9) A suggested receiver clock circuit is a free running multivibrator, synchronized at each transition of the incoming data. Any synch errors occurring during reception of long strings of zeros or ones will have negligible effect on the decoded voice.

Figures 7 though 11 illustrate some typical audio output (before filtering) and digital output waveforms. To make the scope picture stationary, the audio input generator was synchronized with a submultiple of the clock frequency.

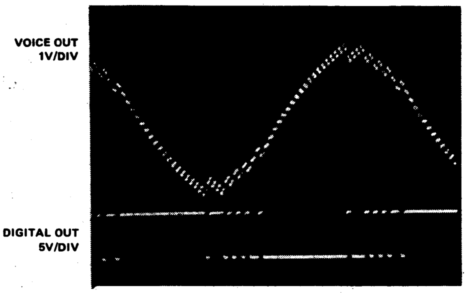
Figure 7 shows the results of a large low frequency sine wave. The somewhat jagged peaks are typical of all CVSD systems. Note that the digital output is continuous "ones" while the waveform is slewing down and continuous "zeros" while slewing up.

Figure 8 shows the excellent recovery from overdriven conditions at low frequency. Some analog type CVSD's have trouble recovering from this condition.

As mentioned previously, CVSD's cannot handle large signals at high frequencies (but these are not generally present in the human voice). Figure 9 shows this limitation where the voice output is slewing at its maximum rate, but cannot catch up with the input. At reduced amplitudes, however, the same signal can be reproduced, as shown in Figure 10.

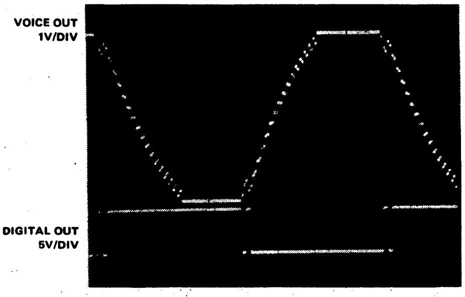
The transfer function curve on the data sheet shows that at 16kHz clock rate, a 1.2V RMS signal can be tracked up to 500Hz. With a 32kHz clock, the same curves may be used, but with each of the indicated frequencies doubled. Likewise, each of the SNR figures shown on the data sheet will be 6dB better with a 32kHz clock.

Figure 11 shows the 10 millivolt voice output waveform at 1/2 the clock rate, when there is no audio input. After filtering, this signal is inaudible.



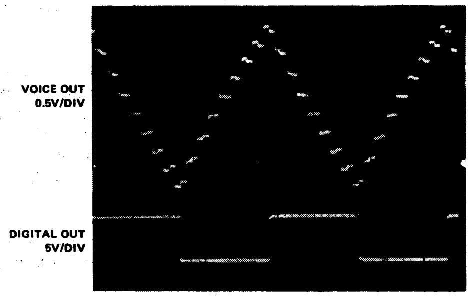
0.5ms/DIV.
VOICE IN = 250Hz, 4V P-P SINE WAVE
CLOCK = 16kHz

Figure 7 — CVSD Large Signal Sine Wave Reconstruction



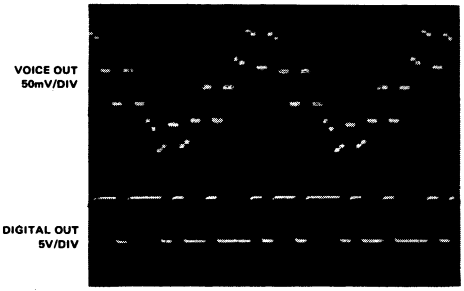
0.5ms/DIV.
VOICE IN = 250Hz, 6V P-P SINE WAVE
CLOCK = 16kHz

Figure 8 — CVSD Large Signal, Low Frequency Clipped Waveform



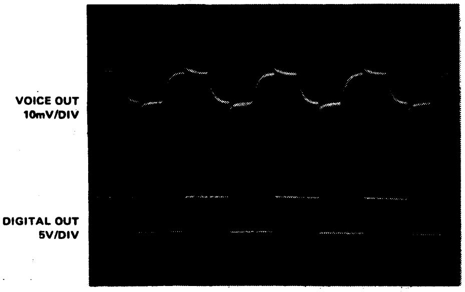
0.2ms/DIV.
VOICE IN = 1kHz, 6V P-P SINE WAVE
CLOCK = 16kHz

Figure 9 — CVSD Large Signal, High Frequency Slew Limiting



0.2ms/DIV.
VOICE IN = 1kHz, 0.15V P-P SINE WAVE
CLOCK = 16kHz

Figure 10 — CVSD Small Signal Sine Wave Reconstruction



50μs/DIV.
VOICE IN = 0
CLOCK = 16kHz

Figure 11 — CVSD Zero Signal Idle Pattern

ANALOG

Chip Information

11

GENERAL INFORMATION

Harris Analog Products are available in chip form to the hybrid micro circuit designer. The standard chips are DC electrically tested to the data sheet limits for the commercial device and are 100% visually inspected. Packaging for shipment consists of waffle pack carriers plus an anti-static cushioning strip for extra protection.

The hybrid industry has rapidly become more diversified and stringent in its requirements for integrated circuits. To meet these demands Harris has several options additional to standard chip processing available upon request at extra cost. For more information consult the nearest Harris Sales Office.

CHIP ORDERING INFORMATION

Standard and special chip sales are available through Harris authorized chip suppliers or direct from the factory. Contact the local Harris Sales Office for pricing and delivery information. (Minimum quantities may apply).

MECHANICAL INFORMATION

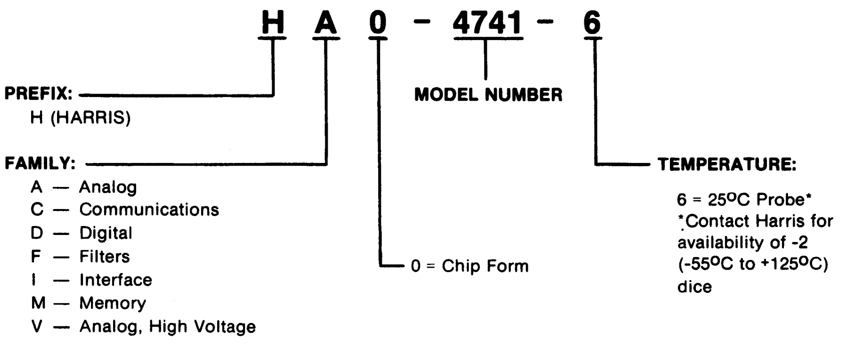
Dimensions: All chip dimensions nominal with a tolerance of ± .003". Maximum chip thickness is .019" + .001".

Bonding Pads: Minimum bonding pad size is .004" x .004" unless otherwise specified.

DICE GEOMETRIES AND DIMENSIONS

May be obtained by contacting the factory or your local Harris Sales Office.

HARRIS PRODUCT CODE EXAMPLE



H A 0 - 4741 - 6

PREFIX:
H (HARRIS)

FAMILY:
A — Analog
C — Communications
D — Digital
F — Filters
I — Interface
M — Memory
V — Analog, High Voltage

0 = Chip Form

MODEL NUMBER

TEMPERATURE:
6 = 25°C Probe*
*Contact Harris for availability of -2 (-55°C to +125°C) dice

Packaging

12

Analog Package Selection Guide 12-2

Package Configurations 12-4

Harris Analog Package Selection Guide

PART NUMBER	PACKAGE CONFIGURATION (See Note)					
	CAN	PLASTIC	CERDIP	SIDE BRAZED	CERAMIC LEADLESS CHIP CARRIER	PLASTIC LEADED CHIP CARRIER
HA-OP07	W	M	A			
HA-OP27	W		A		T	
HA-OP37	W		A		T	
HA-2400/04/05/06		O	C1		T	
HA-2420/25		N	B1		T	
HA-2500/02/05	W	M	A		T	
HA-2510/12/15	W	M	A		T	
HA-2520/22/25	W	M	A		T	
HA-2539		N	B1		T	
HA-2540		N	B1		T	
HA-2541	Y		B1			
HA-2542	Y	N	B2			
HA-2600/02/05	W	M	A			
HA-2620/22/25	W	M, N	A, B1		T	
HA-2630/35	Y					
HA-2640/45	W		A			
HA-2650/55	W	M	A			
HA-2720/25	W		A			
HA-4600/02/05		N	B1			
HA-4741		N	B1		T	
HA-4900/02/05			C1		T	
HA-5002	W	M	A		T	
HA-5033	Y	M				
HA-5102/5112	W	M	A		T	
HA-5104/5114		N	B1		T	
HA-5130/35	W	M	A		T	
HA-5141/41A	W	M	A		T	
HA-5142/42A	W	M	A		T	
HA-5144/44A		N	B1		T	
HA-5147	W		A		T	
HA-5151/52/54	W	M	A			
HA-5160/62	W					
HA-5170	W	M	A		T	
HA-5180	W	M	A		T	
HA-5190/95	Y		B1		T	
HA-5320			B1		T	
HA-5330			B2		T	
HC-5502A		R	G			AB
HC-5504		R	G			AB
HC-5508		S				
HC-5510			G			
HC-5511			F			
HC-5512/12A/12C			C2			
HC-5512D			C2		T	
HC-5552			D			

NOTE: "Package Configuration" references drawings on the following pages. Package designations constructing the part number are explained in the Ordering Information, Section 1.

Solder Dipped Parts add + .003 inches to dimension B & C in Plastic, and dimension ϕB in Cans.

Dimensions are $\frac{\text{MIN}}{\text{MAX}}$ and in inches.

BSC means Basic Spacing Between Centers

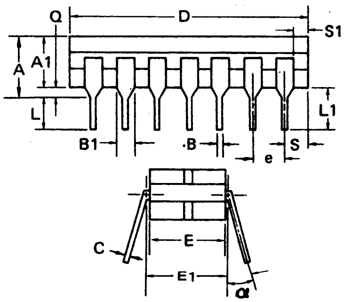
Harris Analog Package Selection Guide (Continued)

PART NUMBER	PACKAGE CONFIGURATION (See Note)					
	CAN	PLASTIC	CERDIP	SIDE BRAZED	CERAMIC LEADLESS CHIP CARRIER	PLASTIC LEADED CHIP CARRIER
HC-5552			D			
HC-5553			E			
HC-5554			C2			
HC-5557			C2			
HC-55536			B1			
HC-55564			B1		T	
HD-0165			G			
HF-10			E			
HI-200	X	N	B1			
HI-201		O	C1		T	
HI-201HS		O	C1		T	
HI-300/01/04/05	X	N	B1			
HI-302/03/06/07		N	B1			
HI-381/387	X	N	B1			
HI-384/390		O	C1			
HI-506/507		S	H		U	AB
HI-506A/507A		S	H			
HI-506L/507L		S	H			
HI-508/509		O	C1		T	AA
HI-508A/509A		O	C1			
HI-508L/509L		P	D			
HI-516		S	H			
HI-518		P	D			AA
HI-524		P	D		T	AA
HI-539		O	C1			AA
HI-546/547		S	H		U	AB
HI-548/549		O	C1		T	AA
HI-562A				J	U	
HI-565A				J		
HI-574A				K	V	
HI-674A				K	V	
HI-774				K		
HI-774A				K	V	
HI-1818A/28A		O	C1			
HI-5040 thru 5051		O	C1			
HI-5043/45		O	C1			
HI-5610				J		
HI-5618A/18B			D			
HI-5660/60A				J		
HI-5680/85/85A/87				J	U	
HI-5690V/95V/97V				J	U	
HI-5721				K		
HI-7541				I		
HI-DAC16B/C				L		
HV-1000/1000A		O				
HY-94741/2		HA				
HY-9574		HB				
HY-9674		HB				
HY-9590/91		HB				
HY-9595/96		HB				

NOTE: "Package Configuration" references drawings on the following pages. Package designations constructing the part number are explained in the Ordering Information, Section 1.

Package Configuration

A B C D E .300 CERAMIC DUAL-IN-LINE

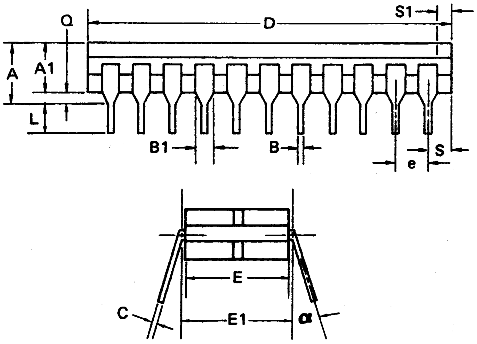


PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
A	8 SSI	.155 .200	.140 .160	.016 .023	.050 .070	.008 .015	.375 .395	.245 .265	.290 .310	.090 .110	.125 .150	.150 .180	.080 MAX	.005 MIN	.015 .060	0° 15°
B1	14 MSI	.155 .200	.140 .170	.016 .023	.050 .070	.008 .015	.753 .785	.265 .285	.290 .310	.090 .110	.125 .150	.150 .180	.080 MAX	.005 MIN	.015 .060	0° 15°
B2	14 LSI	.155 .200	.140 .170	.016 .023	.050 .070	.008 .015	.753 .785	.285 .305	.300 .320	.090 .110	.125 .150	.150 .180	.080 MAX	.005 MIN	.015 .060	0° 15°
C1	16* MSI	.155 .200	.140 .170	.016 .023	.050* .070*	.008 .015	.753 .785	.265 .285	.290 .310	.090 .110	.125 .150	.150 .180	.080 MAX	.005 MIN	.015 .060	0° 15°
C2	16* LSI	.155 .200	.140 .170	.016 .023	.050* .070*	.008 .015	.753 .785	.285 .305	.300 .320	.090 .110	.125 .150	.150 .180	.080 MAX	.005 MIN	.015 .060	0° 15°
D	18 LSI	.155 .200	.140 .170	.016 .023	.050* .070*	.008 .015	.882 .915	.285 .305	.300 .320	.090 .110	.125 .150	.150 .180	.080 MAX	.005 MIN	.015 .060	0° 15°
E	20 LSI	.155 .200	.140 .170	.016 .023	.050* .070*	.008 .015	.940 .970	.285 .305	.300 .320	.090 .110	.125 .150	.150 .180	.080 MAX	.005 MIN	.015 .060	0° 15°

* End leads are half leads where B remains the same and B1 is .035 — .045

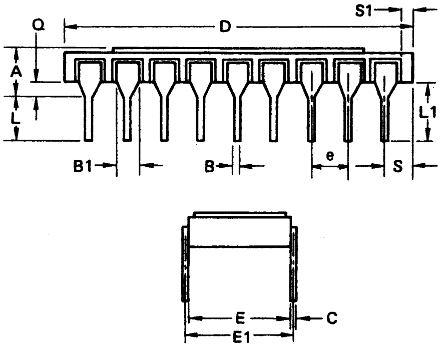
F .400 CERAMIC DUAL-IN-LINE

G H .600 CERAMIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
F .400	22 LSI	.165 .225	.150 .180	.016 .023	.050 .070	.008 .015	1.055 1.085	.375 .395	.385 .415	.090 .110	.125 .150	.150 .180	.080 MAX	.005 MIN	.015 .060	0° 15°
G .600	24 LSI	.165 .225	.150 .180	.016 .023	.050 .070	.008 .015	1.24 1.27	.515 .535	.585 .615	.090 .110	.125 .150	.150 .180	.080 MAX	.005 MIN	.015 .060	0° 15°
H .600	28 LSI	.175 .250	.160 .190	.016 .023	.050 .070	.008 .015	1.44 1.47	.515 .535	.585 .615	.090 .110	.125 .150	.150 .195	.080 MAX	.005 MIN	.015 .060	0° 15°

I .300 SIDEBRAZE DUAL-IN-LINE

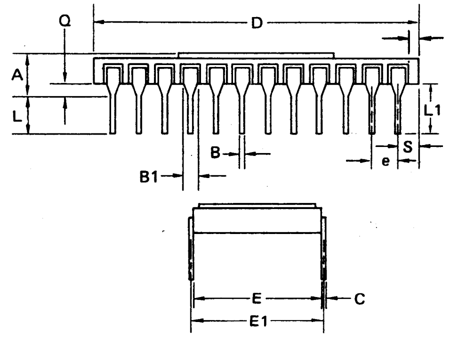


PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
I	18	.101 .150	.016 .023	.045 .060	.008 .015	.880 .910	.280 .300	.290 .310	.100 BSC	.125 .180	.150 .180	.080 MAX	.005 MIN	.025 .045

NOTE: 1) Dimensions are: $\frac{\text{MIN}}{\text{MAX}}$ 2) All Dimensions in Inches 3) BSC Means Basic Spacing Between Centerlines

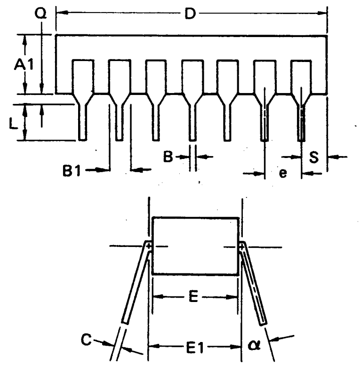
Package Configuration (Continued)

J K L .600 SIDEBRAZE DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
J	24	.120 .154	.016 .023	.040 .054	.008 .015	1.185 1.215	.587 .603	.588 .612	.100 BSC	.125 .180	.150 .180	.080 MAX	.005 MIN	.040 .060
K	28	.120 .154	.016 .023	.040 .054	.008 .015	1.385 1.415	.587 .603	.588 .612	.100 BSC	.125 .180	.150 .195	.080 MAX	.005 MIN	.030 .060
L	40	.120 .154	.016 .023	.040 .054	.008 .015	1.980 2.020	.587 .603	.588 .612	.100 BSC	.125 .180	.150 .195	.080 MAX	.005 MIN	.040 .060

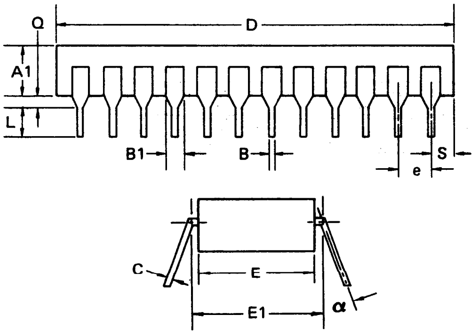
M N O P Q .300 PLASTIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
M	8	.125 .140	.016 .023	.050 .070	.008 .015	.370 .390	.245 .265	.290 .310	.090 .110	.110 .150	.030 .050	.020 .040	0° 15°
N	14	.125 .140	.016 .023	.050 .070	.008 .015	.750 .770	.245 .265	.290 .310	.090 .110	.110 .150	.030 .050	.020 .040	0° 15°
O	16*	.125 .140	.016 .023	.050 .070	.008 .015	.750 .770	.245 .265	.290 .310	.090 .110	.110 .150	.025 .035	.020 .040	0° 15°
P	18	.125 .140	.016 .023	.050 .070	.008 .015	.900 .920	.245 .265	.290 .310	.090 .110	.110 .150	.040 .060	.020 .040	0° 15°
Q	20	.130 .145	.016 .023	.050 .070	.008 .015	1.030 1.050	.250 .270	.290 .310	.090 .110	.110 .150	.060 .080	.020 .040	0° 15°

* Ends leads are half where B remains the same and B1 is .035 — .045

R S .600 PLASTIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
R	24.	.145 .155	.016 .023	.050 .070	.008 .015	1.24 1.26	.540 .560	.590 .610	.090 .110	.110 .150	.045 .095	.020 .040	0° 15°
S	28	.145 .155	.016 .023	.050 .070	.008 .015	1.54 1.57	.540 .560	.590 .610	.090 .110	.110 .150	.110 .160	.020 .040	0° 15°

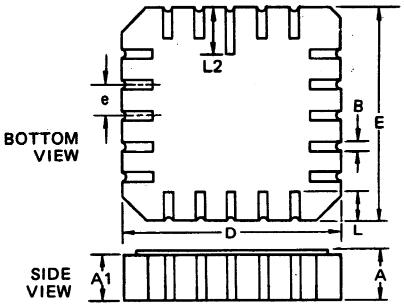
NOTE: 1) Dimensions are: $\frac{\text{MIN}}{\text{MAX}}$ 2) All Dimensions in inches 3) BSC Means Basic Spacing Between Centerlines

Package Configuration (Continued)

T .350 CERAMIC LEADLESS CHIP CARRIER

U .450 CERAMIC LEADLESS CHIP CARRIER

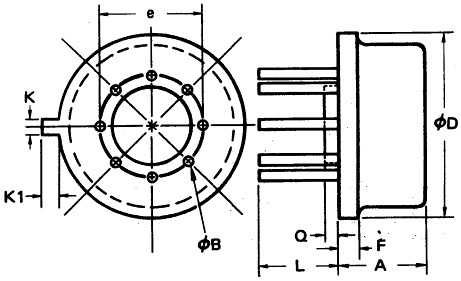
V .650 CERAMIC LEADLESS CHIP CARRIER



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. D	DIM. E	DIM. e	DIM. L	DIM. L2
T	20 .350 SQ	$\frac{.073}{.089}$	$\frac{.063}{.077}$	$\frac{.020}{.030}$	$\frac{.342}{.358}$	$\frac{.342}{.358}$	$\frac{.050}{\text{BSC}}$	$\frac{.042}{.058}$	$\frac{.075}{.095}$
U	28 .450 SQ	$\frac{.073}{.089}$	$\frac{.063}{.077}$	$\frac{.015}{.030}$	$\frac{.445}{.460}$	$\frac{.445}{.460}$	$\frac{.050}{\text{BSC}}$	$\frac{.042}{.058}$	$\frac{.075}{.095}$
V	44 .650 SQ	$\frac{.073}{.089}$	$\frac{.063}{.077}$	$\frac{.020}{.030}$	$\frac{.643}{.662}$	$\frac{.643}{.662}$	$\frac{.050}{\text{BSC}}$	$\frac{.042}{.058}$	$\frac{.075}{.095}$

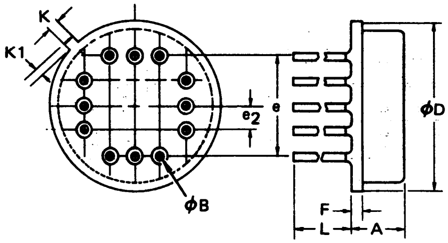
W TO-99 METAL CAN

X TO-100 METAL CAN



PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. F	DIM. K	DIM. K1	DIM. L	DIM. Q
W	8 TO-99	$\frac{.165}{.185}$	$\frac{.016}{.018}$	$\frac{.345}{.365}$	$\frac{.190}{.210}$	$\frac{.020}{.040}$	$\frac{.028}{.034}$	$\frac{.028}{.040}$	$\frac{.505}{.550}$	$\frac{.015}{.040}$
X	10 TO-100	$\frac{.165}{.185}$	$\frac{.016}{.018}$	$\frac{.345}{.365}$	$\frac{.220}{.240}$	$\frac{.020}{.040}$	$\frac{.028}{.034}$	$\frac{.028}{.040}$	$\frac{.505}{.550}$	$\frac{.015}{.040}$

X TO-8 METAL CAN

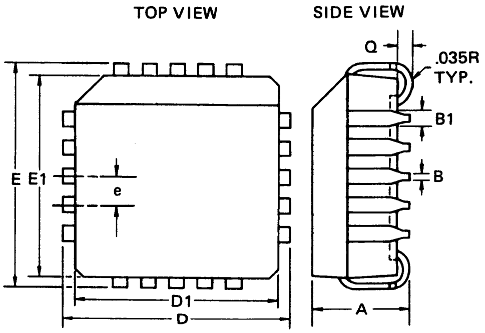


PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. e2	DIM. F	DIM. K	DIM. K1	DIM. L
X	12 TO-8	$\frac{.130}{.150}$	$\frac{.016}{.021}$	$\frac{.585}{.615}$	$\frac{.400}{\text{BSC}}$	$\frac{.100}{\text{BSC}}$	$\frac{.020}{.040}$	$\frac{.027}{.034}$	$\frac{.027}{.045}$	$\frac{.500}{.550}$

NOTE: 1) Dimensions are: $\frac{\text{MIN}}{\text{MAX}}$ 2) All Dimensions in Inches 3) BSC Means Basic Spacing Between Centerlines

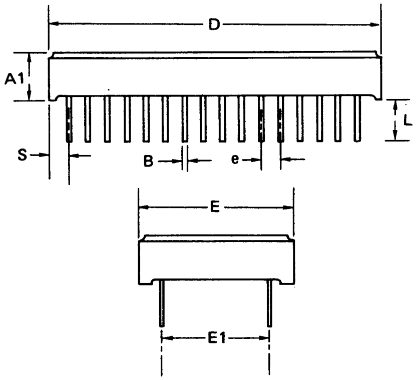
Package Configuration (Continued)

AA AB AC PLASTIC CHIP CARRIER



PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. B1	DIM. D/E	DIM. D1/E1	DIM. e	DIM. Q
AA	20	$\frac{.165}{.180}$	$\frac{.013}{.021}$	$\frac{.026}{.032}$	$\frac{.385}{.395}$	$\frac{.350}{.356}$	$\frac{.050}{\text{BSC}}$	$\frac{.025}{.045}$
AB	28	$\frac{.165}{.180}$	$\frac{.013}{.021}$	$\frac{.026}{.032}$	$\frac{.485}{.495}$	$\frac{.450}{.456}$	$\frac{.050}{\text{BSC}}$	$\frac{.025}{.045}$
AC	44	$\frac{.165}{.180}$	$\frac{.013}{.021}$	$\frac{.026}{.032}$	$\frac{.685}{.695}$	$\frac{.650}{.656}$	$\frac{.050}{\text{BSC}}$	$\frac{.025}{.045}$

HA HB .600 HYBRID PLASTIC DUAL-IN-LINE

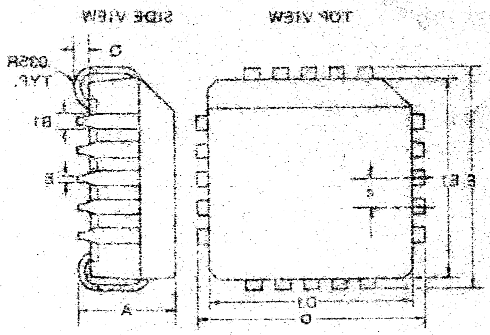


PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S
HA	28	$\frac{\text{MAX}}{.240}$	$\frac{.016}{.025}$	$\frac{\text{MAX}}{1.500}$	$\frac{\text{MAX}}{.810}$	$\frac{.594}{.606}$	$\frac{.090}{.110}$	$\frac{.160}{\text{MIN}}$	$\frac{\text{MAX}}{.100}$
HB	32	$\frac{\text{MAX}}{.240}$	$\frac{.016}{.025}$	$\frac{\text{MAX}}{1.700}$	$\frac{\text{MAX}}{.810}$	$\frac{.594}{.606}$	$\frac{.090}{.110}$	$\frac{.160}{\text{MIN}}$	$\frac{\text{MAX}}{.100}$

NOTE: 1) Dimensions are: $\frac{\text{MIN}}{\text{MAX}}$ 2) All Dimensions in Inches 3) BSC Means Basic Spacing Between Centerlines

Package Configuration (Continued)

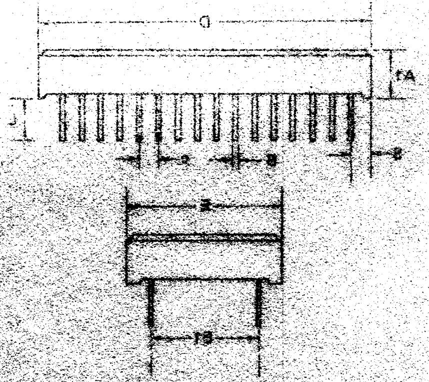
AA AB AC PLASTIC CHIP CARRIER



TOP VIEW
SIDE VIEW
.035R TYP.
C
B1
B
e
E
E1
D1
D
A

PKG. CODE	LEAD COUNT	DIM A	[illegible]	[illegible]	[illegible]	[illegible]	DIM e	DIM Q
AA	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
AB	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
AC	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

HA HB .600 HYBRID PLASTIC DUAL-IN-LINE



D
A1
L
e
B
B
E
E1

PKG. CODE	LEAD COUNT	DIM A1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
HA	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
HB	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

NOTE: 1) Dimensions are: $\frac{\text{MIN}}{\text{MAX}}$ 2) All Dimensions in inches 3) BSC Means Basic Spacing Between Centerlines

Appendices 13

CMOS Digital Products 13-2

CICD Products 13-3

CICD Future Products 13-4

Microwave Products 13-4

Harris Sales Locations 13-5

CMOS Digital Products

80C86 Family: CPUs

80C86	Static 16-bit Microprocessor
80C88	Static 8/16-bit Microprocessor

80C86 Family: Peripherals

82C37A	High Performance Programmable DMA Controller
82C50A	Asynchronous Communication Element
82C52	Full Duplex UART
82C54	Programmable Interval Timer
82C55A	Programmable Peripheral Interface
82C59A	Priority Interrupt Controller
82C82	Octal Latch
82C83H	Octal Latch Inverting Bus Driver
82C84A	Clock Generator Driver
82C85	Static Clock Controller/Generator
82C86H	Octal Bus Transceiver
82C87H	Octal Bus Transceiver (Inverting)
82C88	Bus Controller
82C89	Bus Arbiter

Data Communications

HD-15530	Manchester Encoder-Decoder
HD-15531	Manchester Encoder-Decoder
HD-4702	Programmable Bit Rate Generator
HD-6402	Universal Asynchronous Receiver Transmitter
HD-6406	Programmable Asynchronous Communication Interface
HD-6408	Asynchronous Manchester Adapter
HD-6409	Manchester Encoder-Decoder

CMOS Memory

HM-6504	4K x 1 Synchronous RAM
HM-6508	1K x 1 Synchronous RAM
HM-6514	1K x 4 Synchronous RAM
HM-6516	2K x 8 Synchronous RAM
HM-65162	2K x 8 Asynchronous RAM
HM-6518	1K x 1 Synchronous RAM
HM-65262	16K x 1 Asynchronous RAM
HM-6551	256 x 4 Synchronous RAM
HM-6561	256 x 4 Synchronous RAM
HM-6564	64K Synchronous RAM Module
HM-6616	2K x 8 Fuse Link PROM
HM-6641	512 x 8 Fuse Link PROM
HM-8808A	8K x 8 Asynchronous CMOS RAM Module
HM-8808	8K x 8 Asynchronous CMOS RAM Module
HM-92560	256K Synchronous RAM Module
HM-92570	256K Synchronous RAM Module

CMOS Programmable Logic

HPL-16LC8	Programmable Logic
HPL-16RC4	Programmable Logic
HPL-16RC6	Programmable Logic
HPL-16RC8	Programmable Logic
HPL-82C339	Programmable Chip Select Decoder (PCSD)

CICD Products

Memories

HS-6508RH	1K x 1 CMOS Static RAM (Synchronous)	Rad Hard
HS-6551RH	256 x 4 CMOS Static RAM (Synchronous)	Rad Hard
HS-6504RH	4K x 1 CMOS Static RAM (Synchronous)	Rad Hard
HS-6514RH	1K x 4 CMOS Static RAM (Synchronous)	Rad Hard
HS-6564RH	64K CMOS RAM Module (8K x 8 or 16K x 4)	Rad Hard
HS-65262RH	16K x 1 CMOS Static RAM (Asynchronous)	Rad Hard
HS-6641RH	512 x 8 CMOS PROM (Synchronous)	Rad Hard

80C85 Microprocessor Family

HS-80C85RH	8-Bit CMOS Microprocessor	Rad Hard
HS-81C55RH	256 x 8 CMOS RAM with I/O Ports and Timer	Rad Hard
HS-83C55RH	2K x 8 CMOS ROM with I/O Ports	Rad Hard
HS-54C138RH	3-8-Bit CMOS Decoder	Rad Hard
HS-82C08RH	8-Bit CMOS Bus Transceiver	Rad Hard
HS-82C12RH	8-Bit CMOS Latch	Rad Hard
HS-3374RH	CMOS/TTL Bi-directional Level Shifter	Rad Hard

Multiplexers

HS-508ARH	8 Channel CMOS Analog Multiplexer	Rad Hard
HS-1840RH	16 Channel CMOS Analog Multiplexer	Rad Hard

OP AMPs

HS-3516RH	Wide Band OP AMP	Rad Hard
HS-3530RH	Low Power OP AMP	Rad Hard
HS-5104RH	Quad Low Noise OP AMP	Rad Hard

Analog Switches

HS-302RH	CMOS Analog Switch Dual DPST	Rad Hard
HS-303RH	CMOS Analog Switch Dual SPDT	Rad Hard
HS-306RH	CMOS Analog Switch Dual DPST	Rad Hard
HS-307RH	CMOS Analog Switch Dual SPDT	Rad Hard
HS-384RH	CMOS Analog Switch Dual DPST	Rad Hard
HS-390RH	CMOS Analog Switch Dual SPDT	Rad Hard

Communications

HS-15530RH	CMOS Manchester Encoder/Decoder	Rad Hard
HS-3182	ARINC 429 Bus Interface Line Driver	
HS-3282	CMOS ARINC 429 Bus Interface Circuit	
HS-3273	CMOS MIL-STD-1553 Bus Interface Circuit	
HS-3447	CMOS Data Encription/Decription Device Cypher™	

Semicustom

HS-G0600RH	CMOS Gate Array 600 Gates	Rad Hard
HS-G1200RH	CMOS Gate Array 1200 Gates	Rad Hard
HS-G2500RH	CMOS Gate Array 2500 Gates	Rad Hard
HS-DXXXXRH	CMOS Standard Cell 3 Micron	Rad Hard
HS-CXXXXRH	CMOS Standard Cell 2.5 Micron	Rad Hard

CICD Future Products

Memories

HS-65142RH	1K x 4 CMOS Static RAM High Speed (Asynchronous)	Rad Hard
HS-6616RH	2K x 8 CMOS PROM (Synchronous)	Rad Hard

80C86 Microprocessor Family

HS-80C86RH	16-Bit CMOS Microprocessor	Rad Hard
HS-82C37ARH	CMOS DMA Controller	Rad Hard
HS-82C52RH	CMOS Full Duplex UART	Rad Hard
HS-82C54RH	CMOS Programmable Interval Timer	Rad Hard
HS-82C55RH	CMOS Programmable Peripheral Interface	Rad Hard
HS-82C59ARH	CMOS Programmable Interrupt Controller	Rad Hard
HS-82C85RH	CMOS Static Clock Controller/Generator	Rad Hard

Semicustom

HS-G5000RH	CMOS Gate Array 5000 Gates	Rad Hard

Harris Microwave Semiconductor

GaAs FETs

HMF-0300	125 mW GaAs FET — Chip
HMF-0301	125 mW GaAs FET — Packaged
HMF-0302	125 mW GaAs FET — Flange
HMF-0310	High Gain GaAs FET — Chip
HMF-0314	High Gain GaAs FET — Package
HMF-0600	250 mW GaAs FET — Chip
HMF-0602	250 mW GaAs FET — Flange
HMF-0610	High Gain Power GaAs FET — Chip
HMF-0620	High Gain GaAs FET — Chip
HMF-1200	500 mW GaAs FET — Chip
HMF-1202	500 mW GaAs FET — Flange
HMF-2400	1 W GaAs FET — Chip
HMF-2402	1 W GaAs FET — Flange

GaAs Integrated Circuits

HMD-11011-2	Divide by 10/11 Variable Modulus Divider
HMD-11016-1	Divide by 2/4/8 Binary Counter
HMD-11101-2	5-Input NOR/OR Gate
HMD-11104-2	5-Input NAND/AND Gate
HMD-11131-2	Master/Slave D Flip-Flop
HMD-11301-2	Divide by Two Prescaler
HMD-12141-1	Four-Bit Universal Shift Register

IC Evaluation Kits

HMK-11MSI-1	MSI Evaluation Kit
HMK-11SSI-2	SSI Evaluation Kit

GaAs Programs and Services

Monolithic Microwave Integrated Circuits (MMICs)
Custom Analog Integrated Circuits
Custom Digital Integrated Circuits
Semicustom Digital Integrated Circuits
High Reliability Screening

Harris Sales Locations

U.S. Sales Offices

COMPANY HEADQUARTERS

2401 Palm Bay Road
Palm Bay FL 32905

ALABAMA

P.O. Box 7065
Huntsville, AL 35807
(205) 837-8886

ARIZONA

Suite 250
1717 E. Morten Avenue
Phoenix, AZ 85020
(602) 870-0080

CALIFORNIA

* Suite 320
1503 South Coast Drive
Costa Mesa, CA 92626
(714) 540-2176

* Suite C100
883 Stierlin Road
Mountain View, CA 94043
(415) 964-6443

* Suite 205
6400 Canoga Avenue
Woodland Hills, CA 91367
(818) 992-0686

COLORADO

Suite 200
61 Inverness Drive East
Englewood, CO 80112
(303) 799-8600

FLORIDA

* 1301 Woody Burke Road
P.O. Box 1239
Melbourne, FL 32901
(305) 724-3576

GEORGIA

Suite 400
875 Johnson Ferry Road N.E.
Altanta, GA 30342
(404) 256-4000

ILLINOIS

* Suite M
1555 Mittel Drive
Wood Dale, IL 60191
(312) 860-7884

MASSACHUSETTS

* Suite 3A
83 Cambridge Street
Burlington, MA 01803
(617) 273-5942

MINNESOTA

Suite 703
2850 Metro Drive
Bloomington, MN 55420
(612) 854-3558

NEW YORK

* Suite 426
555 Broadhollow Road
Melville, L.I. NY 11747
(516) 249-4500

NORTH CAROLINA

P.O. Box 31747
Raleigh, NC 27622
(919) 847-8985

OHIO

Suite 204
5880 Sawmill Road
Dublin, OH 43017
(614) 766-4111

OREGON

Suite 250
500 W. 8th Street
Vancouver, WA 98660
(503) 283-7027
(206) 696-0043

PENNSYLVANIA

Suite 1101
996 Old Eagle School Road
Wayne, PA 19087
(215) 687-6680

TEXAS

* 16001 Dallas Parkway
P.O. Box 809022-Mail Zone 32
Dallas, TX 75380-9002
(214) 386-2570

WASHINGTON

33919 9th Avenue South
Federal Way, WA 98003
(206) 838-4878

European Sales Offices

COMPANY HEADQUARTERS

ENGLAND

* Harris/MHS Semiconductor Sales Ltd.
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Winnersh Triangle
Wokingham RG11 5TR
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United Kingdom
TEL: 0734-698787
TWX: 848-174

FRANCE

* Matra-Harris Semiconducteurs
Les Quadrants
3 Avenue du Centre
78182 Saint-Quentin-en-Yvelines
TEL: 3-1-3043 8272
TWX: 697-317

Matra-Harris Semiconducteurs
Electronic Center
La Chanterie Route De Gachet
BP 942
44075 Nantes Cedex
TEL: 33-40-30-30-30
TWX: 711-930

Matra-Harris Semiconducteurs
Locazirst 5
Chemin Des Pres
38240 Meylan
TEL: (33) 76 90 30 90
TWX: 980644F

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Harris/MHS Semiconductors Sales SRL
20092 Cinisello Balsamo
Via Fratelli Cracchi 48
Milan
TEL: 39-2-618-8282
TWX: 324-019

SWEDEN

Harris/MHS Semiconductor Sales AB
Stockholmsvagen 116
183 38 Taby
TEL: 46-8-792-1240
TWX: 14867

WEST GERMANY

* Harris/MHS Semiconductor Sales GmbH
Erfurterstrasse 29
D-8057 Eching (Munich)
TEL: 49-89-3190050
TWX: 524126
TLX: 5213866

Harris/MHS Semiconductor Sales GmbH
Steinhof 37-3
4006 Erkrath
Dusseldorf
TEL: 49-211-242036
TLX: 8582836

* Field Applications
Assistance Available

AUSTRIA

Transistor Vetriebsgesellschaft
mbH & Co. KG.
Auhofstr 41A
A-1130 Wien
TEL: 43-0222-82-94-01
TWX: 133738

BELGIUM

MCA-Tronix
513 Route du Condroz
4020 Liege
TEL: 32-41-362-780
TWX: 4642052

DENMARK

Ditz Schweitzer A.S.
Vallensbaekvej 41
P.O. Box 5
DK-2600 Glostrup
TEL: 45-2-453-044
TWX: 33257

FINLAND

Yleiselektronikka OY
P.O. Box 73
SF-02201 Espoo
TEL: 358-05-62-1122
TWX: 123212

FRANCE

Almex SA
Zone Industrielle
48 Rue de L'Aubepine
92160 Antony
TEL: 1-666-21-12
TWX: 250067

A2M
18 Avenue Dutartre
78150 Le Chesnay
TEL: 3-954-91-13
TWX: 698376

EPROM
185 Rue de Lyon
13015 Marseille
TEL: 91-02-97-76
TWX: 400622

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